

## FEATURES

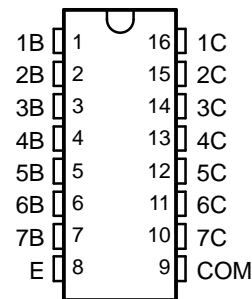
- 500-mA-Rated Collector Current (Single Output)
- High-Voltage Outputs . . . 50 V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
- Relay-Driver Applications

## DESCRIPTION/ORDERING INFORMATION

The ULN2003AI is a high-voltage, high-current Darlington transistor array. This device consists of seven npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single Darlington pair is 500 mA. The Darlington pairs can be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers.

The ULN2003AI has a 2.7-k $\Omega$  series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices.

D, N, OR PW PACKAGE  
(TOP VIEW)



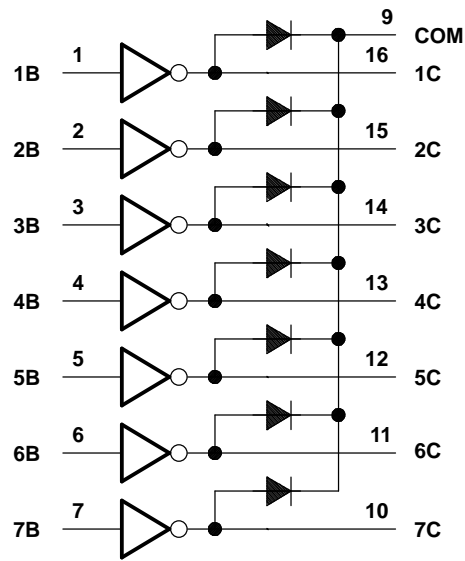
## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 105°C	PDIP (N)	Tube of 425	ULN2003AIN	ULN2003AIN
	SOIC (D)	Tube of 40	ULN2003AID	ULN2003AI
		Reel of 2500	ULN2003AIDR	
	TSSOP (PW)	Reel of 2000	ULN2003AIPWR	UN2003AI

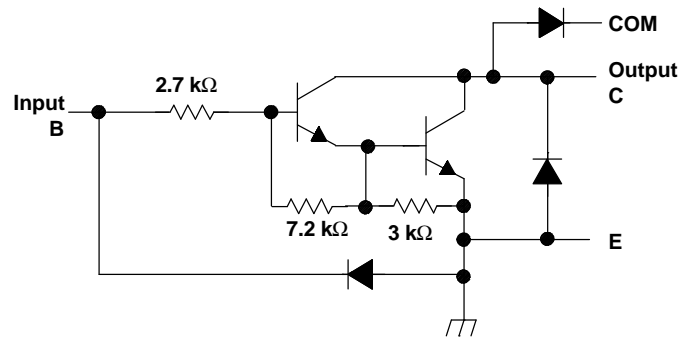


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LOGIC DIAGRAM



SCHEMATICS (EACH DARLINGTON PAIR)



All resistor values shown are nominal.

## Absolute Maximum Ratings<sup>(1)</sup>

at 25°C free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Collector-emitter voltage		50	V
	Clamp diode reverse voltage <sup>(2)</sup>		50	V
V <sub>I</sub>	Input voltage <sup>(2)</sup>		30	V
	Peak collector current <sup>(3)(4)</sup>		500	mA
I <sub>OK</sub>	Output clamp current		500	mA
	Total emitter-terminal current		-2.5	A
T <sub>A</sub>	Operating free-air temperature range	-40	105	°C
θ <sub>JA</sub>	Package thermal impedance <sup>(3)(4)</sup>	D package	73	°C/W
		N package	67	
		PW package	108	
T <sub>J</sub>	Operating virtual junction temperature		150	°C
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the emitter/substrate terminal E<sub>1</sub>, unless otherwise noted.
- (3) Maximum power dissipation is a function of T<sub>J(max)</sub>, θ<sub>JA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is P<sub>D</sub> = (T<sub>J(max)</sub> - T<sub>A</sub>)/θ<sub>JA</sub>. Operating at the absolute maximum T<sub>J</sub> of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

## Electrical Characteristics

 T<sub>A</sub> = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V <sub>I(on)</sub>	On-state input voltage	5	V <sub>CE</sub> = 2 V	I <sub>C</sub> = 200 mA			2.4	V
				I <sub>C</sub> = 250 mA			2.7	
				I <sub>C</sub> = 300 mA			3	
V <sub>CE(sat)</sub>	Collector-emitter saturation voltage	4	I <sub>I</sub> = 250 μA, I <sub>C</sub> = 100 mA		0.9	1.1	V	
			I <sub>I</sub> = 350 μA, I <sub>C</sub> = 200 mA		1	1.3		
			I <sub>I</sub> = 500 μA, I <sub>C</sub> = 350 mA		1.2	1.6		
I <sub>CEX</sub>	Collector cutoff current	1	V <sub>CE</sub> = 50 V, I <sub>I</sub> = 0			50	μA	
V <sub>F</sub>	Clamp forward voltage	7	I <sub>F</sub> = 350 mA		1.7	2	V	
I <sub>I(off)</sub>	Off-state input current	2	V <sub>CE</sub> = 50 V, I <sub>C</sub> = 500 μA	50	65		μA	
I <sub>I</sub>	Input current	3	V <sub>I</sub> = 3.85 V		0.93	1.35	mA	
I <sub>R</sub>	Clamp reverse current	6	V <sub>R</sub> = 50 V			50	μA	
C <sub>i</sub>	Input capacitance		V <sub>I</sub> = 0, f = 1 MHz		15	25	pF	

**ULN2003AI**  
**HIGH-VOLTAGE, HIGH-CURRENT**  
**DARLINGTON TRANSISTOR ARRAY**

SLRS054B–JULY 2003–REVISED FEBRUARY 2005

**Electrical Characteristics**

$T_A = -40^{\circ}\text{C}$  to  $105^{\circ}\text{C}$

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{I(on)}$	On-state input voltage	5	$V_{CE} = 2\text{ V}$	$I_C = 200\text{ mA}$			2.7	V
				$I_C = 250\text{ mA}$			2.9	
				$I_C = 300\text{ mA}$			3	
$V_{CE(sat)}$	Collector-emitter saturation voltage	4	$I_I = 250\text{ }\mu\text{A}$ ,	$I_C = 100\text{ mA}$		0.9	1.2	V
			$I_I = 350\text{ }\mu\text{A}$ ,	$I_C = 200\text{ mA}$		1	1.4	
			$I_I = 500\text{ }\mu\text{A}$ ,	$I_C = 350\text{ mA}$		1.2	1.7	
$I_{CEX}$	Collector cutoff current	1	$V_{CE} = 50\text{ V}$ ,	$I_I = 0$			100	$\mu\text{A}$
$V_F$	Clamp forward voltage	7	$I_F = 350\text{ mA}$			1.7	2.2	V
$I_{I(off)}$	Off-state input current	2	$V_{CE} = 50\text{ V}$ ,	$I_C = 500\text{ }\mu\text{A}$	30	65		$\mu\text{A}$
$I_I$	Input current	3	$V_I = 3.85\text{ V}$			0.93	1.35	$\text{mA}$
$I_R$	Clamp reverse current	6	$V_R = 50\text{ V}$				100	$\mu\text{A}$
$C_i$	Input capacitance		$V_I = 0$ ,	$f = 1\text{ MHz}$		15	25	$\text{pF}$

**Switching Characteristics**

$T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay time, low- to high-level output	See Figure 8		0.25	1	$\mu\text{s}$
$t_{PHL}$	Propagation delay time, high- to low-level output	See Figure 8		0.25	1	$\mu\text{s}$
$V_{OH}$	High-level output voltage after switching	$V_S = 50\text{ V}$ , $I_O \approx 300\text{ mA}$ , See Figure 9	$V_S - 20$			$\text{mV}$

**Switching Characteristics**

$T_A = -40^{\circ}\text{C}$  to  $105^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay time, low- to high-level output	See Figure 8		1	10	$\mu\text{s}$
$t_{PHL}$	Propagation delay time, high- to low-level output	See Figure 8		1	10	$\mu\text{s}$
$V_{OH}$	High-level output voltage after switching	$V_S = 50\text{ V}$ , $I_O \approx 300\text{ mA}$ , See Figure 9	$V_S - 50$			$\text{mV}$

PARAMETER MEASUREMENT INFORMATION

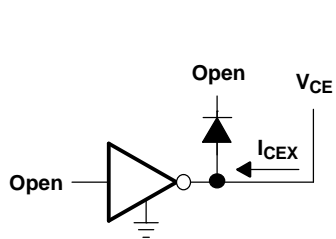


Figure 1.  $I_{CEX}$  Test Circuit

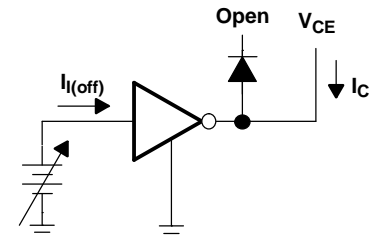


Figure 2.  $I_{I(off)}$  Test Circuit

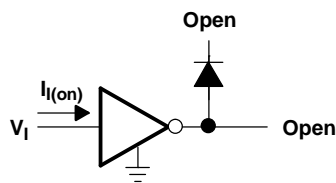
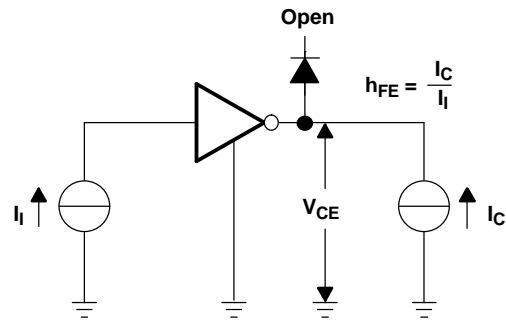


Figure 3.  $I_I$  Test Circuit



NOTE:  $I_I$  is fixed for measuring  $V_{CE(sat)}$ , variable for measuring  $h_{FE}$ .

Figure 4.  $h_{FE}$ ,  $V_{CE(sat)}$  Test Circuit

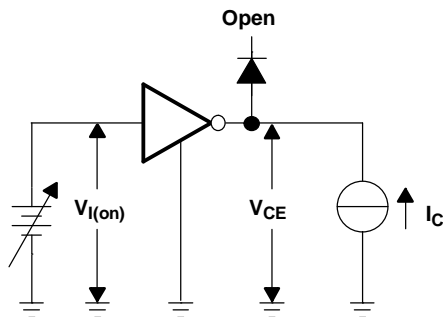


Figure 5.  $V_{I(on)}$  Test Circuit

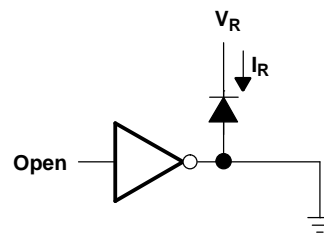


Figure 6.  $I_R$  Test Circuit

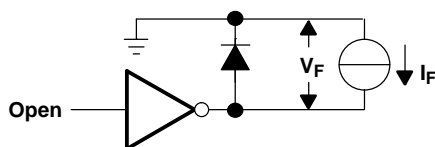


Figure 7.  $V_F$  Test Circuit

PARAMETER MEASUREMENT INFORMATION

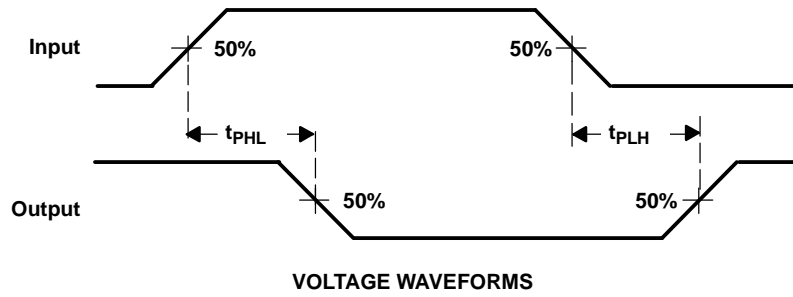
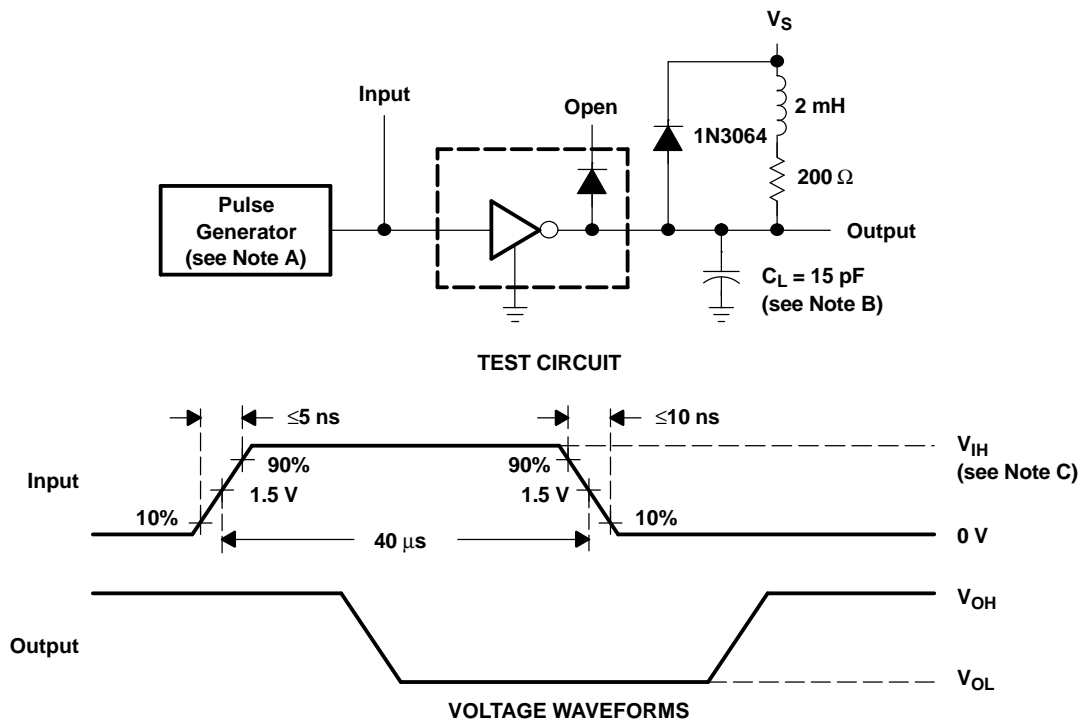


Figure 8. Propagation Delay-Time Waveforms

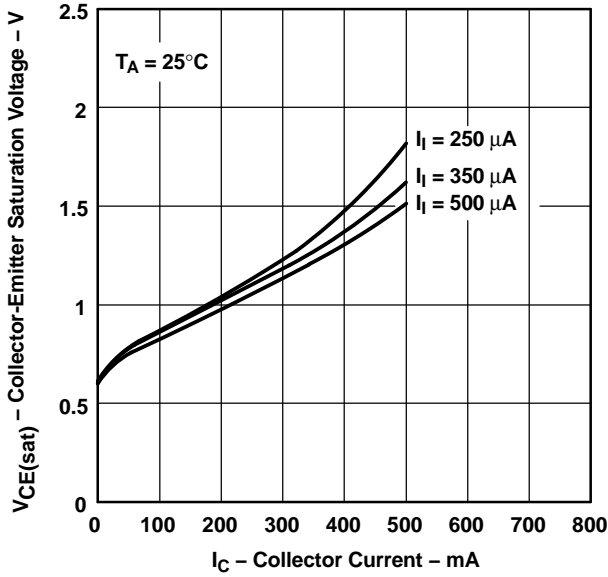


- NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz,  $Z_O = 50 \Omega$ .  
 B.  $C_L$  includes probe and jig capacitance.  
 C. For testing,  $V_{IH} = 3 \text{ V}$

Figure 9. Latch-Up Test Circuit and Voltage Waveforms

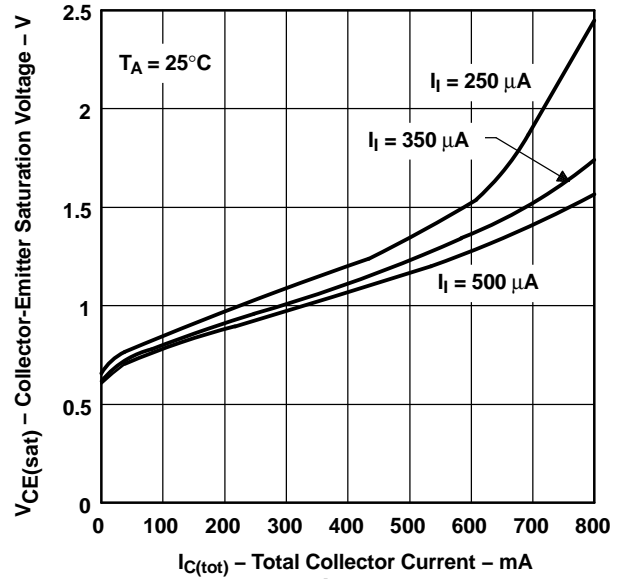
**TYPICAL CHARACTERISTICS**

**COLLECTOR-EMITTER SATURATION VOLTAGE**  
**vs**  
**COLLECTOR CURRENT (ONE DARLINGTON)**



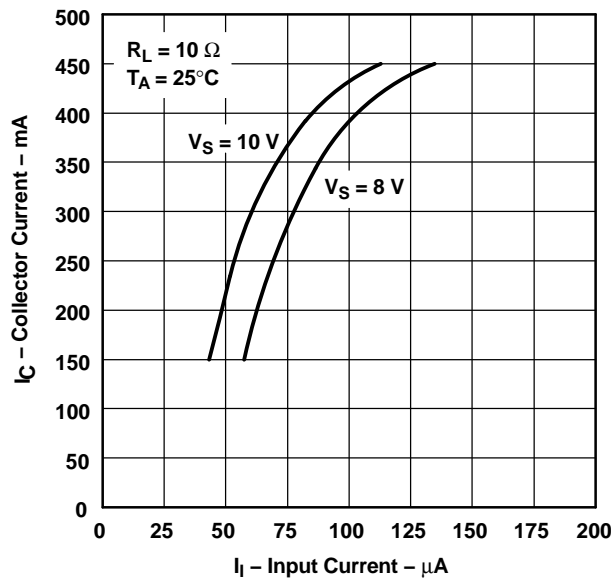
**Figure 10**

**COLLECTOR-EMITTER SATURATION VOLTAGE**  
**vs**  
**TOTAL COLLECTOR CURRENT (TWO DARLINGTONS IN PARALLEL)**



**Figure 11**

**COLLECTOR CURRENT**  
**vs**  
**INPUT CURRENT**



**Figure 12**

THERMAL INFORMATION

D PACKAGE  
 MAXIMUM COLLECTOR CURRENT  
 VS  
 DUTY CYCLE

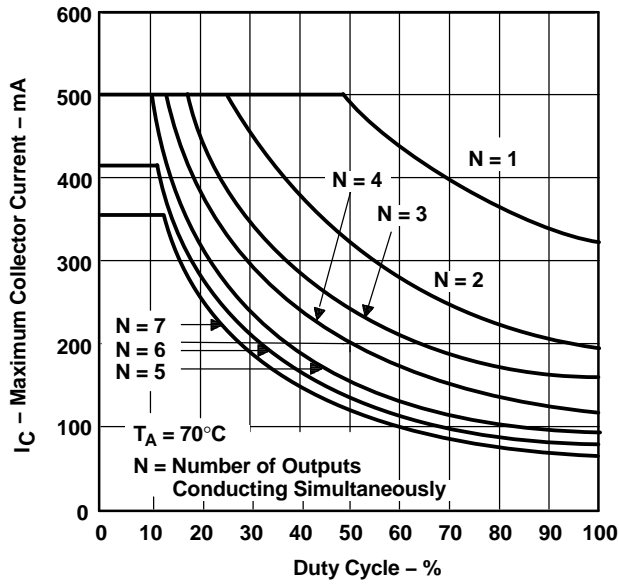


Figure 13

N PACKAGE  
 MAXIMUM COLLECTOR CURRENT  
 VS  
 DUTY CYCLE

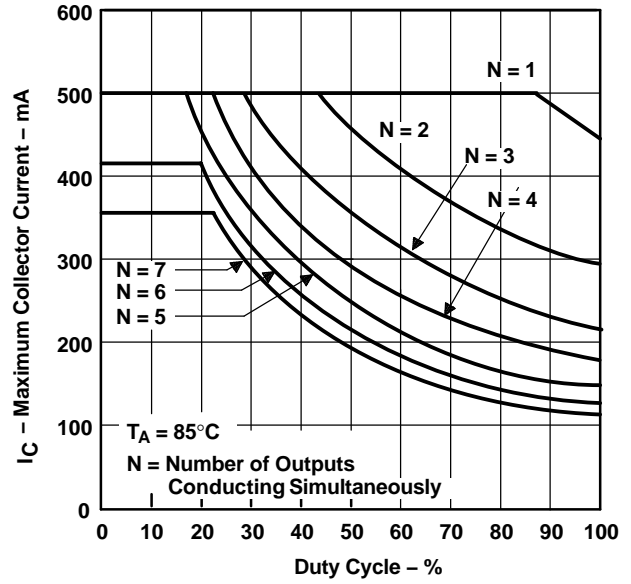
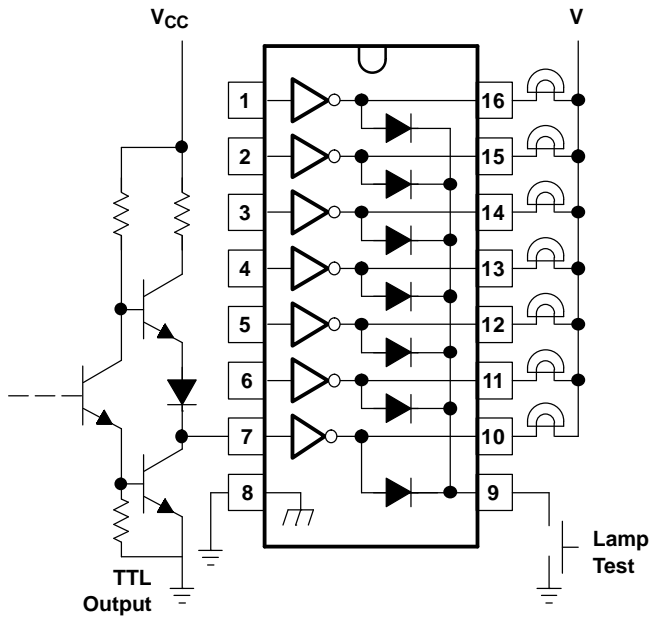
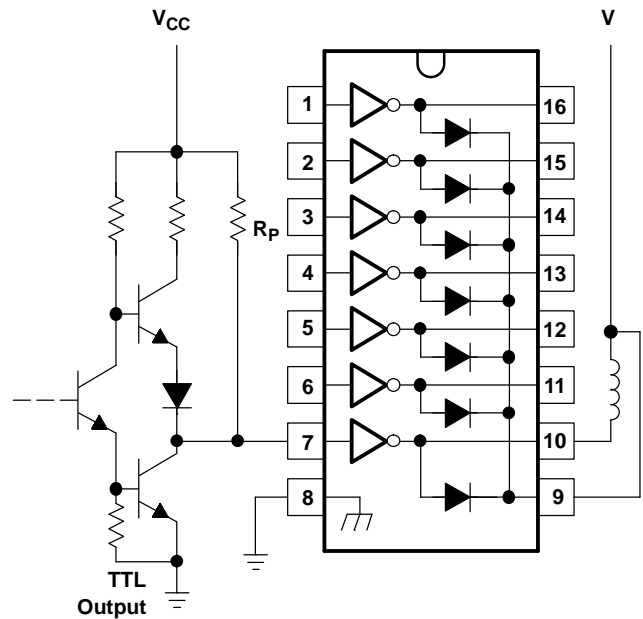


Figure 14

**APPLICATION INFORMATION**



**Figure 15. TTL to Load**



**Figure 16. Use of Pullup Resistors to Increase Drive Current**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
ULN2003AID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULN2003AIDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULN2003AIDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULN2003AIDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULN2003AIDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULN2003AIDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULN2003AIN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
ULN2003AINE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
ULN2003AIPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULN2003AIPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULN2003AIPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULN2003AIPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULN2003AIPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULN2003AIPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is

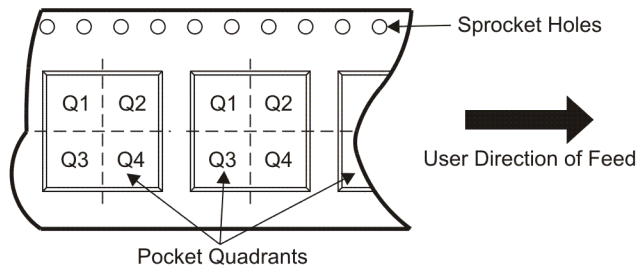
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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ULN2003AIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
ULN2003AIPWR	TSSOP	PW	16	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ULN2003AIDR	SOIC	D	16	2500	333.2	345.9	28.6
ULN2003AIPWR	TSSOP	PW	16	2000	346.0	346.0	29.0

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

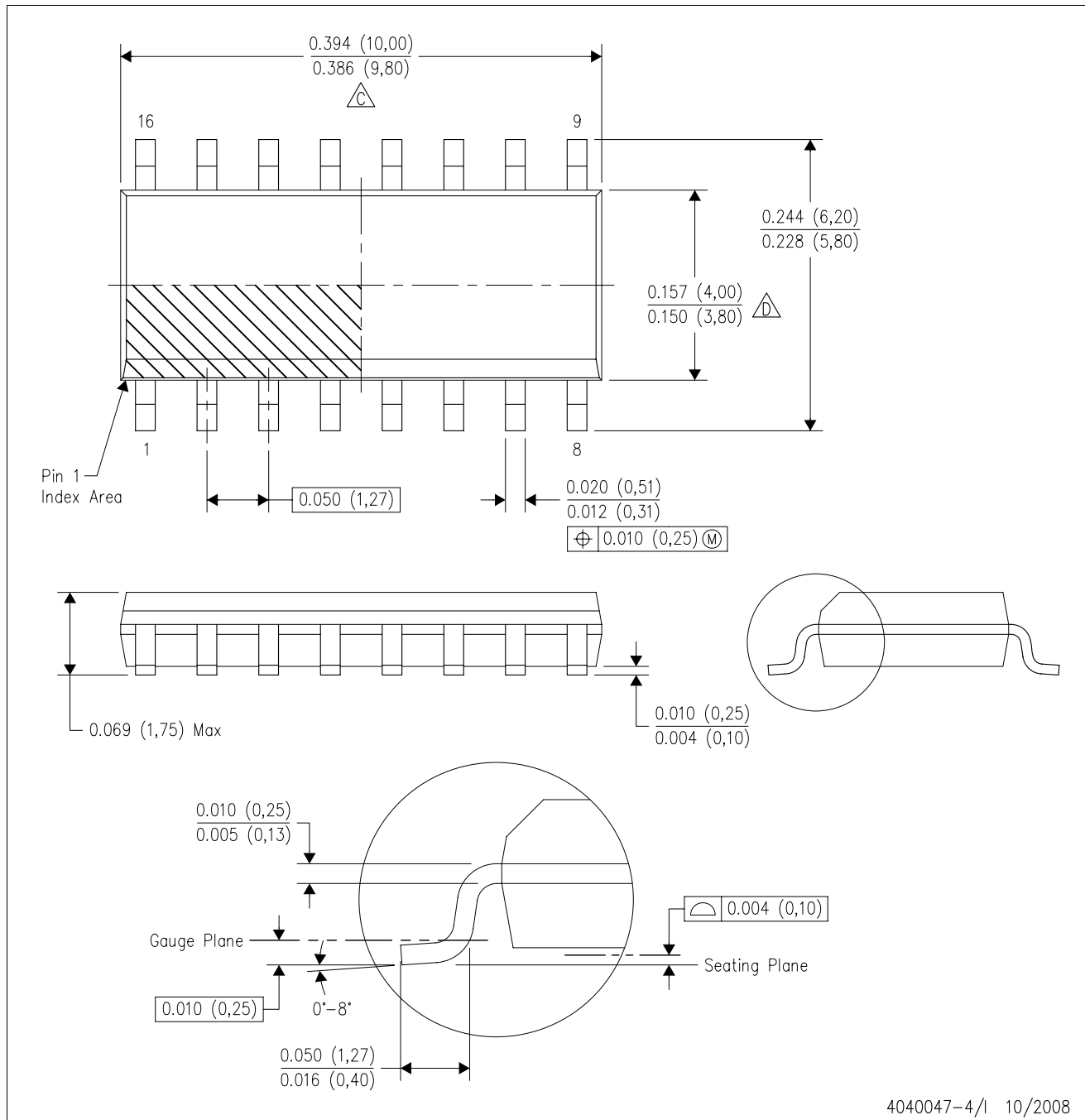


4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

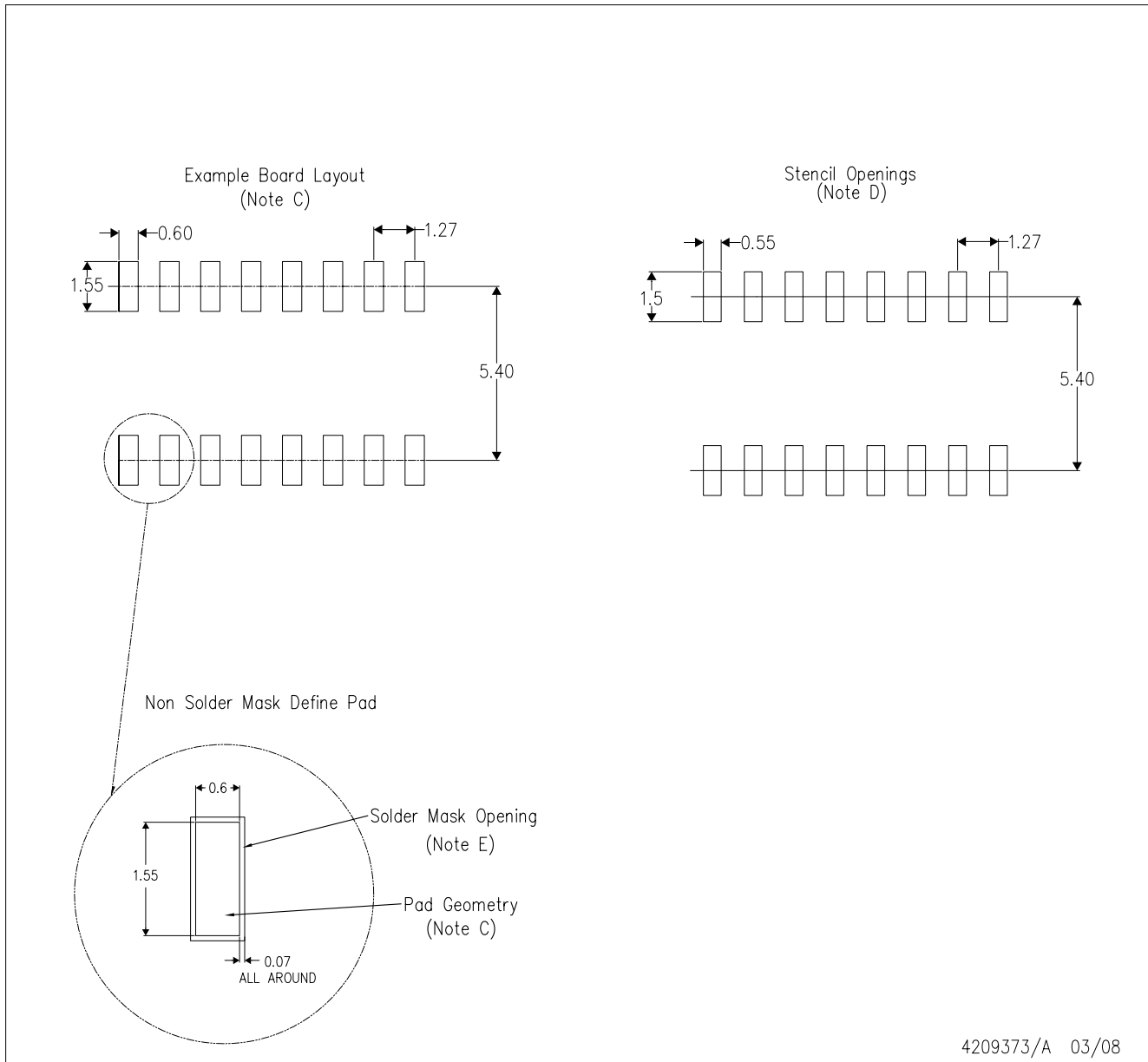
D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AC.

D(R-PDSO-G16)



4209373/A 03/08

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>

### Applications

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