Constant-Voltage Constant-Current Flyback Controller Using Opto-Coupled Feedback

Check for Samples: UCC28740

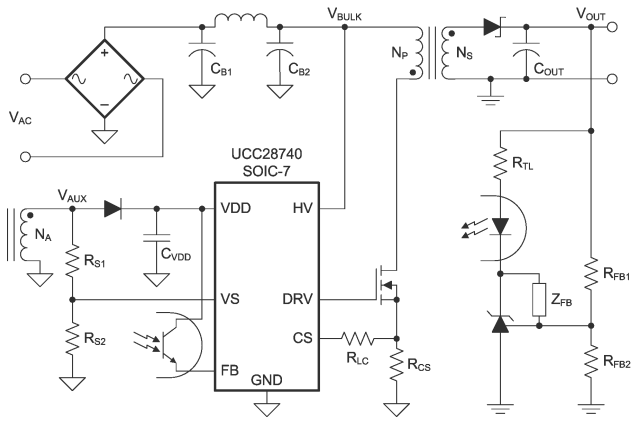
FEATURES

- **Less than 10-mW No-Load Power Capability**
- **Opto-Coupled Feedback for CV, and Primary-Side Regulation (PSR) for CC**
- **Enables ±1% Voltage Regulation and ±5% Current Regulation Across Line and Load**
- **700-V Startup Switch**
- **100-kHz Maximum Switching Frequency Enables High-Power-Density Charger Designs**
- **Resonant-Ring Valley-Switching Operation for Highest Overall Efficiency**
- **Frequency Dithering to Ease EMI Compliance**
- **Clamped Gate-Drive Output for MOSFET**
- **Overvoltage, Low-Line, and Overcurrent Protection Functions**
- **SOIC-7 Package**

APPLICATIONS

- **USB-Compliant Adapters and Chargers for Consumer Electronics**
  - **Smart Phones**
  - **Tablet Computers**
  - **Cameras**
- **Standby Supply for TV and Desktop**
- **White Goods**

SIMPLIFIED APPLICATION DIAGRAM



DESCRIPTION

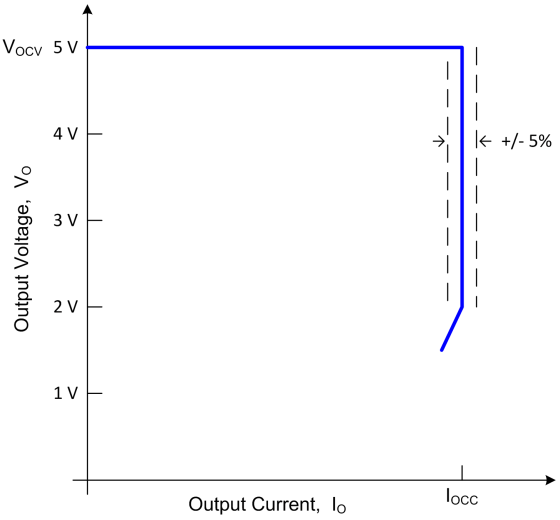
The UCC28740 isolated-flyback power-supply controller provides Constant-Voltage (CV) using an optical coupler to improve transient response to large-load steps. Constant-Current (CC) regulation is accomplished through Primary-side Regulation (PSR) techniques. This device processes information from opto-coupled feedback and an auxiliary flyback winding for precise high-performance control of output voltage and current.

An internal 700-V startup switch, dynamically-controlled operating states, and a tailored modulation profile support ultra-low standby power without sacrificing startup time or output transient response.

Control algorithms in the UCC28740 allow operating efficiencies to meet or exceed applicable standards. The drive output interfaces to a MOSFET power switch. Discontinuous conduction mode (DCM) with valley-switching reduces switching losses. Modulation of switching frequency and primary current-peak amplitude (FM and AM) keeps the conversion efficiency high across the entire load and line ranges.

The controller has a maximum switching frequency of 100 kHz and always maintains control of the peak-primary current in the transformer. Protection features keep primary and secondary component stresses in check. A minimum switching frequency of 170 Hz facilitates the achievement of less than 10-mW no-load power.

TYPICAL V-I DIAGRAM



PRODUCT PREVIEW

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PRODUCT INFORMATION(1)

PACKAGE	PINS	ORDERABLE DEVICES	MINIMUM SWITCHING FREQUENCY (Hz)	OPTIONS
SOIC (D)	7	UCC28740D	170	

(1) See *Orderable Addendum* for specific device ordering information.

ABSOLUTE MAXIMUM RATINGS(1)

		MIN	MAX	UNIT
Start-up pin voltage, HV	V_{HV}		700	V
Bias supply voltage, VDD	V_{VDD}		38	
Continuous gate-current sink	I_{DRV}		50	mA
Continuous gate-current source	I_{DRV}		Self-limiting	
Peak current, VS	I_{FB}		1	
Peak current, FB	I_{VS}		−1.2	
Gate-drive voltage at DRV	V_{DRV}	−0.5	Self-limiting	V
Voltage range	CS	−0.5	5	
	FB	−0.5	7	
	VS	−0.75	7	
Operating junction temperature range	T_J	−55	150	°C
Storage temperature	T_{STG}	−65	150	
Lead temperature 0.6 mm from case for 10 seconds			260	
ESD rating	Human-body model (HBM)		2000	V
	Charged-device model (CDM)		500	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal. These ratings apply over the operating ambient temperature ranges unless otherwise noted.

PRODUCT PREVIEW

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{VDD}	Bias-supply operating voltage	9		35	V
C_{VDD}	VDD bypass capacitor	0.047			µF
I_{FB}	Feedback current, continuous			50	µA
I_{VS}	VS pin current, out of pin			1	mA
T_J	Operating junction temperature	−20		125	°C

THERMAL INFORMATION

THERMAL METRIC(1)		UCC28740 D 7 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	141.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	73.8	
θ_{JB}	Junction-to-board thermal resistance(4)	89.0	
ψ_{JT}	Junction-to-top characterization parameter(5)	23.5	
ψ_{JB}	Junction-to-board characterization parameter(6)	88.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, V_{VDD} = 25 V, HV = open, V_{FB} = 0 V, V_{VS} = 4 V, T_A = –40°C to +125°C, T_J = T_A (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
HIGH-VOLTAGE START UP						
I_{HV}	Start-up current out of VDD	V_{HV} = 100 V, V_{VDD} = 0 V, start state	100	250	500	µA
$I_{HVLKG25}$	Leakage current at HV	V_{HV} = 400 V, run state, T_J = 25°C		0.01	0.5	
BIAS SUPPLY INPUT						
I_{RUN}	Supply current, run	I_{DRV} = 0, run state		2	2.65	mA
I_{WAIT}	Supply current, wait	I_{DRV} = 0, wait state		95	125	µA
I_{START}	Supply current, start	I_{DRV} = 0, V_{VDD} = 18 V, start state, I_{HV} = 0		18	30	
I_{FAULT}	Supply current, fault	I_{DRV} = 0, fault state		95	130	
UNDERVOLTAGE LOCKOUT						
$V_{VDD(on)}$	VDD turnon threshold	V_{VDD} low to high	19	21	23	V
$V_{VDD(off)}$	VDD turnoff threshold	V_{VDD} high to low	7.35	7.75	8.15	
VS INPUT						
V_{VSNC}	Negative clamp level	I_{VSLS} = –300 µA, volts below ground	190	250	325	mV
I_{VSB}	Input bias current	V_{VS} = 4 V	–0.25	0	0.25	µA
FB INPUT						
I_{FBMAX}	Full-range input current	f_{SW} = $f_{SW(min)}$	16	23	30	µA
V_{FBMAX}	Input voltage at full range	I_{FB} = 25 µA, T_J = 25°C	0.75	0.88	1	V
R_{FB}	FB-input resistance, linearized	ΔI_{FB} = 20 µA, centered at I_{FB} = 15 µA, T_J = 25°C	10	14	18	kΩ
CS INPUT						
$V_{CST(max)}$	Maximum CS threshold voltage	I_{FB} = 0 µA(1)	738	773	810	mV
$V_{CST(min)}$	Minimum CS threshold voltage	I_{FB} = 35 µA(1)	170	194	215	
K_{AM}	AM-control ratio	$V_{CST(max)}$ / $V_{CST(min)}$	3.6	4	4.45	V/V
V_{CCR}	Constant-current regulation factor		318	330	343	mV
K_{LC}	Line-compensation current ratio	I_{VSLS} = –300 µA, I_{VSLS} / current out of CS pin	24	25	28.6	A/A
t_{CSLEB}	Leading-edge blanking time	DRV output duration, V_{CS} = 1 V	180	230	280	ns
DRIVERS						
I_{DRS}	DRV source current	V_{DRV} = 8 V, V_{VDD} = 9 V	20	25		mA
R_{DRVLS}	DRV low-side drive resistance	I_{DRV} = 10 mA		6	12	Ω
V_{DRCL}	DRV clamp voltage	V_{VDD} = 35 V		14	16	V
R_{DRVSS}	DRV pulldown in start-state		150	190	230	kΩ
TIMING						
$f_{SW(max)}$	Maximum switching frequency	I_{FB} = 0 µA(1)	91	100	106	kHz
$f_{SW(min)}$	Minimum switching frequency	I_{FB} = 35 µA(1)	140	170	210	Hz
t_{ZTO}	Zero-crossing timeout delay		1.8	2.1	2.55	µs

(1) This device automatically varies the control frequency and current sense thresholds to improve EMI performance. These threshold voltages and frequency limits represent average levels.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, V_{VDD} = 25 V, HV = open, V_{FB} = 0 V, V_{VS} = 4 V, T_A = –40°C to +125°C, T_J = T_A (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
PROTECTION						
V_{OVP}	Overvoltage threshold	At VS input, T_J = 25°C(2)	4.55	4.6	4.71	V
V_{OCP}	Overcurrent threshold	At CS input	1.4	1.5	1.6	
$I_{VSL(run)}$	VS line-sense run current	Current out of VS pin increasing	190	225	275	µA
$I_{VSL(stop)}$	VS line-sense stop current	Current out of VS pin decreasing	70	80	100	
K_{VSL}	VS line sense ratio	$I_{VSL(run)}$ / $I_{VSL(stop)}$	2.45	2.8	3.05	A/A
$T_{J(stop)}$	Thermal-shutdown temperature	Internal junction temperature		165		°C

(2) The overvoltage threshold level at VS decreases with increasing temperature by 0.8 mV/°C. This compensation is included to reduce the power-supply output overvoltage detection variance over temperature.

PRODUCT PREVIEW

DEVICE INFORMATION

Functional Block Diagram

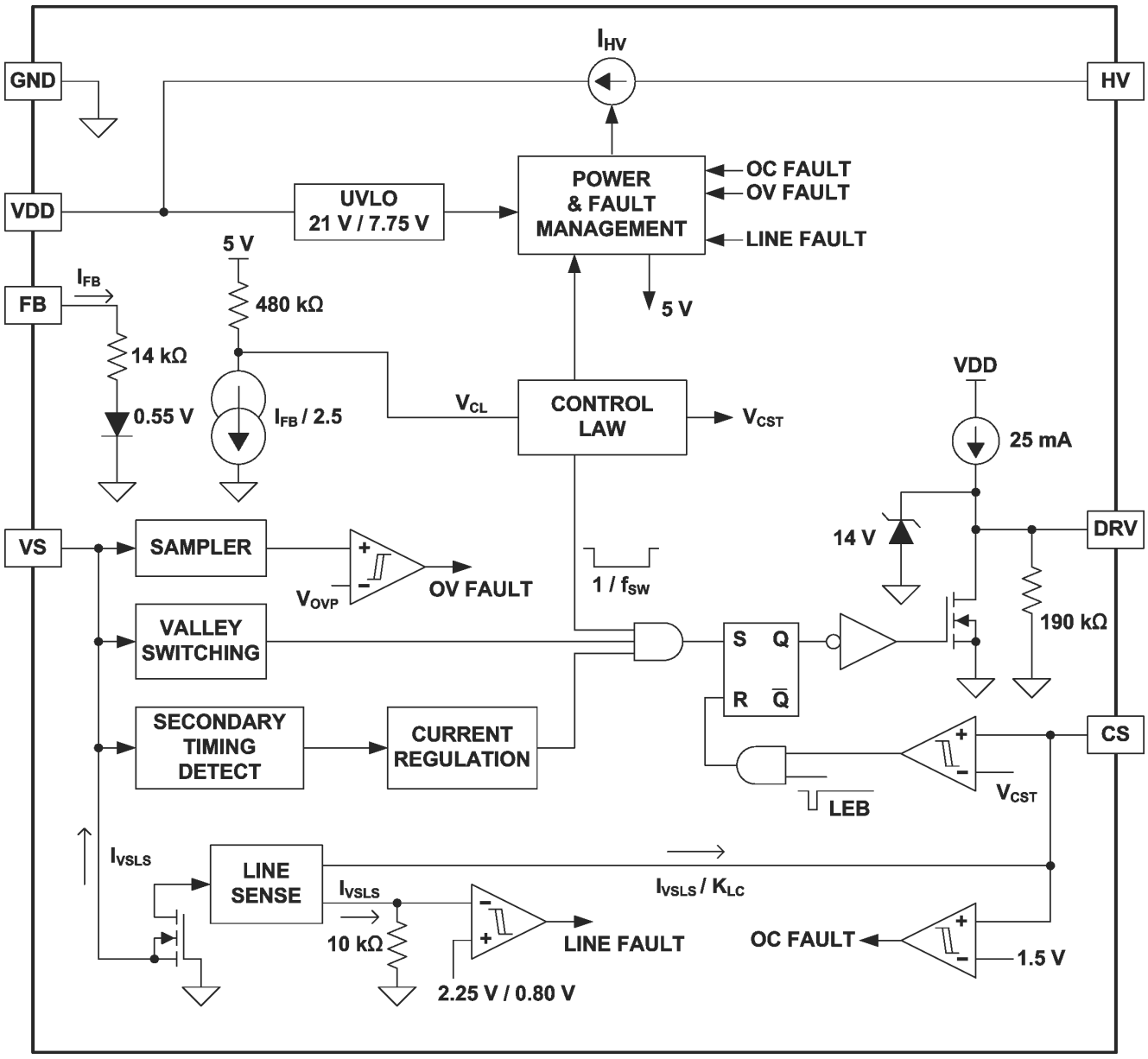
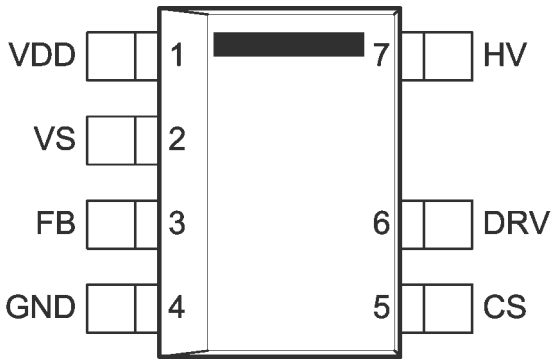


Figure 1. Functional Block Diagram

PRODUCT PREVIEW

SOIC (D) PACKAGE
7 PINS
(TOP VIEW)



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
CS	5	I	The current-sense (CS) input connects to a ground-referenced current-sense resistor in series with the power switch. The resulting voltage monitors and controls the peak primary current. A series resistor is added to this pin to compensate for peak switch-current levels as the AC-mains input varies.
DRV	6	O	Drive (DRV) is an output that drives the gate of an external high-voltage MOSFET switching transistor.
FB	3	I	The feedback (FB) input receives a current signal from the optocoupler output transistor. An internal current mirror divides the feedback current by 2.5 and applies it to an internal pullup resistor to generate a control voltage, V_{CL}. The voltage at this resistor directly drives the control law function, which determines the switching frequency and the peak amplitude of the switching current .
GND	4	—	The ground (GND) pin is both the reference pin for the controller, and the low-side return for the drive output. Special care must be taken to return all AC-decoupling capacitors as close as possible to this pin and avoid any common trace length with analog signal-return paths.
HV	7	I	The high-voltage (HV) pin may connect directly, or through a series resistor, to the rectified bulk voltage and provides a charge to the VDD capacitor for the startup of the power supply.
VDD	1	I	VDD is the bias-supply input pin to the controller. A carefully-placed bypass capacitor to GND is required on this pin.
VS	2	I	Voltage sense (VS) is an input used to provide demagnetization timing feedback to the controller to limit frequency, to control constant-current operation, and to provide output-overvoltage detection. VS is also used for AC-mains input-voltage detection for peak primary-current compensation. This pin connects to a voltage divider between an auxiliary winding and GND. The value of the upper resistor of this divider programs the AC-mains run and stop thresholds, and factors into line compensation at the CS pin.

Detailed Pin Description

VDD (Device Bias Voltage Supply) The VDD pin connects to a bypass capacitor-to-ground. The turnon UVLO threshold is 21 V and turnoff UVLO threshold is 7.75 V with an available operating range up to 35 V on VDD. The typical USB-charging specification requires the output current to operate in constant-current mode from 5 V down to at least 2 V which is achieved easily with a nominal V_{VDD} of approximately 25 V. The additional VDD headroom up to 35 V allows for V_{VDD} to rise due to the leakage energy delivered to the VDD capacitor during high-load conditions.

GND (Ground) UCC28740 has a single ground reference external to the device for the gate-drive current and analog signal reference. Place the VDD-bypass capacitor close to GND and VDD with short traces to minimize noise on the VS, FB, and CS signal pins.

HV (High-Voltage Startup) The HV pin connects directly to the bulk capacitor to provide a startup current to the VDD capacitor. The typical startup current is approximately 250 µA which provides fast charging of the VDD capacitor. The internal HV startup device is active until V_{VDD} exceeds the turnon UVLO threshold of 21 V at which time the HV startup device turns off. In the off state the HV leakage current is very low to minimize standby losses of the controller. When V_{VDD} falls below the 7.75 V UVLO turnoff threshold the HV startup device turns on.

VS (Voltage Sense) The VS pin connects to a resistor-divider from the auxiliary winding to ground. The auxiliary voltage waveform is sampled at the end of the transformer secondary-current demagnetization time to provide accurate control of the output current when in constant-current mode. The waveform on the VS pin determines the timing information to achieve valley-switching, and the timing to control the duty-cycle of the transformer secondary current. Avoid placing a filter capacitor on this input which interferes with accurate sensing of this waveform.

During the MOSFET on-time, this pin also senses VS current generated through R_{S1} by the reflected bulk-capacitor voltage to provide for AC-input run and stop thresholds, and to compensate the current-sense threshold across the AC-input range. For the AC-input run/stop function, the run threshold on VS is 225 µA and the stop threshold is 80 µA.

At the end of off-time demagnetization, the reflected output voltage is sampled at this pin to provide output overvoltage protection. The values for the auxiliary voltage-divider upper-resistor, R_{S1}, and lower-resistor, R_{S2}, are determined by Equation 1 and Equation 2.

$$R_{S1} = \frac{V_{IN(run)} \times \sqrt{2}}{N_{PA} \times I_{VSL(run)}} \quad (1)$$

where

- N_{PA} is the transformer primary-to-auxiliary turns-ratio,
- $V_{IN(run)}$ is the AC RMS voltage to enable turnon of the controller (run), (in case of DC input, leave out the $\sqrt{2}$ term in the equation),
- $I_{VSL(run)}$ is the run-threshold for the current pulled out of the VS pin during the switch on-time (see ELECTRICAL CHARACTERISTICS).

$$R_{S2} = \frac{R_{S1} \times V_{OVP}}{N_{AS} \times (V_{OV} - V_F) - V_{OVP}} \quad (2)$$

where

- V_{OV} is the maximum allowable peak voltage at the converter output,
- V_F is the output-rectifier forward drop at near-zero current,
- N_{AS} is the transformer auxiliary-to-secondary turns-ratio,
- R_{S1} is the VS divider high-side resistance,
- V_{OVP} is the overvoltage detection threshold at the VS input (see ELECTRICAL CHARACTERISTICS).

PRODUCT PREVIEW

FB (Feedback) The FB pin connects to the emitter of an analog-optocoupler output transistor which usually has the collector connected to VDD. The current supplied to FB by the optocoupler is reduced internally by a factor of 2.5 and the resulting current is applied to an internal 480-kΩ resistor to generate the control law voltage (V_{CL}). This V_{CL} directly determines the converter switching frequency and peak primary current required for regulation per the control-law for any given line and load condition.

DRV (Gate Drive) The DRV pin connects to the MOSFET gate pin, usually through a series resistor. The gate driver provides a gate-drive signal limited to 14 V. The turnon characteristic of the driver is a 25-mA current source which limits the turnon dv/dt of the MOSFET drain and reduces the leading-edge current spike while still providing a gate-drive current to overcome the Miller plateau. The gate-drive turnoff current is determined by the R_{DSON} of the low-side driver along with any external gate-drive resistance. Adding external gate resistance reduces the MOSFET drain turn-off dv/dt, if necessary.

CS (Current Sense) The current-sense pin connects through a series resistor (R_{LC}) to the current-sense resistor (R_{CS}). The maximum current-sense threshold ($V_{CST(max)}$) is 0.773 V for $I_{PP(max)}$, and the minimum current-sense threshold ($V_{CST(min)}$) is 0.194 V for $I_{PP(min)}$. R_{LC} provides the feed-forward line compensation to eliminate changes in I_{PP} with input voltage due to the propagation delay of the internal comparator and MOSFET turnoff time. An internal leading-edge blanking time of 235 ns eliminates sensitivity to the MOSFET turnon current spike. Placing a bypass capacitor on the CS pin is unnecessary. The target output current in constant-current (CC) regulation determines the value of R_{CS}. The values of R_{CS} and R_{LC} are calculated using Equation 3 and Equation 4. The term V_{CCR} is the product of the demagnetization constant, 0.425, and $V_{CST(max)}$. $V_{CCR}$is held to a tighter accuracy than either of its constituent terms. The term η_{XFMR} accounts for the energy stored in the transformer but not delivered to the secondary. This term includes transformer resistance and core loss, bias power, and primary-to-secondary leakage ratio.

Example:

With a transformer core and winding loss of 5%, primary-to-secondary leakage inductance of 3.5%, and bias power to output power ratio of 0.5%, the η_{XFMR} value at full power is approximately: 1 - 0.05 - 0.035 - 0.005 = 0.91.

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2I_{OCC}} \times \sqrt{\eta_{XFMR}} \quad (3)$$

where

- V_{CCR} is a constant-current regulation factor (see ELECTRICAL CHARACTERISTICS),
- N_{PS} is the transformer primary-to-secondary turns-ratio (a ratio of 13 to 15 is typical for 5-V output),
- I_{OCC} is the target output current in constant-current regulation,
- η_{XFMR} is the transformer efficiency at full power.

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times t_D \times N_{PA}}{L_P} \quad (4)$$

where

- R_{S1} is the VS pin high-side resistor value,
- R_{CS} is the current-sense resistor value,
- t_D is the total current-sense delay consisting of MOSFET turnoff delay, plus approximately 50 ns internal delay,
- N_{PA} is the transformer primary-to-auxiliary turns-ratio,
- L_P is the transformer primary inductance,
- K_{LC} is a current-scaling constant for line compensation (see ELECTRICAL CHARACTERISTICS).

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

V_{VDD} = 25 V, T_J = 25°C, unless otherwise noted.

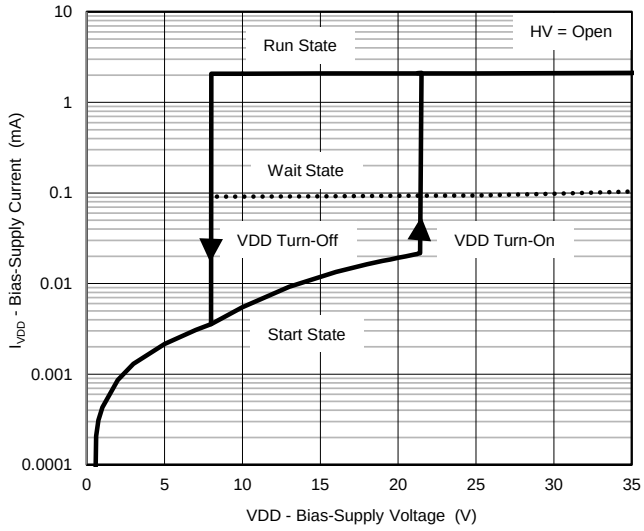


Figure 2. Bias-Supply Current vs. Bias-Supply Voltage

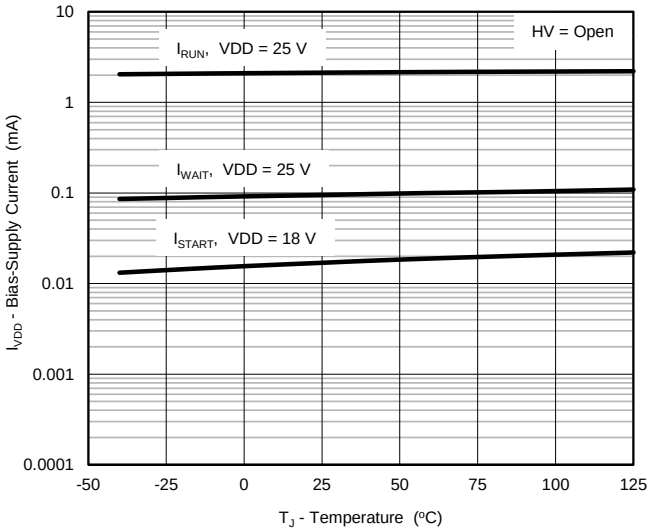


Figure 3. Bias-Supply Current vs. Temperature

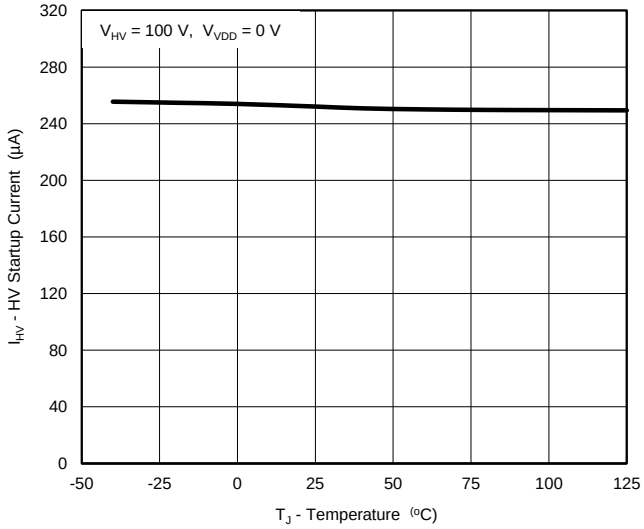


Figure 4. HV Startup Current vs. Temperature

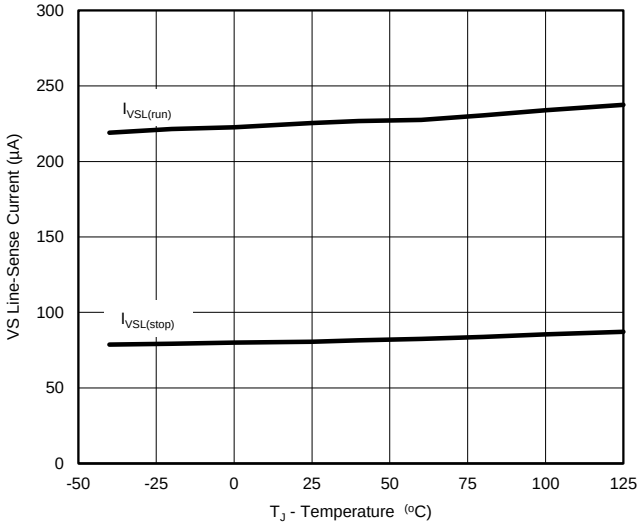


Figure 5. VS Line-Sense Currents vs. Temperature

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

V_{VDD} = 25 V, T_J = 25°C, unless otherwise noted.

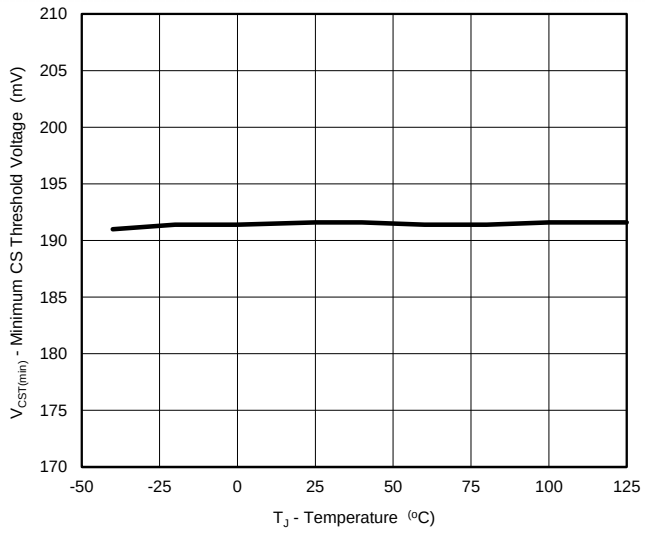


Figure 6. Minimum CS Threshold vs. Temperature

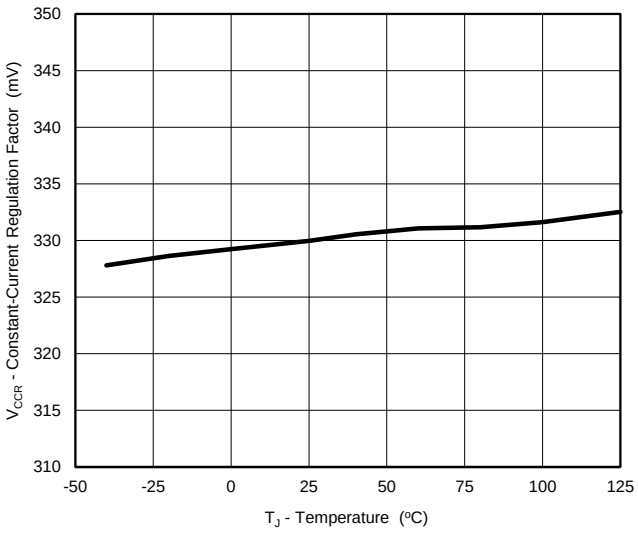


Figure 7. Constant-Current Regulation Factor vs. Temperature

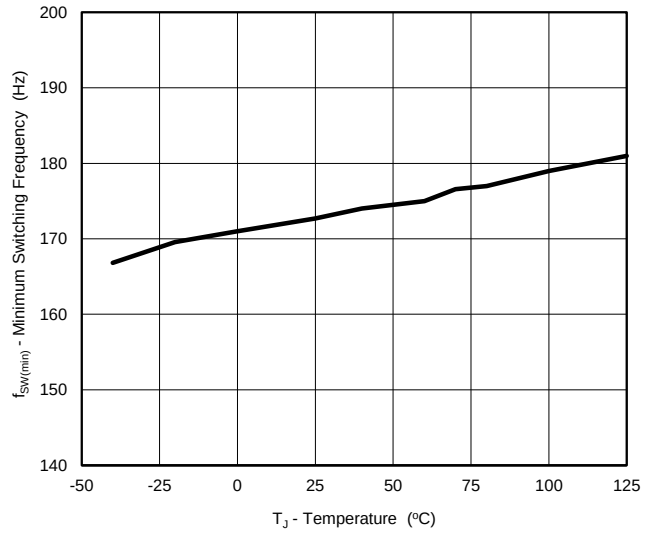


Figure 8. Minimum Switching Frequency vs. Temperature

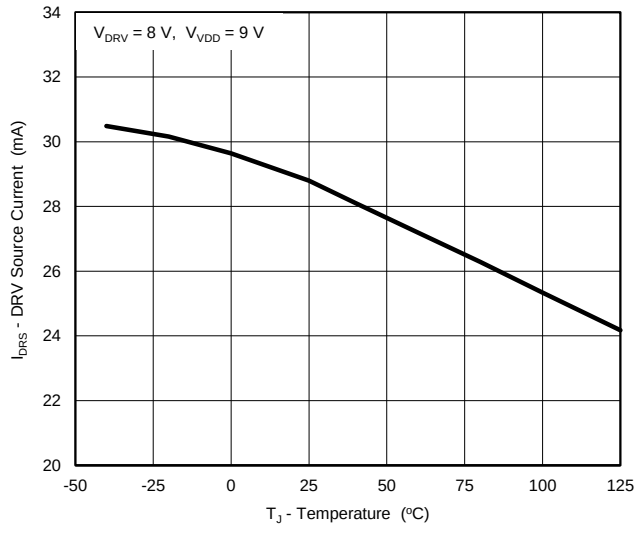


Figure 9. DRV Source Current vs. Temperature

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

V_{VDD} = 25 V, T_J = 25°C, unless otherwise noted.

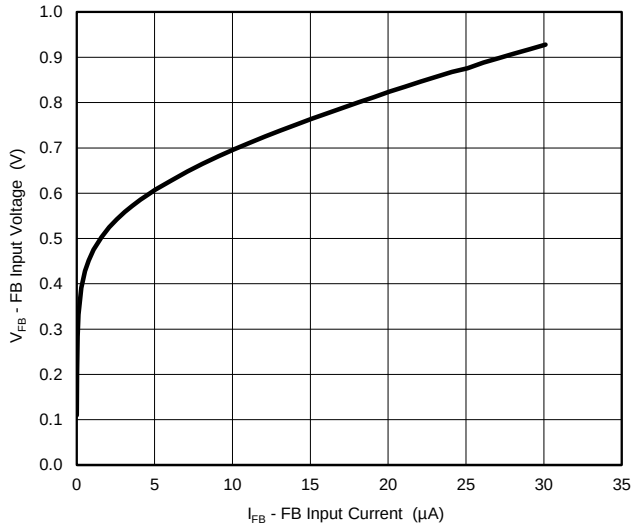


Figure 10. FB Input Voltage vs. FB Input Current

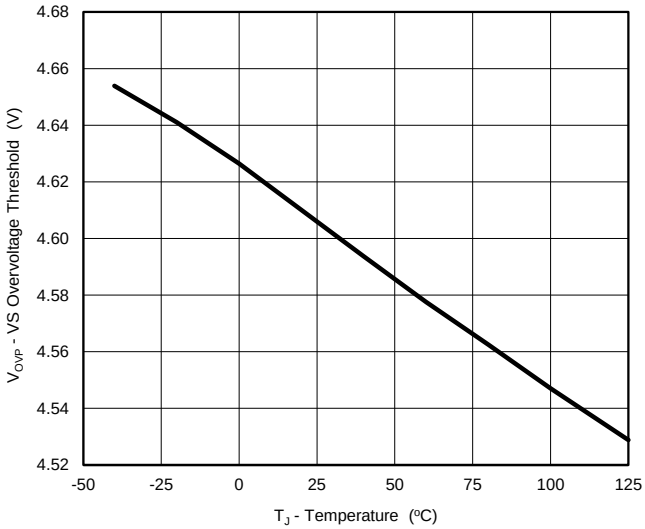


Figure 11. VS Overvoltage Threshold vs. Temperature

PRODUCT PREVIEW

FUNCTIONAL DESCRIPTION

The UCC28740 is a flyback power-supply controller which provides high-performance voltage regulation using an optically-coupled feedback signal from a secondary-side voltage regulator. The device provides accurate constant-current regulation using primary-side feedback. The controller operates in discontinuous-conduction mode (DCM) with valley-switching to minimize switching losses. The control law scheme combines frequency with primary peak-current amplitude modulation to provide high conversion efficiency across the load range. The control law provides a wide dynamic operating range of output power which allows the power-supply designer to easily achieve less than 30-mW standby power dissipation using a standard shunt-regulator and optocoupler. For a target of less than 10-mW standby power, careful loss-management design with a low-power regulator and high-CTR optocoupler is required.

During low-power operating conditions, the power-management features of the controller reduce the device-operating current at switching frequencies below 32 kHz. At and above this frequency, the UCC28740 includes features in the modulator to reduce the EMI peak energy of the fundamental switching frequency and harmonics. A complete low-cost and low component-count charger-solution is realized using a straight-forward design process.

Secondary-Side Optically-Coupled Constant-Voltage (CV) Regulation

Figure 12 shows a simplified flyback convertor with the main output-regulation blocks of the device shown, along with typical implementation of secondary-side-derived regulation. The power-train operation is the same as any DCM-flyback circuit. A feedback current is optically coupled to the controller from a shunt-regulator sensing the output voltage.

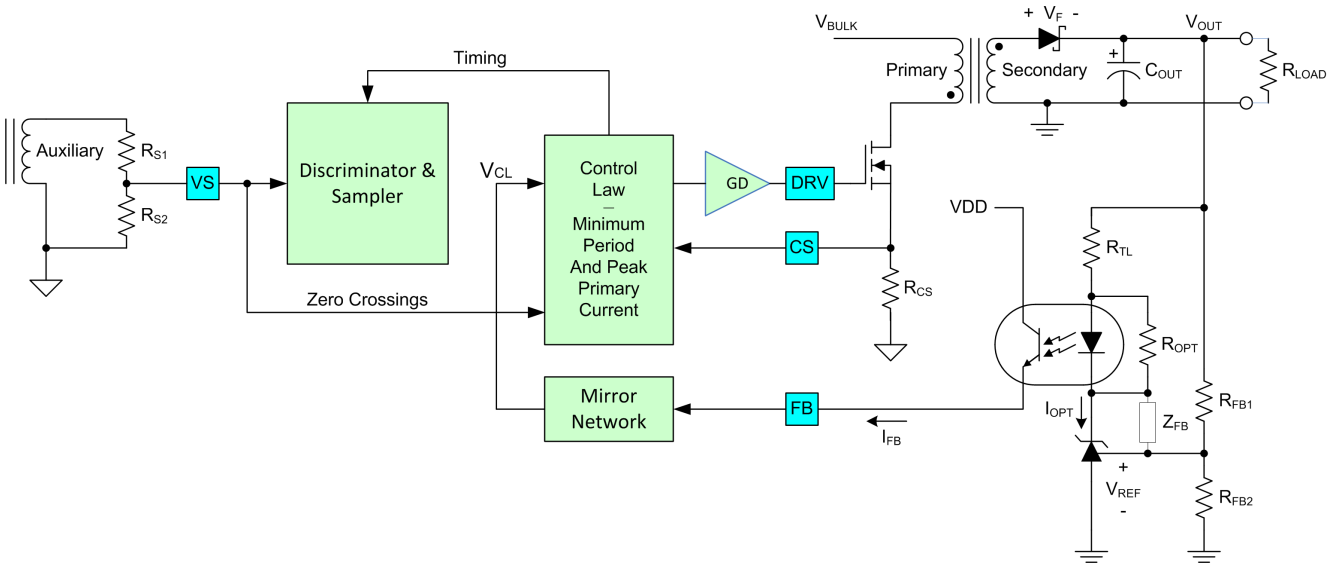


Figure 12. Simplified Flyback Convertor (With The Main Voltage Regulation Blocks)

In this configuration, a secondary-side shunt-regulator, such as the TL431, generates a current through the input photo-diode of an optocoupler. The photo-transistor delivers a proportional current that is dependent on the current-transfer ratio (CTR) of the optocoupler to the FB input of the UCC28740 controller. This FB current then converts into the V_{CL} by the input-mirror network, detailed in the device block diagram (see Figure 1). Output-voltage variations convert to FB-current variations. The FB-current variations modify the V_{CL} which dictates the appropriate I_{PP} and f_{SW} necessary to maintain CV regulation. At the same time, the VS input senses the auxiliary winding voltage during the transfer of transformer energy to the secondary output to monitor for an output overvoltage condition. When f_{SW} reaches the target maximum frequency, chosen between 32 kHz and 100 kHz, CC operation is entered and further increases in V_{CL} have no effect.

PRODUCT PREVIEW

Figure 13 shows that as the secondary current decreases to zero, a clearly-defined down slope reflects the decreasing rectifier V_F combined with stray resistance voltage-drop ($I_S R_S$). To achieve an accurate representation of the secondary output voltage on the auxiliary winding, the discriminator reliably blocks the leakage-inductance reset and ringing while continuously sampling the auxiliary voltage during the down slope after the ringing diminishes. The discriminator then captures the voltage signal at the moment that the secondary-winding current reaches zero. The internal overvoltage threshold on VS is 4.6 V. Temperature compensation of –0.8 mV/°C on the overvoltage threshold offsets the change in the output-rectifier forward voltage with temperature. The resistor divider is selected as outlined in the VS pin description (see Detailed Pin Description).

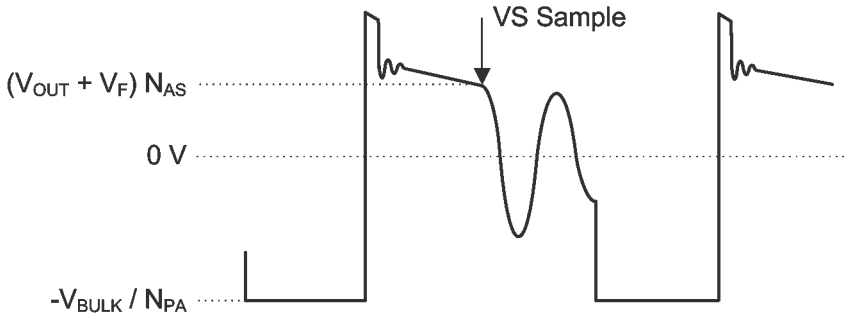


Figure 13. Auxiliary-Winding Voltage

The UCC28740 VS-signal sampler includes signal-discrimination methods to ensure an accurate sample of the output voltage from the auxiliary winding. Controlling some details of the auxiliary-winding signal to ensure reliable operation is necessary; specifically, the reset time of the leakage inductance and the duration of any subsequent leakage-inductance ringing. See Figure 14 for a detailed illustration of waveform criteria to ensure a reliable sample on the VS pin.

The first detail to examine is the duration of the leakage-inductance reset pedestal, t_{LK_RESET}, in Figure 14. Because t_{LK_RESET} mimics the waveform of the secondary-current decay, followed by a sharp downslope, t_{LK_RESET} is internally blanked for a duration which scales with the peak primary current. Keeping the leakage-reset time to less than 600 ns for $I_{PP(min)}$, and less than 2.2 µs for $I_{PP(max)}$ is important.

The second detail is the amplitude of ringing on the V_{AUX} waveform following t_{LK_RESET}. The peak-to-peak voltage variation at the VS pin must be less than 100 mVp-p for at least 200 ns before the end of the demagnetization time (t_{DM}). A concern with excessive ringing usually occurs during light or no-load conditions, when t_{DM} is at the minimum. The tolerable ripple on VS is scaled up to the auxiliary-winding voltage by R_{S1} and R_{S2}, and is equal to 100 mV × (R_{S1} + R_{S2}) / R_{S2} .

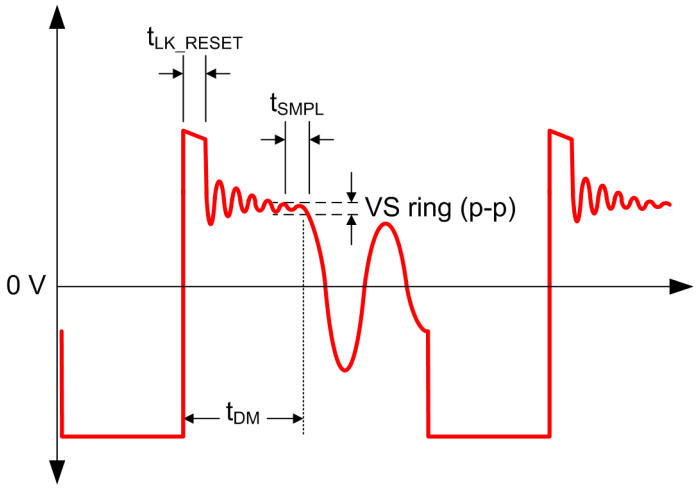


Figure 14. Auxiliary-Winding Waveform Details

During voltage regulation, the controller operates in frequency-modulation mode and amplitude-modulation mode, as shown in Figure 15. The internal operating-frequency limits of the device are 100 kHz and $f_{SW(min)}$. The maximum operating frequency of the converter at full-load is generally chosen to be slightly lower than 100 kHz to allow for tolerances, or significantly lower due to switching-loss considerations. The maximum operating frequency and primary peak current chosen determine the transformer primary inductance of the converter. The shunt-regulator bias power, output preload resistor (if any), and low-power conversion efficiency determine the minimum-operating frequency of the converter. Voltage-loop stability compensation is applied at the shunt-regulator which drives the opto-coupled feedback signal. The tolerances chosen for the shunt-regulator reference and the sense resistors determines the regulation accuracy.

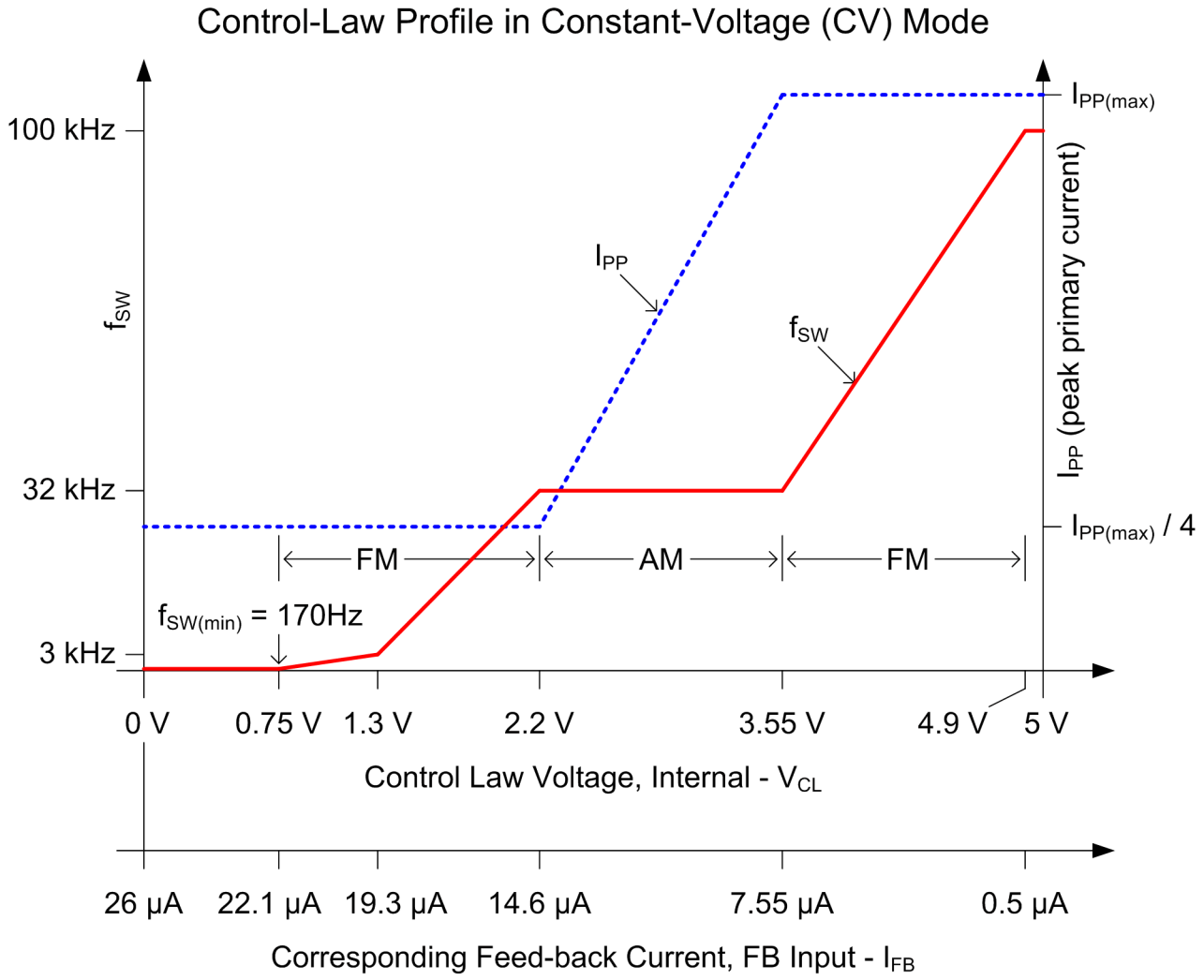


Figure 15. Frequency And Amplitude Modulation Modes (During CV Regulation)

The level of feedback current (I_{FB}) into the FB pin determines the internal V_{CL} which determines the operating point of the controller while in CV mode. When I_{FB} rises above 22 µA, no further decrease in f_{SW} occurs. When the output-load current increases to the point where maximum f_{SW} is reached, control transfers to CC mode. All current, voltage, frequency, breakpoints, and curve-segment linearity depicted in Figure 15 are nominal. Figure 15 indicates the general operation of the controller while in CV mode, although minor variations may occur from part to part. An internal frequency-dithering mechanism is enabled when I_{FB} is less than 14.6 µA to help reduce conducted EMI (including during CC-mode operation), and is disabled otherwise.

PRODUCT PREVIEW

Primary-Side Constant-Current (CC) Regulation

When the load current of the converter increases to the predetermined constant-current limit, operation enters CC mode. In CC mode, output voltage regulation is lost and the shunt-regulator drives the current and voltage at FB to minimum. During CC mode, timing information at the VS pin and current information at the CS pin allow accurate regulation of the average current of the secondary winding. The CV-regulation control law dictates that as load increases approaches CC regulation the primary peak current will be at $I_{PP(max)}$. The primary peak current, turns-ratio, demagnetization time t_{DM}, and switching period t_{SW} determine the secondary average output current (see Figure 16). Ignoring leakage-inductance effects, the average output current is given by Equation 5. When the demagnetization duty-cycle reaches the CC-regulation reference, D_{MAGCC}, in the current-control block, the controller operates in frequency modulation (FM) mode to control the output current for any output voltage at or below the voltage-regulation target as long as the auxiliary winding keeps V_{VDD} above the UVLO turnoff threshold. As the output voltage falls, t_{DM} increases. The controller acts to increase t_{SW} to maintain the ratio of t_{DM} to switching period (t_{DM} / t_{SW}) at a maximum of 0.425 (D_{MAGCC}), thereby maintaining a constant average output current.

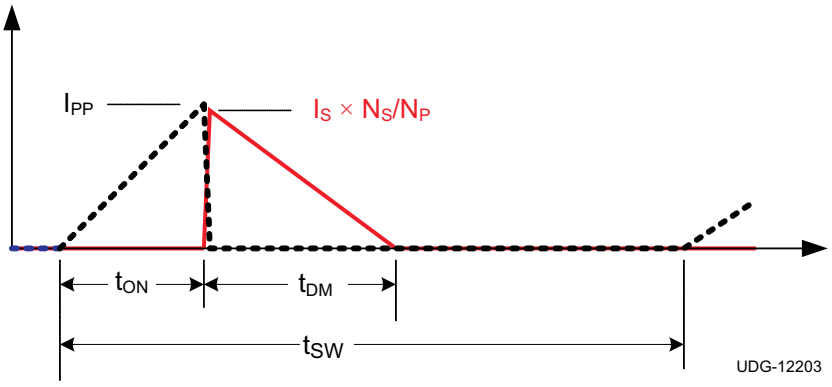


Figure 16. Transformer-Current Relationship

$$I_{OUT} = \frac{I_{PP}}{2} \times \frac{N_P}{N_S} \times \frac{t_{DM}}{t_{SW}} \quad (5)$$

Fast, accurate, opto-coupled CV control combined with line-compensated PSR CC control results in high-performance voltage and current regulation which minimizes voltage deviations due to heavy load and unload steps, as illustrated by the V-I curve in Figure 17.

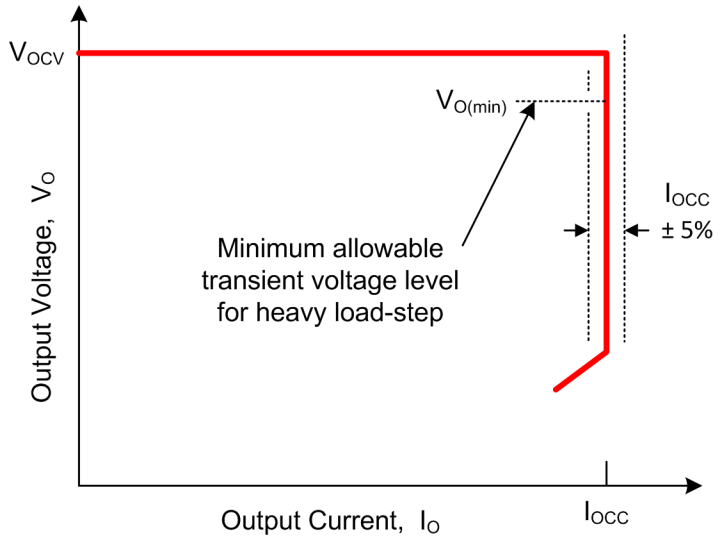


Figure 17. Typical Target Output V-I Characteristic

Valley-Switching and Valley-Skipping

The UCC28740 uses valley-switching to reduce switching losses in the MOSFET, to reduce induced-EMI, and to minimize the turnon current spike at the current-sense resistor. The controller operates in valley-switching in all load conditions unless the V_{DS} ringing diminishes to the point where valleys are no longer detectable.

As shown in Figure 18, the UCC28740 operates in a valley-skipping mode (also known as valley-hopping) in most load conditions to maintain an accurate voltage or current regulation point and still switch on the lowest available V_{DS} voltage.

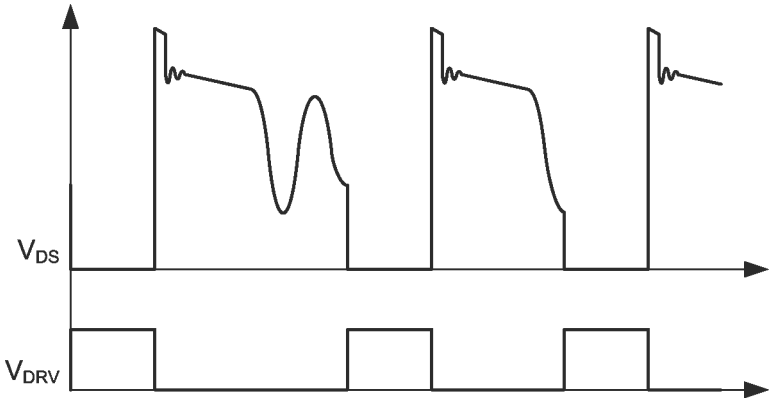


Figure 18. Valley-Skipping Mode

Valley-skipping modulates each switching cycle into discrete period durations. During FM operation, the switching cycles are periods when energy is delivered to the output in fixed packets, where the power-per-cycle varies discretely with the switching period. During operating conditions when the switching period is relatively short, such as at high-load and low-line, the average power delivered per cycle varies significantly based on the number of valleys skipped between cycles. As a consequence, valley-skipping adds additional ripple voltage to the output with a frequency and amplitude dependent upon the loop-response of the shunt-regulator. For a load with an average power level between that of cycles with fewer valleys skipped and cycles with more valleys skipped, the voltage-control loop modulates the FB current according to the loop-bandwidth and toggles between longer and shorter switching periods to match the required average output power.

Startup Operation

An internal high-voltage startup switch, connected to the bulk-capacitor voltage (V_{BULK}) through the HV pin, charges the VDD capacitor. This startup switch functions similarly to a current source providing typically 250 µA to charge the VDD capacitor. When V_{VDD} reaches the 21-V UVLO turnon threshold the controller is enabled, the converter starts switching, and the startup switch turns off.

Often at initial turnon, the output capacitor is in a fully-discharged state. The first three switching-cycle current peaks are limited to $I_{PP(min)}$ to monitor for any initial input or output faults with limited power delivery. After these three cycles, if the sampled voltage at VS is less than 1.33 V, the controller operates in a special startup mode. In this mode, the primary current peak amplitude of each switching cycle is limited to approximately 0.63 × $I_{PP(max)}$ and D_{MAGCC} increases from 0.425 to 0.735. These modifications to $I_{PP(max)}$ and D_{MAGCC} during startup allows high-frequency charge-up of the output capacitor to avoid audible noise while the demagnetization voltage is low. Once the sampled VS voltage exceeds 1.38 V, D_{MAGCC} is restored to 0.425 and the primary current peak resumes as $I_{PP(max)}$. While the output capacitor charges, the converter operates in CC mode to maintain a constant output current until the output voltage enters regulation. Thereafter, the controller responds to the condition dictated by the control law. The time to reach output regulation consists of the time the VDD capacitor charges to 21 V plus the time the output capacitor charges.

PRODUCT PREVIEW

Fault Protection

The UCC28740 provides extensive fault protection. The protection functions include:

- Output overvoltage
- Input undervoltage
- Internal overtemperature
- Primary overcurrent fault
- CS-pin fault
- VS-pin fault

A UVLO reset and restart sequence applies to all fault-protection events.

The output-overvoltage function is determined by the voltage feedback on the VS pin. If the voltage sample of VS exceeds 4.6 V, the device stops switching and the internal current consumption becomes I_{FAULT} which discharges the VDD capacitor to the UVLO-turnoff threshold. After that, the device returns to the start state and a startup sequence ensues.

The UCC28740 always operates with cycle-by-cycle primary peak current control. The normal operating voltage range of the CS pin is 0.773 V to 0.194 V. An additional protection, not filtered by leading-edge blanking, occurs if the CS pin voltage reaches 1.5 V, which results in a UVLO reset and restart sequence.

Current into the VS pin during the MOSFET on-time determines the line-input run and stop thresholds. While the VS pin clamps close to GND during the MOSFET on-time, the current through R_{S1} is monitored to determine a sample of V_{BULK}. A wide separation of the run and stop thresholds allows for clean startup and shutdown of the power supply with the line voltage. The run-current threshold is 225 µA and the stop-current threshold is 80 µA.

The internal overtemperature-protection threshold is 165°C. If the junction temperature reaches this threshold the device initiates a UVLO-reset cycle. If the temperature is still high at the end of the UVLO cycle, the protection cycle repeats.

Protection is included in the event of component failures on the VS pin. If complete loss of feedback information on the VS pin occurs, the controller stops switching and restarts.

DESIGN PROCEDURE

This procedure outlines the steps to design a constant-voltage, constant-current flyback converter using the UCC28740 controller. See Figure 19 for component names and network locations. The design procedure equations use terms that are defined below.

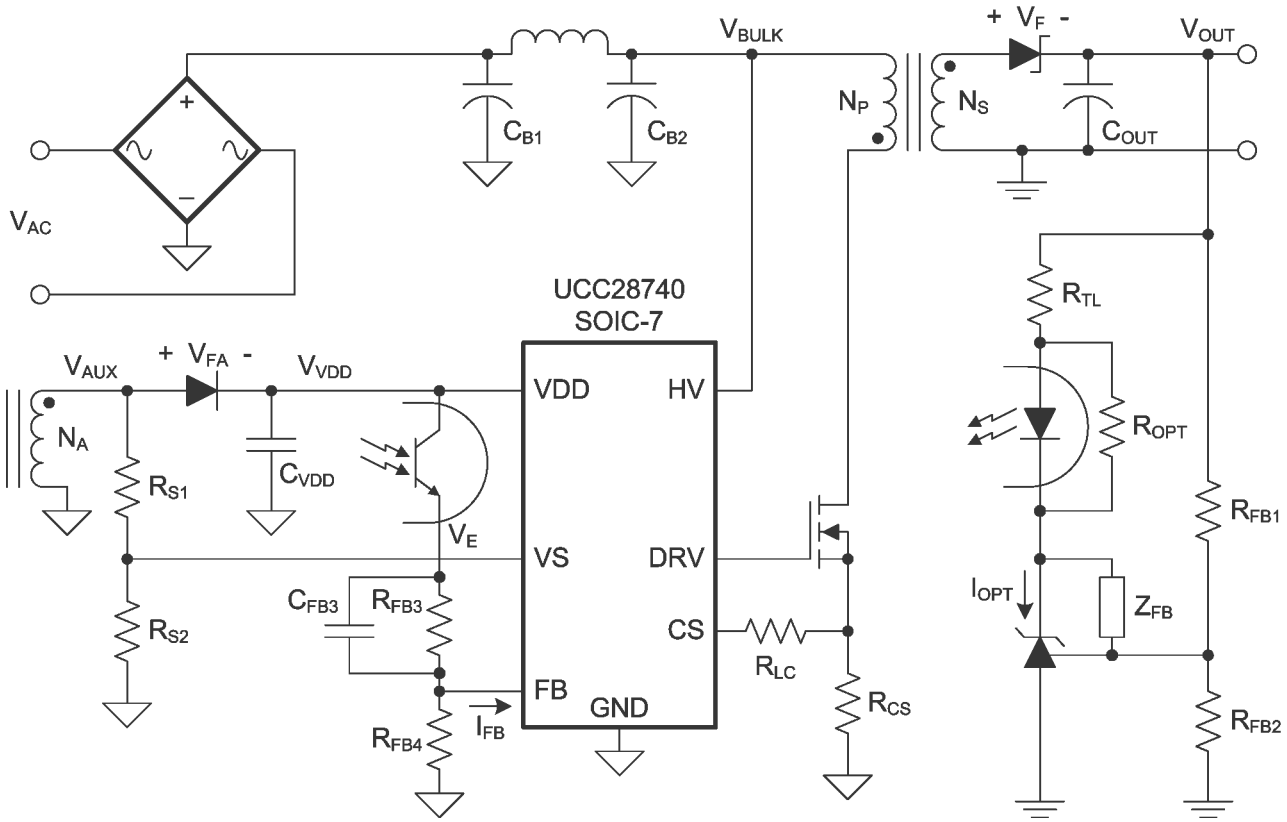


Figure 19. Design Procedure Application Example

Definition of Terms

Capacitance Terms in Farads

C_{BULK} The total input capacitance of C_{B1} and C_{B2}.

C_{VDD} The minimum required capacitance on the VDD pin.

C_{OUT} The minimum output capacitance required.

Duty Cycle Terms

D_{MAGCC} The secondary diode conduction duty-cycle limit in CC mode, 0.425.

D_{MAX} MOSFET on-time duty-cycle.

Frequency Terms in Hertz

f_{LINE} The minimum input-line frequency.

f_{MAX} The target full-load maximum switching frequency of the converter.

f_{MIN} The steady-state minimum switching frequency of the converter.

$f_{SW(min)}$ The minimum possible switching frequency (see ELECTRICAL CHARACTERISTICS).

PRODUCT PREVIEW

Current Terms in Amperes

I_{OCC} The converter output constant-current target.

$I_{PP(max)}$ The maximum transformer primary peak current.

I_{START} The startup bias-supply current (see ELECTRICAL CHARACTERISTICS).

I_{TRAN} The required positive load-step current.

$I_{VSL(run)}$ The VS-pin run current (see ELECTRICAL CHARACTERISTICS).

Current and Voltage Scaling Terms

K_{AM} The maximum-to-minimum peak primary current ratio (see ELECTRICAL CHARACTERISTICS).

K_{LC} The current-scaling constant for line compensation(see ELECTRICAL CHARACTERISTICS).

Transformer Terms

L_P The transformer primary inductance.

N_{AS} The transformer auxiliary-to-secondary turns-ratio.

N_{PA} The transformer primary-to-auxiliary turns-ratio.

N_{PS} The transformer primary-to-secondary turns-ratio.

Power Terms in Watts

P_{IN} The converter maximum input power.

P_{OUT} The full-load output power of the converter.

P_{SB} The total standby power.

Resistance Terms in Ohms

R_{CS} The primary peak-current programming resistance.

R_{ESR} The total ESR of the output capacitor(s).

R_{PL} The preload resistance on the output of the converter.

R_{S1} The high-side VS-pin sense resistance.

R_{S2} The low-side VS-pin sense resistance.

Timing Terms in Seconds

t_D The total current-sense delay including MOSFET-turnoff delay; add 50 ns to MOSFET delay.

$t_{DM(min)}$ The minimum secondary rectifier conduction time.

$t_{ON(min)}$ The minimum MOSFET on time.

t_R The resonant frequency during the DCM dead time.

t_{RESP} The maximum response time of the voltage-regulation control-loop to the maximum required load-step.

Voltage Terms in Volts

V_{BLK} The highest bulk-capacitor voltage for standby power measurement.

$V_{BULK(min)}$ The minimum valley voltage on C_{B1} and C_{B2} at full power.

V_{CCR} The constant-current regulation factor (see ELECTRICAL CHARACTERISTICS).

$V_{CST(max)}$ The CS-pin maximum current-sense threshold (see ELECTRICAL CHARACTERISTICS).

$V_{CST(min)}$ The CS-pin minimum current-sense threshold (see ELECTRICAL CHARACTERISTICS).

$V_{VDD(off)}$ The UVLO turnoff voltage (see ELECTRICAL CHARACTERISTICS).

PRODUCT PREVIEW

$V_{VDD(on)}$ The UVLO turnon voltage (see ELECTRICAL CHARACTERISTICS).

V_{DSPK} The MOSFET drain-to-source peak voltage at high line.

V_F The secondary-rectifier forward-voltage drop at near-zero current.

V_{FA} The auxiliary-rectifier forward-voltage drop.

V_{LK} The estimated leakage-inductance energy reset voltage.

$V_{O\Delta}$ The output voltage drop allowed during the load-step transient in CV mode.

V_{OCBC} The target cable-compensation voltage added to V_{OCV} (provided by an external adjustment circuit applied to the shunt-regulator). Set equal to 0 V if not used.

V_{OCC} The converter lowest output voltage target while in constant-current regulation.

V_{OCV} The regulated output voltage of the converter.

V_{OV} The maximum allowable peak output voltage.

V_{OVP} The overvoltage-detection level at the VS input (see ELECTRICAL CHARACTERISTICS).

V_{REVA} The peak reverse voltage on the auxiliary rectifier.

V_{REVS} The peak reverse voltage on the secondary rectifier.

V_{RIPPLE} The output peak-to-peak ripple voltage at full-load.

AC Voltage Terms in V_{RMS}

$V_{IN(max)}$ The maximum input voltage to the converter.

$V_{IN(min)}$ The minimum input voltage to the converter.

$V_{IN(run)}$ The converter startup (run) input voltage.

Efficiency Terms

η The converter overall efficiency at full-power output.

η_{SB} The estimated efficiency of the converter at no-load condition, excluding startup resistance or bias losses. For a 5-V USB-charger application, 60% to 65% is a good initial estimate.

η_{XFMR} The transformer primary-to-secondary power-transfer efficiency.

PRODUCT PREVIEW

Standby Power Estimate and No-Load Switching Frequency

Assuming minimal no-load standby power is a critical design requirement, determine the estimated no-load power loss based on an accounting of all no-load operating and leakage currents at their respective voltages. Close attention to detail is necessary to account for all of the sources of leakage, however, in many cases, prototype measurement is the only means to obtain a realistic estimation of total primary and secondary leakage currents. At present, converter standby power is certified by compliance-agency authorities based on steady-state room-temperature operation at the highest nominal input voltage rating (typically 230 Vrms).

Equation 6 estimates the standby power loss from the sum of all leakage currents of the primary-side components of the converter. These leakage currents are measured in aggregate by disconnecting the HV input of the controller from the bulk-voltage rail to prevent operating currents from interfering with the leakage measurement.

$$P_{PRI\_SB} = V_{BULK} \times \sum_{k=1}^{n_p} I_{PRI\_LK_k} \tag{6}$$

Equation 7 estimates the standby power loss from the sum of all leakage and operating currents of the secondary-side components on the output of the converter. Leakage currents result from reverse voltage applied across the output rectifier and capacitors, while the operating current includes currents required by the shunt-regulator, optocoupler, and associated components.

$$P_{SEC\_SB} = V_{OCV} \times \sum_{k=1}^{n_s} I_{SEC_k} \tag{7}$$

Equation 8 estimates the standby power loss from the sum of all leakage and operating currents of the auxiliary-side components on the controller of the converter. Leakage currents of the auxiliary diode and capacitor are usually negligible. The operating current includes the wait-state current, I_{WAIT}, of the UCC28740 controller, plus the optocoupler-output current for the FB network in the steady-state no-load condition. The VDD voltage in the no-load condition V_{VDDNL} are the lowest practicable value to minimize loss.

$$P_{AUX\_SB} = V_{VDDNL} \times \sum_{k=1}^{n_a} I_{AUX_k} \tag{8}$$

Note that P_{PRI_SB} is the only loss that is not dependent on transformer conversion efficiency. P_{SEC_SB} and P_{AUX_SB} are processed through the transformer and incur additional losses as a consequence. Typically, the transformer no-load conversion efficiency η_{SWNL} lies in the range of 0.50 to 0.70. Total standby input power (no-load condition) is estimated by Equation 9.

$$P_{SB} = P_{PRI\_SB} + \frac{1}{\eta_{SWNL}} \left(P_{SEC\_SB} + P_{AUX\_SB} \right) \tag{9}$$

Although the UCC28740 is capable of operating at the minimum switching frequency of 170 Hz, a typical converter is likely to require a higher frequency to sustain operation at no-load. An accurate estimate of the no-load switching frequency f_{SWNL} entails a thorough accounting of all switching-related energy losses within the converter including parasitic elements of the power-train components. In general, f_{SWNL} is likely to lie within the range of 400 Hz to 800 Hz. A more detailed treatment of standby power and no-load frequency is beyond the scope of this data sheet.

Input Bulk Capacitance and Minimum Bulk Voltage

Determine the minimum voltage on the input bulk capacitance, C_{B1} and C_{B2} total, in order to determine the maximum Np-to-Ns turns-ratio of the transformer. The input power of the converter based on target full-load efficiency, the minimum input RMS voltage, and the minimum AC input frequency determine the input capacitance requirement.

Maximum input power is determined based on I_{OCC}, V_{OCV}, V_{CBC} (if used), and the full-load conversion-efficiency target.

$$P_{IN} = \frac{(V_{OCV} + V_{CBC}) \times I_{OCC}}{\eta} \quad (10)$$

Equation 11 provides an accurate solution for the total input capacitance based on a target minimum bulk-capacitor voltage. Alternatively, to target a given input capacitance value, iterate the minimum capacitor voltage to achieve the target capacitance value.

$$C_{BULK} = \frac{2P_{IN} \times \left(0.25 + \frac{1}{2\pi} \times \arcsin\left(\frac{V_{BULK(min)}}{\sqrt{2} \times V_{IN(min)}}\right)\right)}{\left(2V_{IN(min)}^{\ 2} - V_{BULK(min)}^{\ 2}\right) \times f_{LINE}} \quad (11)$$

Transformer Turns-Ratio, Inductance, Primary Peak Current

The target maximum switching frequency at full-load, the minimum input-capacitor bulk voltage, and the estimated DCM quasi-resonant time determine the maximum primary-to-secondary turns-ratio of the transformer.

Initially determine the maximum-available total duty-cycle of the on-time and secondary conduction time based on the target switching frequency, f_{MAX}, and DCM resonant time. For DCM resonant frequency, assume 500 kHz if an estimate from previous designs is not available. At the transition-mode operation limit of DCM, the interval required from the end of secondary current conduction to the first valley of the V_{DS} voltage is ½ of the DCM resonant period (t_R), or 1 µs assuming 500 kHz resonant frequency. The maximum allowable MOSFET on-time D_{MAX} is determined using Equation 12.

$$D_{MAX} = 1 - D_{MAGCC} - \left(\frac{t_R}{2} \times f_{MAX}\right) \quad (12)$$

When D_{MAX} is known, the maximum primary-to-secondary turns-ratio is determined with Equation 13. D_{MAGCC} is defined as the secondary-diode conduction duty-cycle during CC operation and is fixed internally by the UCC28740 at 0.425. The total voltage on the secondary winding must be determined, which is the sum of V_{OCV}, V_F, and V_{OCBC}. For the 5-V USB-charger applications, a turns ratio range of 13 to 15 is typically used.

$$N_{PS(max)} = \frac{D_{MAX} \times V_{BULK(min)}}{D_{MAGCC} \times (V_{OCV} + V_F + V_{OCBC})} \quad (13)$$

A higher turns-ratio generally improves efficiency, but may limit operation at low input voltage. Transformer design iterations are generally necessary to evaluate system-level performance trade-offs. When the optimum turns-ratio N_{PS} is determined from a detailed transformer design, use this ratio for the following parameters.

The UCC28740 constant-current regulation is achieved by maintaining D_{MAGCC} at the maximum primary peak current setting. The product of D_{MAGCC} and $V_{CST(max)}$ defines a CC-regulating voltage factor V_{CCR} which is used with N_{PS} to determine the current-sense resistor value necessary to achieve the regulated CC target, I_{OCC} (see Equation 14).

Because a small portion of the energy stored in the transformer does not transfer to the output, a transformer-efficiency term is included in the R_{CS} equation. This efficiency number includes the core and winding losses, the leakage-inductance ratio, and a bias-power to maximum-output-power ratio. An overall-transformer efficiency of 0.91 is a good estimate based on 3.5% leakage inductance, 5% core & winding loss, and 0.5% bias power, for example. Adjust these estimates as appropriate based on each specific application.

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2I_{OCC}} \times \sqrt{\eta_{XFMR}} \quad (14)$$

The primary transformer inductance is calculated using the standard energy storage equation for flyback transformers. Primary current, maximum switching frequency, output voltage and current targets, and transformer power losses are included in Equation 16.

First, determine the transformer primary peak current using Equation 15. Peak primary current is the maximum current-sense threshold divided by the current-sense resistance.

PRODUCT PREVIEW

$$I_{PP(max)} = \frac{V_{CST(max)}}{R_{CS}} \quad (15)$$

$$L_P = \frac{2(V_{OCV} + V_F + V_{OCBC}) \times I_{OCC}}{\eta_{XFMR} \times I_{PP(max)}^2 \times f_{MAX}} \quad (16)$$

N_{AS} is determined by the lowest target operating output voltage while in constant-current regulation and by the VDD UVLO turnoff threshold of the UCC28740. Additional energy is supplied to VDD from the transformer leakage-inductance which allows a lower turns ratio to be used in many designs.

$$N_{AS} = \frac{V_{VDD(off)} + V_{FA}}{V_{OCC} + V_F} \quad (17)$$

Transformer Parameter Verification

Because the selected transformer turns-ratio affects the MOSFET V_{DS} and the secondary and auxiliary rectifier reverse voltages, a review of these voltages is important. In addition, internal timing constraints of the UCC28740 require a minimum on time of the MOSFET (t_{ON}) and a minimum demagnetization time (t_{DM}) of the transformer in the high-line minimum-load condition. The selection of f_{MAX}, L_P, and R_{CS} affects the minimum t_{ON} and t_{DM}.

Equation 18 and Equation 19 determine the reverse voltage stresses on the secondary and auxiliary rectifiers. Stray inductance can impress additional voltage spikes upon these stresses and snubbers may be necessary.

$$V_{REVS} = \frac{V_{IN(max)} \times \sqrt{2}}{N_{PS}} \times V_{OV} \quad (18)$$

$$V_{REVA} = \frac{V_{IN(max)} \times \sqrt{2}}{N_{PA}} \times V_{VDD} \quad (19)$$

For the MOSFET V_{DS} peak voltage stress, an estimated leakage inductance voltage spike (V_{LK}) is included.

$$V_{DSPK} = \left(V_{IN(max)} \times \sqrt{2}\right) + \left(V_{OCV} + V_F + V_{OCBC}\right) \times N_{PS} + V_{LK} \quad (20)$$

Equation 21 determines if $t_{ON(min)}$ exceeds the minimum t_{ON} target of 280 ns (maximum t_{CSLEB}). Equation 22 verifies that $t_{DM(min)}$ exceeds the minimum t_{DM} target of 1.2 µs.

$$t_{ON(min)} = \frac{L_P}{V_{IN(max)} \times \sqrt{2}} \times \frac{I_{PP(max)}}{K_{AM}} \quad (21)$$

$$t_{DM(min)} = \frac{t_{ON(min)} \times V_{IN(max)} \times \sqrt{2}}{N_{PS} \times \left(V_{OCV} + V_F\right)} \quad (22)$$

VS Resistor Divider, Line Compensation

The VS divider resistors determine the output overvoltage detection point of the flyback converter. The high-side divider resistor (R_{S1}) determines the input-line voltage at which the controller enables continuous DRV operation. R_{S1} is determined based on transformer primary-to-auxiliary turns-ratio and desired input voltage operating threshold.

$$R_{S1} = \frac{V_{IN(run)} \times \sqrt{2}}{N_{PA} \times I_{VSL(run)}} \quad (23)$$

The low-side VS pin resistor is then selected based on the desired overvoltage limit, V_{OV}.

$$R_{S2} = \frac{R_{S1} \times V_{OVP}}{N_{AS} \times \left(V_{OV} - V_F\right) - V_{OVP}} \quad (24)$$

PRODUCT PREVIEW

The UCC28740 maintains tight constant-current regulation over varying input line by using the line-compensation feature. The line-compensation resistor (R_{LC}) value is determined by current flowing in R_{S1} and the total internal gate-drive and external MOSFET turnoff delay. Assume an internal delay of 50 ns in the UCC28740.

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times t_D \times N_{PA}}{L_P} \quad (25)$$

Output Capacitance

The output capacitance value is often determined by the transient-response requirement from the no-load condition. For example, in typical low-power USB-charger applications, there is a requirement to maintain a minimum transient V_O of 4.1 V with a load-step I_{TRAN} from 0 mA to 500 mA. Yet new higher-performance applications require smaller transient voltage droop $V_{O\Delta}$ with I_{TRAN} of much greater amplitude (such as from no-load to full-load), which drives the need for high-speed opto-coupled voltage feedback.

$$C_{OUT} \geq \frac{I_{TRAN} \times t_{RESP}}{V_{O\Delta}}$$

where

- t_{RESP} is the time delay from the moment I_{TRAN} is applied to the moment when I_{FB} falls below 1 µA (26)

Additional considerations for the selection of appropriate output capacitors include ripple-current, ESR, and ESL ratings necessary to meet reliability and ripple-voltage requirements. Detailed design criteria for these considerations are beyond the scope of this datasheet.

VDD Capacitance, C_{VDD}

The capacitance on VDD must supply the primary-side operating current used during startup and between low-frequency switching pulses. The largest result of three independent calculations denoted in Equation 27, Equation 28, and Equation 29 determines the value of C_{VDD}.

At startup, when $V_{VDD(on)}$ is reached, C_{VDD} alone supplies the device operating current and MOSFET gate current until the output of the converter reaches the target minimum-operating voltage in CC regulation, V_{OCC}. Now the auxiliary winding sustains VDD for the UCC28740 above UVLO. The total output current available to the load and to charge the output capacitors is the CC-regulation target, I_{OCC}. Equation 27 assumes that *all* of the output current of the converter is available to charge the output capacitance until V_{OCC} is achieved. For typical applications, Equation 27 includes an estimated $q_G f_{SW(max)}$ of average gate-drive current and a 1-V margin added to V_{VDD}.

$$C_{VDD} \geq \frac{\left(I_{RUN} + q_G f_{SW(max)}\right) \times \frac{C_{OUT} \times V_{OCC}}{I_{OCC}}}{V_{VDD(on)} - \left(V_{VDD(off)} + 1V\right)} \quad (27)$$

During a worst-case un-load transient event from full-load to no-load, C_{OUT} overcharges above the normal regulation level for a duration of t_{OV}, until the output shunt-regulator loading is able to drain V_{OUT} back to regulation. During t_{OV}, the voltage feedback loop and optocoupler are saturated, driving maximum I_{FB} and temporarily switching at $f_{SW(min)}$. The auxiliary bias current expended during this situation exceeds that normally required during the steady-state no-load condition. Equation 28 calculates the value of C_{VDD} (with a safety factor of 2) required to ride through the t_{OV} duration until steady-state no-load operation is achieved.

$$C_{VDD} \geq \frac{2 \times I_{AUXNL(max)} \times t_{OV}}{V_{VDDFL} - \left(V_{VDD(off)} + 1V\right)} \quad (28)$$

Finally, in the steady-state no-load operating condition, total no-load auxiliary-bias current, I_{AUXNL} is provided by the converter switching at a no-load frequency, f_{SWNL}, which is generally higher than $f_{SW(min)}$. C_{VDD} is calculated to maintain a target VDD ripple voltage lower than ΔV_{VDD}, using Equation 29.

PRODUCT PREVIEW

$$C_{VDD} \geq \frac{I_{AUXNL} \times \frac{1}{f_{SWNL}}}{\Delta V_{VDD}} \quad (29)$$

Feedback Network Biasing

Achieving very low standby power while maintaining high-performance load-step transient response requires careful design of the feedback network. Optically-coupled secondary-side regulation is used to provide the rapid response needed when a heavy load step occurs during the no-load condition. One of the most commonly used devices to drive the optocoupler is the TL431 shunt-regulator, due to its simplicity, regulation performance, and low cost. This device requires a minimum bias current of 1 mA to maintain regulation accuracy. Together with the UCC28740 primary-side controller, careful biasing will ensure less than 30 mW of standby power loss at room temperature. Where a more stringent standby loss limit of less than 10 mW is required, the TLV431 device is recommended due to its minimum 80-µA bias capability.

Facilitating these low standby-power targets is the approximate 23-µA range of the FB input for full to no-load voltage regulation. The control-law profile graph (see Figure 15) shows that for FB-input current greater than 22 µA, no further reduction in switching frequency is possible. Therefore, minimum power is converted at $f_{SW(min)}$. However, the typical minimum steady-state operating frequency tends to be in the range of several-hundred Hertz, and consequently the maximum steady-state FB current at no-load will be less than I_{FBMAX}. Even so, prudent design practice dictates that I_{FBMAX} should be used for conservative steady-state biasing calculations. At this current level, V_{FBMAX} can be expected at the FB input.

Referring to the Design Procedure Application Example in Figure 19, the main purpose of R_{FB4} is to speed up the turnoff time of the optocoupler in the case of a heavy load-step transient condition. The value of R_{FB4} is determined empirically due to the variable nature of the specific optocoupler chosen for the design, but tends to fall within the range of 10 kΩ to 100 kΩ. A tradeoff must be made between a lower value for faster transient response and a higher value for lower standby power. R_{FB4} also serves to set a minimum bias current for the optocoupler and to drain dark current.

It is important to understand the distinction between *steady-state* no-load bias currents and voltages which affect standby power, and the varying extremes of these same currents and voltages which affect regulation during transient conditions. Design targets for minimum standby loss and maximum transient response often result in conflicting requirements for component values. Trade-offs, such as for R_{FB4} as discussed previously, must be made.

During standby operation, the total auxiliary current (used in Equation 8) is the sum of I_{WAIT} into the IC and the no-load optocoupler-output current I_{CENL}. This optocoupler current is given by Equation 30.

$$I_{CENL} = I_{FBMAX} + \frac{V_{FBMAX}}{R_{FB4}} \quad (30)$$

For fast response, the optocoupler-output transistor is biased to minimize the variation of V_{CE} between full-load and no-load operation. Connecting the emitter directly to the FB input of the UCC28740 is possible, however, an unload-step response may unavoidably drive the optocoupler into saturation which will overload the FB input with full VDD applied. A series-resistor R_{FB3} is necessary to limit the current into FB and to avoid excess draining of C_{VDD} during this type of transient situation. The value of R_{FB3} is chosen to limit the excess I_{FB} and R_{FB4} current to an acceptable level when the optocoupler is saturated. Like R_{FB4}, the R_{FB3} value is also chosen empirically during prototype evaluation to optimize performance based on the conditions present during that situation. A starting value may be estimated using Equation 31.

$$R_{FB3} = \frac{V_{VDDNL} - 1V}{I_{CENL}} \quad (31)$$

Note that R_{FB3} is estimated based on the expected no-load VDD voltage, but full-load VDD voltage will be higher resulting in initially higher I_{CE} current during the unload-step transient condition. Because R_{FB3} is interposed between V_E and the FB input, the optocoupler transistor V_{CE} varies considerably more as I_{CE} varies and transient response time is reduced. Capacitor C_{FB3} across R_{FB3} helps to improve the transient response again. The value of C_{FB3} is estimated initially by equating the $R_{FB3}C_{FB3}$ time constant to 1 ms, and later is adjusted higher or lower for optimal performance during prototype evaluation.

The optocoupler transistor-output current I_{CE} is proportional to the optocoupler diode input current by its current transfer ratio, CTR. Although many optocouplers are rated with nominal CTR between 50% and 600%, or are ranked into narrower ranges, the actual CTR obtained at the low currents used with the UCC28740 falls around 5% to 15%. At full-load regulation, when I_{FB} is near zero, V_{FB} is still approximately 0.4 V and this sets a minimum steady-state current for I_{CE} through R_{FB4}. After choosing an optocoupler, the designer must characterize its CTR over the range of low output currents expected in this application, because optocoupler data sheets rarely include such information. The actual CTR obtained is required to determine the diode input current range at the secondary-side shunt-regulator.

Referring again to Figure 19, the shunt-regulator (typically a TL431) current must be at least 1 mA even when almost no optocoupler diode current flows. Since even a near-zero diode current establishes a forward voltage, R_{OPT} is selected to provide the minimum 1-mA regulator bias current. The optocoupler input diode must be characterized by the designer to obtain the actual forward voltage versus forward current at the low currents expected. At the full-load condition of the converter, I_{FB} is around 0.5 µA, I_{CE} may be around (0.4 V / R_{FB4}), and CTR at this level is about 10%, so the diode current typically falls in the range of 25 µA to 100 µA. Typical opto-diode forward voltage at this level is about 0.97 V which is applied across R_{OPT}. If R_{OPT} is set equal to 1 kΩ, this provides 970 µA plus the diode current for I_{OPT}.

As output load decreases, the voltage across the shunt-regulator also decreases to increase the current through the optocoupler diode. This increases the diode forward voltage across R_{OPT}. CTR at no-load (when I_{CE} is higher) is generally a few percent higher than CTR at full-load (when I_{CE} is lower). At steady-state no-load condition, the shunt-regulator current is maximized and can be estimated by Equation 30 and Equation 32. I_{OPTNL}, plus the sum of the leakage currents of all the components on the output of the converter, constitute the total current required for use in Equation 7 to estimate secondary-side standby loss.

$$I_{OPTNL} = \frac{I_{CENL}}{CTR_{NL}} + \frac{V_{OPTNL}}{R_{OPT}} \tag{32}$$

The shunt-regulator voltage can decrease to a minimum, saturated level of about 2 V. To prevent excessive diode current, a series resistor, R_{TL}, is added to limit I_{OPT} to the maximum value necessary for regulation. Equation 33 provides an estimated initial value for R_{TL}, which may be adjusted for optimal limiting later during the prototype evaluation process.

$$R_{TL} = \frac{V_{OUTNL} - V_{OPTNL} - 2V}{I_{OPTNL}} \tag{33}$$

The output-voltage sense-network resistors R_{FB1} and R_{FB2} are calculated in the usual manner based on the shunt-regulator reference voltage and input bias current. Having characterized the optocoupler at low currents and determined the initial values of R_{FB1}, R_{FB2}, R_{FB3}, R_{FB4}, C_{FB3}, R_{OPT} and R_{TL} using the above procedure, the DC-bias states of the feedback network can be established for steady-state full-load and no-load conditions. Adjustments of these initial values may be necessary to accommodate variations of the UCC28740, optocoupler, and shunt-regulator parameters for optimal overall performance.

The shunt-regulator compensation network, Z_{FB}, is determined using well-established design techniques for control-loop stability. Typically, a type-II compensation network is used. The compensation design procedure is beyond the scope of this datasheet.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC28740D	PREVIEW	SOIC	D	7	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		U28740	
UCC28740DR	PREVIEW	SOIC	D	7	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		U28740	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

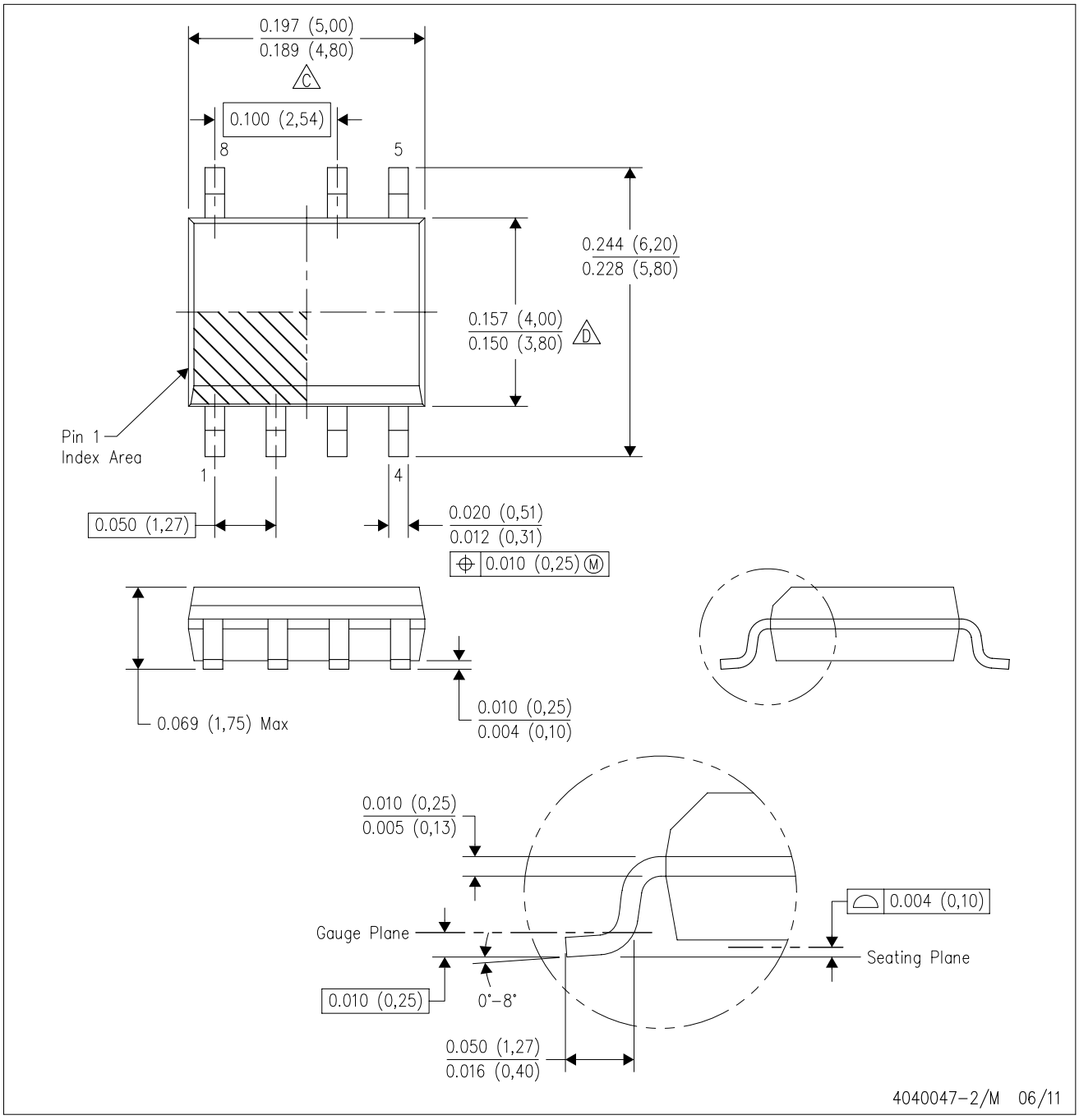
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

D (R–PDSO–G7) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265