Single Channel High-Speed, Low-Side Gate Driver (with 4-A Peak Source and 8-A Peak Sink)

Check for Samples: UCC27511

FEATURES

- Low-Cost, Gate-Driver Device Offering Superior Replacement of NPN and PNP Discrete Solutions
- 4-A Peak Source and 8-A Peak Sink Asymmetrical Drive
- Strong Sink Current in Asymmetrical Drive Offers Enhanced Immunity Against Miller C*dV/dt Turn On
- Split Output Configuration (allows easy and independent adjustment of turn-on and turn-off speeds)
- Fast Propagation Delays (13-ns typical)
- Fast Rise/Fall Times (9-ns and 7-ns typical)
- 4.5-V to 18-V Single Supply Range
- Outputs Held Low During VDD UVLO (ensures glitch free operation at power-up and power-down)
- TTL/CMOS Compatible Logic Threshold, (independent of supply voltage)
- Hysteretic Logic Thresholds for High Noise Immunity
- Dual Input Design (choice of an inverting (IN- pin) or non-inverting (IN+ pin) driver configuration)
  - Unused Input Pin can be Used for Enable or Disable Function
- Output Held Low when Input Pins are Floating
- Input and Enable Pin Voltage Levels Not Restricted by VDD Pin Bias Supply Voltage
- Operating Temperature Range of -40°C to 140°C

APPLICATIONS

- Switch-Mode Power Supplies
- DC-to-DC Converters
- Companion Gate Driver Devices for Digital Power Controllers (using 3.3-V to a 5-V PWM signal)
- Solar Power, Motor Control, UPS
- Gate Driver for Emerging Wide Band-Gap Power Devices (such as GaN)

DESCRIPTION

The UCC27511 single-channel, high-speed, low-side gate driver device is capable of effectively driving MOSFET and IGBT power switches. Using a design that inherently minimizes shoot-through current, UCC27511 is capable of sourcing and sinking high, peak current pulses into capacitive loads offering rail-to-rail drive capability and extremely small propagation delay typically 13 ns.

The UCC27511 provides 4-A source, 8-A sink (asymmetrical drive) peak-drive current capability. Strong sink capability in asymmetrical drive boosts immunity against parasitic, Miller C*dV/dt turn-on effect. The UCC27511 device also features a unique split output configuration where the gate-drive current is sourced through OUTH pin and sunk through OUTL pin. This unique pin arrangement allows the user to apply independent turn-on and turn-off resistors to the OUTH and OUTL pins respectively and easily control the switching dV/dt.

UCC27511 is designed to operate over a wide VDD range of 4.5 V to 18 V and wide temperature range of -40°C to 140°C. Internal Under Voltage Lockout (UVLO) circuitry on VDD pin holds output low outside VDD operating range. The capability to operate at low voltage levels such as below 5 V, along with best in class switching characteristics, is especially suited for driving emerging wide band-gap power switching devices such as GaN power semiconductor devices.

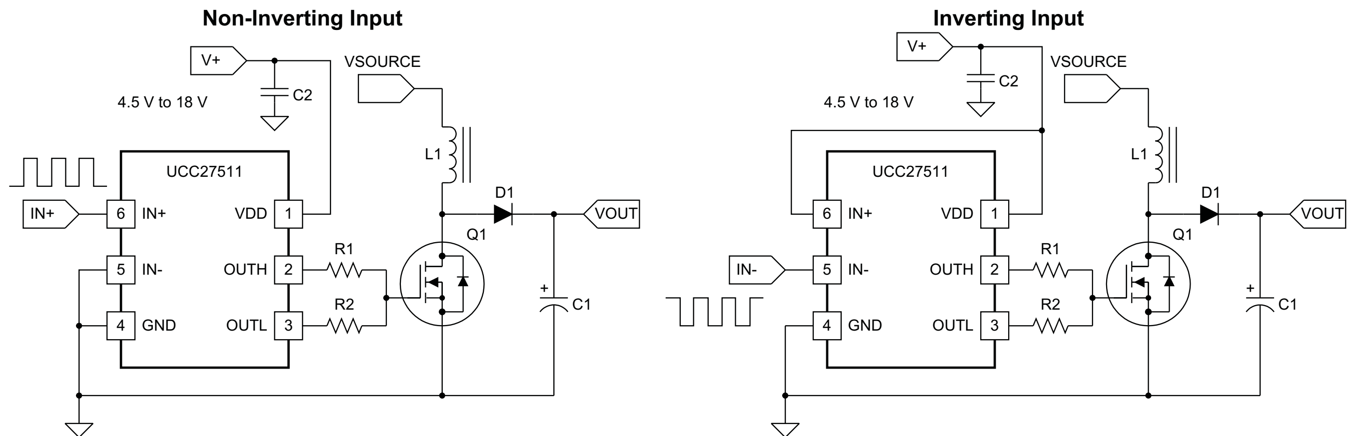
ADVANCE INFORMATION

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ADVANCE INFORMATION concerns new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

Copyright © 2012, Texas Instruments Incorporated

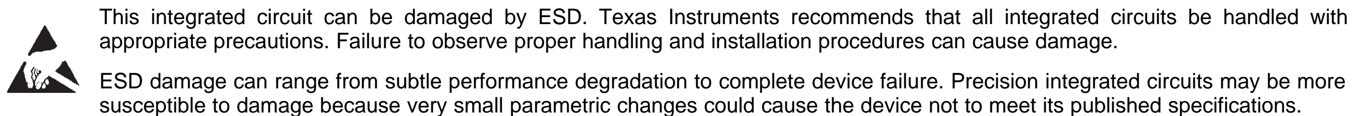
Typical Application Diagrams



DESCRIPTION (CONT.)

UCC27511 features a dual-input design which offers flexibility of implementing both inverting (IN- pin) and non-inverting (IN+ pin) configuration with the same device. Either IN+ or IN- pin can be used to control the state of the driver output. The unused input pin can be used for enable/disable function. For safety purpose, internal pull-up and pull-down resistors on the input pins ensure that outputs are held low when input pins are in floating condition. Hence the unused input pin cannot be left floating and needs to be properly biased to ensure that driver output is in enabled for normal operation.

The input pin threshold of the UCC27511 device is based on TTL/CMOS-compatible low-voltage logic which is fixed and independent of the VDD supply voltage. Wide hysteresis between the high and low thresholds offers excellent noise immunity.


This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)(2)

PART NUMBER	PACKAGE	PEAK CURRENT (SOURCE/SINK)	INPUT THRESHOLD LOGIC	OPERATING TEMPERATURE RANGE, T_A
UCC27511DBV	SOT-23 6-pin	4-A/8-A (Asymmetrical Drive)	CMOS/TTL-Compatible (low voltage, independent of VDD bias voltage)	-40°C to 140°C

(1) For the most current package and ordering information, see Package Option Addendum at the end of this document.
(2) All packages use Pb-Free lead finish of Pd-Ni-Au which is compatible with MSL level 1 at 255°C to 260°C peak reflow temperature to be compatible with either lead free or Sn/Pb soldering operations. DRS package is rated MSL level 2.

ADVANCE INFORMATION

 Copyright © 2012, Texas Instruments Incorporated

ABSOLUTE MAXIMUM RATINGS[1][2][3]

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage range	VDD	-0.3	20	V
OUTH voltage		-0.3	VDD + 0.3	
OUTL voltage		-0.3	20	
Output continuous current (OUTH source current and OUTL sink current)	I_{OUT_DC} (source)		0.3	A
	I_{OUT_DC} (sink)		0.6	
Output pulsed current (0.5 ms) (OUTH source current and OUTL sink current)	I_{OUT_pulsed}(source)		4	
	I_{OUT_pulsed}(sink)		8	
IN+, IN-[4]		-0.3	20	V
ESD	Human Body Model, HBM		2000	
	Charged Device Model, CDM SOT-23		500	
Operating virtual junction temperature range, T_J		-40	150	°C
Storage temperature range, T_{STG}		-65	150	
Lead temperature	Soldering, 10 sec.		300	
	Reflow		260	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See Packaging Section of the datasheet for thermal limitations and considerations of packages.
(3) These devices are sensitive to electrostatic discharge; follow proper device handling procedures.
(4) Maximum voltage on input pins is not restricted by the voltage on the VDD pin.

THERMAL INFORMATION

THERMAL METRIC[1]		PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance[2]		°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[3]		
θ_{JB}	Junction-to-board thermal resistance[4]		
ψ_{JT}	Junction-to-top characterization parameter[5]		
ψ_{JB}	Junction-to-board characterization parameter[6]		
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[7]		

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ADVANCE INFORMATION

Copyright © 2012, Texas Instruments Incorporated

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

	MIN	TYP	MAX	UNIT
Supply voltage range, VDD	4.5	12	18	V
Operating junction temperature range	-40		140	°C
Input voltage, IN+ and IN-	0		18	V
Enable voltage, EN	0		18	V

ELECTRICAL CHARACTERISTICS

VDD = 12 V, $T_A = T_J$ = -40°C to 140°C, 1-μF capacitor from VDD to GND. Currents are positive into, negative out of the specified terminal.

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNITS
BIAS Currents							
$I_{DD(off)}$	Startup current	VDD = 3.4 V	IN+ = VDD, IN- = GND	40	100	160	μA
			IN+ = IN- = GND or IN+ = IN- = VDD	25	75	145	
			IN+ = GND, IN- = VDD	20	60	115	
Under Voltage Lockout (UVLO)							
V_{ON}	Supply start threshold	T_A = 25°C		3.91	4.20	4.5	V
		T_A = -40°C to 140°C		3.70	4.20	4.65	
V_{OFF}	Minimum operating voltage after supply start			3.45	3.9	4.35	
V_{DD_H}	Supply voltage hysteresis			0.2	0.3	0.5	
Inputs (IN+, IN-)							
V_{IN_H}	Input signal high threshold	Output high for IN+ pin, Output low for IN- pin			2.2	2.4	V
V_{IN_L}	Input signal low threshold	Output low for IN+ pin, Output high for IN- pin		1.0	1.2		
V_{IN_HYS}	Input signal hysteresis				1.0		
Source/Sink Current							
$I_{SRC/SNK}$	Source/sink peak current(1)	C_{LOAD} = 0.22 μF, F_{SW} = 1 kHz			-4/+8		A
Outputs (OUTH, OUTL, OUT)							
V_{DD}- V_{OH}	High output voltage	VDD = 12 V, I_{OUTH} = -10 mA			50	90	mV
		VDD = 4.5 V, I_{OUTH} = -10 mA			60	130	
V_{OL}	Low output voltage	VDD = 12, I_{OUTL} = 10 mA			5	6.5	
		VDD = 4.5 V, I_{OUTL} = 10 mA				10	
R_{OH}	Output pull-up resistance(2)	VDD = 12 V, I_{OUTH} = -10 mA			5.0	7.5	Ω
		VDD = 4.5 V, I_{OUTH} = -10 mA			5.0	11.0	
R_{OL}	Output pull-down resistance	VDD = 12 V, I_{OUTH} = 10 mA			0.375	0.650	
		VDD = 4.5 V, I_{OUTH} = 10 mA			0.375	0.650	

(1) Ensured by Design.
(2) R_{OH} represents on-resistance of P-Channel MOSFET in pull-up structure of the UCC27511's output stage.

ADVANCE INFORMATION

Copyright © 2012, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS (continued)

VDD = 12 V, T_A = T_J = -40°C to 140°C, 1-μF capacitor from VDD to GND. Currents are positive into, negative out of the specified terminal.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
Switching Time						
t_R	Rise time(3)	VDD = 12 V C_{LOAD} = 1.8 nF, connected to OUTH and OUTL pins tied together		8	12	ns
		VDD = 4.5 V C_{LOAD} = 1.8 nF, connected to OUTH and OUTL pins tied together	4	16	22	
t_F	Fall time(3)	VDD = 12 V C_{LOAD} = 1.8 nF, connected to OUTH and OUTL pins tied together		7	11	
		VDD=4.5V C_{LOAD} = 1.8 nF, connected to OUTH and OUTL pins tied together	4	7	11	
t_{D1}	IN+ to output propagation delay(3)	VDD = 12 V 5-V input pulse C_{LOAD} = 1.8 nF, connected to OUTH and OUTL pins tied together	4	13	23	
		VDD = 4.5 V 5-V input pulse C_{LOAD} = 1.8 nF, connected to OUTH and OUTL pins tied together	4	15	26	
t_{D2}	IN- to output propagation delay(3)	VDD = 12 V C_{LOAD} = 1.8 nF, connected to OUTH and OUTL pins tied together	4	13	23	
		VDD = 4.5 V C_{LOAD} = 1.8 nF, connected to OUTH and OUTL pins tied together	4	19	30	

(3) See timing diagrams in Figure 1, Figure 2, Figure 3 and Figure 4.

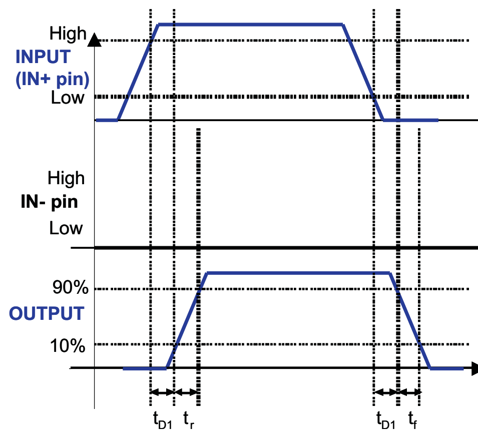


Figure 1. Non-Inverting Configuration (PWM Input to IN+ pin (IN- pin tied to GND), Output represents OUTH and OUTL pins tied together)

ADVANCE INFORMATION

Copyright © 2012, Texas Instruments Incorporated

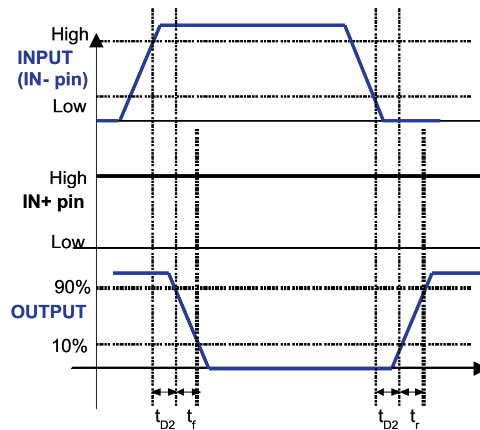


Figure 2. Inverting Configuration (PWM input to IN- pin (IN+ pin tied to VDD), Output represents OUTH and OUTL pins tied together)

ADVANCE INFORMATION

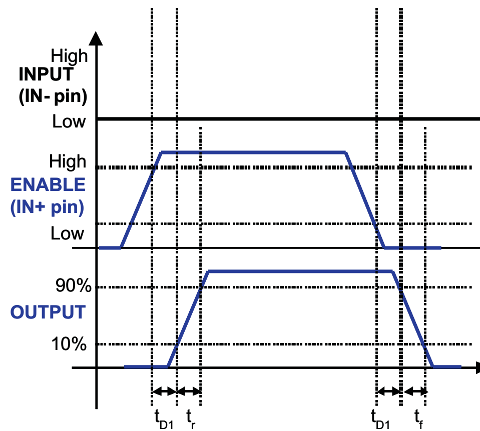


Figure 3. Enable and Disable Function Using IN+ Pin (Enable and disable signal applied to IN+ pin, PWM input to IN- pin, Output represents OUTH and OUTL pins tied together)

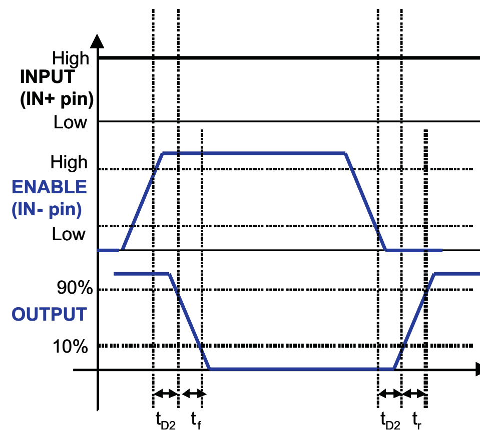
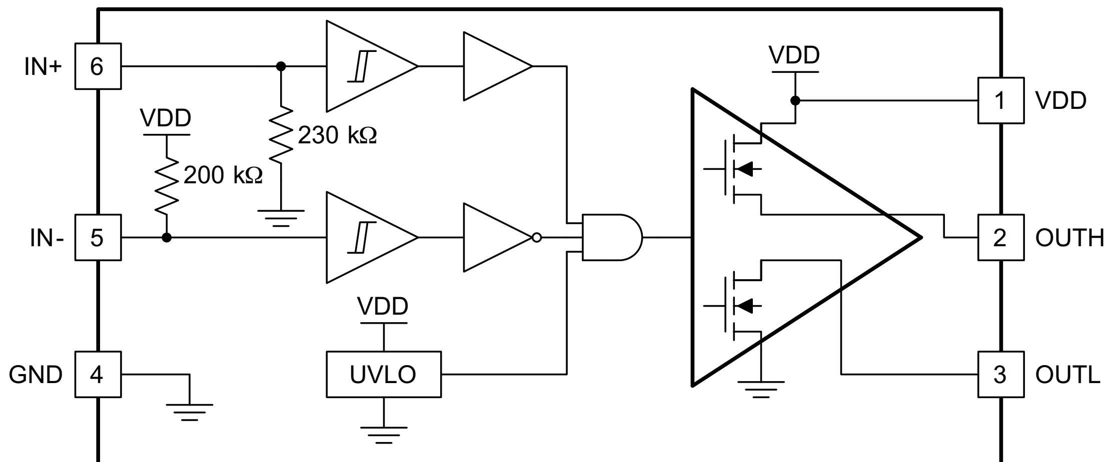


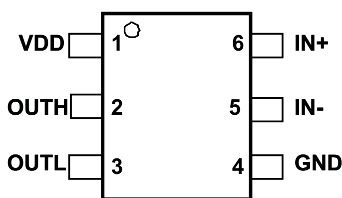
Figure 4. Enable and Disable Function Using IN- Pin (Enable and disable signal applied to IN- pin, PWM input to IN+ pin, Output represents OUTH and OUTL pins tied together)

Copyright © 2012, Texas Instruments Incorporated

DEVICE INFORMATION

Functional Block Diagrams





TERMINAL FUNCTIONS

TERMINAL		I/O	FUNCTION
PIN NUMBER	NAME		
1	VDD	I	**Bias supply input.**
2	OUTH	O	**Sourcing current output of driver**. Connect resistor between OUTH and Gate of power switching device to adjust turn-on speed.
3	OUTL	O	**Sinking current output of driver.** Connect resistor between OUTL and Gate of power switching device to adjust turn-off speed.
4	GND	-	**Ground.** All signals referenced to this pin.
5	IN-	I	**Inverting input.** When the driver is used in non-inverting configuration connect IN- to GND in order to enable output, OUT held LOW if IN- is unbiased or floating
6	IN+	I	**Non-inverting input.** When the driver is used in inverting configuration connect IN+ to VDD in order to enable output, OUT held LOW if IN+ is unbiased or floating

Table 1. Device Logic Table

IN+ PIN	IN- PIN	OUTH PIN	OUTL PIN	OUT (OUTH and OUTL pins tied together)
L	L	High impedance	L	L
L	H	High impedance	L	L
H	L	H	High impedance	H
H	H	High impedance	L	L
x[(1)]	Any	High impedance	L	L
Any	x[(1)]	High impedance	L	L

(1) x = Floating Condition

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
UCC27511DBVR	PREVIEW	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC27511DBVT	PREVIEW	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC27517DBVR	PREVIEW	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC27517DBVT	PREVIEW	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

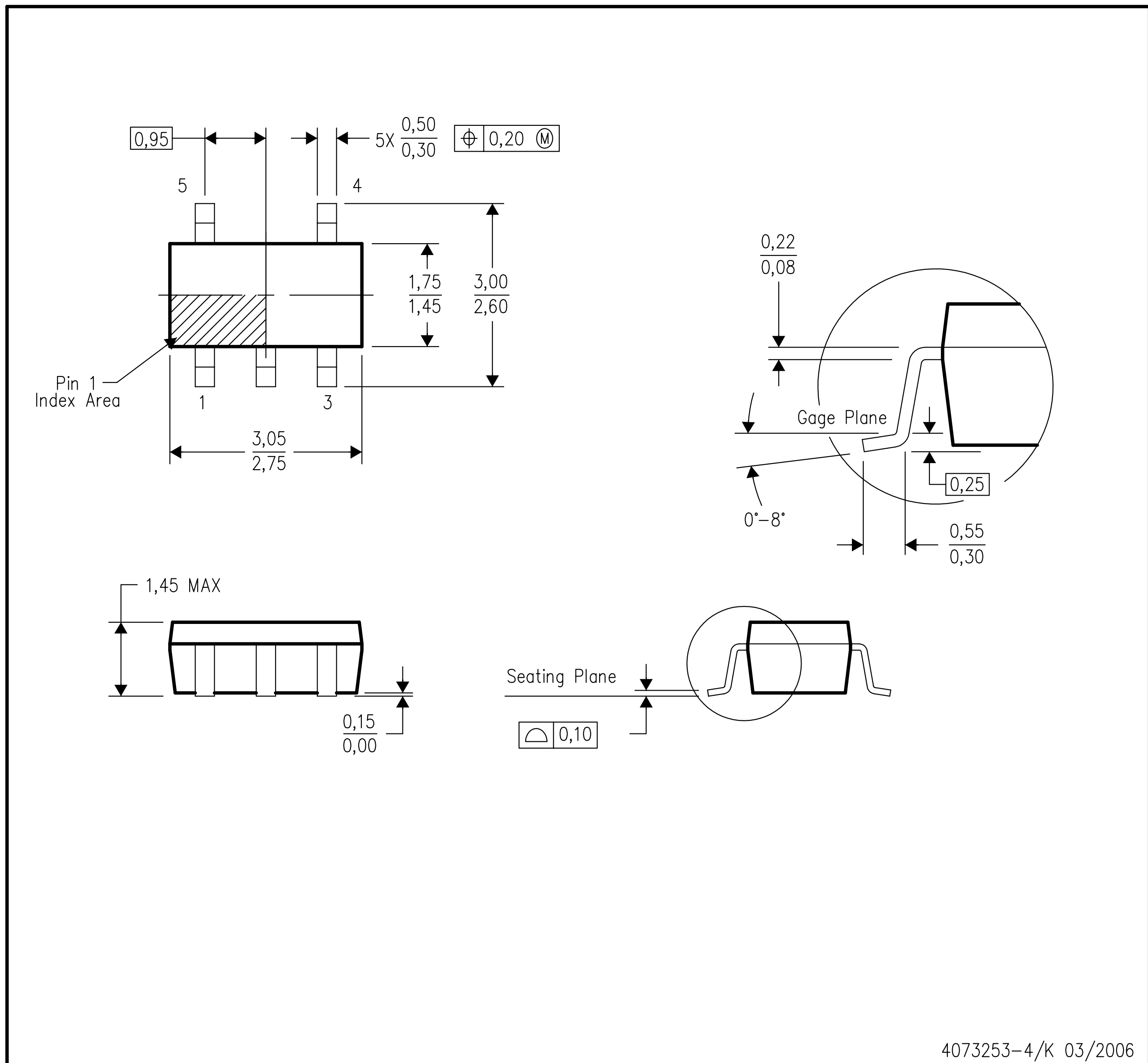
[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

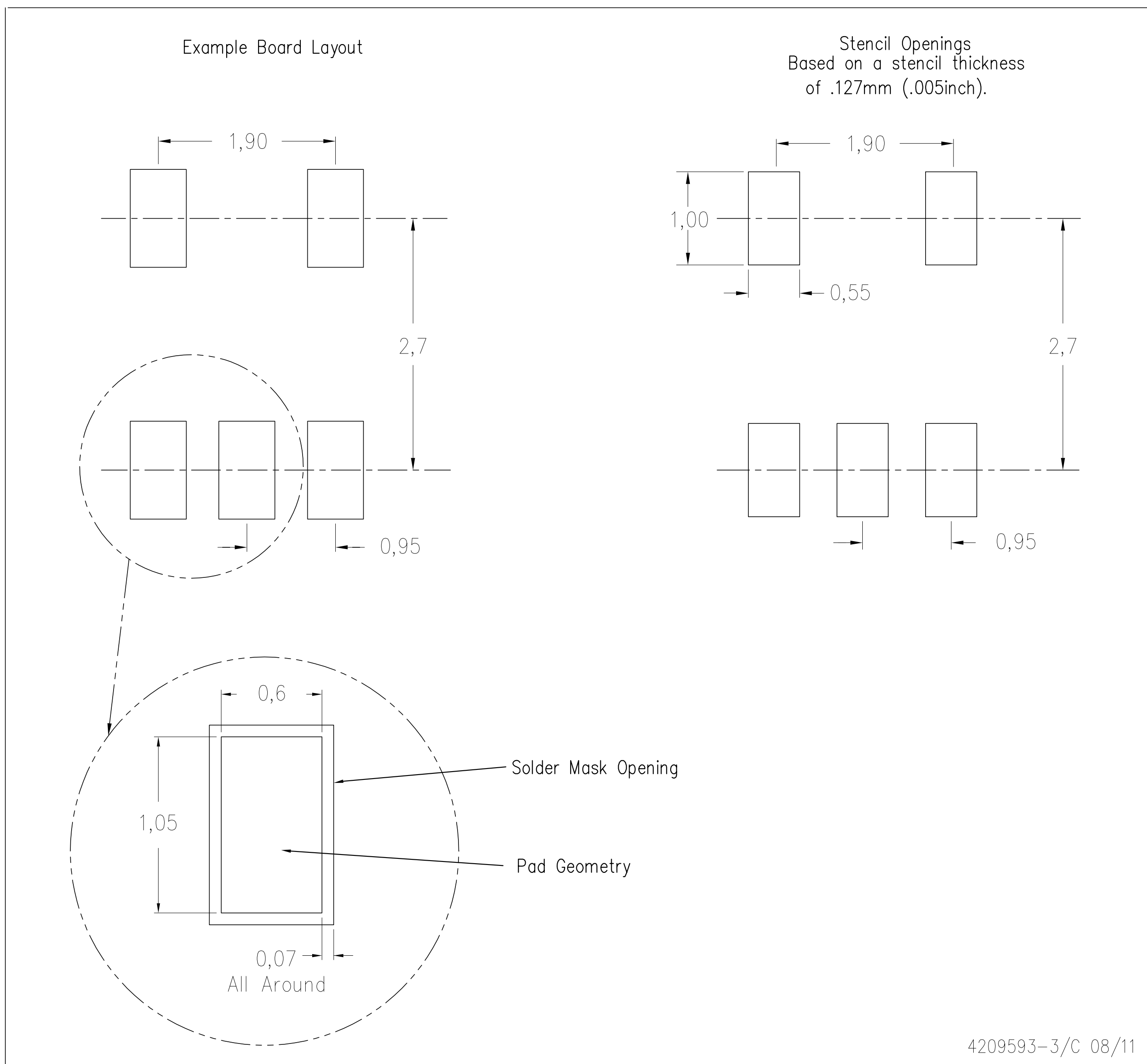
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



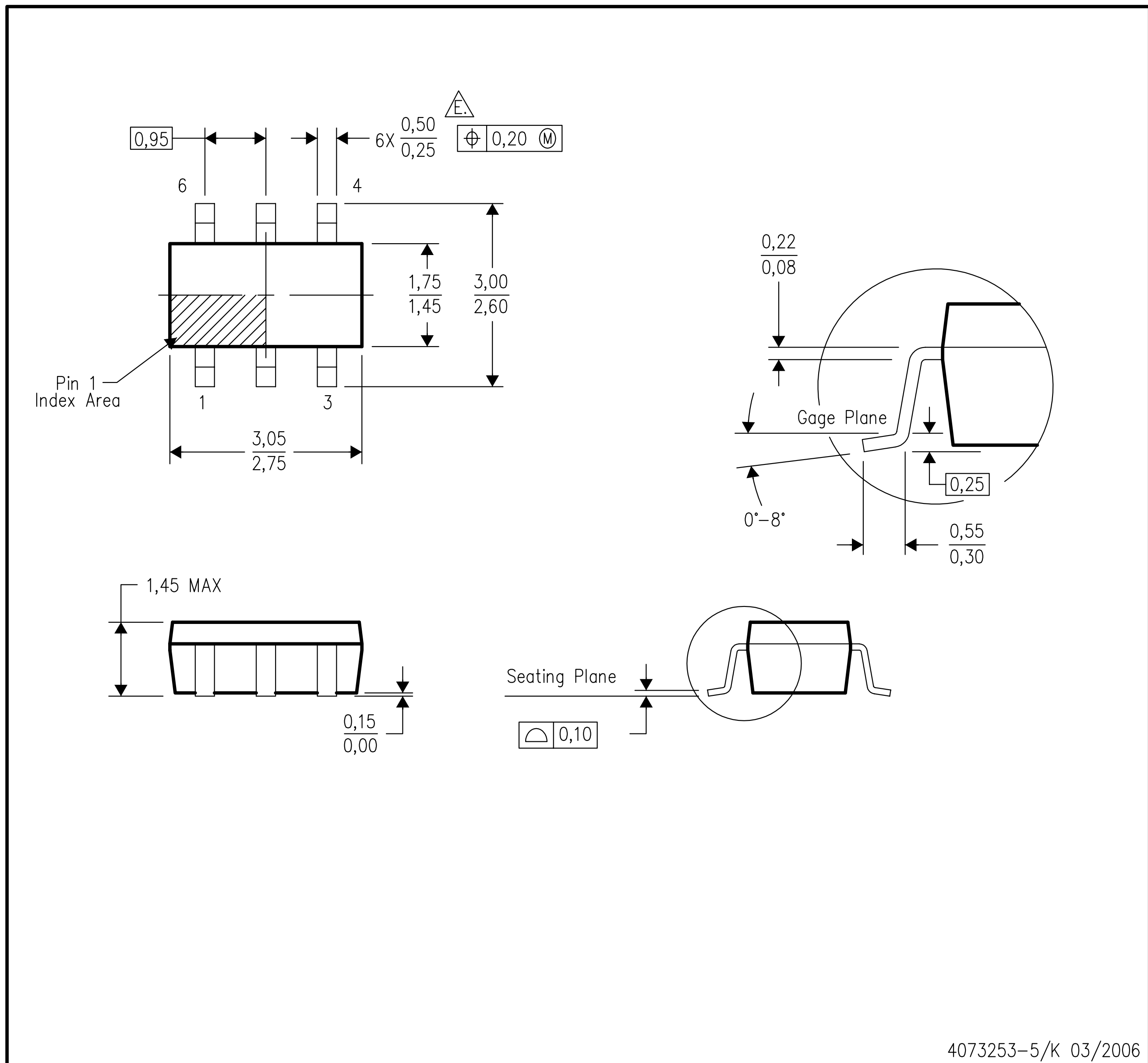
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DBV (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- E. Falls within JEDEC MO-178 Variation AB, except minimum lead width.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		
		TI E2E Community Home Page	e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2012, Texas Instruments Incorporated