

High Speed PWM Controller

FEATURES

- Compatible with Voltage or Current-Mode Topologies
- Practical Operation @ Switching Frequencies to 1.0MHz
- 50ns Propagation Delay to Output
- High Current Totem Pole Output (1.5A peak)
- Wide Bandwidth Error Amplifier
- Fully Latched Logic with Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Soft Start/Max. Duty Cycle Control
- Under-Voltage Lockout with Hysteresis
- Low Start Up Current (1.1mA)
- Trimmed Bandgap Reference (5.1V \pm 1%)

DESCRIPTION

The UC1823 family of PWM control ICs is optimized for high frequency switched mode power supply applications. Particular care was given to minimizing propagation delays through the comparators and logic circuitry while maximizing bandwidth and slew rate of the error amplifier. This controller is designed for use in either current-mode or voltage-mode systems with the capability for input voltage feed-forward.

Protection circuitry includes a current limit comparator, a TTL compatible shutdown port, and a soft start pin which will double as a maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at the output. An under-voltage lockout section with 800mV of hysteresis assures low start up current. During under-voltage lockout, the output is high impedance. The current limit reference (pin 11) is a DC input voltage to the current limit comparator. Consult specifications for details.

These devices feature a totem pole output designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The on state is defined as a high level.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pins 15, 13)	30V
Output Current, Source or Sink (Pin14)	
DC	0.5A
Pulse (0.5 μ s)	2.0A
Analog Inputs (Pins 1, 2, 7, 8, 9, 11)	-0.3V to +6V
Clock Output Current (Pin 4)	-5mA
Error Amplifier Output Current (Pin 3)	5mA
Soft Start Sink Current (Pin 8)	20mA

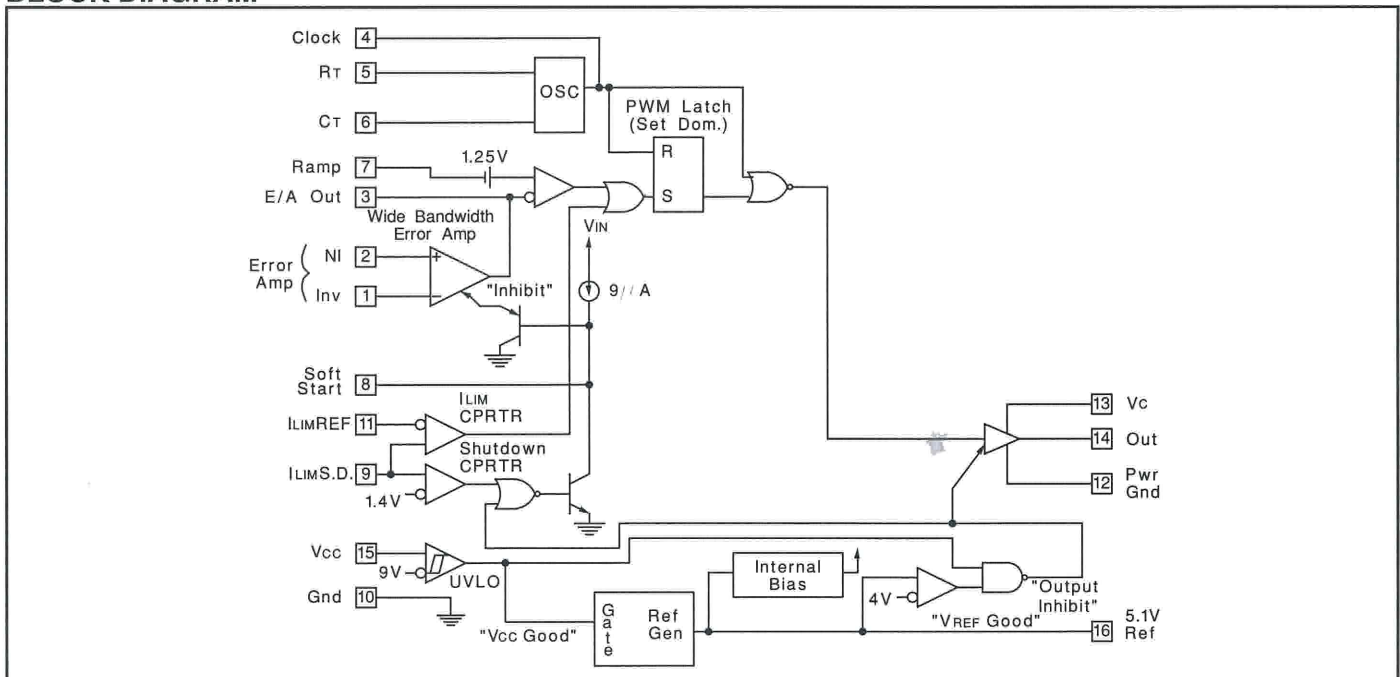
Oscillator Charging Current (Pin 5)	-5mA
Power Dissipation at T _A = 60 °C	1W
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Note: All voltages are with respect to ground, Pin 10.

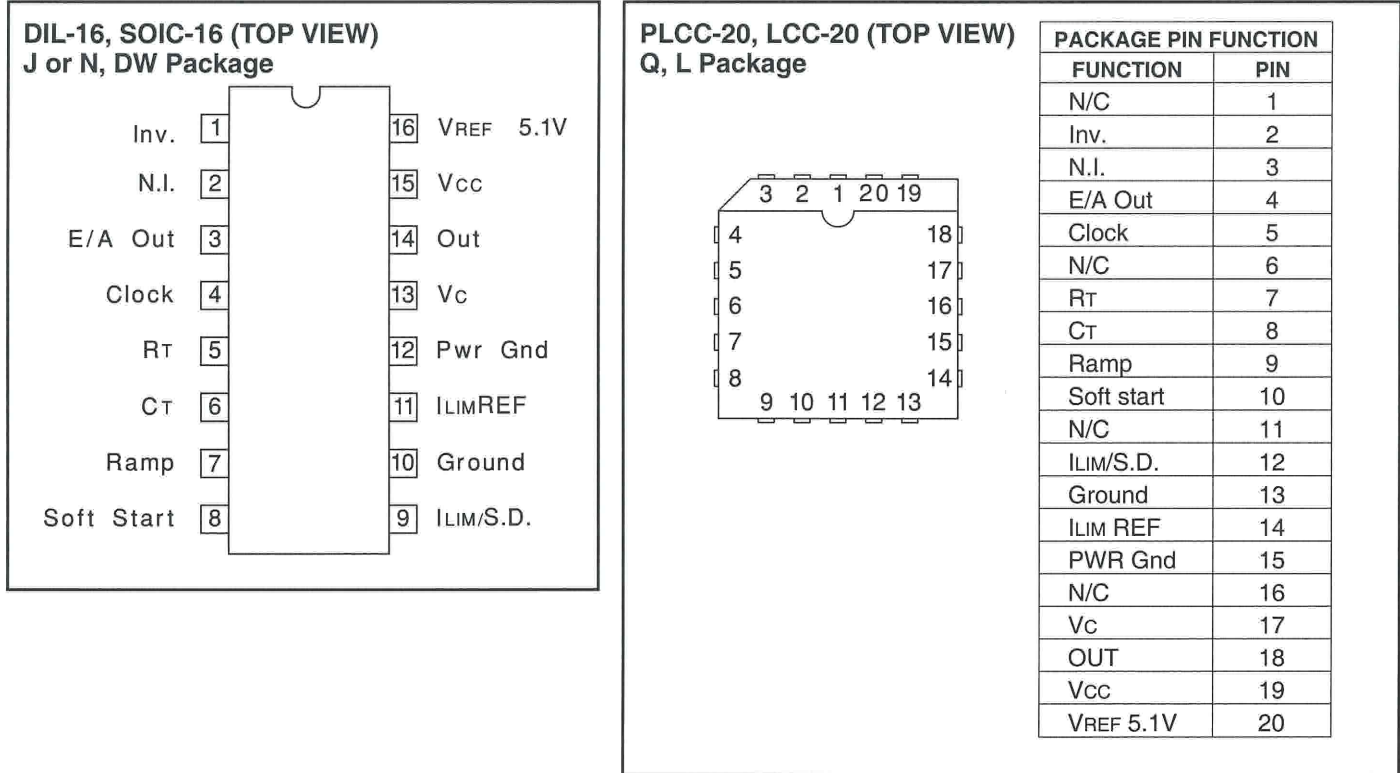
Currents are positive into the specified terminal.

Consult Packaging Section of Databook for thermal limitations

BLOCK DIAGRAM



CONNECTION DIAGRAMS



THERMAL PACKAGING INFORMATION

PACKAGE	θ_{JA}	θ_{JC}
J-16	80 - 120	28 (Note2)
N-16	90 (Note1)	45
DW-16	45 - 90 (Note1)	25
PLCC-20 Q Package	43 - 75 (Note1)	34
LCC-20 LPackage	70 - 80	20 (Note2)

Note 1. Specified θ_{JA} (junction to ambient) is for devices mounted to 5-in-2 FR4 PC board with one ounce copper where noted. When resistance range is given, lower values are for 5-in-2 aluminum PC board. Test PWB was 0.062 in thick and typically used 0.635 mm trace widths for power pkgs and 1.3 mm trace widths for non-power pkgs with a 100 x 100 mil probe land area at the end of each trace.

Note 2. θ_{JC} data values stated were derived from MIL-STD-1835B. MIL-STD-1835B states that "The baseline values shown are worst case (mean + 2s) for a 60 x 60 mil microcircuit device silicon die and applicable for devices with die sizes up to 14400 square mils. For device die sizes greater than 14400 square mils use the following values; dual-in-line, 11°C/W; flat pack, 10°C/W; pin grid array, 10°C/W"

ELECTRICAL CHARACTERISTICS: Unless otherwise noted, these specifications apply for $R_T = 3.65k$, $C_T = 1nF$, $V_{CC} = 15V$, $0^\circ C < T_A < +70^\circ C$ for the UC3823, $-25^\circ C < T_A < +85^\circ C$ for the UC2823, and $-55^\circ C < T_A < +125^\circ C$ for the UC1823, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC1823 UC2823			UC3823			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	$T_J = 25^\circ C$, $I_O = 1mA$	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	$10 < V_{CC} < 30V$		2	20		2	20	mV
Load Regulation	$1 < I_O < 10mA$		5	20		5	20	mV
Temperature Stability*	$T_{MIN} < T_A < T_{MAX}$		0.2	0.4		0.2	0.4	mV/ $^\circ C$
Total Output Variation*	Line, Load, Temp.	5.00		5.20	4.95		5.25	
Output Noise Voltage*	$10Hz < f < 10kHz$		50			50		μV
Long Term Stability*	$T_J = 125^\circ C$, 1000 hrs.		5	25		5	25	mV
Short Circuit Current	$V_{REF} = 0V$	-15	-50	-100	-15	-50	-100	mA
Oscillator Section								
Initial Accuracy*	$T_J = 25^\circ C$	360	400	440	360	400	440	kHz
Voltage Stability*	$10 < V_{CC} < 30V$		0.2	2		0.2	2	%
Temperature Stability*	$T_{MIN} < T_A < T_{MAX}$ (UC1823)		12					%
	$T_{MIN} < T_A < T_{MAX}$ (UC2823)		5					%
	$T_{MIN} < T_A < T_{MAX}$ (UC3823)					5		%
Total Variation*	Line, Temp.	340		460	340		460	kHz
Clock Out High		3.9	4.5		3.9	4.5		V
Clock Out Low			2.3	2.9		2.3	2.9	V
Ramp Peak*		2.6	2.8	3.0	2.6	2.8	3.0	V
Ramp Valley*		0.7	1.0	1.25	0.7	1.0	1.25	V
Error Amplifier Section								
Input Offset Voltage				10			15	mV
Input Bias Current			0.6	3		0.6	3	μA
Input Offset Current			0.1	1		0.1	1	μA
Open Loop Gain	$1 < V_O < 4V$	60	95		60	95		dB
CMRR	$1.5 < V_{CM} < 5.5V$	75	95		75	95		dB
PSRR	$10 < V_{CC} < 30V$	85	110		85	110		dB
Output Sink Current	$V_{PIN3} = 1V$	1	2.5		1	2.5		mA
Output Source Current	$V_{PIN3} = 4V$	-0.5	-1.3		-0.5	-1.3		mA
Output High Voltage	$I_{PIN3} = -0.5mA$	4.0	4.7	5.0	4.0	4.7	5.0	V
Output Low Voltage	$I_{PIN3} = 1mA$	0	0.5	1.0	0	0.5	1.0	V
Unity Gain Bandwidth*		3	5.5		3	5.5		MHz
Slew Rate*		6	12		6	12		V/ μS
Ramp Valley to Peak*		1.6	1.8	2.0	1.6	1.8	2.0	V

* These parameters are ensured by design but not 100% tested in production.

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PARAMETER	TEST CONDITIONS	UC1823 UC2823			UC3823			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
PWM Comparator Section								
Pin 7 Bias Current	$V_{PIN 7} = 0V$		-1	-5		-1	-5	μA
Duty Cycle Range		0		80	0		85	%
Pin 3 Zero D.C. Threshold	$V_{PIN 7} = 0V$	1.1	1.25		1.1	1.25		V
Delay to Output*			50	80		50	80	ns
Soft-Start Section								
Charge Current	$V_{PIN 8} = 0.5V$	3	9	20	3	9	20	μA
Discharge Current	$V_{PIN 8} = 1V$	1			1			mA
Current Limit/Shutdown Section								
Pin 9 Bias Current	$0 < V_{PIN 9} < 4V$			± 10			± 10	μA
Current Limit Offset	$V_{PIN 11} = 1.1V$			15			15	mV
Current Limit Common Mode Range ($V_{PIN 11}$)		1.0		1.25	1.0		1.25	V
Shutdown Threshold		1.25	1.40	1.55	1.25	1.40	1.55	V
Delay to Output*			50	80		50	80	ns
Output Section								
Output Low Level	$I_{OUT} = 20mA$		0.25	0.40		0.25	0.40	V
	$I_{OUT} = 200mA$		1.2	2.2		1.2	2.2	V
Output High Level	$I_{OUT} = -20mA$	13.0	13.5		13.0	13.5		V
	$I_{OUT} = -200mA$	12.0	13.0		12.0	13.0		V
Collector Leakage	$V_C = 30V$		100	500		100	500	μA
Rise/Fall Time*	$C_L = 1nF$		30	60		30	60	ns
Under-Voltage Lockout Section								
Start Threshold		8.8	9.2	9.6	8.8	9.2	9.6	V
UVLO Hysteresis		0.4	0.8	1.2	0.4	0.8	1.2	V
Supply Current								
Start Up Current	$V_{CC} = 8V$		1.1	2.5		1.1	2.5	mA
I_{CC}	$V_{PIN 1}, V_{PIN 7}, V_{PIN 9} = 0V, V_{PIN 2} = 1V$		22	33		22	33	mA

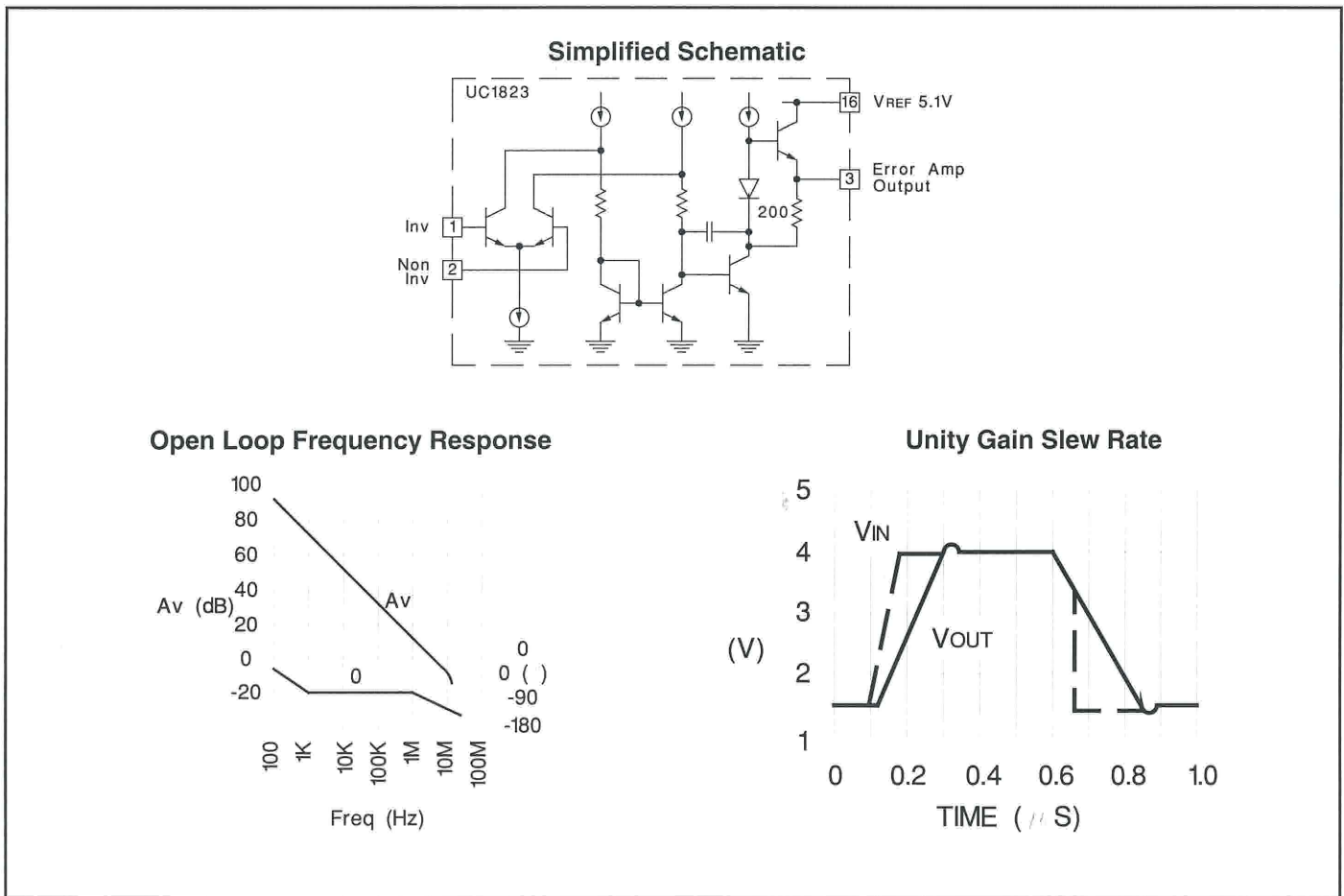
* These parameters are ensured by design but not 100% tested in production.

UC1823 PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

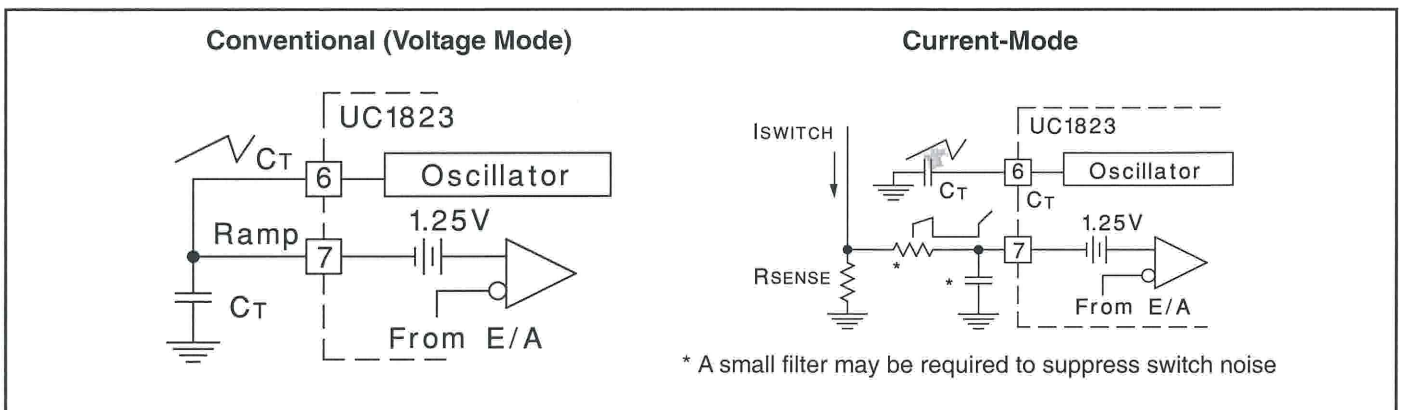
High speed circuits demand careful attention to layout and component placement. To assure proper performance of the UC1823, follow these rules. 1) Use a ground plane. 2) Damp or clamp parasitic inductive kick energy from the gate of driven MOSFET. Don't allow the output pins to ring below ground. A series gate resistor or a shunt 1 Amp Schottky diode at the output pin will serve

this purpose. 3) Bypass VCC, Vc, and VREF. Use 0.1 μ F monolithic ceramic capacitors with low equivalent series inductance. Allow less than 1 cm of total lead length for each capacitor between the bypassed pin and the ground plane. 4) Treat the timing capacitor, CT, like a bypass capacitor.

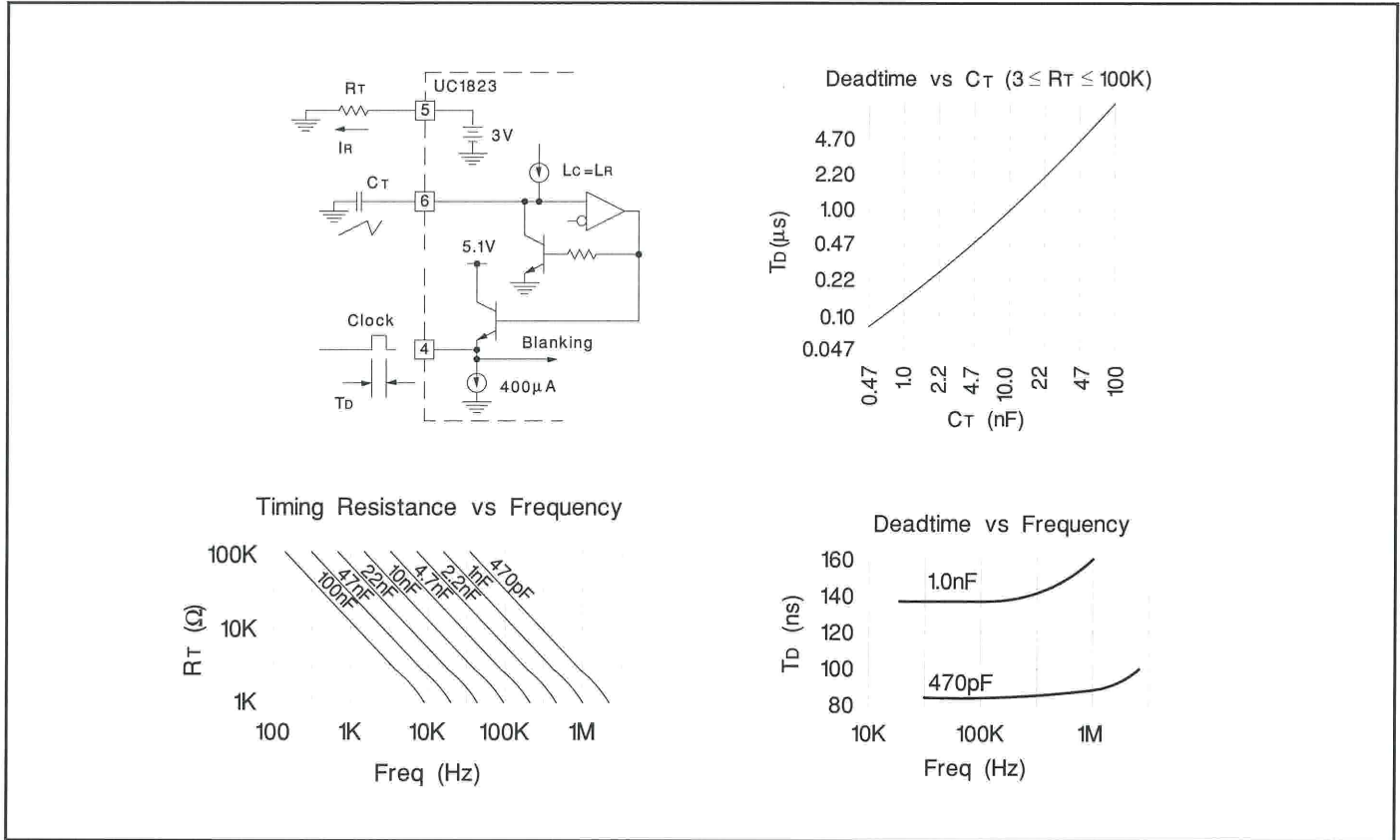
ERROR AMPLIFIER CIRCUIT



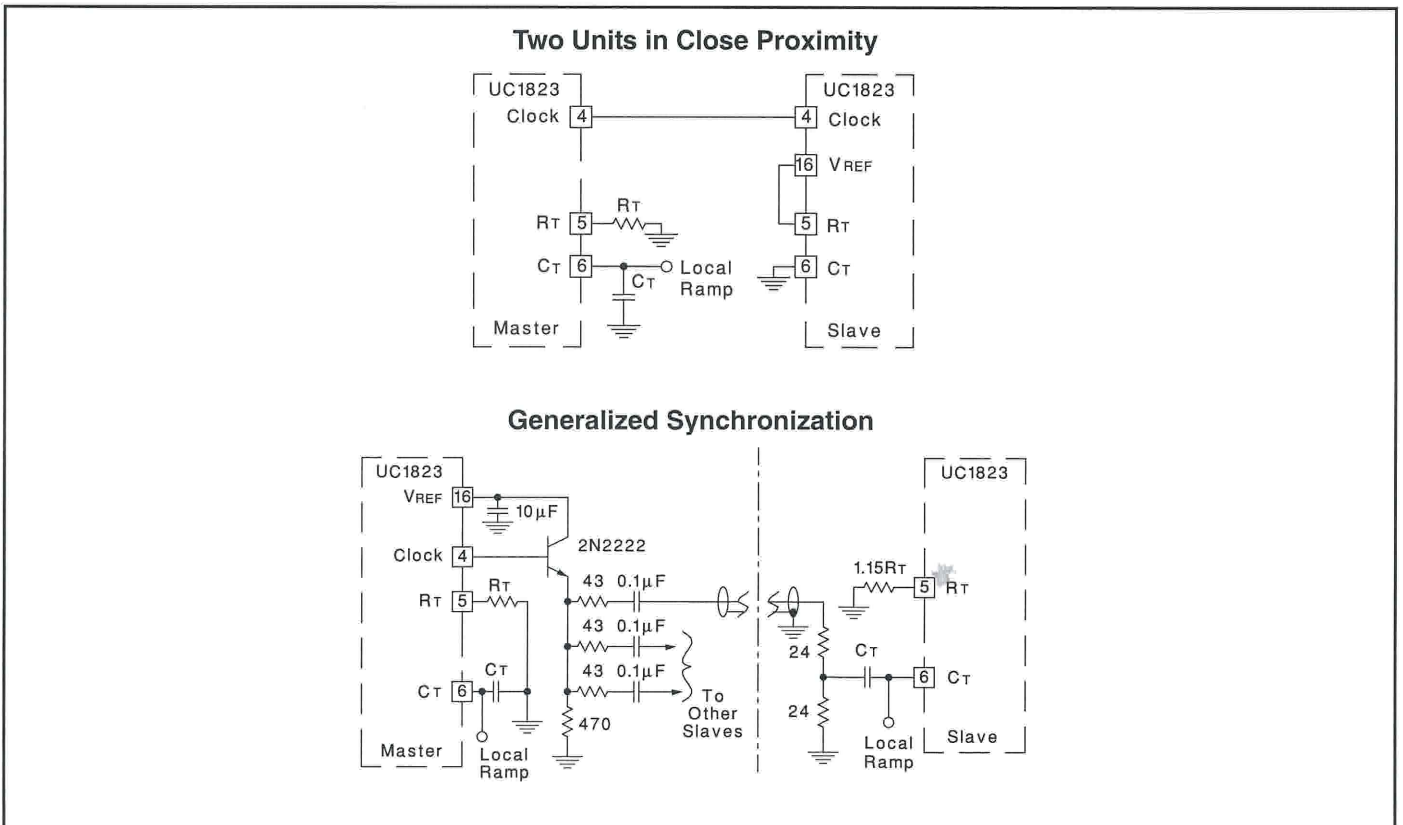
PWM APPLICATIONS



OSCILLATOR CIRCUIT

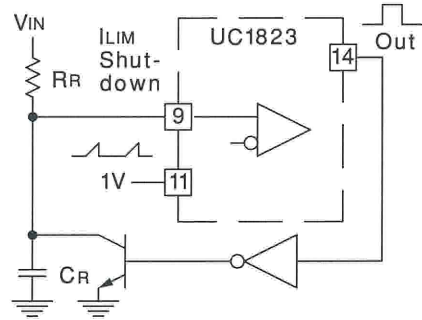


SYNCHRONIZED OPERATION



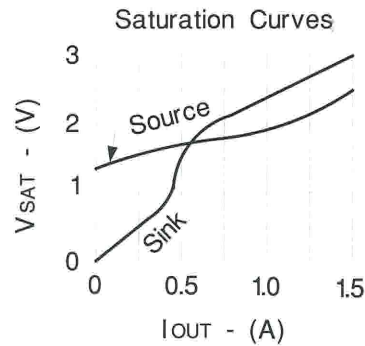
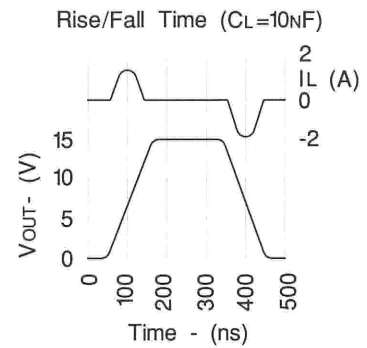
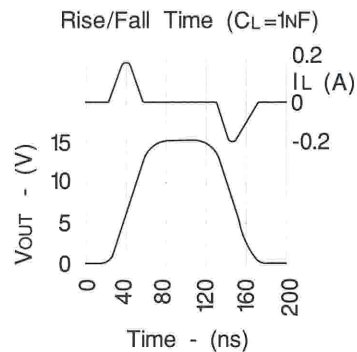
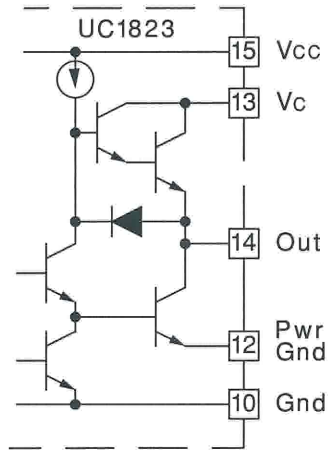
CONSTANT VOLT-SECOND CLAMP CIRCUIT

The circuit shown here will achieve a constant volt-second product clamp over varying input voltages. The ramp generator components, R_T and C_R are chosen so that the ramp at Pin 9 crosses the 1V threshold at the same time the desired maximum volt-second product is reached. The delay through the inverter must be such that the ramp capacitor can be completely discharged during the minimum deadtime.

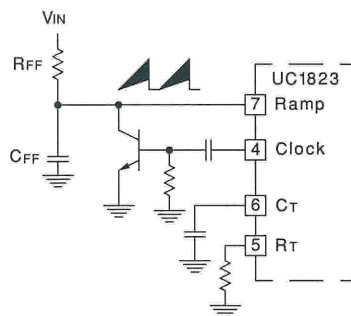


OUTPUT SECTION

Simplified Schematic



FEED FORWARD TECHNIQUE FOR OFF-LINE VOLTAGE MODE APPLICATION



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-89905012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8990501EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
UC1823J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
UC1823J883B	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
UC1823L	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
UC1823L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
UC2823DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2823DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2823DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2823DWTRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2823N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2823NG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2823Q	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UC2823QG3	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UC2823QTR	ACTIVE	PLCC	FN	20	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UC2823QTRG3	ACTIVE	PLCC	FN	20	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UC3823DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3823DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3823DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3823DWTRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3823N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3823NG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3823Q	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UC3823QG3	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UC3823QTR	ACTIVE	PLCC	FN	20	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UC3823QTRG3	ACTIVE	PLCC	FN	20	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

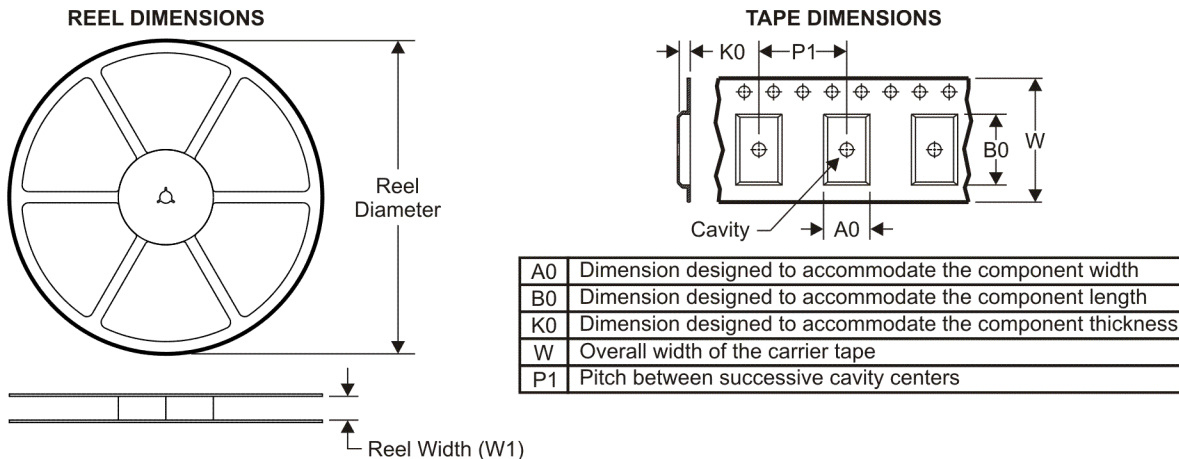
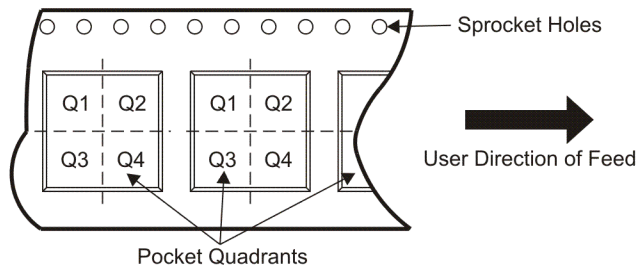
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2823DWTR	SOIC	DW	16	2000	330.0	16.4	10.85	10.8	2.7	12.0	16.0	Q1
UC2823QTR	PLCC	FN	20	1000	330.0	16.4	10.3	10.3	4.9	12.0	16.0	Q1
UC3823DWTR	SOIC	DW	16	2000	330.0	16.4	10.85	10.8	2.7	12.0	16.0	Q1
UC3823QTR	PLCC	FN	20	1000	330.0	16.4	10.3	10.3	4.9	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2823DWTR	SOIC	DW	16	2000	346.0	346.0	33.0
UC2823QTR	PLCC	FN	20	1000	346.0	346.0	33.0
UC3823DWTR	SOIC	DW	16	2000	346.0	346.0	33.0
UC3823QTR	PLCC	FN	20	1000	346.0	346.0	33.0

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