TUSB1210 Stand-Alone USB Transceiver Chip Silicon

1 Device Overview

1.1 Features

- USB2.0 PHY Transceiver Chip, Designed to Interface With a USB Controller Through a ULPI Interface, Fully Compliant With:
  - *Universal Serial Bus Specification* Rev. 2.0
  - *On-The-Go Supplement to the USB 2.0 Specification* Rev. 1.3
  - *UTMI+ Low Pin Interface (ULPI) Specification* Rev. 1.1
  - *ULPI 12-pin SDR Interface*
- DP/DM Line External Component Compensation (Patent #US7965100 B1)
- Interfaces to Host, Peripheral and OTG Device Cores; Optimized for Portable Devices or System ASICs With Built-in USB OTG Device Core
- Complete USB OTG Physical Front-End That Supports Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)
- V_{BUS} Overvoltage Protection Circuitry Protects V_{BUS} Pin in Range –2 V to 20 V
- Internal 5-V Short-Circuit Protection of DP, DM, and ID Pins for Cable Shorting to V_{BUS} Pin
- ULPI Interface:
  - I/O Interface (1.8 V) Optimized for Nonterminated 50-Ω Line Impedance
  - ULPI CLOCK Pin (60 MHz) Supports Both Input and Output Clock Configurations
  - Fully Programmable ULPI-Compliant Register Set
- Full Industrial Grade Operating Temperature Range From –40°C to 85°C
- Available in a 32-Pin Quad Flat No Lead [QFN (RHB)] Package

1.2 Applications

- Mobile Phones
- Portable Computers
- Tablet Devices
- Video Game Consoles
- Desktop Computers
- Portable Music Players

1.3 Description

The TUSB1210 is a USB2.0 transceiver chip, designed to interface with a USB controller through a ULPI interface. The device supports all USB2.0 data rates (high-speed 480 Mbps, full-speed 12 Mbps, and low-speed 1.5 Mbps), and is compliant to both host and peripheral modes. The device additionally supports a UART mode and legacy ULPI serial modes. TUSB1210 also supports the OTG (Ver1.3) optional addendum to the USB 2.0 Specification, including HNP and SRP.

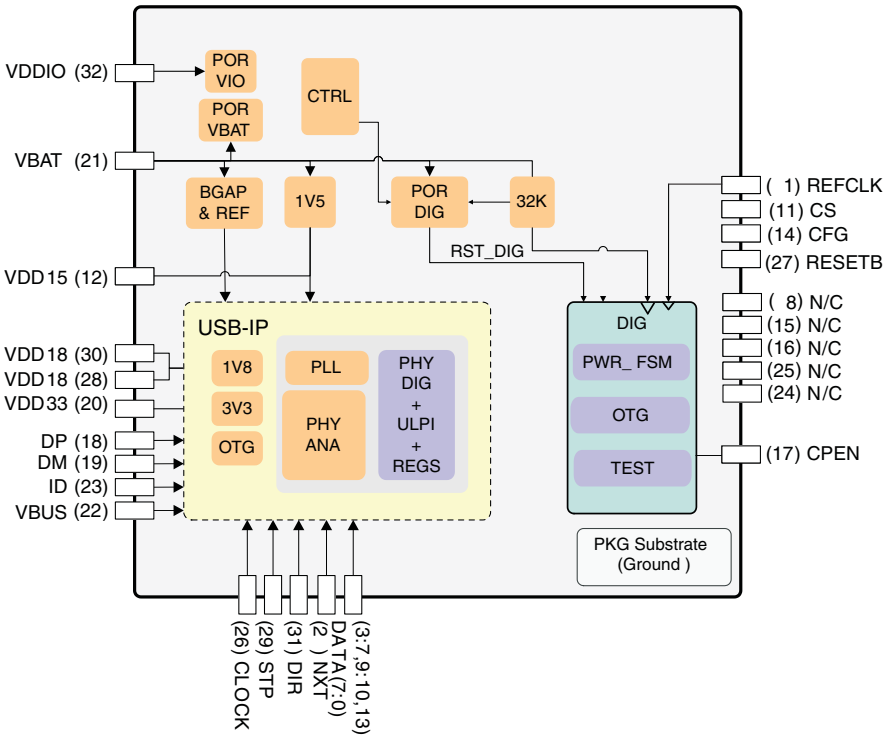
The DP/DM external component compensation in the transmitter compensates for variations in the series impendence in order to match with the data line impedance and the receiver input impedance, to limit data reflections and thereby improve eye diagrams.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TUSB1210	VQFN (32)	5.00 mm x 5.00 mm

(1) For more information, see Section 8, *Mechanical Packaging and Orderable Information*.

1.4 TUSB1210 Block Diagram



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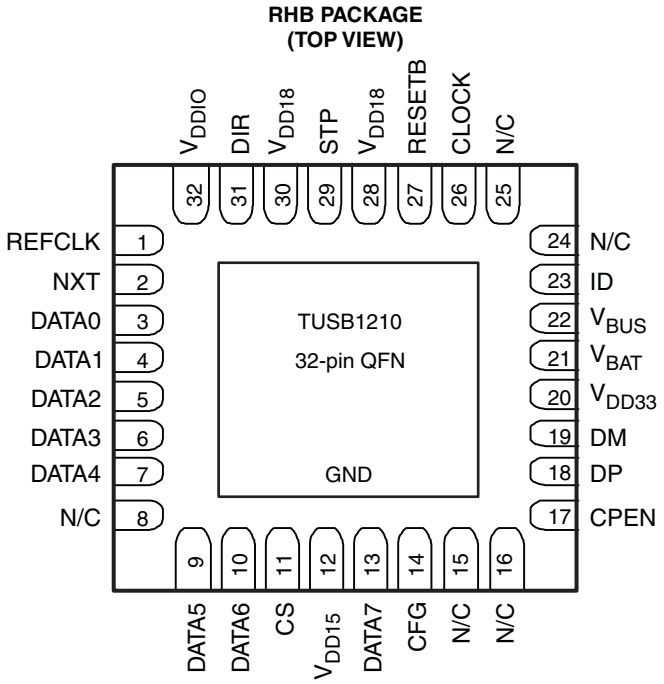
2 Revision History

Changes from Revision F (July 2013) to Revision G	Page
• Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

3 Pin Configuration and Functions

3.1 Pin Description



Pin Functions

PIN		A/D	TYPE	LEVEL	DESCRIPTION
NO.	NAME				
1	REFCLK	A	I	3.3 V	V_{DD33} Reference clock input (square-wave only). Tie to GND when pin 26 (CLOCK) is required to be Input mode. Connect to square-wave reference clock of amplitude in the range of 3 V to 3.6 V when Pin 26 (CLOCK) is required to be Output mode. See pin 14 (CFG) description for REFCLK input frequency settings.
2	NXT	D	O	V_{DDIO}	ULPI NXT output signal
3	DATA0	D	I/O	V_{DDIO}	ULPI DATA input/output signal 0 synchronized to CLOCK
4	DATA1	D	I/O	V_{DDIO}	ULPI DATA input/output signal 1 synchronized to CLOCK
5	DATA2	D	I/O	V_{DDIO}	ULPI DATA input/output signal 2 synchronized to CLOCK
6	DATA3	D	I/O	V_{DDIO}	ULPI DATA input/output signal 3 synchronized to CLOCK
7	DATA4	D	I/O	V_{DDIO}	ULPI DATA input/output signal 4 synchronized to CLOCK
8	N/C	–	–	V_{DDIO}	No connect
9	DATA5	D	I/O	V_{DDIO}	ULPI DATA input/output signal 5 synchronized to CLOCK
10	DATA6	D	I/O	V_{DDIO}	ULPI DATA input/output signal 6 synchronized to CLOCK
11	CS	D	I	V_{DDIO}	Active-high chip select pin. When low the IC is in power down and ULPI bus is tri-stated. When high normal operation. Tie to V_{DDIO} if unused.
12	VDD15	A	power		1.5-V internal LDO output. Connect to external filtering capacitor.
13	DATA7	D	I/O	V_{DDIO}	ULPI DATA input/output signal 7 synchronized to CLOCK
14	CFG	D	I	V_{DDIO}	REFCLK clock frequency configuration pin. Two frequencies are supported: 19.2 MHz when 0, or 26 MHz when 1.
15	N/C	–	–	–	No connect
16	N/C	–	–	–	No connect
17	CPEN	D	O	V_{DD33}	CMOS active-high digital output control of external 5V VBUS supply
18	DP	A	I/O	V_{DD33}	DP pin of the USB connector
19	DM	A	I/O	V_{DD33}	DM pin of the USB connector

Pin Functions (continued)

PIN		A/D	TYPE	LEVEL	DESCRIPTION
NO.	NAME				
20	V_{DD33}	A	power	V_{DD33}	3.3-V internal LDO output. Connect to external filtering capacitor.
21	V_{BAT}	A	power	V_{BAT}	Input supply voltage or battery source
22	V_{BUS}	A	power	V_{BUS}	V_{BUS} pin of the USB connector
23	ID	A	I/O	V_{DD33}	Identification (ID) pin of the USB connector
24	N/C	–	–	–	No connect
25	N/C	–	–	–	No connect
26	CLOCK	D	O	V_{DDIO}	ULPI 60 MHz clock on which ULPI data is synchronized. Two modes are possible: Input Mode: CLOCK defaults as an input. Output Mode: When an input clock is detected on REFCLK pin (after 4 rising edges) then CLOCK will change to an output.
27	RESETB	D	I	V_{DDIO}	When low, all digital logic (except 32 kHz logic required for power up sequencing) including registers are reset to their default values, and ULPI bus is tri-stated. When high, normal USB operation.
28	V_{DD18}	A	power	V_{DD18}	External 1.8-V supply input. Connect to external filtering capacitor.
29	STP	D	I	V_{DDIO}	ULPI STP input signal
30	V_{DD18}	A	power	V_{DD18}	External 1.8-V supply input. Connect to external filtering capacitor.
31	DIR	D	O	V_{DDIO}	ULPI DIR output signal
32	V_{DDIO}	A	I	V_{DDIO}	External 1.8V supply input for digital I/Os. Connect to external filtering capacitor.

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Main battery supply voltage (2)		0	5	V
	Voltage on any input(3)	Where supply represents the voltage applied to the power supply pin associated with the input	–0.3	$1 \times V_{CC}$ +0.3	V
	V_{BUS} input		–2	20	V
	ID, DP, DM inputs	Stress condition guaranteed 24h	–0.3	5.25	V
V_{DDIO}	IO supply voltage	Continuous		1.98	V
T_A	Ambient temperature range		–40	85	°C
T_J	Ambient temperature range	Absolute maximum rating	–40	150	°C
		For parametric compliance	–40	125	
	Ambient temperature for parametric compliance	With max 125°C as junction temperature	–40	85	°C
	DP, DM, ID high voltage short circuit	DP, DM or ID pins short circuited to V_{BUS} supply, in any mode of TUSB1210 operation, continuously for 24 hours		5.25	V
	DP, DM, ID low voltage short circuit	DP, DM or ID pins short circuited to GND in any mode of TUSB1210 operation, continuously for 24 hours	0		V

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Section 4.3* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The product will have negligible reliability impact if voltage spikes of 5.5 V occur for a total (cumulative over lifetime) duration of 5 milliseconds.
(3) Except V_{BAT} input, V_{BUS}, ID, DP, and DM pads

4.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–55	125	°C
V_{ESD}	Electrostatic discharge (ESD) performance:	Human body model (HBM), per ANSI/ESDA/JEDEC JS001, all pins(1)	2000	2000	kV
		Charged device model (CDM), per JESD22-C101, all pins(2)	500	500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{BAT}	Battery supply voltage		2.7	3.6	4.8	V
$V_{BAT\ CERT}$	Battery supply voltage for USB 2.0 compliancy (USB 2.0 certification)	When V_{DD33} is supplied internally	3.15			V
		When V_{DD33} is shorted to V_{BAT} externally	3.05			
V_{DDIO}	Digital IO pin supply		1.71		1.98	V
T_A	Ambient temperature range		–40		85	°C

4.4 Thermal Information

PARAMETER		MEASUREMENT METHOD	VALUE	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	EIA/JESD 51-1	34.72	°C/W
θ_{JC} top	Junction-to-case top thermal resistance (1)	No current JEDEC specification (2)	37.3	°C/W
θ_{JC} bottom	Junction-to-case bottom thermal resistance (3)	No current JEDEC specification (2)	3.6	°C/W
θ_{JB}	Junction-to-board thermal resistance or junction-to-pin thermal resistance	EIA/ JESD 51-8.	10.3	°C/W
Ψ_{JT}	Junction-to-top of package (not a true thermal resistance)	EIA/JESD 51-2	0.5	°C/W
Ψ_{JB}	Junction-to-board (not a true thermal resistance)	EIA/JESD 51-6	10.5	°C/W

(1) Top is surface of the package facing away from the PCB.
(2) Refer to measurement method in Chapter 2 of *IC Package Thermal Metrics* (SPRA953).
(3) Bottom surface is the surface of the package facing towards the PCB.

4.5 Power Consumption

Table 4-1 describes the power consumption depending on the use cases.

NOTE

The typical power consumption is obtained in the nominal operating conditions and with the TUSB1210 standalone.

Table 4-1. Power Consumption

MODE	CONDITIONS	SUPPLY	TYPICAL CONSUMPTION	UNIT
OFF Mode	V_{BAT} = 3.6 V, V_{DDIO} = 1.8 V, V_{DD18} = 1.8 V, CS = 0 V	I_{VBAT}	8	µA
		I_{VDDIO}	3	
		I_{VDD18}	5	
		I_{TOTAL}	16	
Suspend Mode	V_{BUS} = 5 V, V_{BAT} = 3.6 V, V_{DDIO} = 1.8 V, No clock	I_{VBAT}	204	µA
		I_{VDDIO}	3	
		I_{VDD18}	3	
		I_{TOTAL}	210	
HS USB Operation (Synchronous Mode)	V_{BAT} = 3.6 V, V_{DDIO} = 1.8 V, V_{DD18} = 1.8 V, active USB transfer	I_{VBAT}	24.6	mA
		I_{VDDIO}	1.89	
		I_{VDD18}	21.5	
		I_{TOTAL}	48	
FS USB Operation (Synchronous Mode)	V_{BAT} = 3.6 V, V_{DDIO} = 1.8 V, active USB transfer	I_{VBAT}	25.8	mA
		I_{VDDIO}	1.81	
		I_{VDD18}	4.06	
		I_{TOTAL}	31.7	
Reset Mode	RESETB = 0 V, V_{BUS} = 5 V, V_{BAT} = 3.6 V, V_{DDIO} = 1.8 V, No clock	I_{VBAT}	237	µA
		I_{VDDIO}	3	
		I_{VDD18}	3	
		I_{TOTAL}	243	

4.6 I/O Electrical Characteristics

4.6.1 Analog I/O Electrical Characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
CPEN Output Pin						
VOL_{CPEN}	CPEN low-level output voltage	I_{OL} = 3 mA			0.3	V
VOH_{CPEN}	CPEN high-level output voltage	I_{OH} = –3 mA	V_{DD33}–0.3			V

4.6.2 Digital I/O Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLOCK						
V_{OL}	Low-level output voltage	Frequency = 60 MHz, Load = 10 pF			0.45	V
V_{OH}	High-level output voltage		V_{DDIO} - 0.45			V
STP, DIR, NXT, DATA0 to DATA7						
V_{OL}	Low-level output voltage	Frequency = 60 MHz, Load = 10 pF			0.45	V
V_{OH}	High-level output voltage		V_{DDIO} - 0.45			V

4.6.3 Electrical Characteristics: Digital IO Pins (Non-ULPI)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
CS, CFG, RESETB Input Pins						
V_{IL}	Maximum low-level input voltage				0.35 * V_{DDIO}	V
V_{IH}	Minimum high-level input voltage		0.65 * V_{DDIO}			V
RESETB Input Pin Timing Spec						
$t_{w(POR)}$	Internal power-on reset pulse width		0.2			µs
$t_{w(RESET)}$	External RESETB pulse width	Applied to external RESETB pin when CLOCK is toggling.	8			CLOCK cycles

4.7 Clock Specifications

4.7.1 USB PLL Reference Clock

The USB PLL block generates the clocks used to synchronize :

- the ULPI interface (60 MHz clock)
- the USB interface (depending on the USB data rate, 480 Mbps, 12 Mbps or 1.5 Mbps)

TUSB1210 requires an external reference clock which is used as an input to the 480 MHz USB PLL block. Depending on the clock configuration, this reference clock can be provided either at REFCLK pin or at CLOCK pin. By default CLK pin is configured as an input.

Two clock configurations are possible:

- Input clock configuration (see Section 4.7.2)
- Output clock configuration (see Section 4.7.3)

4.7.2 ULPI Input Clock Configuration

In this mode REFCLK must be externally tied to GND. CLOCK remains configured as an input.

When the ULPI interface is used in input clock configuration, i.e., the 60 MHz ULPI clock is provided to TUSB1210 on Clock pin, then this is used as the reference clock for the 480 MHz USB PLL block.

Table 4-2. Electrical Characteristics: Clock Input

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Clock input duty cycle		40		60%	
f_{CLK}	Clock nominal frequency			60		MHz
	Clock input rise/fall time	In % of clock period t_{CLK} (= $1/f_{CLK}$)			10%	
	Clock input frequency accuracy				250	ppm
	Clock input integrated jitter				600	ps rms

4.7.3 ULPI Output Clock Configuration

In this mode a reference clock must be externally provided on REFCLK pin When an input clock is detected on REFCLK pin then CLK will automatically change to an output, i.e., 60 MHz ULPI clock is output by TUSB1210 on CLK pin.

Two reference clock input frequencies are supported. REFCLK input frequency is communicated to TUSB1210 via a configuration pin, CFG, see f_{REFCLK} in Table 6-2 for frequency correspondence. TUSB1210 supports square-wave reference clock input only. Reference clock input must be square-wave of amplitude in the range 3.0 V to 3.6 V.

Table 4-3. Electrical Characteristics: REFCLK

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	REFCLK input duty cycle		40		60%	
f_{REFCLK}	REFCLK nominal frequency	When CFG pin is tied to GND		19.2		MHz
		When CFG pin is tied to V_{DDIO}		26		
	REFCLK input rise/fall time	In % of clock period t_{REFCLK} (= $1/f_{REFCLK}$)			20%	
	REFCLK input frequency accuracy				250	ppm
	REFCLK input integrated jitter				600	ps rms
	REFCLK HIZ Leakage current				3	µA
	REFCLK HIZ Leakage current		–3			

4.7.4 Clock 32 kHz

An internal clock generator running at 32 kHz has been implemented to provide a low-speed, low-power clock to the system

Table 4-4. Performances

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output duty cycle	Input duty cycle 40–60%	48%	50%	52%	
Output frequency		23	32	38	kHz

4.7.5 Reset

All logic is reset if CS = 0 or V_{BAT} are not present.

All logic (except 32 kHz logic) is reset if V_{DDIO} is not present.

PHY logic is reset when any supplies are not present (V_{DDIO}, V_{DD15}, V_{DD18}, V_{DD33}) or if RESETB pin is low.

TUSB1210 may be reset manually by toggling the RESETB pin to GND for at lease 200 ns.

If manual reset via RESETB is not required then RESETB pin may be tied to V_{DDIO} permanently.

4.8 Power Module

This chapter describes the electrical characteristics of the voltage regulators and timing characteristics of the supplies digitally controlled within the TUSB1210.

4.8.1 Power Modules

4.8.1.1 Power Providers

Table 4-5. Summary of TUSB1210 Power Providers(1)

NAME	USAGE	TYPE	TYPICAL VOLTAGE (V)	MAXIMUM CURRENT (mA)
V_{DD15}	Internal	LDO	1.5	50
V_{DD18}	External	LDO	1.8	30
V_{DD33}	Internal	LDO	3.1	15

(1) V_{DD33} may be supplied externally, or by shorting the V_{DD33} pin to V_{BAT} pin provided V_{BAT} min is in range [3.2 V : 3.6 V]. Note that the V_{DD33} LDO will always power-on when the chip is enabled, irrespective of whether V_{DD33} is supplied externally or not. In the case the V_{DD33} pin is not supplied externally in the application, the electrical specs for this LDO are provided below.

4.8.1.2 V_{DD33} Regulator

The V_{DD33} internal LDO regulator powers the USB PHY, charger detection, and OTG functions of the USB subchip inside TUSB1210. Table 4-6 describes the regulator characteristics.

V_{DD33} regulator takes its power from V_{BAT}.

Since the USB2.0 standard requires data lines to be biased with pullups biased from a supply greater than 3 V, and since V_{DD33} regulator has an inherent voltage drop from its input, V_{BAT}, to its regulated output, TUSB1210 will not meet USB 2.0 Standard if operated from a battery whose voltage is lower than 3.3 V.

Table 4-6. V_{DD33} Internal LDO Regulator Characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{INVDD33}$	Input voltage	V_{BAT} USB		V_{VDD33} typ + 0.2	3.6	4.5	V
V_{VDD33}	Output voltage	ON mode,	VUSB3V3_VSEL = '000	2.4	2.5	2.6	V
			VUSB3V3_VSEL = '001	2.65	2.75	2.85	
			VUSB3V3_VSEL = '010	2.9	3.0	3.1	
			VUSB3V3_VSEL = '011 (default)	3.0	3.1	3.2	
			VUSB3V3_VSEL = '100	3.1	3.2	3.3	
			VUSB3V3_VSEL = '101	3.2	3.3	3.4	
			VUSB3V3_VSEL = '110	3.3	3.4	3.5	
			VUSB3V3_VSEL = '111	3.4	3.5	3.6	
I_{VDD33}	Rated output current	V_{BAT} USB	Active mode			15	mA
			Suspend/reset mode			1	

4.8.1.3 V_{DD18} Supply

The V_{DD18} supply is powered externally at the V_{DD18} pin. See Table 6-2 for external components.

4.8.1.4 V_{DD15} Regulator

The V_{DD15} internal LDO regulator powers the USB subchip inside TUSB1210. Table 4-7 describes the regulator characteristics.

Table 4-7. V_{DD15} Internal LDO Regulator Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN\ VDD15}$	Input voltage	On mode, $V_{IN\ VDD15} = V_{BAT}$	2.7	3.6	4.5	V
V_{VDD15}	Output voltage	$V_{INVDD15\ min} – V_{INVDD15\ max}$	1.45	1.56	1.65	V
I_{VDD15}	Rated output current	On mode			30	mA

4.8.2 Power Management

4.8.2.1 Power On Sequence

4.8.2.1.1 Timing Diagram

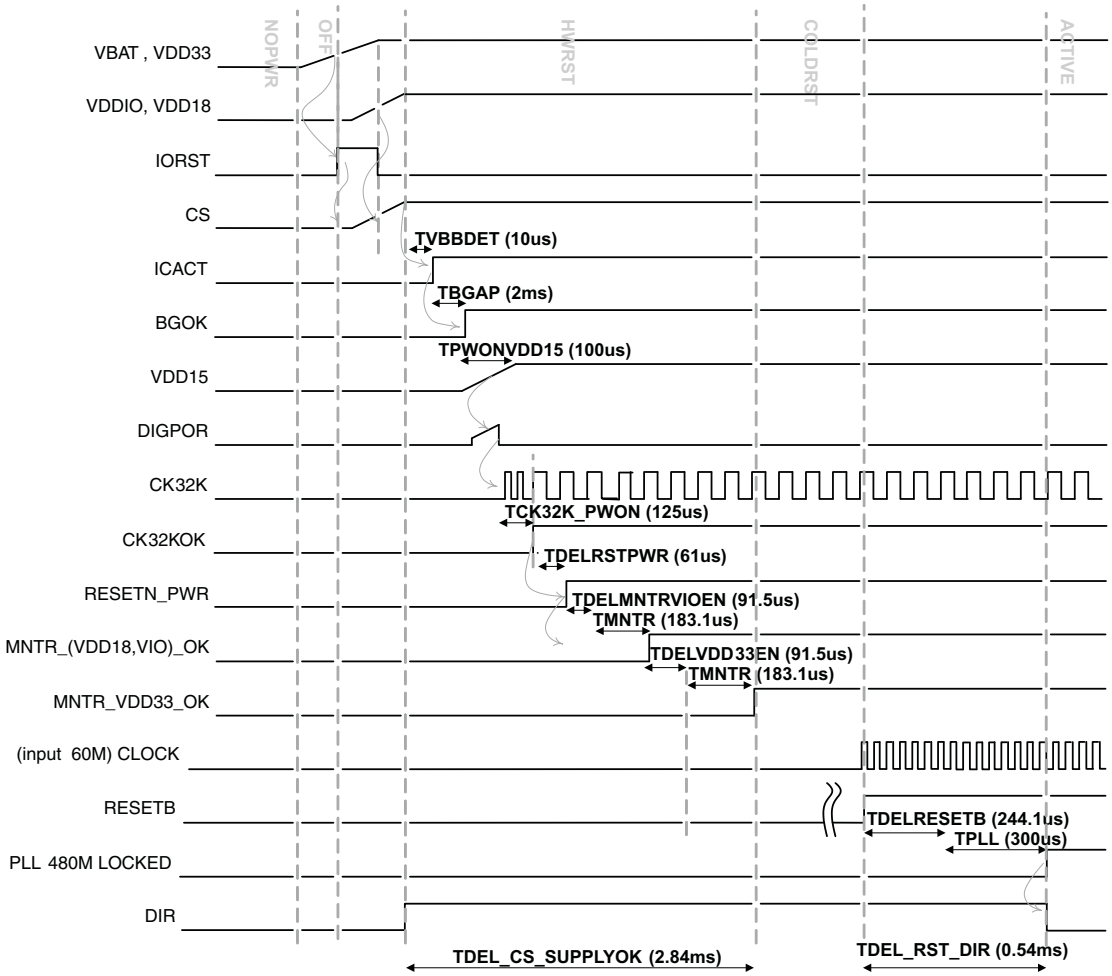


Figure 4-1. TUSB1210 Power-Up Timing (ULPI Clock Input Mode)

4.8.2.2 Timers and Debounce

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
$T_{DEL\_CS\_SUPPLYOK}$	Chip-select-to-supplies OK delay			2.84	4.10	ms
$T_{DEL\_RST\_DIR}$	RESETB to PHY PLL locked and DIR falling-edge delay			0.54	0.647	ms
T_{VBBDET}	V_{BAT} detection delay			10		us
T_{BGAP}	Bandgap power-on delay			2		ms
$T_{PWONVDD15}$	V_{DD15} power-on delay			100		us
$T_{PWONCK32K}$	32-KHz RC-OSC power-on delay			125		us
$T_{DELRSTPWR}$	Power control reset delay			61		us
$T_{DELMNTRVIOEN}$	Monitor enable delay			91.5		us
T_{MNTR}	Supply monitoring debounce			183.1		us
$T_{DELVDD33EN}$	V_{DD33} LDO enable delay			93.75		us
$T_{DELRESETB}$	RESETB internal delay			244.1		us
T_{PLL}	PLL lock time			300		us

4.9 Timing Parameter Definitions

The timing parameter symbols used in the timing requirement and switching characteristic tables are created in accordance with JEDEC Standard 100. To shorten the symbols, some pin names and other related terminologies have been abbreviated as shown in Table 4-8.

Table 4-8. Timing Parameter Definitions

LOWERCASE SUBSCRIPTS	
SYMBOL	**PARAMETER**
C	Cycle time (period)
D	Delay time
Dis	Disable time
En	Enable time
H	Hold time
Su	Setup time
START	Start bit
T	Transition time
V	Valid time
W	Pulse duration (width)
X	Unknown, changing, or don't care level
H	High
L	Low
V	Valid
IV	Invalid
AE	Active edge
FE	First edge
LE	Last edge
Z	High impedance

4.10 Interface Target Frequencies

Table 4-9 assumes testing over the recommended operating conditions.

Table 4-9. TUSB1210 Interface Target Frequencies

IO INTERFACE	INTERFACE DESIGNATION		TARGET FREQUENCY 1.5 V
USB	Universal serial bus	High speed	480 Mbits/s
		Full speed	12 Mbits/s
		Low speed	1.5 Mbits/s

4.11 Typical Characteristics

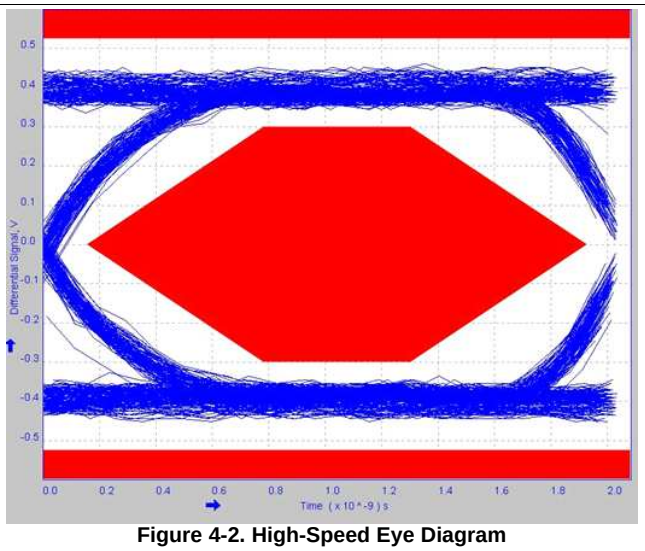


Figure 4-2. High-Speed Eye Diagram

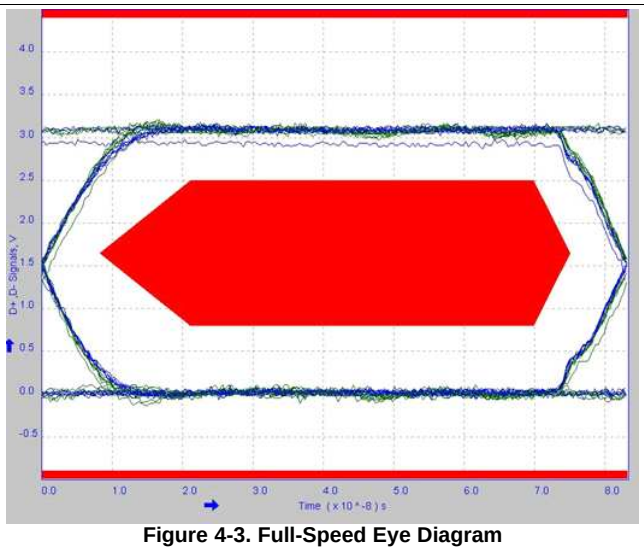


Figure 4-3. Full-Speed Eye Diagram

5 Detailed Description

5.1 Overview

The TUSB1210 is a USB2.0 transceiver chip, designed to interface with a USB controller via a ULPI interface. It supports all USB2.0 data rates High-Speed, Full-Speed, and Low-Speed. Compliant to both Host and Peripheral (OTG) modes. It additionally supports a UART mode and legacy ULPI serial modes. TUSB1210 Integrates a 3.3-V LDO, which makes it flexible to work with either battery operated systems or pure 3.3 V supplied systems. Also, it has an integrated PLL Supporting 2 Clock Frequencies 19.2 MHz/26 MHz. The ULPI clock pin (60 MHz) supports both input and output clock configurations. TUSB1210 has very low power consumption, optimized for portable devices, and complete USB OTG Physical Front-End that supports Host Negotiation Protocol (HNP) and Session Request Protocol (SRP).

TUSB1210 is optimized to be interfaced through a 12-pin SDR UTMI Low Pin Interface (ULPI), supporting both input clock and output clock modes, with 1.8 V interface supply voltage.

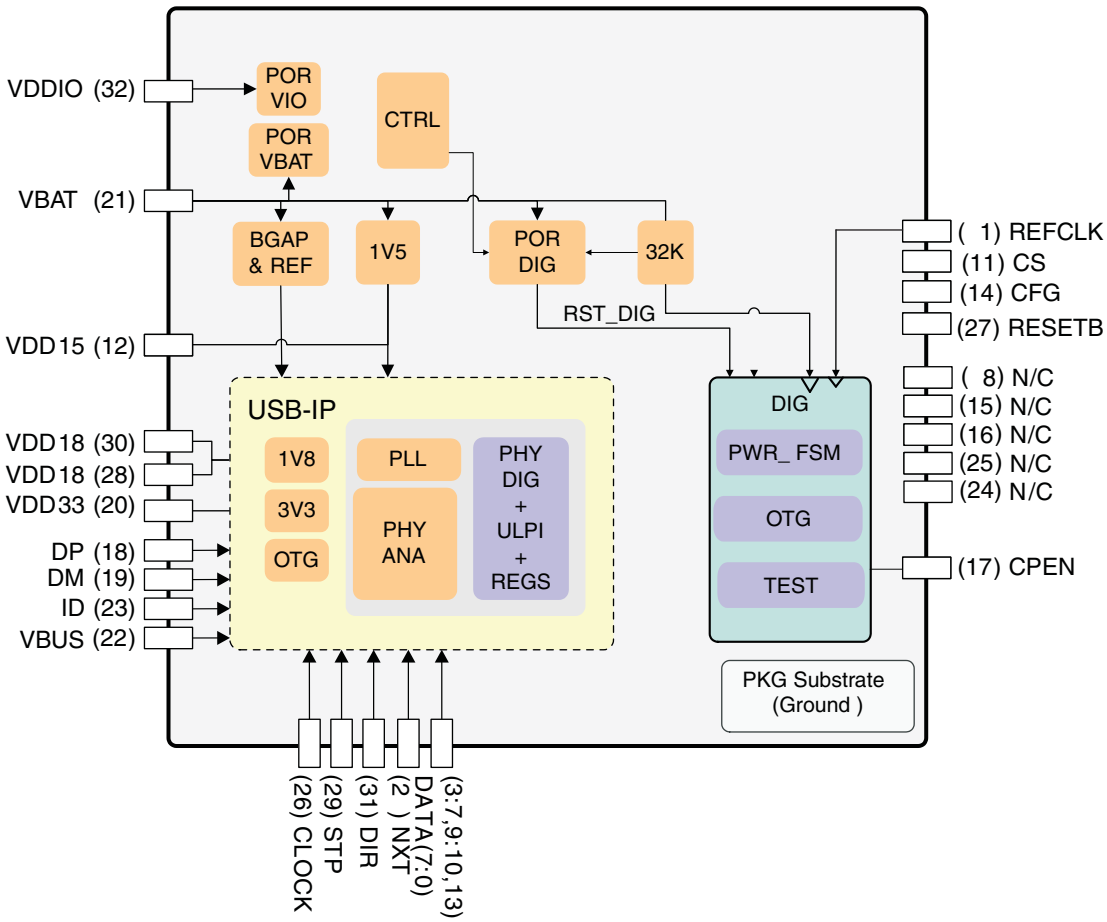
TUSB1210 integrates a 3.3 V LDO, which makes it flexible to work with either battery operated systems or pure 3.3 V supplied systems. Both the main supply and the 3.3 V power domain can be supplied through an external switched-mode converter for optimized power efficiency.

TUSB1210 includes a POR circuit to detect supply presence on V_{BAT} and V_{DDIO} pins. TUSB1210 can be disabled or configured in low power mode for energy saving.

TUSB1210 is protected against accidental shorts to 5 V or ground on its exposed interface (DP/DM/ID). It is also protected against up to 20 V surges on V_{BUS}.

TUSB1210 integrates a high-performance low-jitter 480 MHz PLL and supports two clock configurations. Depending on the required link configuration, TUSB1210 supports both ULPI input and output clock mode : input clock mode, in which case a square-wave 60 MHz clock is provided to TUSB1210 at the ULPI interface CLOCK pin; and output clock mode in which case TUSB1210 can accept a square-wave reference clock at REFCLK of either 19.2 MHz, 26 MHz. Frequency is indicated to TUSB1210 via the configuration pin CFG. This can be useful if a reference clock is already available in the system.

5.2 Functional Block Diagram



5.3 Processor Subsystem

5.3.1 USB Transceiver

The TUSB1210 device includes a universal serial bus (USB) on-the-go (OTG) transceiver that supports USB 480 Mb/s high-speed (HS), 12 Mb/s full-speed (FS), and USB 1.5 Mb/s low-speed (LS) through a 12-pin UTMI+ low pin interface (ULPI).

NOTE

LS device mode is not allowed by a USB2.0 HS capable PHY, therefore it is not supported by TUSB1210. This is clearly stated in USB2.0 standard Chapter 7, page 119, second paragraph: "*A high-speed capable upstream facing transceiver must not support low-speed signaling mode.*." There is also some related commentary in Chapter 7.1.2.3.

5.3.1.1 TUSB1210 Modes vs ULPI Pin Status

Table 5-1, Table 5-2, and Table 5-3 show the status of each of the 12 ULPI pins including input/output direction and whether output pins are driven to '0' or to '1', or pulled up/pulled down via internal pullup/pulldown resistors.

Note that pullup/pulldown resistors are automatically replaced by driven '1'/'0' levels respectively once internal IORST is released, with the exception of the pullup on STP which is maintained in all modes.

Pin assignment changes in ULPI 3-pin serial mode, ULPI 6-pin serial mode, and UART mode. Unused pins are tied low in these modes as shown below.

Table 5-1. TUSB1210 Modes vs ULPI Pin Status:ULPI Synchronous Mode Power-Up

		ULPI SYNCHRONOUS MODE POWER-UP							
		UNTIL IORST RELEASE		PLL OFF		PLL ON + STP HIGH		PLL ON + STP LOW	
PIN NO.	PIN NAME	DIR	PU/PD	DIR	PU/PD	DIR	PU/PD	DIR	PU/PD
26	CLOCK	Hiz	PD	I	PD	IO	-	IO	-
31	DIR	Hiz	PU	O, (‘1’)	-	O, (‘0’)	-	O	-
2	NXT	Hiz	PD	O, (‘0’)	-	O, (‘0’)	-	O	-
29	STP	Hiz	PU	I	PU	I	PU	I	PU
3	DATA0	Hiz	PD	O, (‘0’)	-	I	PD	IO	-
4	DATA1	Hiz	PD	O, (‘0’)	-	I	PD	IO	-
5	DATA2	Hiz	PD	O, (‘0’)	-	I	PD	IO	-
6	DATA3	Hiz	PD	O, (‘0’)	-	I	PD	IO	-
7	DATA4	Hiz	PD	O, (‘0’)	-	I	PD	IO	-
9	DATA5	Hiz	PD	O, (‘0’)	-	I	PD	IO	-
10	DATA6	Hiz	PD	O, (‘0’)	-	I	PD	IO	-
13	DATA7	Hiz	PD	O, (‘0’)	-	I	PD	IO	-

Table 5-2. TUSB1210 Modes vs ULPI Pin Status: USB Suspend Mode

		SUSPEND MODE		LINK / EXTERNAL RECOMMENDED SETTING DURING SUSPEND MODE	
PIN NO.	PIN NAME	DIR	PU/PD	DIR	PU/PD
26	CLOCK	I	-	O	-
31	DIR	O, (‘1’)	-	I	-
2	NXT	O, (‘0’)	-	I	-
29	STP	I	PU(1)	O, (‘0’)	-
3	DATA0	O, (LINESTATE0)	-	I	-
4	DATA1	O, (LINESTATE1)	-	I	-
5	DATA2	O, (‘0’)	-	I	-
6	DATA3	O, (INT)	-	I	-
7	DATA4	O, (‘0’)	-	I	-
9	DATA5	O, (‘0’)	-	I	-
10	DATA6	O, (‘0’)	-	I	-
13	DATA7	O, (‘0’)	-	I	-

(1) Can be disabled by software before entering Suspend Mode to reduce current consumption

Table 5-3. TUSB1210 Modes vs ULPI Pin Status: ULPI 6-Pin Serial Mode and UART Mode

	ULPI 6-PIN SERIAL MODE			ULPI 3-PIN SERIAL MODE			UART MODE		
PIN NO.	PIN NAME	DIR	PU/PD	PIN NAME	DIR	PU/PD	PIN NAME	DIR	PU/PD
26	CLOCK (1)	IO	-	CLOCK (1)	IO	-	CLOCK (1)	IO	-
31	DIR	O	-	DIR	O	-	DIR	O	-
2	NXT	O	-	NXT	O	-	NXT	O	-
29	STP	I	PU	STP	I	PU	STP	I	PU
3	TX_ENABLE	I	-	TX_ENABLE	I	-	TXD	I	-
4	TX_DAT	I	-	DAT	IO	-	RXD	IO	-
5	TX_SE0	I	-	SE0	IO	-	tie low	O	-
6	INT	O	-	INT	O	-	INT	O	-

Table 5-3. TUSB1210 Modes vs ULPI Pin Status: ULPI 6-Pin Serial Mode and UART Mode (continued)

	ULPI 6-PIN SERIAL MODE			ULPI 3-PIN SERIAL MODE			UART MODE		
PIN NO.	PIN NAME	DIR	PU/PD	PIN NAME	DIR	PU/PD	PIN NAME	DIR	PU/PD
7	RX_DP	O	-	tie low	O	-	tie low	O	-
9	RX_DM	O	-	tie low	O	-	tie low	O	-
10	RX_RCV	O	-	tie low	O	-	tie low	O	-
13	tie low	O	-	tie low	O	-	tie low	O	-

5.3.1.2 ULPI Interface Timing

Table 5-4. ULPI Interface Timing

PARAMETER		INPUT CLOCK		OUTPUT CLOCK		UNIT
		MIN	MAX	MIN	MAX	
T_{SC},T_{SD}	Set-up time (control in, 8-bit data in)		3		6	ns
T_{SC},T_{HD}	Hold time (control in, 8-bit data in)	1.5		0		ns
T_{DC},T_{DD}	Output delay (control out, 8-bit data out)		6		9	ns

5.3.1.3 PHY Electrical Characteristics

The PHY is the physical signaling layer of the USB 2.0. It essentially contains all the drivers and receivers required for physical data and protocol signaling on the DP and DM lines.

The PHY interfaces to the USB controller through a standard 12-pin digital interface called UTMI+ low pin interface (ULPI).

The transmitters and receivers inside the PHY are classified into two main classes.

- The full-speed (FS) and low-speed (LS) transceivers. These are the legacy USB1.x transceivers.
- The HS (HS) transceivers

In order to bias the transistors and run the logic, the PHY also contains reference generation circuitry which consists of:

- A DPLL which does a frequency multiplication to achieve the 480-MHz low-jitter lock necessary for USB and also the clock required for the switched capacitor resistance block.
- A switched capacitor resistance block which is used to replicate an external resistor on chip.

Built-in pullup and pulldown resistors are used as part of the protocol signaling.

Apart from this, the PHY also contains circuitry which protects it from accidental 5-V short on the DP and DM lines.

5.3.1.3.1 LS/FS Single-Ended Receivers

In addition to the differential receiver, there is a single-ended receiver (SE–, SE+) for each of the two data lines D+/–. The main purpose of the single-ended receivers is to qualify the D+ and D– signals in the full-speed/low-speed modes of operation.

Table 5-5. LS/FS Single-Ended Receivers

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
	USB single-ended receivers					
SK_{WVP_VM}	Skew between VP and VM	Driver outputs unloaded	–2	0	2	ns
V_{SE_HYS}	Single-ended hysteresis		50			mV
V_{IH}	High (driven)		2			V
V_{IL}	Low				0.8	V
V_{TH}	Switching threshold		0.8		2	V

5.3.1.3.2 LS/FS Differential Receiver

A differential input receiver (Rx) retrieves the LS/FS differential data signaling. The differential voltage on the line is converted into digital data by a differential comparator on DP/DM. This data is then sent to a clock and data recovery circuit which recovers the clock from the data. An additional serial mode exists in which the differential data is directly output on the RXRCV pin.

Table 5-6. LS/FS Differential Receiver

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
V_{DI}	Differential input sensitivity	Ref. USB2.0	200			mV
V_{CM}	Differential Common mode range	Ref. USB2.0	0.8		2.5	V

5.3.1.3.3 LS/FS Transmitter

The USB transceiver (Tx) uses a differential output driver to drive the USB data signal D+/– onto the USB cable. The driver's outputs support 3-state operation to achieve bidirectional half-duplex transactions.

Table 5-7. LS Transmitter

PARAMETER			COMMENTS	MIN	TYP	MAX	UNIT
V_{OL}	Low		Ref. USB2.0	0		300	mV
V_{OH}	High (driven)		Ref. USB2.0	2.8		3.6	V
V_{CRS}	Output signal crossover voltage		Ref. USB2.0, covered by eye diagram	1.3		2	V
T_{FR}	Rise time		Ref. USB2.0, covered by eye diagram	75		300	ns
T_{FF}	Fall time			75		300	ns
T_{FRFM}	Differential rise and fall time matching			80		125	%
T_{FDRATE}	Low-speed data rate		Ref. USB2.0, covered by eye diagram	1.4775		1.5225	Mb/s
T_{DJ1}	Source jitter total (including frequency tolerance)	To next transition	Ref. USB2.0, covered by eye diagram	–25		25	ns
T_{DJ2}		For paired transitions		–10		10	
T_{FEOPT}	Source SE0 interval of EOP		Ref. USB2.0, covered by eye diagram	1.25		1.5	us
	Downstream eye diagram		Ref. USB2.0, covered by eye diagram				
V_{CM}	Differential common mode range		Ref. USB2.0	0.8		2.5	V

Table 5-8. FS Transmitter

PARAMETER			COMMENTS	MIN	TYP	MAX	UNIT
V_{OL}	Low		Ref. USB2.0	0		300	mV
V_{OH}	High (driven)		Ref. USB2.0	2.8		3.6	V
VCRS	Output signal crossover voltage		Ref. USB2.0, covered by eye diagram	1.3		2	V
t_{FR}	Rise time		Ref. USB2.0	4		20	ns
t_{FF}	Fall time		Ref. USB2.0	4		20	ns
t_{FRFM}	Differential rise and fall time matching		Ref. USB2.0, covered by eye diagram	90		111.11	%
Z_{DRV}	Driver output resistance		Ref. USB2.0	28		44	Ω
TFDRATE	Full-speed data rate		Ref. USB2.0, covered by eye diagram	11.97		12.03	Mb/s
T_{DJ1}	Source jitter total (including frequency tolerance)	To next transition	Ref. USB2.0, covered by eye diagram	–2		2	ns
T_{DJ2}		For paired transitions		–1		1	
TFEOPT	Source SE0 interval of EOP		Ref. USB2.0, covered by eye diagram	160		175	ns

Table 5-8. FS Transmitter (continued)

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
	Downstream eye diagram	Ref. USB2.0, covered by eye diagram				
	Upstream eye diagram					

5.3.1.3.4 HS Differential Receiver

The HS receiver consists of the following blocks:

A differential input comparator to receive the serial data

- A squelch detector to qualify the received data
- An oversampler-based clock data recovery scheme followed by a NRZI decoder, bit unstuffing, and serial-to-parallel converter to generate the ULPI DATAOUT

Table 5-9. HS Differential Receiver

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
VHSSQ	High-speed squelch detection threshold (differential signal amplitude)	Ref. USB2.0	100		150	mV
VHSDSC	High-speed disconnect detection threshold (differential signal amplitude)	Ref. USB2.0	525		625	mV
	High-speed differential input signaling levels	Ref. USB2.0, specified by eye pattern templates				mV
VHSCM	High-speed data signaling common mode voltage range (guidelines for receiver)	Ref. USB2.0	–50		500	mV
	Receiver jitter tolerance	Ref. USB2.0, specified by eye pattern templates			150	ps

5.3.1.3.5 HS Differential Transmitter

The HS transmitter is always operated via the ULPI parallel interface. The parallel data on the interface is serialized, bit stuffed, NRZI encoded, and transmitted as a dc output current on DP or DM depending on the data. Each line has an effective 22.5-Ω load to ground, which generates the voltage levels for signaling.

A disconnect detector is also part of the HS transmitter. A disconnect on the far end of the cable causes the impedance seen by the transmitter to double thereby doubling the differential amplitude seen on the DP/DM lines.

Table 5-10. HS Transmitter

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
V_{HSOI}	High-speed idle level	Ref. USB2.0	–10		10	mV
V_{HSOH}	High-speed data signaling high	Ref. USB2.0	360		440	mV
V_{HSOL}	High-speed data signaling low	Ref. USB2.0	–10		10	mV
VCHIRPJ	Chirp J level (differential voltage)	Ref. USB2.0	700		1100	mV
VCHIRPK	Chirp K level (differential voltage)	Ref. USB2.0	-900		-500	mV
THSR	Rise Time (10% - 90%)	Ref. USB2.0, covered by eye diagram	500			ps
THSR	Fall time (10% - 90%)	Ref. USB2.0, covered by eye diagram	500			ps
ZHSDRV	Driver output resistance (which also serves as high-speed termination)	Ref. USB2.0	40.5		49.5	Ω
THSDRAT	High-speed data range	Ref. USB2.0, covered by eye diagram	479.76		480.24	Mb/s
	Data source jitter	Ref. USB2.0, covered by eye diagram				
	Downstream eye diagram	Ref. USB2.0, covered by eye diagram				
	Upstream eye diagram	Ref. USB2.0, covered by eye diagram				

5.3.1.3.6 UART Transceiver

In this mode, the ULPI data bus is redefined as a 2-pin UART interface, which exchanges data through a direct access to the FS/LS analog transmitter and receiver.

Table 5-11. USB UART Interface Timing Parameters

PARAMETER		MIN	MAX	UNIT
$t_{PH\_DP\_CON}$	Phone D+ connect time	100		ms
$t_{PH\_DISC\_DET}$	Phone D+ disconnect time	150		ms
f_{UART_DFLT}	Default UART signaling rate (typical rate)		9600	bps

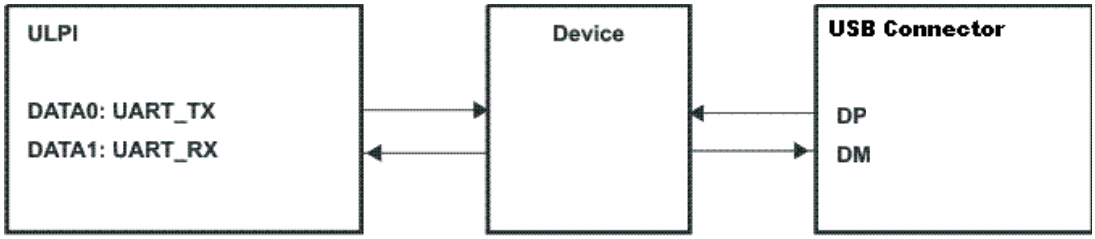


Figure 5-1. USB UART Data Flow

Table 5-12. CEA-2011/UART Transceiver

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
	UART Transmitter CEA-2011					
$t_{PH\_UART\_EDGE}$	Phone UART edge rates	DP_PULLDOWN asserted			1	Ms
V_{OH_SER}	Serial interface output high	ISOURCE = 4 mA	2.4	3.3	3.6	V
V_{OL_SER}	Serial interface output low	ISINK = –4 mA	0	0.1	0.4	V
	UART Receiver CEA-2011					
VI_{H_SER}	Serial interface input high	DP_PULLDOWN asserted	2			V
V_{IL_SER}	Serial interface input low	DP_PULLDOWN asserted			0.8	V
V_{TH}	Switching threshold		0.8		2	V

Table 5-13. Pullup/Pulldown Resistors

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
RPUI	Bus pullup resistor on upstream port (idle bus)	Bus idle	0.9	1.1	1.575	kΩ
RPUA	Bus pullup resistor on upstream port (receiving)	Bus driven/driver's outputs unloaded	1.425	2.2	3.09	
VIHZ	High (floating)	Pullups/pulldowns on both DP and DM lines	2.7		3.6	V
VPH_DP_UP	Phone D+ pullup voltage	Driver's outputs unloaded	3	3.3	3.6	V
	Pulldown resistors					
RPH_DP_DWN	Phone D+/– pulldown	Driver's outputs unloaded	14.25	18	24.8	kΩ
RPH_DM_DWN						
VIHZ	High (floating)	Pullups/pulldowns on both DP and DM lines	2.7		3.6	V
	D+/– Data line					
CINUB	Upstream facing port	[1.0]		22	75	pF
VOTG_DATA_LKG	On-the-go device leakage	[2]			0.342	V
ZINP	Input impedance exclusive of pullup/pulldown	Driver's outputs unloaded	300			kΩ

5.3.1.4 OTG Electrical Characteristics

The on-the-go (OTG) block integrates three main functions:

- The USB plug detection function on V_{BUS} and ID
- The ID resistor detection
- The V_{BUS} level detection

Table 5-14. OTG V_{BUS} Electrical

PARAMETER		COMMENTS		MIN	TYP	MAX	UNIT
V_{BUS} Comparators							
VA_SESS_VLD	A-device session valid			0.8	1.4	2.0	V
VA_VBUS_VLD	A-device V_{BUS} valid			4.4	4.5	4.625	V
VB_SESS_END	B-device session end			0.2	0.5	0.8	V
VB_SESS_VLD	B-device session valid			2.1	2.4	2.7	V
V_{BUS} Line							
RA_BUS_IN	A-device V_{BUS} input impedance to ground	SRP (V_{BUS} pulsing) capable A-device not driving V_{BUS}		40	70	100	kΩ
RB_SRP_DWN	B-device V_{BUS} SRP pulldown	5.25 V / 8 mA, Pullup voltage = 3 V		0.656	10		kΩ
RB_SRP_UP	B-device V_{BUS} SRP pullup	(5.25 V – 3 V) / 8 mA, Pullup voltage = 3 V		0.281	1	2	kΩ
$t_{RISE\_SRP\_UP\_MAX}$	B-device V_{BUS} SRP rise time maximum for OTG-A communication	0 to 2.1 V with < 13 µF load	RV_{BUS} = 0 Ω and R1KSERIES = '0'			31.4	ms
			RV_{BUS} = 1000 Ω ±10% and R1KSERIES = '1'			57.8	
			RV_{BUS} = 1200 Ω and R1KSERIES = '1'			64	
			RV_{BUS} = 18000 Ω and R1KSERIES = '1'			85.4	

Table 5-14. OTG V_{BUS} Electrical (continued)

PARAMETER		COMMENTS		MIN	TYP	MAX	UNIT
$t_{RISE\_SRP\_UP\_MIN}$	B-device V_{BUS} SRP rise time minimum for standard host connection	0.8 to 2.0 V with > 97 µF load	RV_{BUS} = 0 Ω and R1KSERIES = '0'	46.2			ms
			RV_{BUS} = 10000 Ω and R1KSERIES = '1'	96			
			RV_{BUS} = 1200 Ω and R1KSERIES = '1'	100			
			RV_{BUS} = 1800 Ω and R1KSERIES = '1'	100			

Table 5-15. OTG ID Electrical

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
ID Comparators — ID External Resistors Specifications						
R_{ID_GND}	ID ground comparator	ID_GND interrupt	12	20	28	kΩ
R_{ID_FLOAT}	ID Float comparator	ID_FLOAT interrupt	200		500	kΩ
	ID Line					
$R_{PH\_ID\_UP}$	Phone ID pullup to VPH_ID_UP	ID unloaded (V_{RUSB})	70	90	286	kΩ
$VP_{H\_ID\_UP}$	Phone ID pullup voltage	Connected to V_{RUSB}	2.5		3.2	V
	ID line maximum voltage				5.25	V

5.4 Memory

5.4.1 Register Map

5.4.1.1 TUSB1210 Product

Table 5-16. USB Register Summary

REGISTER NAME	TYPE	REGISTER WIDTH (BITS)	PHYSICAL ADDRESS
VENDOR_ID_LO	R	8	0x00
VENDOR_ID_HI	R	8	0x01
PRODUCT_ID_LO	R	8	0x02
PRODUCT_ID_HI	R	8	0x03
FUNC_CTRL	RW	8	0x04
FUNC_CTRL_SET	RW	8	0x05
FUNC_CTRL_CLR	RW	8	0x06
IFC_CTRL	RW	8	0x07
IFC_CTRL_SET	RW	8	0x08
IFC_CTRL_CLR	RW	8	0x09
OTG_CTRL	RW	8	0x0A
OTG_CTRL_SET	RW	8	0x0B
OTG_CTRL_CLR	RW	8	0x0C
USB_INT_EN_RISE	RW	8	0x0D
USB_INT_EN_RISE_SET	RW	8	0x0E
USB_INT_EN_RISE_CLR	RW	8	0x0F
USB_INT_EN_FALL	RW	8	0x10
USB_INT_EN_FALL_SET	RW	8	0x11
USB_INT_EN_FALL_CLR	RW	8	0x12
USB_INT_STS	R	8	0x13
USB_INT_LATCH	R	8	0x14
DEBUG	R	8	0x15

Table 5-16. USB Register Summary (continued)

REGISTER NAME	TYPE	REGISTER WIDTH (BITS)	PHYSICAL ADDRESS
SCRATCH_REG	RW	8	0x16
SCRATCH_REG_SET	RW	8	0x17
SCRATCH_REG_CLR	RW	8	0x18
Reserved	R	8	0x19 0x2E
ACCESS_EXT_REG_SET	RW	8	0x2F
Reserved	R	8	0x30 0x3C
VENDOR_SPECIFIC1	RW	8	0x3D
VENDOR_SPECIFIC1_SET	RW	8	0x3E
VENDOR_SPECIFIC1_CLR	RW	8	0x3F
VENDOR_SPECIFIC2	RW	8	0x80
VENDOR_SPECIFIC2_SET	RW	8	0x81
VENDOR_SPECIFIC2_CLR	RW	8	0x82
VENDOR_SPECIFIC1_STS	R	8	0x83
VENDOR_SPECIFIC1_LATCH	R	8	0x84
VENDOR_SPECIFIC3	RW	8	0x85
VENDOR_SPECIFIC3_SET	RW	8	0x86
VENDOR_SPECIFIC3_CLR	RW	8	0x87

5.4.1.1.1 VENDOR_ID_LO

ADDRESS OFFSET	0x00		
PHYSICAL ADDRESS	0x00	**INSTANCE**	USB_SCUSB
DESCRIPTION	Lower byte of vendor ID supplied by USB-IF (TI Vendor ID = 0x0451)		
TYPE	R		
WRITE LATENCY			

7	6	5	4	3	2	1	0
VENDOR_ID							

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:00	VENDOR_ID		R	0x51

5.4.1.1.2 VENDOR_ID_HI

ADDRESS OFFSET	0x01		
PHYSICAL ADDRESS	0x01	**INSTANCE**	USB_SCUSB
DESCRIPTION	Upper byte of vendor ID supplied by USB-IF (TI Vendor ID = 0x0451)		
TYPE	R		
WRITE LATENCY			

7	6	5	4	3	2	1	0
VENDOR_ID							

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:00	VEN DOR_ID		R	0x04

5.4.1.1.3 PRODUCT_ID_LO

ADDRESS OFFSET	0x02		
PHYSICAL ADDRESS	0x02	**INSTANCE**	USB_SCUSB
DESCRIPTION	Lower byte of Product ID supplied by Vendor (TUSB1210 Product ID is 0x1507).		
TYPE	R		
WRITE LATENCY			

7	6	5	4	3	2	1	0
PRODUCT_ID							

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:00	PRODUCT_ID		R	0x07

5.4.1.1.4 PRODUCT_ID_HI

ADDRESS OFFSET	0x03		
PHYSICAL ADDRESS	0x03	**INSTANCE**	USB_SCUSB
DESCRIPTION	Upper byte of Product ID supplied by Vendor (TUSB1210 Product ID is 0x1507).		
TYPE	R		
WRITE LATENCY			

7	6	5	4	3	2	1	0
PRODUCT_ID							

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:00	PRODUCT_ID		R	0x15

5.4.1.1.5 FUNC_CTRL

ADDRESS OFFSET	0x04		
PHYSICAL ADDRESS	0x04	**INSTANCE**	USB_SCUSB
DESCRIPTION	Controls UTMI function settings of the PHY.		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	SUSPENDM	RESET	OPMODE		TERMSELECT	XCVRSELECT	

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		R	0
6	SUSPENDM	Active low PHY suspend. Put PHY into Low Power Mode. In Low Power Mode the PHY power down all blocks except the full speed receiver, OTG comparators, and the ULPI interface pins. The PHY automatically set this bit to '1' when Low Power Mode is exited.	RW	1
5	RESET	Active high transceiver reset. Does not reset the ULPI interface or ULPI register set. Once set, the PHY asserts the DIR signal and reset the UTMI core. When the reset is completed, the PHY de-asserts DIR and clears this bit. After de-asserting DIR, the PHY re-assert DIR and send an RX command update. Note: This bit is auto-cleared, this explain why it can't be read at '1'.	RW	0

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
4:03	OPMODE	Select the required bit encoding style during transmit 0x0: Normal operation 0x1: Non-driving 0x2: Disable bit-stuff and NRZI encoding 0x3: Reserved (No SYNC and EOP generation feature not supported)	RW	0x0
2	TERMSELECT	Controls the internal 1.5Kohms pull-up resistor and 45ohms HS terminations. Control over bus resistors changes depending on XcvrSelect, OpMode, DpPulldown and DmPulldown.	RW	0
1:00	XCVRSELECT	Select the required transceiver speed. 0x0: Enable HS transceiver 0x1: Enable FS transceiver 0x2: Enable LS transceiver 0x3: Enable FS transceiver for LS packets (FS preamble is automatically pre-pended)	RW	0x1

5.4.1.1.6 FUNC_CTRL_SET

ADDRESS OFFSET	0x05		
PHYSICAL ADDRESS	0x05	**INSTANCE**	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the func_ctrl register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	SUSPENDM	RESET	OPMODE		TERMSELECT	XCVRSELECT	

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		R	0
6	SUSPENDM		RW	1
5	RESET		RW	0
4:03	OPMODE		RW	0x0
2	TERMSELECT		RW	0
1:00	XCVRSELECT		RW	0x1

5.4.1.1.7 FUNC_CTRL_CLR

ADDRESS OFFSET	0x06		
PHYSICAL ADDRESS	0x06	**INSTANCE**	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the func_ctrl register with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	SUSPENDM	RESET	OPMODE		TERMSELECT	XCVRSELECT	

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		R	0
6	SUSPENDM		RW	1
5	RESET		RW	0
4:03	OPMODE		RW	0x0
2	TERMSELECT		RW	0
1:00	XCVRSELECT		RW	0x1

5.4.1.1.8 IFC_CTRL

ADDRESS OFFSET	0x07		
PHYSICAL ADDRESS	0x07	**INSTANCE**	USB_SCUSB
DESCRIPTION	Enables alternative interfaces and PHY features.		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
INTERFACE_PROTECT_DISABLE	INDICATORPASSTHRU	INDICATORCOMPLEMENT	AUTORESUME	CLOCKSUSPENDM	CARKITMODE	FSLSSERIALMODE_3PIN	FSLSSERIALMODE_6PIN

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	INTERFACE_PROTECT_DISABLE	Controls circuitry built into the PHY for protecting the ULPI interface when the link tri-states stp and data. 0b: Enables the interface protect circuit 1b: Disables the interface protect circuit	RW	0
6	INDICATORPASSTHRU	Controls whether the complement output is qualified with the internal vbusvalid comparator before being used in the VBUS State in the RXCMD. 0b: Complement output signal is qualified with the internal VBUSVALID comparator. 1b: Complement output signal is not qualified with the internal VBUSVALID comparator.	RW	0
5	INDICATORCOMPLEMENT	Tells the PHY to invert EXTERNALVBUSINDICATOR input signal, generating the complement output. 0b: PHY will not invert signal EXTERNALVBUSINDICATOR (default) 1b: PHY will invert signal EXTERNALVBUSINDICATOR	RW	0
4	AUTORESUME	Enables the PHY to automatically transmit resume signaling. Refer to USB specification 7.1.7.7 and 7.9 for more details. 0 = AutoResume disabled 1 = AutoResume enabled (default)	RW	1
3	CLOCKSUSPENDM	Active low clock suspend. Valid only in Serial Modes. Powers down the internal clock circuitry only. Valid only when SuspendM = 1b. The PHY must ignore ClockSuspend when SuspendM = 0b. By default, the clock will not be powered in Serial and Carkit Modes. 0b : Clock will not be powered in Serial and UART Modes.	RW	0

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
		1b : Clock will be powered in Serial and UART Modes.		
2	CARKITMODE	Changes the ULPI interface to UART interface. The PHY automatically clear this field when UART mode is exited. 0b: UART disabled. 1b: Enable serial UART mode.	RW	0
1	FSLSSERIALMODE_3PIN	Changes the ULPI interface to 3-pin Serial. The PHY must automatically clear this field when serial mode is exited. 0b: FS/LS packets are sent using parallel interface 1b: FS/LS packets are sent using 4-pin serial interface	RW	0
0	FSLSSERIALMODE_6PIN	Changes the ULPI interface to 6-pin Serial. The PHY must automatically clear this field when serial mode is exited. 0b: FS/LS packets are sent using parallel interface 1b: FS/LS packets are sent using 6-pin serial interface	RW	0

5.4.1.1.9 IFC_CTRL_SET

ADDRESS OFFSET	0x08		
PHYSICAL ADDRESS	0x08	**INSTANCE**	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the ifc_ctrl register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
INTERFACE_PROTECT_DISABLE	INDICATORPASSTHRU	INDICATORCOMPLEMENT	AUTORESUME	CLOCKSUSPENDM	CARKITMODE	FSLSSERIALMODE_3PIN	FSLSSERIALMODE_6PIN

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	INTERFACE_PROTECT_DISABLE		RW	0
6	INDICATORPASSTHRU		RW	0
5	INDICATORCOMPLEMENT		RW	0
4	AUTORESUME		RW	1
3	CLOCKSUSPENDM		RW	0
2	CARKITMODE		RW	0
1	FSLSSERIALMODE_3PIN		RW	0
0	FSLSSERIALMODE_6PIN		R	0

5.4.1.1.10 IFC_CTRL_CLR

ADDRESS OFFSET	0x09		
PHYSICAL ADDRESS	0x09	**INSTANCE**	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the ifc_ctrl register with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
INTERFACE_PROTECT_DISABLE	IN DICATORPASSTHRU	INDICATORCOMPLEMENT	AUTORESUME	CLOCKSUSPENDM	CARKITMODE	FSLSSERIALMODE_3PIN	FSLSSERIALMODE_6PIN

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	INTERFACE_PROTECT_DISABLE		RW	0
6	INDICATORPASSTHRU		RW	0
5	INDICATORCOMPLEMENT		RW	0
4	AUTORESUME		RW	1
3	CLOCKSUSPENDM		RW	0
2	CARKITMODE		RW	0
1	FSLSSERIALMODE_3PIN		RW	0
0	FSLSSERIALMODE_6PIN		R	0

5.4.1.1.11 OTG_CTRL

ADDRESS OFFSET	0x0A		
PHYSICAL ADDRESS	0x0A	**INSTANCE**	USB_SCUSB
DESCRIPTION	Controls UTMI+ OTG functions of the PHY.		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
USEEXTERNALVBUSINDICATOR	DRVVBUSEXTERNAL	DRVVBUS	CHRGVBUS	DISCHRGVBUS	DMPULLDOWN	DPPULLDOWN	IDPULLUP

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	USEEXTERNALVBUSINDICATOR	Tells the PHY to use an external VBUS over-current indicator. 0b: Use the internal OTG comparator (VA_VBUS_VLD) or internal VBUS valid indicator (default) 1b: Use external VBUS valid indicator signal.	RW	0
6	DRVVBUSEXTERNAL	Selects between the internal and the external 5 V VBUS supply. 0b: Pin17 (CPEN) is disabled (output GND level). TUSB1210 does not support internal VBUS supply. 1b: Pin17 (CPEN) is set to '1' (output VDD33 voltage level) if DRVVBUS bit is '1', else Pin17 (CPEN) is disabled (output GND level) if DRVVBUS bit is '0'	RW	0
5	DRVVBUS	VBUS output control bit 0b : do not drive VBUS 1b : drive 5V on VBUS Note: Both DRVVBUS and DRVVBUSEXTERNAL bits must be set to 1 in order to to set Pin17 (CPEN). CPEN pin can be used to enable an external VBUS supply	RW	0
4	CHRGVBUS	Charge VBUS through a resistor. Used for VBUS pulsing SRP. The Link must first check that VBUS has been discharged (see DischrgVbus register bit), and that both D+ and D- data lines have been low (SE0) for 2ms. 0b : do not charge VBUS 1b : charge VBUS	RW	0
3	DISCHRGVBUS	Discharge VBUS through a resistor. If the Link sets this bit to 1, it waits for an RX CMD indicating SessEnd has transitioned from 0 to 1, and then resets this bit to 0 to stop the discharge. 0b : do not discharge VBUS 1b : discharge VBUS	RW	0
2	DMPULLDOWN	Enables the 15k Ohm pull-down resistor on D-. 0b : Pull-down resistor not connected to D-. 1b : Pull-down resistor connected to D-.	RW	1
1	DPPULLDOWN	Enables the 15k Ohm pull-down resistor on D+. 0b : Pull-down resistor not connected to D+. 1b : Pull-down resistor connected to D+.	RW	1
0	IDPULLUP	Connects a pull-up to the ID line and enables sampling of the signal level. 0b : Disable sampling of ID line. 1b : Enable sampling of ID line.	RW	0

5.4.1.1.12 OTG_CTRL_SET

ADDRESS OFFSET	0x0B		
PHYSICAL ADDRESS	0x0B	**INSTANCE**	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the otg_ctrl register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
USEEXTERNALVBUSINDICATOR	DRVVBUSEXTERNAL	DRVVBUS	CHRGVBUS	DISCHRGVBUS	DMPULLDOWN	DPPULLDOWN	IDPULLUP

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	USEEXTERNALVBUSINDICATOR		RW	0
6	DRVVBUSEXTERNAL		RW	0
5	DRVVBUS		RW	0
4	CHRGVBUS		RW	0
3	DISCHRGVBUS		RW	0
2	DMPULLDOWN		RW	1
1	DPPULLDOWN		RW	1
0	IDPULLUP		RW	0

5.4.1.1.13 OTG_CTRL_CLR

ADDRESS OFFSET	0x0C		
PHYSICAL ADDRESS	0x0C	**INSTANCE**	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the otg_ctrl register with read/Clear-only property (write '1' to clear a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
USEEXTERNALVBUSINDICATOR	DRVVBUSEXTERNAL	DRVVBUS	CHRGVBUS	DISCHRGVBUS	DMPULLDOWN	DPPULLDOWN	IDPULLUP

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	USEEXTERNALVBUSINDICATOR		RW	0
6	DRVVBUSEXTERNAL		RW	0
5	DRVVBUS		RW	0
4	CHRGVBUS		RW	0
3	DISCHRGVBUS		RW	0
2	DMPULLDOWN		RW	1
1	DPPULLDOWN		RW	1
0	IDPULLUP		RW	0

5.4.1.1.14 USB_INT_EN_RISE

ADDRESS OFFSET	0x0D		
PHYSICAL ADDRESS	0x0D	**INSTANCE**	USB_SCUSB
DESCRIPTION	If set, the bits in this register cause an interrupt event notification to be generated when the corresponding PHY signal changes from low to high. By default, all transitions are enabled.		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	IDGND_RISE	SESSEND_RISE	SESSVALID_RISE	VBUSVALID_RISE	HOSTDISCONNECT_RISE

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	IDGND_RISE	Generate an interrupt event notification when IdGnd changes from low to high.	RW	1
		Event is automatically masked if IdPullup bit is clear to 0 and for 50ms after IdPullup is set to 1.		
3	SESSEND_RISE	Generate an interrupt event notification when SessEnd changes from low to high.	RW	1

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
2	SESSVALID_RISE	Generate an interrupt event notification when SessValid changes from low to high. SessValid is the same as UTMI+ AValid.	RW	1
1	VBUSVALID_RISE	Generate an interrupt event notification when VbusValid changes from low to high.	RW	1
0	HOSTDISCONNECT_RISE	Generate an interrupt event notification when Hostdisconnect changes from low to high. Applicable only in host mode (DpPulldown and DmPulldown both set to 1b).	RW	1

5.4.1.1.15 USB_INT_EN_RISE_SET

ADDRESS OFFSET	0x0E		
PHYSICAL ADDRESS	0x0E	**INSTANCE**	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the usb_int_en_rise register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	IDGND_RISE	SESSEND_RISE	SESSVALID_RISE	VBUSVALID_RISE	HOSTDISCONNECT_RISE

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	IDGND_RISE		RW	1
3	SESSEND_RISE		RW	1
2	SESSVALID_RISE		RW	1
1	VBUSVALID_RISE		RW	1
0	HOSTDISCONNECT_RISE		RW	1

5.4.1.1.16 USB_INT_EN_RISE_CLR

ADDRESS OFFSET	0x0F		
PHYSICAL ADDRESS	0x0F	**INSTANCE**	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the usb_int_en_rise register with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	IDGND_RISE	SESSEN D_RISE	SESSVALID_RISE	VBUSVALID_RISE	HOSTDISCONNECT_RISE

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	IDGND_RISE		RW	1
3	SESSEND_RISE		RW	1
2	SESSVALID_RISE		RW	1
1	VBUSVALID_RISE		RW	1
0	HOSTDISCONNECT_RISE		RW	1

5.4.1.1.17 USB_INT_EN_FALL

ADDRESS OFFSET	0x10		
PHYSICAL ADDRESS	0x10	**INSTANCE**	USB_SCUSB
DESCRIPTION	If set, the bits in this register cause an interrupt event notification to be generated when the corresponding PHY signal changes from low to high. By default, all transitions are enabled.		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	IDGND_FALL	SESSEND_FALL	SESSVALID_FALL	VBUSVALID_FALL	HOSTDISCONNECT_FALL

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	IDGND_FALL	Generate an interrupt event notification when IdGnd changes from high to low. Event is automatically masked if IdPullup bit is clear to 0 and for 50ms after IdPullup is set to 1.	RW	1
3	SESSEND_FALL	Generate an interrupt event notification when SessEnd changes from high to low.	RW	1
2	SESSVALID_FALL	Generate an interrupt event notification when SessValid changes from high to low. SessValid is the same as UTMI+ AValid.	RW	1

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
1	VBUSVALID_FALL	Generate an interrupt event notification when VbusValid changes from high to low.	RW	1
0	HOSTDISCONNECT_FALL	Generate an interrupt event notification when Hostdisconnect changes from high to low. Applicable only in host mode (DpPulldown and DmPulldown both set to 1b).	RW	1

5.4.1.1.18 USB_INT_EN_FALL_SET

ADDRESS OFFSET	0x11		
PHYSICAL ADDRESS	0x11	**INSTANCE**	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the usb_int_en_fall register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action)		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	IDGND_FALL	SESSEND_FALL	SESSVALID_FALL	VBUSVALID_FALL	HOSTDISCONNECT_FALL

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	IDGND_FALL		RW	1
3	SESSEND_FALL		RW	1
2	SESSVALID_FALL		RW	1
1	VBUSVALID_FALL		RW	1
0	HOSTDISCONNECT_FALL		RW	1

5.4.1.1.19 USB_INT_EN_FALL_CLR

ADDRESS OFFSET	0x12		
PHYSICAL ADDRESS	0x12	**INSTANCE**	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the usb_int_en_fall register with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	IDGND_FALL	SESSEND_FALL	SESSVALID_FALL	VBUSVALID_FALL	HOSTDISCONNECT_FALL

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	IDGND_FALL		RW	1
3	SESSEN D_FALL		RW	1
2	SESSVALID_FALL		RW	1
1	VBUSVALID_FALL		RW	1
0	HOSTDISCONNECT_FALL		RW	1

5.4.1.1.20 USB_INT_STS

ADDRESS OFFSET	0x13		
PHYSICAL ADDRESS	0x13	**INSTANCE**	USB_SCUSB
DESCRIPTION	Indicates the current value of the interrupt source signal.		
TYPE	R		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	IDGND	SESSEND	SESSVALID	VBUSVALID	HOSTDISCONNECT

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	IDGND	Current value of UTMI+ IdGnd output. This bit is not updated if IdPullup bit is reset to 0 and for 50 ms after IdPullup is set to 1.	R	0
3	SESSEND	Current value of UTMI+ SessEnd output.	R	0
2	SESSVALID	Current value of UTMI+ SessValid output. SessValid is the same as UTMI+ AValid.	R	0
1	VBUSVALID	Current value of UTMI+ VbusValid output.	R	0
0	HOSTDISCONNECT	Current value of UTMI+ Hostdisconnect output. Applicable only in host mode. Automatically reset to 0 when Low Power Mode is entered. NOTE: Reset value is '0' when host is connected. Reset value is '1' when host is disconnected.	R	0

5.4.1.1.21 USB_INT_LATCH

ADDRESS OFFSET	0x14		
PHYSICAL ADDRESS	0x14	**INSTANCE**	USB_SCUSB
DESCRIPTION	These bits are set by the PHY when an unmasked change occurs on the corresponding internal signal. The PHY will automatically clear all bits when the Link reads this register, or when Low Power Mode is entered. The PHY also clears this register when Serial Mode or Carkit Mode is entered regardless of the value of ClockSuspendM. The PHY follows the rules defined in Table 26 of the ULPI spec for setting any latch register bit. It is important to note that if register read data is returned to the Link in the same cycle that a USB Interrupt Latch bit is to be set, the interrupt condition is given immediately in the register read data and the Latch bit is not set. Note that it is optional for the Link to read the USB Interrupt Latch register in Synchronous Mode because the RX CMD byte already indicates the interrupt source directly		
TYPE	R		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	IDGND_LATCH	SESSEND_LATCH	SESSVALID_LATCH	VBUSVALID_LATCH	HOSTDISCONNECT_LATCH

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	IDGND_LATCH	Set to 1 by the PHY when an unmasked event occurs on IdGnd. Cleared when this register is read.	R	0
3	SESSEND_LATCH	Set to 1 by the PHY when an unmasked event occurs on SessEnd. Cleared when this register is read.	R	0

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
2	SESSVALID_LATCH	Set to 1 by the PHY when an unmasked event occurs on SessValid. Cleared when this register is read. SessValid is the same as UTMI+ AValid.	R	0
1	VBUSVALID_LATCH	Set to 1 by the PHY when an unmasked event occurs on VbusValid. Cleared when this register is read.	R	0
0	HOSTDISCONNECT_LATCH	Set to 1 by the PHY when an unmasked event occurs on Hostdisconnect. Cleared when this register is read. Applicable only in host mode. NOTE: As this IT is enabled by default, the reset value depends on the host status Reset value is '0' when host is connected. Reset value is '1' when host is disconnected.	R	0

5.4.1.1.22 DEBUG

ADDRESS OFFSET	0x15		
PHYSICAL ADDRESS	0x15	**INSTANCE**	USB_SCUSB
DESCRIPTION	Indicates the current value of various signals useful for debugging.		
TYPE	R		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LINESTATE	

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		R	0
6	Reserved		R	0
5	Reserved		R	0
4	Reserved		R	0
3	Reserved		R	0
2	Reserved		R	0
1:00	LINESTATE	These signals reflect the current state of the single ended receivers. They directly reflect the current state of the DP (LineState[0]) and DM (LineState[1]) signals. Read 0x0: SE0 (LS/FS), Squelch (HS/Chirp) Read 0x1: LS: 'K' State, FS: 'J' State, HS: !Squelch, Chirp: !Squelch & HS_Differential_Receiver_Output Read 0x2: LS: 'J' State, FS: 'K' State, HS: Invalid, Chirp: !Squelch & !HS_Differential_Receiver_Output Read 0x3: SE1 (LS/FS), Invalid (HS/Chirp)	R	0x0

5.4.1.1.23 SCRATCH_REG

ADDRESS OFFSET	0x16		
PHYSICAL ADDRESS	0x16	**INSTANCE**	USB_SCUSB

DESCRIPTION	Empty register byte for testing purposes. Software can read, write, set, and clear this register and the PHY functionality will not be affected.
TYPE	RW
WRITE LATENCY	

7	6	5	4	3	2	1	0
SCRATCH							

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:00	SCRATCH	Scratch data.	RW	0x00

5.4.1.1.24 SCRATCH_REG_SET

ADDRESS OFFSET	0x17		
PHYSICAL ADDRESS	0x17	**INSTANCE**	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the scratch_reg register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
SCRATCH							

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:00	SCRATCH		RW	0x00

5.4.1.1.25 SCRATCH_REG_CLR

ADDRESS OFFSET	0x18		
PHYSICAL ADDRESS	0x18	**INSTANCE**	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the scratch_reg with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
SCRATCH							

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7:00	SCRATCH		RW	0x00

5.4.1.1.26 VENDOR_SPECIFIC1

ADDRESS OFFSET	0x3D		
PHYSICAL ADDRESS	0x3D	**INSTANCE**	USB_SCUSB
DESCRIPTION	Power Control register .		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
SPARE	MNTR_VUSBIN_OK_EN	ID_FLOAT_EN	ID_RES_EN	BVALID_FALL	BVALID_RISE	SPARE	ABNORMALSTRESS_EN

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	SPARE	Reserved. The link must never write a 1b to this bit.	RW	0
6	MNTR_VUSBIN_OK_EN	When set to 1, it enables RX CMDs for high to low or low to high transitions on MNTR_VUSBIN_OK. This bit is provided for debugging purposes.	RW	0
5	ID_FLOAT_EN	When set to 1, it enables RX CMDs for high to low or low to high transitions on ID_FLOAT. This bit is provided for debugging purposes.	RW	0
4	ID_RES_EN	When set to 1, it enables RX CMDs for high to low or low to high transitions on ID_RESA, ID_RESB and ID_RESC. This bit is provided for debugging purposes.	RW	0
3	BVALID_FALL	Enables RX CMDs for high to low transitions on BVALID. When BVALID changes from high to low, the USB TRANS will send an RX CMD to the link with the alt_int bit set to 1b. This bit is optional and is not necessary for OTG devices. This bit is provided for debugging purposes. Disabled by default.	RW	0
2	BVALID_RISE	Enables RX CMDs for low to high transitions on BVALID. When BVALID changes from low to high, the USB Trans will send an RX CMD to the link with the alt_int bit set to 1b. This bit is optional and is not necessary for OTG devices. This bit is provided for debugging purposes. Disabled by default.	RW	0
1	SPARE	Reserved. The link must never write a 1b to this bit.	RW	0
0	ABNORMALSTRESS_EN	When set to 1, it enables RX CMDs for low to high and high to low transitions on ABNORMALSTRESS. This bit is provided for debugging purposes.	RW	0

5.4.1.1.27 VENDOR_SPECIFIC1_SET

ADDRESS OFFSET	0x3E		
PHYSICAL ADDRESS	0x3E	**INSTANCE**	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the func_ctrl register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATEN CY			

7	6	5	4	3	2	1	0
SPARE	MNTR_VUSBIN_OK_EN	ID_FLOAT_EN	ID_RES_EN	BVALID_FALL	BVALID_RISE	SPARE	ABNORMALSTRESS_EN

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	SPARE		RW	0
6	MNTR_VUSBIN_OK_EN		RW	0
5	ID_FLOAT_EN		RW	0
4	ID_RES_EN		RW	0
3	BVALID_FALL		RW	0
2	BVALID_RISE		RW	0
1	SPARE		RW	0
0	ABNORMALSTRESS_EN		RW	0

5.4.1.1.28 VENDOR_SPECIFIC1_CLR

ADDRESS OFFSET	0x3F		
PHYSICAL ADDRESS	0x3F	**INSTANCE**	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the func_ctrl register with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
SPARE	MNTR_VUSBIN_OK_EN	ID_FLOAT_EN	ID_RES_EN	BVALID_FALL	BVALID_RISE	SPARE	ABNORMALSTRESS_EN

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	SPARE		RW	0
6	MNTR_VUSBIN_OK_EN		RW	0
5	ID_FLOAT_EN		RW	0
4	ID_RES_EN		RW	0
3	BVALID_FALL		RW	0
2	BVALID_RISE		RW	0
1	SPARE		RW	0
0	ABNORMALSTRESS_EN		RW	0

5.4.1.1.29 VENDOR_SPECIFIC2

ADDRESS OFFSET	0x80		
PHYSICAL ADDRESS	0x80	**INSTANCE**	USB_SCUSB
DESCRIPTION	Eye diagram programmability and DP/DM swap control .		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
SPARE	DATAPOLARITY	ZHSDRV		IHSTX			

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	SPARE		RW	0
6	DATAPOLARITY	Control data polarity on dp/dm	RW	1
5:04	ZHSDRV	High speed output impedance configuration for eye diagram tuning : 00 45.455 Ω 01 43.779 Ω 10 42.793 Ω 11 42.411 Ω	RW	0x0
3:00	IHSTX	High speed output drive strength configuration for eye diagram tuning : 0000 17.928 mA 0001 18.117 mA 0010 18.306 mA 0011 18.495 mA 0100 18.683 mA 0101 18.872 mA 0110 19.061 mA 0111 19.249 mA 1000 19.438 mA 1001 19.627 mA 1010 19.816 mA 1011 20.004 mA 1100 20.193 mA 1101 20.382 mA 1110 20.570 mA 1111 20.759 mA IHSTX[0] is also the AC BOOST enable IHSTX[0] = 0 à AC BOOST is disabled IHSTX[0] = 1 à AC BOOST is enabled	RW	0x1

5.4.1.1.30 VENDOR_SPECIFIC2_SET

ADDRESS OFFSET	0x81		
PHYSICAL ADDRESS	0x81	**INSTANCE**	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the VENDOR_SPECIFIC1 register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
SPARE	DATAPOLARITY	ZHSDRV		IHSTX			

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	SPARE		RW	0
6	DATAPOLARITY		RW	1
5:04	ZHSDRV		RW	0x0
3:00	IHSTX		RW	0x1

5.4.1.1.31 VENDOR_SPECIFIC2_CLR

ADDRESS OFFSET	0x82		
PHYSICAL ADDRESS	0x82	**INSTANCE**	USB_SCUSB
DESCRIPTION	This register doesn't physically exist. It is the same as the VENDOR_SPECIFIC1 register with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action).		
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
SPARE	DATAPOLARITY	ZHSDRV		IHSTX			

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	SPARE		RW	0
6	DATAPOLARITY		RW	1
5:04	ZHSDRV		RW	0x0
3:00	IHSTX		RW	0x1

5.4.1.1.32 VENDOR_SPECIFIC1_STS

ADDRESS OFFSET	0x83		
PHYSICAL ADDRESS	0x83	**INSTANCE**	USB_SCUSB
DESCRIPTION	Indicates the current value of the interrupt source signal.		
TYPE	R		
WRITE LATEN CY			

7	6	5	4	3	2	1	0
Reserved	MNTR_VUSBIN_OK_STS	ABNORMALSTRESS_STS	ID_FLOAT_STS	ID_RESC_STS	ID_RESB_STS	ID_RESA_STS	BVALID_STS

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		R	0
6	MNTR_VUSBIN_OK_STS	Current value of MNTR_VUSBIN_OK output	R	0
5	ABNORMALSTRESS_STS	Current value of ABNORMALSTRESS output	R	0
4	ID_FLOAT_STS	Current value of ID_FLOAT output	R	0
3	ID_RESC_STS	Current value of ID_RESC output	R	0
2	ID_RESB_STS	Current value of ID_RESB output	R	0
1	ID_RESA_STS	Current value of ID_RESA output	R	0
0	BVALID_STS	Current value of VB_SESS_VLD output	R	0

5.4.1.1.33 VENDOR_SPECIFIC1_LATCH

ADDRESS OFFSET	0x84		
PHYSICAL ADDRESS	0x84	**INSTANCE**	USB_SCUSB
DESCRIPTION	These bits are set by the PHY when an unmasked change occurs on the corresponding internal signal. The PHY will automatically clear all bits when the Link reads this register, or when Low Power Mode is entered. The PHY also clears this register when Serial mode is entered regardless of the value of ClockSuspendM. The PHY follows the rules defined in Table 26 of the ULPI spec for setting any latch register bit.		
TYPE	R		
WRITE LATENCY			

7	6	5	4	3	2	1	0
Reserved	MNTR_VUSBIN_OK_LATCH	ABNORMALSTRESS_LATCH	ID_FLOAT_LATCH	ID_RESC_LATCH	ID_RESB_LATCH	ID_RESA_LATCH	BVALID_LATCH

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		R	0
6	MNTR_VUSBIN_OK_LATCH	Set to 1 when an unmasked event occurs on MNTR_VUSBIN_OK_LATCH. Clear on read register.	R	0
5	ABNORMALSTRESS_LATCH	Set to 1 when an unmasked event occurs on ABNORMALSTRESS. Clear on read register.	R	0
4	ID_FLOAT_LATCH	Set to 1 when an unmasked event occurs on ID_FLOAT. Clear on read register.	R	0
3	ID_RESC_LATCH	Set to 1 when an unmasked event occurs on ID_RESC. Clear on read register.	R	0
2	ID_RESB_LATCH	Set to 1 when an unmasked event occurs on ID_RESB. Clear on read register.	R	0
1	ID_RESA_LATCH	Set to 1 when an unmasked event occurs on ID_RESA. Clear on read register.	R	0
0	BVALID_LATCH	Set to 1 when an unmasked event occurs on VB_SESS_VLD. Clear on read register.	R	0

5.4.1.1.34 VENDOR_SPECIFIC3

ADDRESS OFFSET	0x85		
PHYSICAL ADDRESS	0x85	**INSTANCE**	USB_SCUSB
DESCRIPTION			
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
RESERVED	SOF_EN	CPEN_OD	CPEN_ODOS	IDGND_DRV	VUSB3V3_VSEL		

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		RW	0
6	SOF_EN	0: HS USB SOF detector disabled. 1: Enable HS USB SOF detection when PHY is set in device mode. SOF are output on CPEN pin. HS USB SOF (start-of-frame) output clock is available on CPEN pin when this bit is set. HS USB SOF packet rate is 8 kHz. This bit is provided for debugging purpose only. It must never been write to '1' in functional mode	RW	0
5	CPEN_OD	This bit has no effect when CPEN_ODOS = '0', else : 0: CPEN pad is in OS (Open Source) mode. In this case CPEN pin has an internal NMOS driver, and will be active LOW. Externally there should be a pullup resistor on CPEN (min 1kohm) to a supply voltage (max 3.6V). 1: CPEN pad is in OD (Open Drain) mode In this case CPEN pin has an internal PMOS driver, and will be active HIGH. Externally there should be a pull-down resistor on CPEN (min 1 kΩ to GND.	RW	0
4	CPEN_ODOS	Mode selection bit for CPEN pin. 0 : CPEN pad is in CMOS mode 1: CPEN pad is in OD (Open Drain) or OS (Open Source) mode (controlled by CPEN_OD bit)	RW	0
3	IDGND_DRV	Drives ID pin to ground	RW	0x0

2:00	VUSB3V3_VSEL	000 VRUSB3P1V = 2.5 V 001 VRUSB3P1V = 2.75 V 010 VRUSB3P1V = 3.0 V 011 VRUSB3P1V = 3.10 V (default) 100 VRUSB3P1V = 3.20 V 101 VRUSB3P1V = 3.30 V 110 VRUSB3P1V = 3.40 V 111 VRUSB3P1V = 3.50 V	RW	0x3

5.4.1.1.35 VENDOR_SPECIFIC3_SET

ADDRESS OFFSET	0x86		
PHYSICAL ADDRESS	0x86	**INSTANCE**	USB_SCUSB
DESCRIPTION			
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
RESERVED	SOF_EN	CPEN_OD	CPEN_ODOS	IDGND_DRV	VUSB3V3_VSEL		

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		RW	0
6	SOF_EN		RW	0
5	CPEN_OD		RW	0
4	CPEN _ODOS		RW	0
3	IDGND_DRV		RW	0x0
2:00	VUSB3V3_VSEL		RW	0x3

5.4.1.1.36 VENDOR_SPECIFIC3_CLR

ADDRESS OFFSET	0x87		
PHYSICAL ADDRESS	0x87	**INSTANCE**	USB_SCUSB
DESCRIPTION			
TYPE	RW		
WRITE LATENCY			

7	6	5	4	3	2	1	0
RESERVED	SOF_EN	CPEN_OD	CPEN_ODOS	IDGND_DRV	VUSB3V3_VSEL		

BITS	FIELD NAME	DESCRIPTION	TYPE	RESET
7	Reserved		RW	0
6	SOF_EN		RW	0
5	CPEN_OD		RW	0
4	CPEN_ODOS		RW	0
3	IDGND_DRV		RW	0x0
2:00	VUSB3V3_VSEL		RW	0x3

6 Application, Implementation, and Layout

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

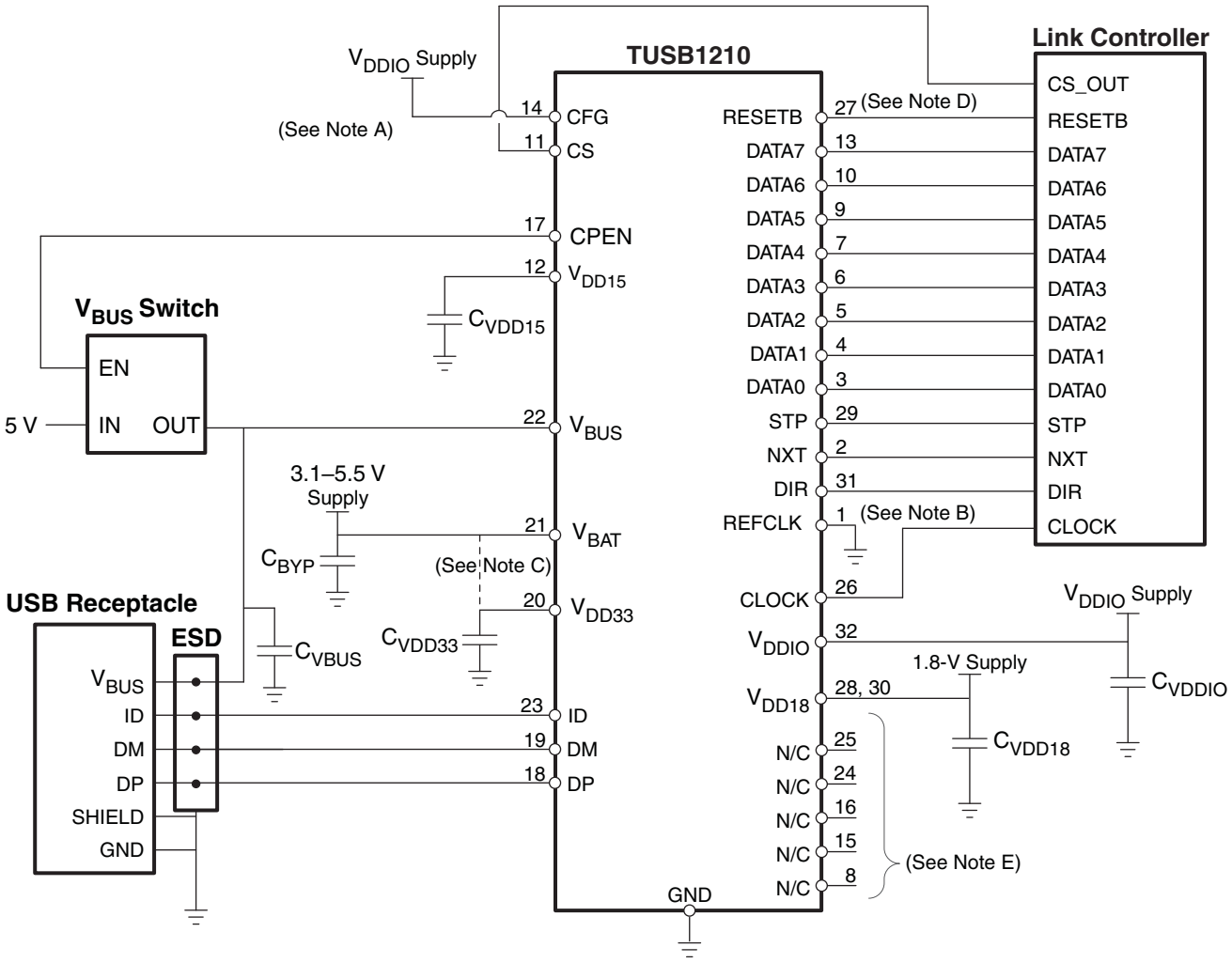
6.1 Application Information

The TUSB1210 is a USB2.0 transceiver chip, designed to interface with a USB controller via a ULPI interface. It supports all USB2.0 data rates High-Speed, Full-Speed, and Low-Speed and it's compliant to both Host and Peripheral (OTG) modes. Use the following design procedure to select the wished operation mode. This section presents a simplified discussion of the design process.

6.2 Typical Application

6.2.1 Host or OTG, ULPI Input Clock Mode Application

Figure 6-1 shows a suggested application diagram for TUSB1210 in the case of ULPI input-clock mode (60 MHz ULPI clock is provided by link processor), in Host or OTG application. Note this is just one example, it is of course possible to operate as HOST or OTG while also in ULPI output-clock mode.



A. Pin 11 (CS) : can be tied high to VI_O if CS_OUT pin unavailable; Pin 14 (CFG) : tie-high is Don't Care since ULPI clock is used in input mode
B. Pin 1 (REFCLK) : must be tied low
C. Ext 3 V supply supported
D. Pin 27 (RESETB) can be tied to V_{DDIO} if unused.
E. Pins labeled N/C (no-connect) are truly no-connect, and can be tied or left floating.

Figure 6-1. Host or OTG, ULPI Input Clock Mode Application Diagram

6.2.1.1 Design Requirements

Table 6-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{BAT}	3.3 V
V_{DDIO}	1.8 V
V_{BUS}	5.0 V
USB Support	HS, FS, LS
USB On the Go (OTG)	Yes
Clock Sources	60 MHz Clock

6.2.1.2 Detailed Design Procedure

Connect the TUSB1210 device as is shown in Figure 6-1.

6.2.1.2.1 External Components

Table 6-2. TUSB1210 External Components

FUNCTION	COMPONENT	REFERENCE	VALUE	NOTE	LINK
V_{DDIO}	Capacitor	CVDDIO	100 nF	Suggested value, application dependent	Figure 6-1
V_{DD33}	Capacitor	CVDD33	2.2 µF	Range: [0.45 µF : 6.5 µF] , ESR = [0 : 600 mΩ] for f> 10 kHz	Figure 6-1
V_{DD15}	Capacitor	CVDD15	2.2 µF	Range: [0.45 µF : 6.5 µF] , ESR = [0 : 600 mΩ] for f> 10 kHz	Figure 6-1
V_{DD18}	Capacitor	Ext 1.8V supply	100 nF	Suggested value, application dependent	Figure 6-1
		CVDD18			
V_{BAT}	Capacitor	CBYP	100 nF(1)	Range: [0.45 µF : 6.5 µF] , ESR = [0 : 600 mΩ] for f> 10 kHz	Figure 6-1
V_{BUS}	Capacitor	CVBUS	See table 1.2	Place close to USB connector	Figure 6-1

(1) Recommended value but 2.2 uF may be sufficient in some applications

Table 6-3. TUSB1210 V_{BUS} Capacitors

FUNCTION	COMPONENT	REFERENCE	VALUE	NOTE	LINK
VBUS - HOST	Capacitor	CVBUS	>120 µF		Figure 6-1
VBUS – DEVICE	Capacitor	CVBUS	4.7 µF	Range: 1.0 µF to 10.0 µF	Figure 6-1
VBUS - OTG	Capacitor	CVBUS	4.7 µF	Range: 1.0 µF to 6.5 µF	Figure 6-1

6.2.1.2.2 TUSB121x USB2.0 Product Family Board Layout Recommendations

Table 6-4. TUSB121x USB2.0 Product Family Board Layout Recommendations

Item	USB General Considerations
1.00	USB design requires symmetrical termination and symmetrical component placement along the DP and DM paths
1.01	Place the USB host controller and major components on the unrouted board first.
1.02	Place the USB host controller, as close as possible to the transceiver device, that is, ULPI interface traces as short as possible
1.03	Route high-speed clock and high-speed USB. Route differential pairs first. Since these signals are critical and long length traces are to be avoided, it is therefore recommended to route DP/DM before routing less critical signals on the board. A similar recommendation is true for CLK, and ULPI signals which should be routed with equalized trace length.
1.04	Maintain maximum possible distance between high-speed clocks/periodic signals to high speed USB differential pairs and any connector leaving the PCB (such as I/O connectors, control, and signal headers or power connectors).
1.05	Place the USB receptacle at the board edge
1.06	Maximum TI-recommended external capacitance on DP (or DM) lines is 4 pF • This capacitance is the sum of all external discrete components, that is, the total capacitance on DP (or DM) lines including trace capacitance can be larger than 4 pF. • All discrete components should be placed as close as possible to the USB receptacle.
1.07	Place the low-capacitance ESD protections as close as possible to the USB receptacle, with no other external devices in between.
1.08	Common mode chokes degrade signal quality, thus they should only be used if EMI performance enhancement is absolutely necessary.
1.09	Place the common mode choke (if required to improve EMI performance) as close as possible to the USB receptacle (but after the ESD device(s)).
	USB Interface (DP, DM)
2.00	Separate signal traces into similar categories and route similar signal traces together, that is, DP/DM and ULPI.
2.01	Route the USB receptacle ground pin to the analog ground plane of the device with multiple via connections.
2.02	Route the DP/DM trace pair together.
2.03	For HS-capable devices, route the DP/DM signals from the device to the USB receptacle with an optimum trace length of 5 cm. Maximum trace length 1-way delay of 0.5 ns (7.5 cm for 67 ps/cm in FR-3).
2.04	Match the DP/DM trace lengths. Maximum mismatch allowable is 150 mils (~0.4 cm).
2.05	Route the DP/DM signals with 90-Ω differential impedance, and 22.5~30-Ω common-mode impedance (objective is to have Zodd ~= Z0 = Zdiff/2 = 45 Ω).
2.06	Use an impedance calculator to determine the trace width and spacing required for the specific board stack up being used.
2.07	Keep the maximum possible distance between DP and DM signals from the other platform clocks, power sources and digital / analog signals
2.08	Do not route DP/DM signals over or under crystals, oscillators, clock synthesizers, magnetic devices, or ICs that use clocks.
2.09	Avoid changing the routing layer for DP/DM traces. If unavoidable, use multiple vias.
2.10	Minimize bends and corners on DP/DM traces.
2.11	When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities.
2.12	Avoid creating stubs on the DP/DM traces as stubs cause signal reflections and affect global signal quality.
2.13	If stubs are unavoidable, they must be less than 200 mils (~0.5 cm).

Table 6-4. TUSB121x USB2.0 Product Family Board Layout Recommendations (continued)

Item	USB General Considerations
2.14	Route DP/DM signals over continuous VCC or GND planes, without interruption, avoiding crossing anti-etch (plane splits), which increase both inductance and radiation levels by introducing a greater loop area.
2.15	Route DP/DM signals with at least 25 mils (~0.65 mm) away from any plane splits.
2.16	Follow the 20*h thumb rule by keeping traces at least 20*(height above the plane) away from the edge of the plane (VCC or GND, depending on the plane the trace is over).
2.17	Changing signal layers is preferable to crossing plane splits if a choice must be made.
2.18	If crossing a plane split is completely unavoidable, proper placement of stitching capacitors can minimize the adverse effects on EMI and signal quality performance caused by crossing the split.
2.19	Avoid anti-etch on the ground plane.
	ULPI Interface (ULPIDATA<7:0>, ULPICLK, ULPINXT, ULPIDIR, ULPISTP)
3.00	Route ULPI 12-pin bus as a 50-Ω single-ended adapted bus.
3.01	Route ULPI 12-pin bus with minimum trace lengths and a strict maximum of 90 mm, to ensure timing. (Timing budget 600 ps maximum 1-way delay assuming 66 ps/cm.)
3.02	Route ULPI 21-pin bus equalizing paths lengths as much as possible to have equal delays.
3.03	Route ULPI 12-pin bus as clock signals and set a minimum spacing of 3 times the trace width (S < 3W).
3.04	If the 3W minimum spacing is not respected, the minimum spacing for clock signals based on EMI testing experience is 50 mils (1.27 mm).
3.05	Route ULPI 12-pin bus with a dedicated ground plane.
3.06	Place and route the ULPI monitoring buffers as close as possible from the device ULPI bus (on test boards).
	USB Clock (USBCLKIN, CLK_IN1, CLK_IN0)
4.00	Route the USB clock with the minimum possible trace length.
4.01	Keep the maximum possible distance between the USB clock and the other platform clocks, power sources, and digital and analog signals.
4.02	Route the USBCLKIN, CLK_IN1 and CLK_IN0 inputs as 50-Ω single-ended signals.
	USB Power Supply (VBUS, REG3V3, REG1V5, VBAT)
5.00	VBUS must be a power plane from the device VBUS ball to the USB receptacle, or if a power plan is not possible, VBUS must be as large as possible.
5.01	Power signals must be wide to accommodate current level.

6.2.1.2.3 Unused Pins Connection

- **VBUS:** Input. Recommended to tie to GND if unused. However leaving V_{BUS} floating is also acceptable since internally there is an 80 kOhm resistance to ground.
- **REFCLK:** Input. If REFCLK is unused, and 60 MHz clock is provided by MODEM (60 MHz should be connected to CLOCK pin in this case) then tie REFCLK to GND.
- **CFG:** Tie to GND if REFCLK is 19.2MHz, or tie to V_{DDIO} if REFCLK is 26 MHz. Tie to either GND or V_{DDIO} (doesn't matter which) if REFCLK not used (i.e., ULPI input clock configuration).

6.2.1.3 Application Curve

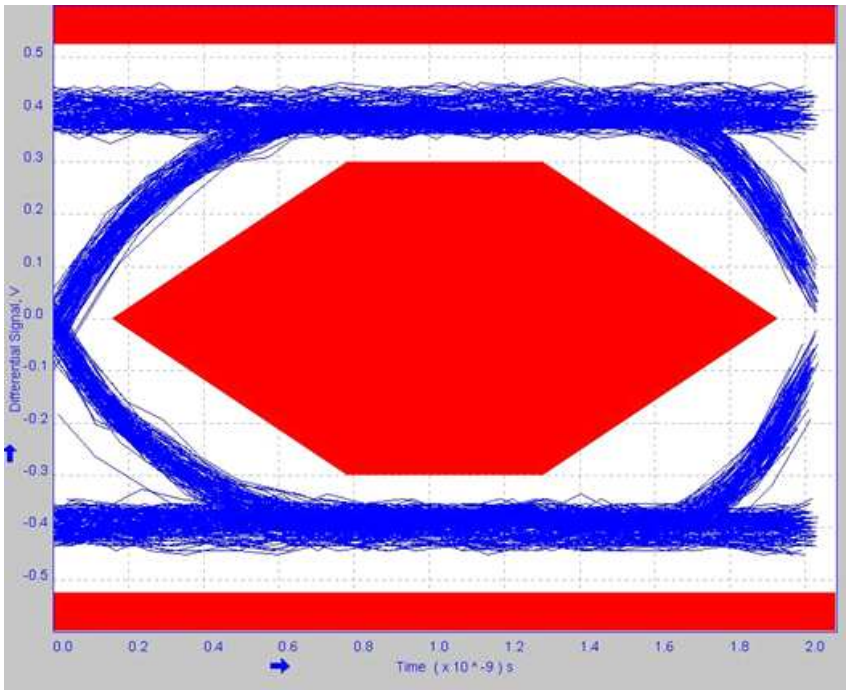
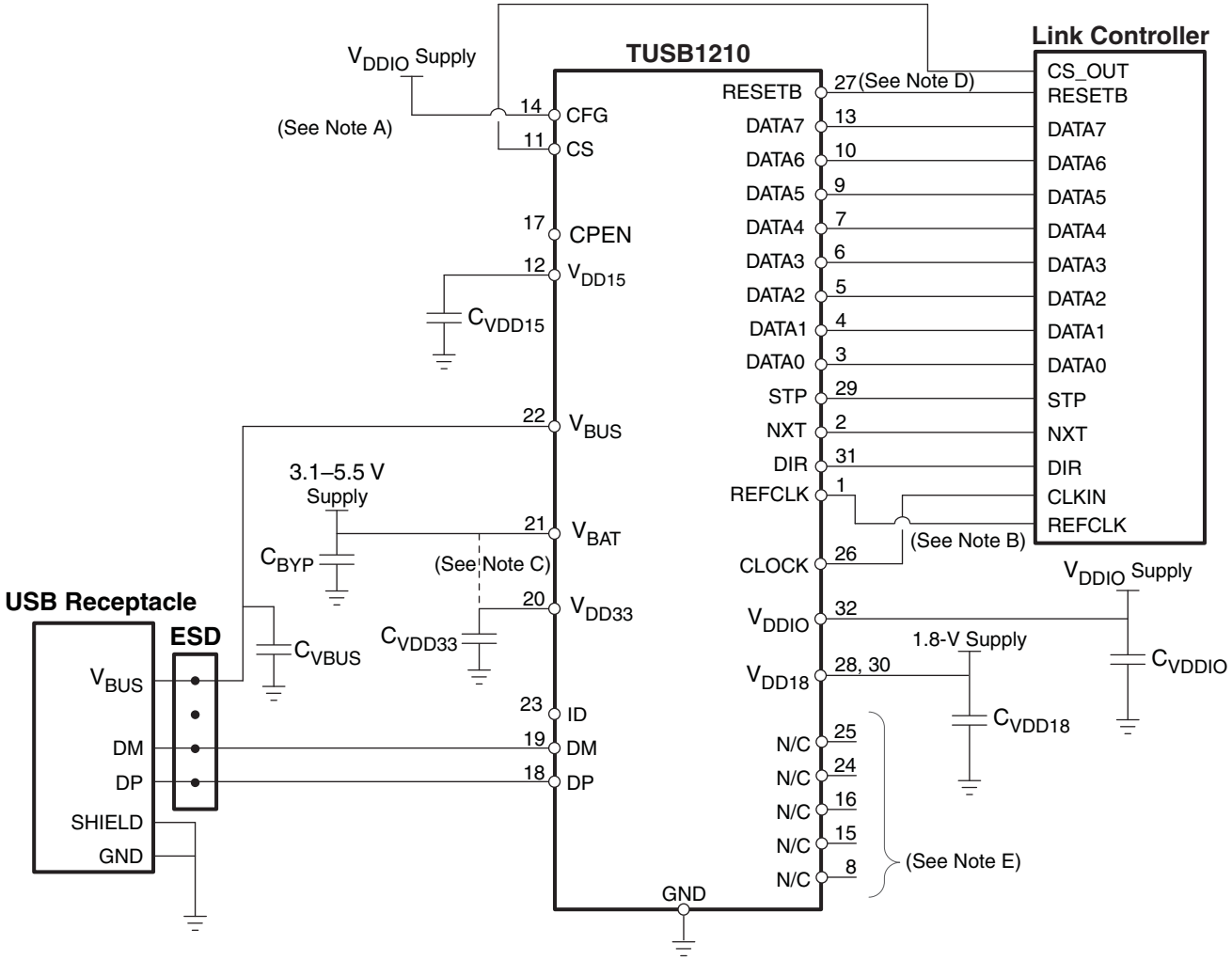


Figure 6-2. High-Speed Eye Diagram

6.2.2 Device, ULPI Output Clock Mode Application

Figure 6-3 shows a suggested application diagram for TUSB1210 in the case of ULPI output clock mode (60 MHz ULPI clock is provided by TUSB1210, while link processor or another external circuit provides REFCLK), in Device mode application. Note this is just one example, it is of course possible to operate as Device while also in ULPI input-clock mode. Refer also to Figure 6-1.



A. Pin 11 (CS) : can be tied high to V_{IO} if CS_OUT pin unavailable; Pin 14 (CFG) : Tied to V_{DDIO} for 26MHz REFCLK mode here, tie to GND for 19.2MHz mode.
B. Pin 1 (REFCLK) : connect to external 3.3V square-wave reference clock
C. Ext 3 V supply supported
D. Pin 27 (RESETB) can be tied to V_{DDIO} if unused.
E. Pins labeled N/C (no-connect) are truly no-connect, and can be tied or left floating.

Figure 6-3. Device, ULPI Output Clock Mode Application Diagram

6.2.2.1 Design Requirements

Table 6-5. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{BAT}	3.3 V
V_{DDIO}	1.8 V
V_{BUS}	5.0 V
USB Support	HS, FS, LS
Clock Sources	26 MHz or 19.2 MHz Oscillator

6.2.2.2 Detailed Design Procedure

Connect the TUSB1210 device as is shown in Figure 6-3.

Refer to Table 6-4 and *Section 6.2.1.2.1*.

6.2.2.2.1 Unused Pins Connection

- **ID:** Input. Leave floating if unused or TUSB1210 is Device mode only. Tie to GND through RID < 1 kOhm if Host mode.
- **REFCLK:** Input. If REFCLK is unused, and 60 MHz clock is provided by MODEM (60 MHz should be connected to CLOCK pin in this case) then tie REFCLK to GND.
- **CFG:** Tie to GND if REFCLK is 19.2MHz, or tie to V_{DDIO} if REFCLK is 26 MHz. Tie to either GND or V_{DDIO} (doesn't matter which) if REFCLK not used (i.e., ULPI input clock configuration).

6.2.2.3 Application Curve

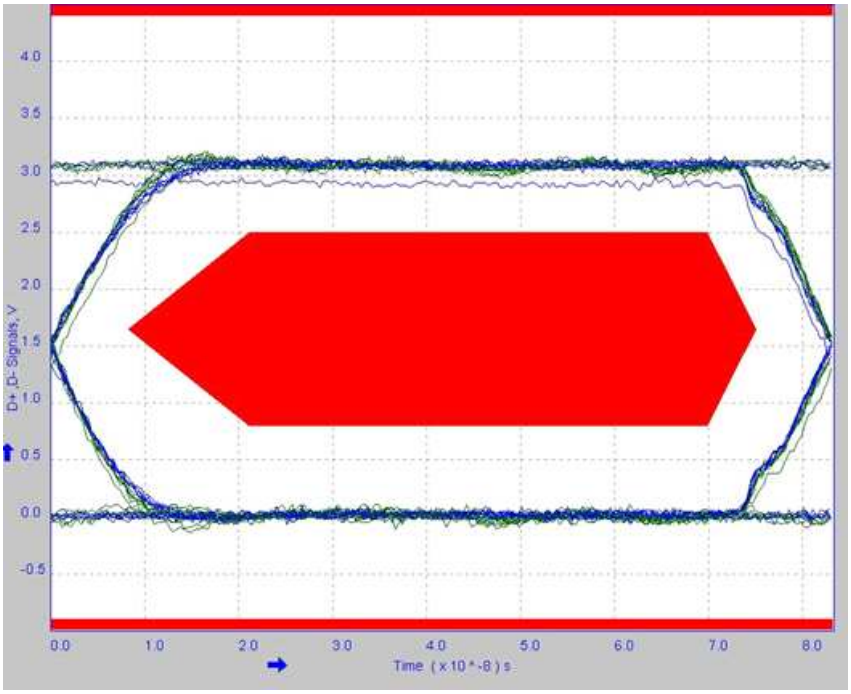


Figure 6-4. Full-Speed Eye Diagram

6.3 Layout

6.3.1 Layout Guidelines

- The V_{DDIO} pins of the TUSB1210 supply 1.8-V (nominal) power to the core of the TUSB1210. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- The V_{BAT} pin of the TUSB1210 supply 3.3-V (nominal) power rail to the TUSB1210. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- The V_{BUS} pin of the TUSB1210 supply 5-V (nominal) power rail to the TUSB1210. This pin is normally connected to the V_{BUS} pin of the USB connector.
- All power rails require 0.1 µF decoupling capacitors for stability and noise immunity. The smaller decoupling capacitors should be placed as close to the TUSB1210 power pins as possible with an optimal grouping of two of differing values per pin.

6.3.1.1 Ground

It is recommended that almost one board ground plane be used in the design. This provides the best image plane for signal traces running above the plane. An earth or chassis ground is implemented only near the USB port connectors on a different plane for EMI and ESD purposes.

6.3.2 Layout Example

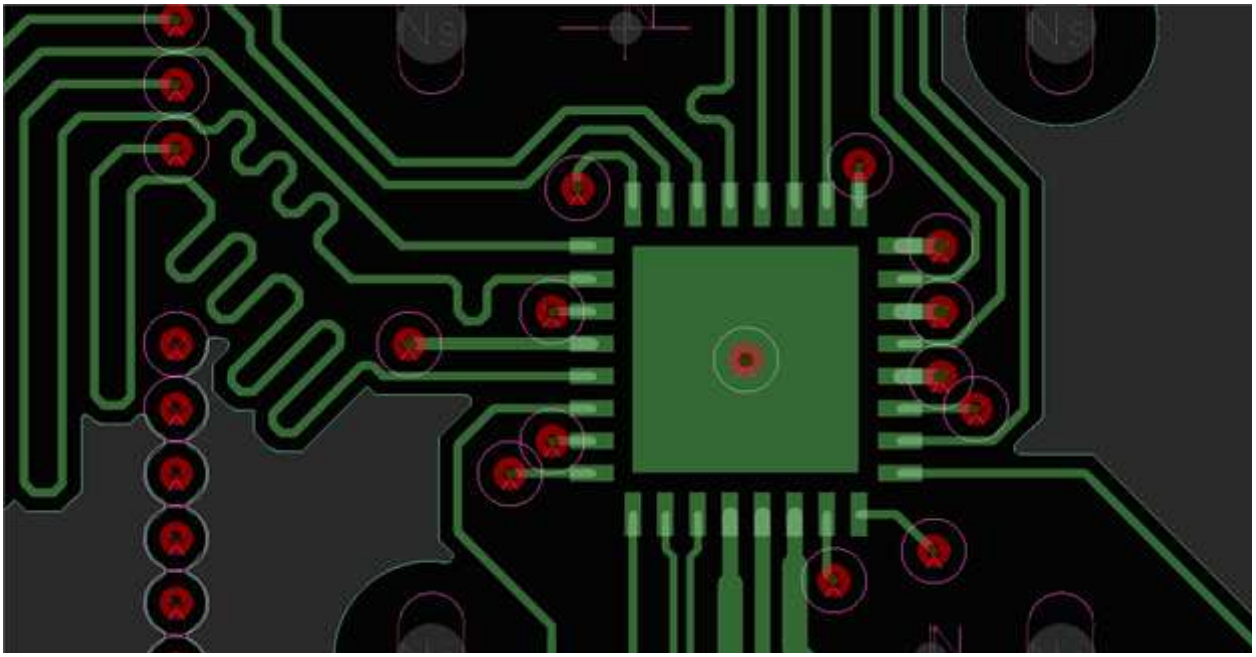


Figure 6-5. TUSB1210 Layout Example

6.4 Power Supply Recommendations

V_{BUS}, and V_{BAT}, and V_{DDIO}, are needed for power the TUSB1210. Recommended operation is for V_{BAT} to be present before V_{DDIO}. Applying V_{DDIO} before V_{BAT} to TUSB1210 is not recommended as there is a diode from V_{DDIO} to V_{BAT} which will be forward biased when V_{DDIO} is present but V_{BAT} is not present. TUSB1210 does not strictly require V_{BUS} to function.

6.4.1 TUSB1210 Power Supply

- The V_{DDIO} pins of the TUSB1210 supply 1.8 V (nominal) power to the core of the TUSB1210. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.

- The V_{BAT} pin of the TUSB1210 supply 3.3 V (nominal) power rail to the TUSB1210. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- The V_{BUS} pin of the TUSB1210 supply 5.0 V (nominal) power rail to the TUSB1210. This pin is normally connected to the V_{BUS} pin of the USB connector.
- The V_{BUS} pin of the TUSB1210 supply 5.0 V (nominal) power rail to the TUSB1210. This pin is normally connected to the V_{BUS} pin of the USB connector.

7 Device and Documentation Support

7.1 Documentation Support

The following documents describe the TUSB1210 processor/MPU. Copies of these documents are available on the Internet at www.ti.com.

SLLZ066 ***Silicon Errata.*** Describes the known exceptions to the functional specifications for the . . .

7.2 Trademarks

All trademarks are the property of their respective owners.

7.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical Packaging and Orderable Information

8.1 Via Channel

The T package has been specially engineered with Via Channel technology. This allows larger than normal PCB via and trace sizes and reduced PCB signal layers to be used in a PCB design with the 0.65-mm pitch package, and substantially reduces PCB costs. It allows PCB routing in only two signal layers (four layers total) due to the increased layer efficiency of the Via Channel BGA technology.

Via Channel technology implemented on the [*your package*] package makes it possible to build an [*your device*]-based product with a 4-layer PCB, but a 4-layer PCB may not meet system performance goals. Therefore, system performance using a 4-layer PCB design must be evaluated during product design.

8.2 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSB1210BRHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	T1210B	Samples
TUSB1210BRHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	T1210B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

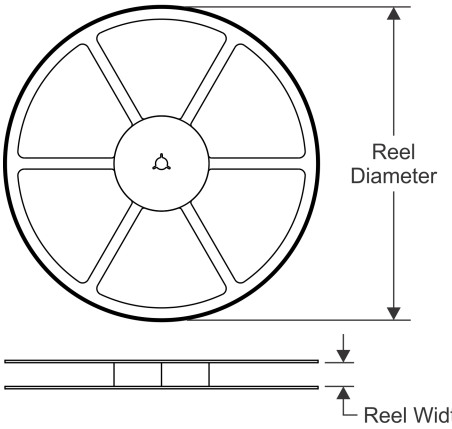
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

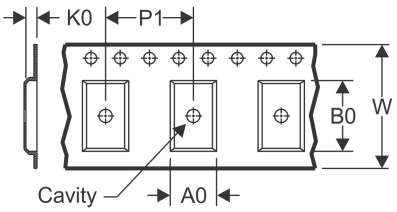
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

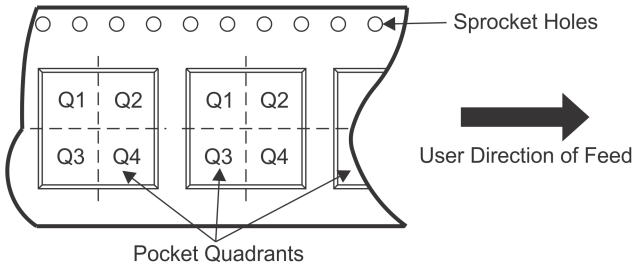


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

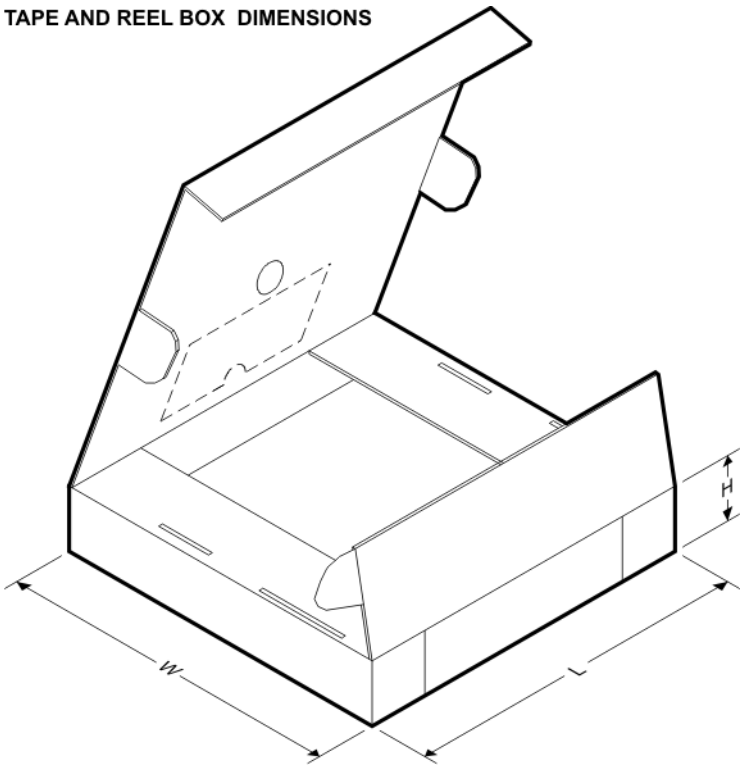
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB1210BRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TUSB1210BRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

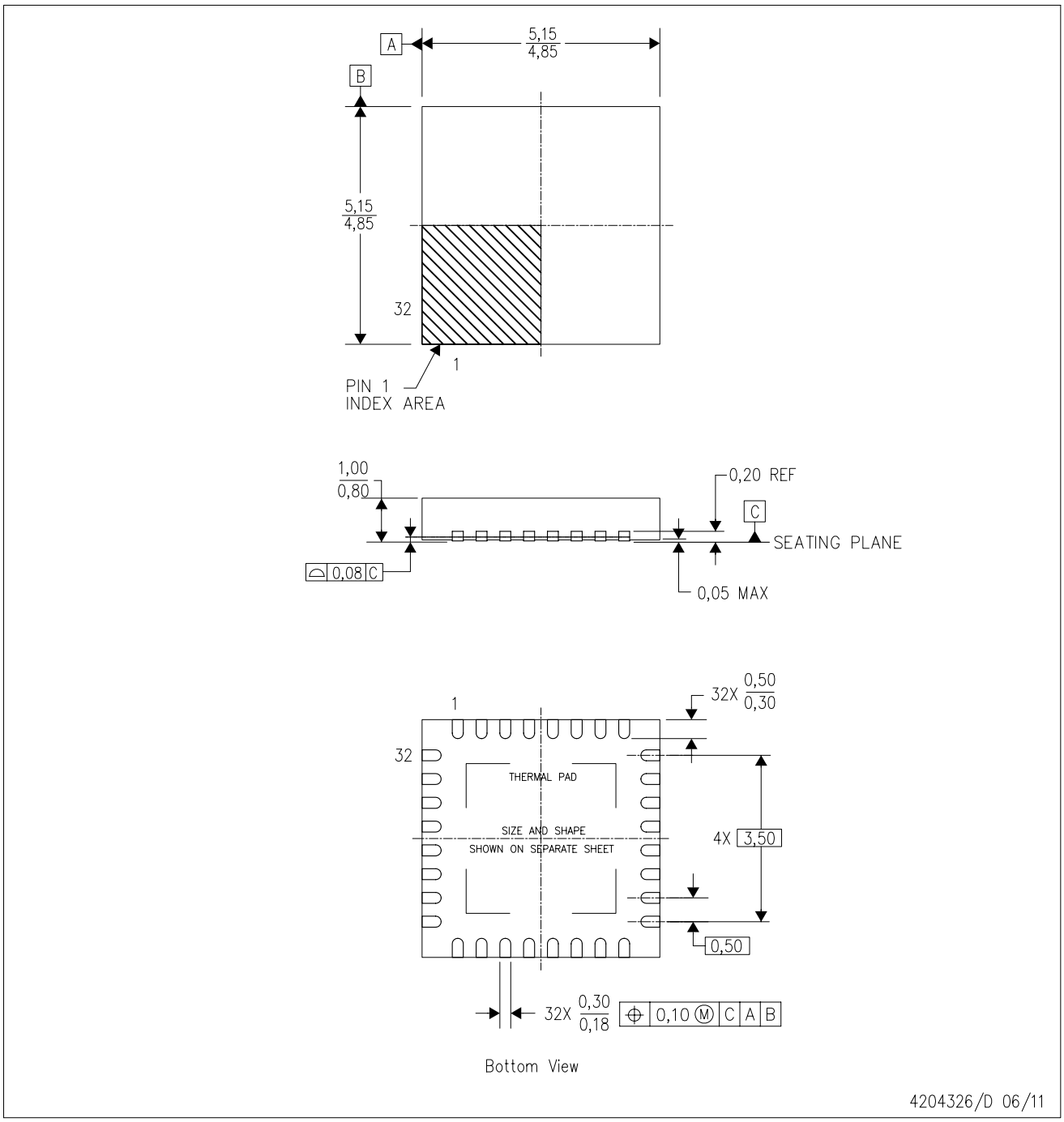
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB1210BRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
TUSB1210BRHBT	VQFN	RHB	32	250	210.0	185.0	35.0

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

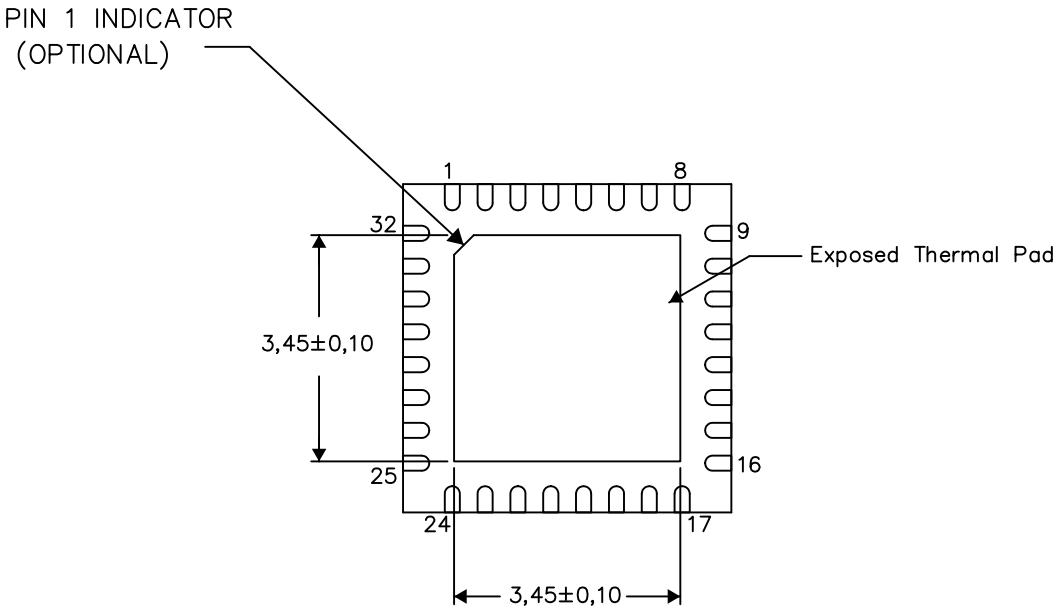
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



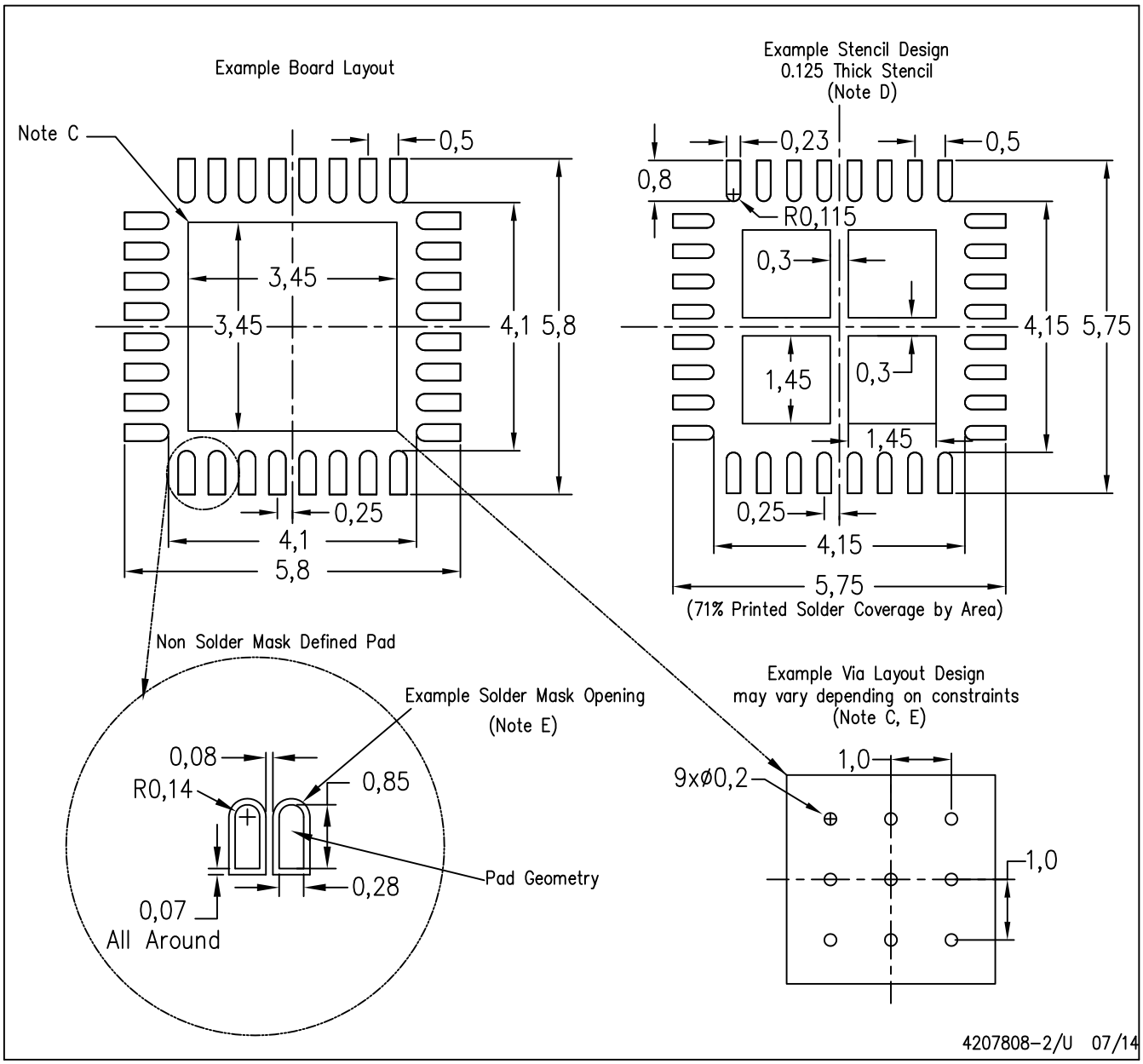
Bottom View

Exposed Thermal Pad Dimensions

4206356–2/AB 07/14

NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

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