SBAS162G – NOVEMBER 2000 – REVISED JUNE 2007

I²C TOUCH SCREEN CONTROLLER

FEATURES

- 2.5V TO 5.25V OPERATION
- INTERNAL 2.5V REFERENCE
- DIRECT BATTERY MEASUREMENT (0.5V TO 6V)
- ON-CHIP TEMPERATURE MEASUREMENT
- TOUCH-PRESSURE MEASUREMENT
- I²C INTERFACE SUPPORTS: Standard, Fast, and High-Speed Modes
- AUTO POWER DOWN
- TSSOP-16 AND VFBGA-48 PACKAGES

APPLICATIONS

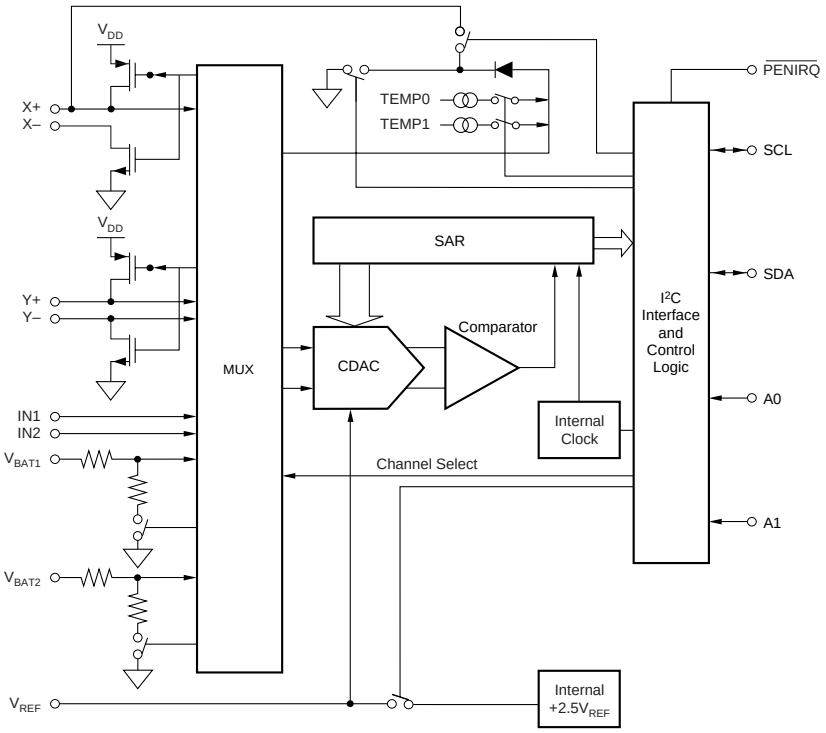
- PERSONAL DIGITAL ASSISTANTS
- PORTABLE INSTRUMENTS
- POINT-OF-SALES TERMINALS
- PAGERS
- TOUCH SCREEN MONITORS
- CELLULAR PHONES

DESCRIPTION

The TSC2003 is a 4-wire resistive touch screen controller. It also features direct measurement of two batteries, two auxiliary analog inputs, temperature measurement, and touch-pressure measurement.

The TSC2003 has an on-chip 2.5V reference that can be utilized for the auxiliary inputs, battery monitors, and temperature-measurement modes. The reference can also be powered down when not used to conserve power. The internal reference will operate down to 2.7V supply voltage while monitoring the battery voltage from 0.5V to 6V.

The TSC2003 is available in the small TSSOP-16 and VFBGA-48 packages and is specified over the –40°C to +85°C temperature range.



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PACKAGE/ORDERING INFORMATION(1)

PRODUCT	MAXIMUM RELATIVE ACCURACY (LSB)	MAXIMUM GAIN ERROR (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER
TSC2003	±2	±4	TSSOP-16	PW	–40°C to +85°C	TSC2003I	TSC2003IPW
TSC2003	±2	±4	TSSOP-16	PW	–40°C to +85°C	TSC2003I	TSC2003IPWT
TSC2003	±2	±4	TSSOP-16	PW	–40°C to +85°C	TSC2003I	TSC2003IPWR
TSC2003	±2	±4	TSSOP-16	PW	–40°C to +85°C	TSC2003I	TSC2003IPWRG4
TSC2003	±2	±4	VFBGA-48	ZQC	–40°C to +85°C	BC2003	TSC2003IZQCT
TSC2003	±2	±4	VFBGA-48	ZQC	–40°C to +85°C	BC2003	TSC2003IZQCR

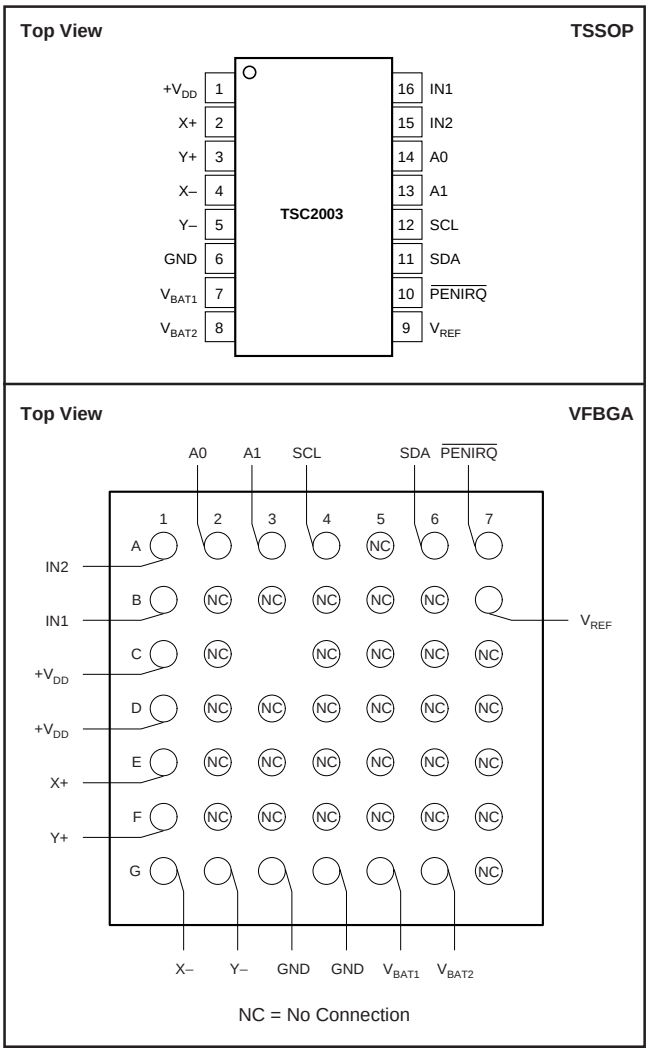
NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or refer to our web site at www.ti.com.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS(1)

$+V_{DD}$ to GND	–0.3V to +6V
Digital Input Voltage to GND	–0.3V to $+V_{DD}$ + 0.3V
Analog Input Voltage to GND. All Pins Except 7, 8	–0.3V to $+V_{DD}$ + 0.3V
Analog Input Voltage Pins 7, 8 to GND	–0.3V to +6.0V
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Power Dissipation	$(T_J \text{ Max} - T_A)/\theta_{JA}$
TSSOP Package	
Junction Temperature (T_J Max)	+150°C
θ_{JA} Thermal Impedance	+115.2°C/W
Lead Temperature, Soldering	
Vapor Phase (60s)	+215°C
Infrared (15s)	+220°C
VFBGA Package	
Junction Temperature (T_J Max)	+125°C
θ_{JA} Thermal Impedance	+50°C/W
Lead Temperature, Soldering	
Vapor Phase (60s)	+215°C
Infrared (15s)	+220°C

NOTE: (1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PIN DESCRIPTIONS

TSSOP PIN #	VFBGA PIN #	NAME	DESCRIPTION
1	C1, D1	$+V_{DD}$	Power Supply
2	E1	X+	X+ Position Input
3	F1	Y+	Y+ Position Input
4	G1	X–	X– Position Input
5	G2	Y–	Y– Position Input
6	G3, G4	GND	Ground
7	G5	V_{BAT1}	Battery Monitor Input
8	G6	V_{BAT2}	Battery Monitor Input
9	B7	V_{REF}	Voltage Reference Input/Output
10	A7	$\overline{\text{PENIRQ}}$	Pen Interrupt. Open Drain Output (Requires 30kΩ to 100kΩ pull-up resistor externally).
11	A6	SDA	Serial Data
12	A4	SCL	Serial Clock
13	A3	A1	I^2C Bus Address Input A1
14	A2	A0	I^2C Bus Address Input A0
15	A1	IN2	Auxiliary A/D Converter Input
16	B1	IN1	Auxiliary A/D Converter Input

ELECTRICAL CHARACTERISTICS

At T_A = –40°C to +85°C, $+V_{DD}$ = +2.7V, V_{REF} = 2.5V external voltage, I^2C bus frequency = 3.4MHz, 12-bit mode and digital inputs = GND or $+V_{DD}$, unless otherwise noted.

PARAMETER	CONDITIONS	TSC2003I MIN	TYP	MAX	UNITS
ANALOG INPUT					
Full-Scale Input Span		0		V_{REF}	V
Absolute Input Range		–0.2		$+V_{DD}$ +0.2	V
Capacitance			25		pF
Leakage Current			0.1		µA
SYSTEM PERFORMANCE					
Resolution			12		Bits
No Missing Codes	Standard and Fast Mode	11			Bits
	High-Speed Mode	10			Bits
Integral Linearity Error	Standard and Fast Mode			±2	LSB(1)
	High-Speed Mode			±4	LSB
Offset Error				±6	LSB
Gain Error				±4	LSB
Noise	Including Internal V_{REF}		70		µVrms
Power-Supply Rejection Ratio			70		dB
SAMPLING DYNAMICS					
Throughput Rate			50		ksps
Channel-to-Channel Isolation	V_{IN} = 2.5Vp-p at 50kHz		100		dB
SWITCH DRIVERS					
On-Resistance					
Y+, X+			5.5		Ω
Y–, X–			7.3		Ω
Drive Current(2)	Duration 100ms			50	mA
REFERENCE OUTPUT					
Internal Reference Voltage		2.45	2.50	2.55	V
Internal Reference Drift			25		ppm/°C
Output Impedance	Internal Reference ON		300		Ω
	Internal Reference OFF		1		GΩ
Quiescent Current	PD1 = 1, PD0 = 0, SDA, SCL High		750		µA
REFERENCE INPUT					
Range		2.0		V_{DD}	V
Resistance	PD1 = PD0 = 0		1		GΩ
BATTERY MONITOR					
Input Voltage Range		0.5		6.0	V
Input Impedance	Sampling Battery		10		kΩ
	Battery Monitor OFF		1		GΩ
Accuracy	External V_{REF} = 2.5V	–2		+2	%
	Internal Reference	–3		+3	%
TEMPERATURE MEASUREMENT					
Temperature Range		–40		+85	°C
Resolution	Differential Method(3)		1.6		°C
	TEMP0(4)		0.3		°C
Accuracy	Differential Method(3)		±2		°C
	TEMP0(4)		±3		°C
DIGITAL INPUT/OUTPUT					
Logic Family			CMOS		
Logic Levels, Except $\overline{PENIRQ}$					
V_{IH}	$\lvert I_{IH} \rvert \le +5\mu A$	$+V_{DD}$ • 0.7		$+V_{DD}$ + 0.3	V
V_{IL}	$\lvert I_{IL} \rvert \le +5\mu A$	–0.3		$+V_{DD}$ • 0.3	V
V_{OH}	I_{OH} = –250µA	$+V_{DD}$ • 0.8			V
V_{OL}	I_{OL} = 250µA			0.4	V
$\overline{PENIRQ}$ V_{OL}	30kΩ Pull-Up			0.4	V
Data Format			Straight Binary		
Input Capacitance	SDA, SCL Lines			10	pF

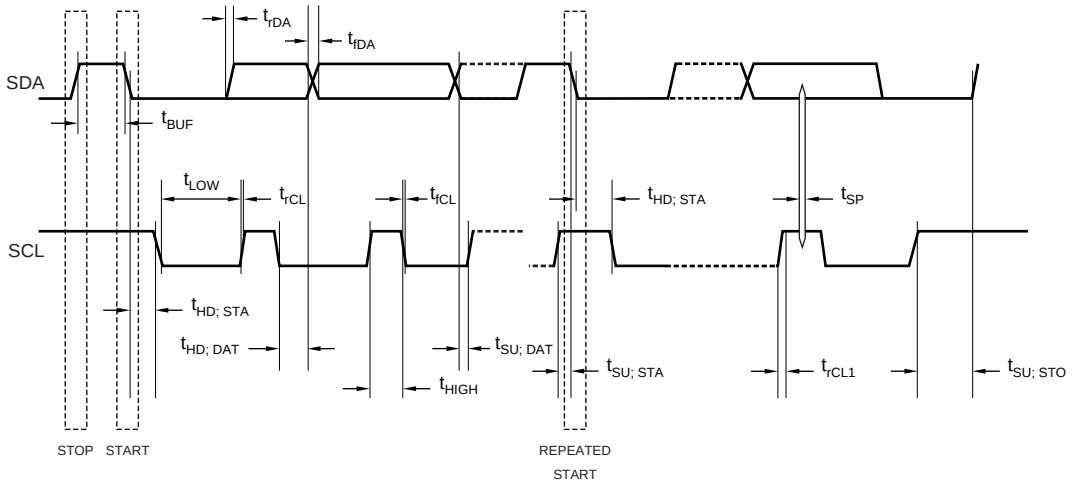
ELECTRICAL CHARACTERISTICS (Cont.)

At T_A = –40°C to +85°C, $+V_{DD}$ = +2.7V, V_{REF} = 2.5V external voltage, I^2C bus frequency = 3.4MHz, 12-bit mode and digital inputs = GND or $+V_{DD}$, unless otherwise noted.

PARAMETER	CONDITIONS	TSC2003I			
		MIN	TYP	MAX	UNITS
POWER-SUPPLY REQUIREMENTS					
$+V_{DD}$	Specified Performance	2.7		3.6	V
	Operating Range	2.5		5.25	V
Quiescent Current	Internal Reference OFF, PD1 = PD0 = 0				
	High-Speed Mode: SCL = 3.4MHz		254	650	µA
	Fast Mode: SCL = 400kHz		95		µA
	Standard Mode: SCL = 100kHz		63		µA
	Internal Reference ON, PD0 = 0		1005		µA
Power-Down Current when Part is Not Addressed	Internal Reference OFF, PD1 = PD0 = 0				
	High-Speed Mode: SCL = 3.4MHz		90		µA
	Fast Mode: SCL = 400kHz		21		µA
	Standard Mode: SCL = 100kHz		4		µA
	PD1 = PD0 = 0, SDA = SCL = $+V_{DD}$			3	µA
Power Dissipation	$+V_{DD}$ = +2.7V			1.8	mW
TEMPERATURE RANGE					
Specified Performance		–40		+85	°C

NOTES: (1) LSB means Least Significant Bit. With V_{REF} equal to +2.5V, one LSB is 610µV. (2) Ensured by design, but not tested. Exceeding 50mA source current may result in device degradation. (3) Difference between TEMP0 and TEMP1 measurement. No calibration necessary. (4) Temperature drift is –2.1mV/°C.

TIMING DIAGRAM



TIMING CHARACTERISTICS

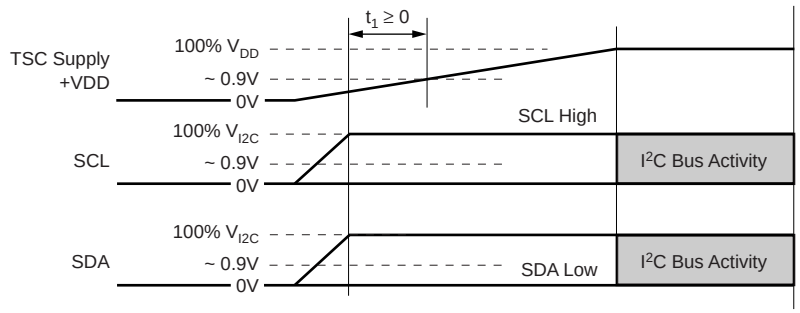
At T_A = –40°C to +85°C, $+V_{DD}$ = +2.7V, unless otherwise noted. All values referred to V_{IHMIN} and V_{ILMAX} levels.

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
SCL Clock Frequency	f_{SCL}	Standard Mode	0	100	kHz
		Fast Mode	0	400	kHz
		High-Speed Mode, C_b = 100pF max	0	3.4	MHz
		High-Speed Mode, C_b = 400pF max	0	1.7	MHz
Bus Free Time Between a STOP and Start Condition	t_{BUF}	Standard Mode	4.7		µs
		Fast Mode	1.3		µs
Hold Time (Repeated) START Condition	$t_{HD;\ STA}$	Standard Mode	4.0		µs
		Fast Mode	600		ns
		High-Speed Mode	160		ns
LOW Period of the SCL Clock	t_{LOW}	Standard Mode	4.7		µs
		Fast Mode	1.3		µs
		High-Speed Mode, C_b = 100pF max	160		ns
		High-Speed Mode, C_b = 400pF max	320		ns
HIGH Period of the SCL Clock	t_{HIGH}	Standard Mode	4.0		µs
		Fast Mode	600		ns
		High-Speed Mode, C_b = 100pF max	60		ns
		High-Speed Mode, C_b = 400pF max	120		ns
Setup Time for a Repeated START Condition	$t_{SU;\ STA}$	Standard Mode	4.7		µs
		Fast Mode	600		ns
		High-Speed Mode	160		ns
Data Setup Time	$t_{SU;\ DAT}$	Standard Mode	250		ns
		Fast Mode	100		ns
		High-Speed Mode	10		ns
Data Hold Time	$t_{HD;\ DAT}$	Standard Mode	0	3.45	µs
		Fast Mode	0	0.9	µs
		High-Speed Mode, C_b = 100pF max	0	70	ns
		High-Speed Mode, C_b = 400pF max	0	150	ns
Rise Time of SCL Signal	t_{rCL}	Standard Mode		1000	ns
		Fast Mode	$20 + 0.1C_b$	300	ns
		High-Speed Mode, C_b = 100pF max	10	40	ns
		High-Speed Mode, C_b = 400pF max	20	80	ns
Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge Bit	t_{rCL1}	Standard Mode		1000	ns
		Fast Mode	$20 + 0.1C_b$	300	ns
		High-Speed Mode, C_b = 100pF max	10	80	ns
		High-Speed Mode, C_b = 400pF max	20	160	ns
Fall Time of SCL Signal	t_{fCL}	Standard Mode		300	ns
		Fast Mode	$20 + 0.1C_b$	300	ns
		High-Speed Mode, C_b = 100pF max	10	40	ns
		High-Speed Mode, C_b = 400pF max	20	80	ns
Rise Time of SDA Signal	t_{rDA}	Standard Mode		1000	ns
		Fast Mode	$20 + 0.1C_b$	300	ns
		High-Speed Mode, C_b = 100pF max	10	80	ns
		High-Speed Mode, C_b = 400pF max	20	160	ns
Fall Time of SDA Signal	t_{fDA}	Standard Mode		300	ns
		Fast Mode	$20 + 0.1C_b$	300	ns
		High-Speed Mode, C_b = 100pF max	10	80	ns
		High-Speed Mode, C_b = 400pF max	20	160	ns
Setup Time for STOP Condition	$t_{SU;\ STO}$	Standard Mode	4.0		µs
		Fast Mode	600		ns
		High-Speed Mode	160		ns
Capacitive Load for SDA or SCL Line	C_b	Standard Mode		400	pF
		Fast Mode		400	pF
		High-Speed Mode, SCL = 1.7MHz		400	pF
		High-Speed Mode, SCL = 3.4MHz		100	pF
Pulse Width of Spike Suppressed	t_{SP}	Fast Mode	0	50	ns
		High-Speed Mode	0	10	ns
Noise Margin at the HIGH Level for Each Connected Device (Including Hysteresis)	V_{nH}	Standard Mode Fast Mode High-Speed Mode	$0.2V_{DD}$		V
Noise Margin at LOW Level for Each Connected Device (Including Hysteresis)	V_{nL}	Standard Mode Fast Mode High-Speed Mode	$0.1V_{DD}$		V

POWER-ON SEQUENCE TIMING

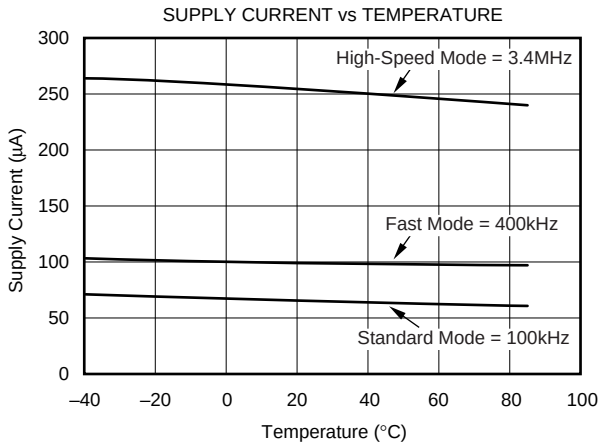
During TSC2003 power-up, the I^2C bus should be idle. In other words, the SDA and SCL lines must be high before the TSC supply (+VDD) ramps up greater than 0.9V. If the TSC uses the same supply as the the I^2C bus pull-up resistors (V_{I2C}), then a 1µF capacitor placed very close to the TSC supply pin will cause the TSC supply to ramp up more slowly (refer to the Power-On Sequence timing diagram). If the TSC supply (+VDD) is different than the supply to the I^2C bus pull-up resistors (V_{I2C}), then V_{I2C} should be turned on before the TSC supply (+VDD) is powered up.

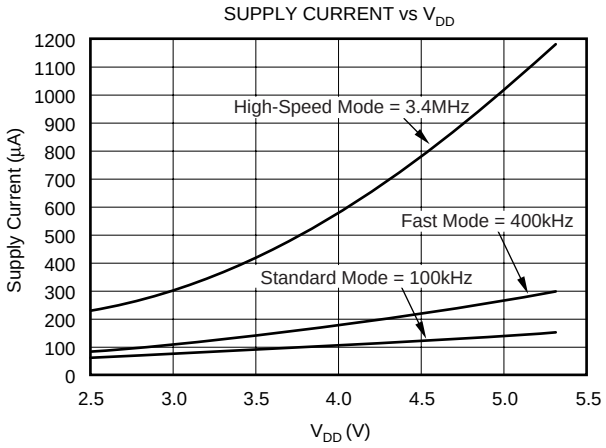
POWER-ON SEQUENCE TIMING DIAGRAM

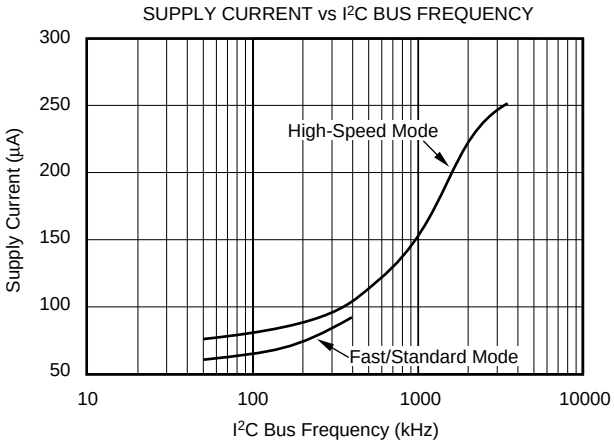


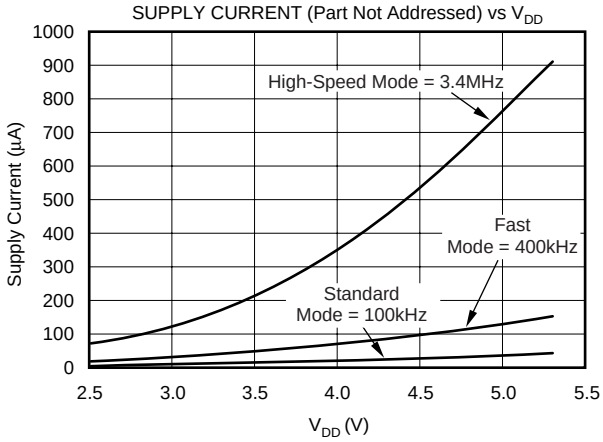
TYPICAL CHARACTERISTICS: +2.7V

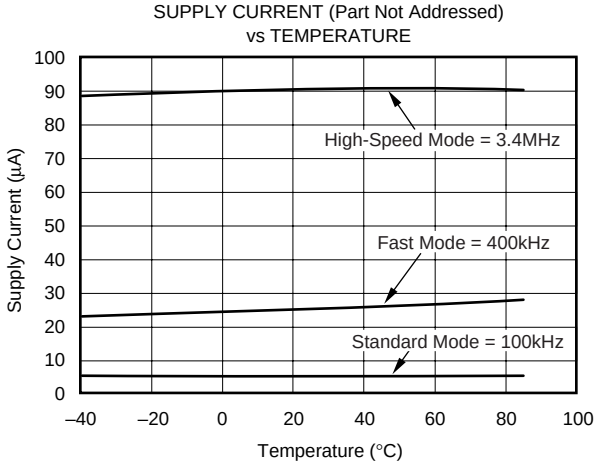
At T_A = +25°C, $+V_{DD}$ = +2.7V, V_{REF} = External +2.5V, I²C bus frequency = 3.4MHz, PD1 = PD0 =0, unless otherwise noted.

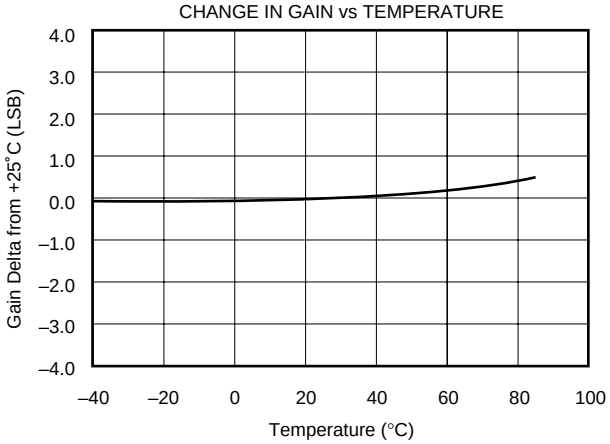








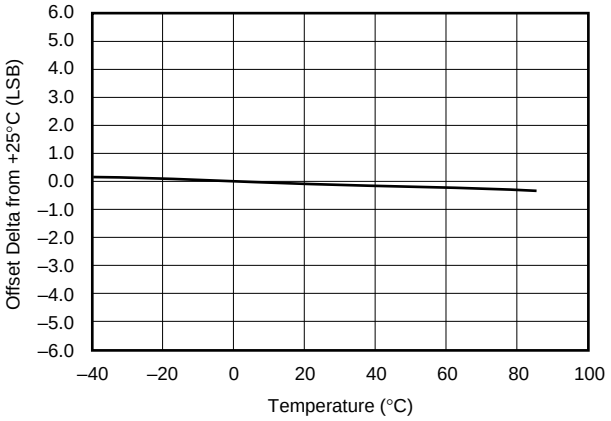




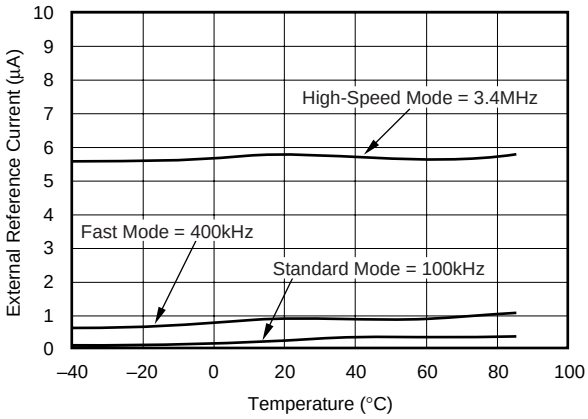
TYPICAL CHARACTERISTICS: +2.7V (Cont.)

At T_A = +25°C, $+V_{DD}$ = +2.7V, V_{REF} = External +2.5V, I^2C bus frequency = 3.4MHz, PD1 = PD0 =0, unless otherwise noted.

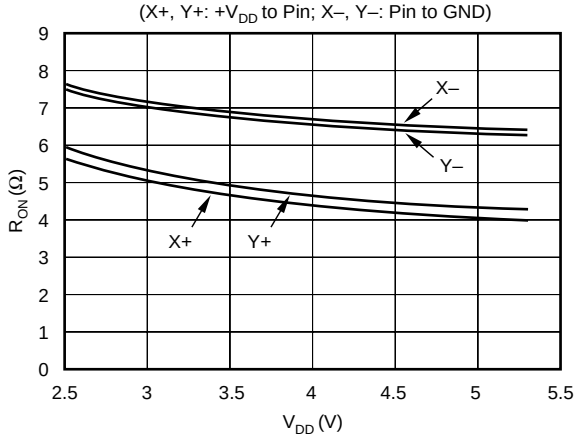
CHANGE IN OFFSET vs TEMPERATURE



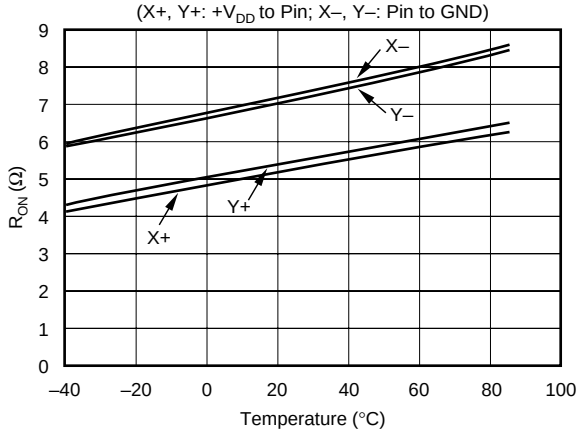
EXTERNAL REFERENCE CURRENT vs TEMPERATURE



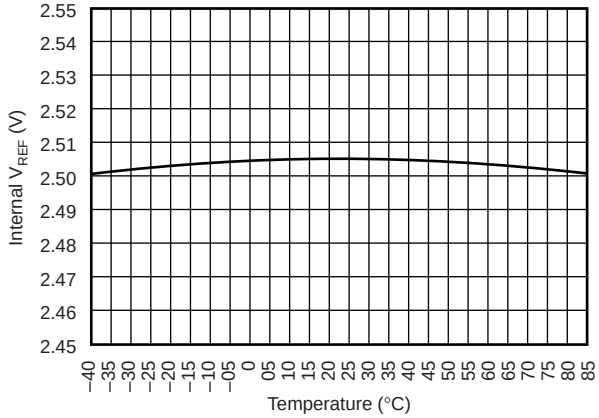
SWITCH-ON RESISTANCE vs V_{DD}
(X+, Y+: $+V_{DD}$ to Pin; X–, Y–: Pin to GND)



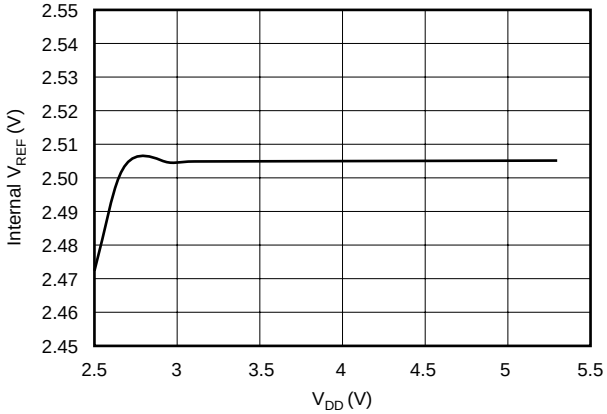
SWITCH-ON RESISTANCE vs TEMPERATURE
(X+, Y+: $+V_{DD}$ to Pin; X–, Y–: Pin to GND)



INTERNAL V_{REF} vs TEMPERATURE

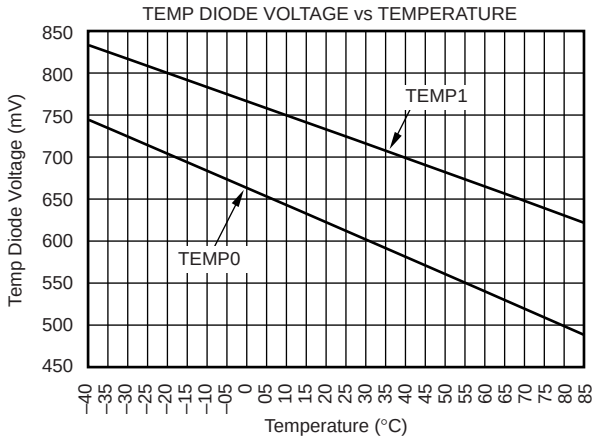


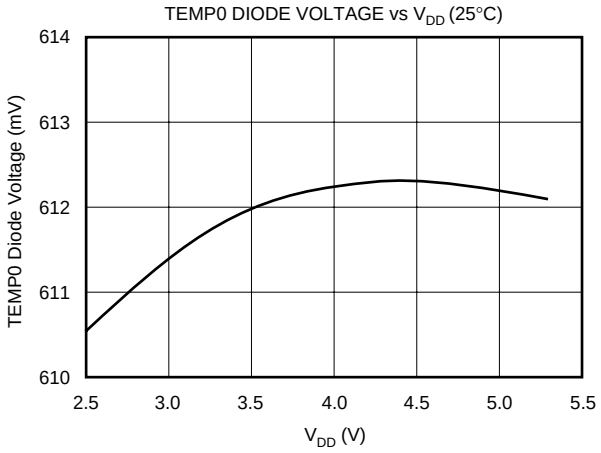
INTERNAL V_{REF} vs V_{DD}

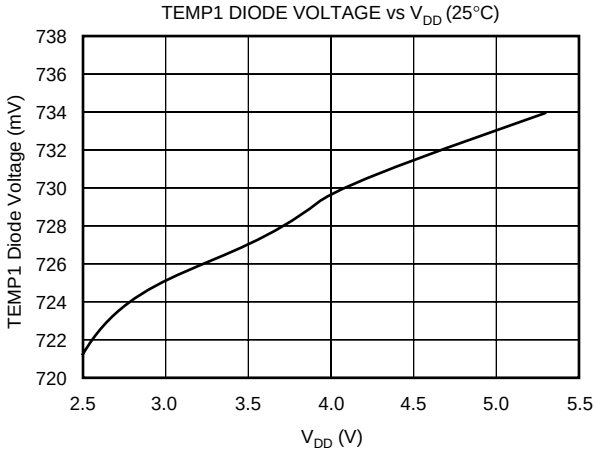


TYPICAL CHARACTERISTICS: +2.7V (Cont.)

At T_A = +25°C, $+V_{DD}$ = +2.7V, V_{REF} = External +2.5V, I²C bus frequency = 3.4MHz, PD1 = PD0 =0, unless otherwise noted.







THEORY OF OPERATION

The TSC2003 is a classic Successive Approximation Register (SAR) Analog-to-Digital (A/D) converter. The architecture is based on capacitive redistribution which inherently includes a sample-and-hold function. The converter is fabricated on a 0.6µ CMOS process.

The basic operation of the TSC2003 is shown in Figure 1. The device features an internal 2.5V reference and an internal clock. Operation is maintained from a single supply of 2.7V to 5.25V. The internal reference can be overdriven with an external, low-impedance source between 2V and $+V_{DD}$. The value of the reference voltage directly sets the input range of the converter.

The analog input (X, Y, and Z parallel coordinates, auxiliary inputs, battery voltage, and chip temperature) to the converter is provided via a multiplexer. A unique configuration of low on-resistance switches allows an unselected A/D converter input channel to provide power, and an accompanying pin to provide ground for an external device. By maintaining a differential input to the converter, and a differential reference architecture, it is possible to negate the switch's on-resistance error (should this be a source of error for the particular measurement).

ANALOG INPUT

See Figure 2 for a block diagram of the input multiplexer on the TSC2003, the differential input of the A/D converter, and the converter's differential reference.

When the converter enters the Hold mode, the voltage difference between the +IN and –IN inputs (see Figure 2) is captured on the internal capacitor array. The input current on the analog inputs depends on the conversion rate of the device. During the sample period, the source must charge the internal sampling capacitor (typically 25pF). After the capacitor has been fully charged, there is no further input current. The amount of charge transfer from the analog source to the converter is a function of conversion rate.

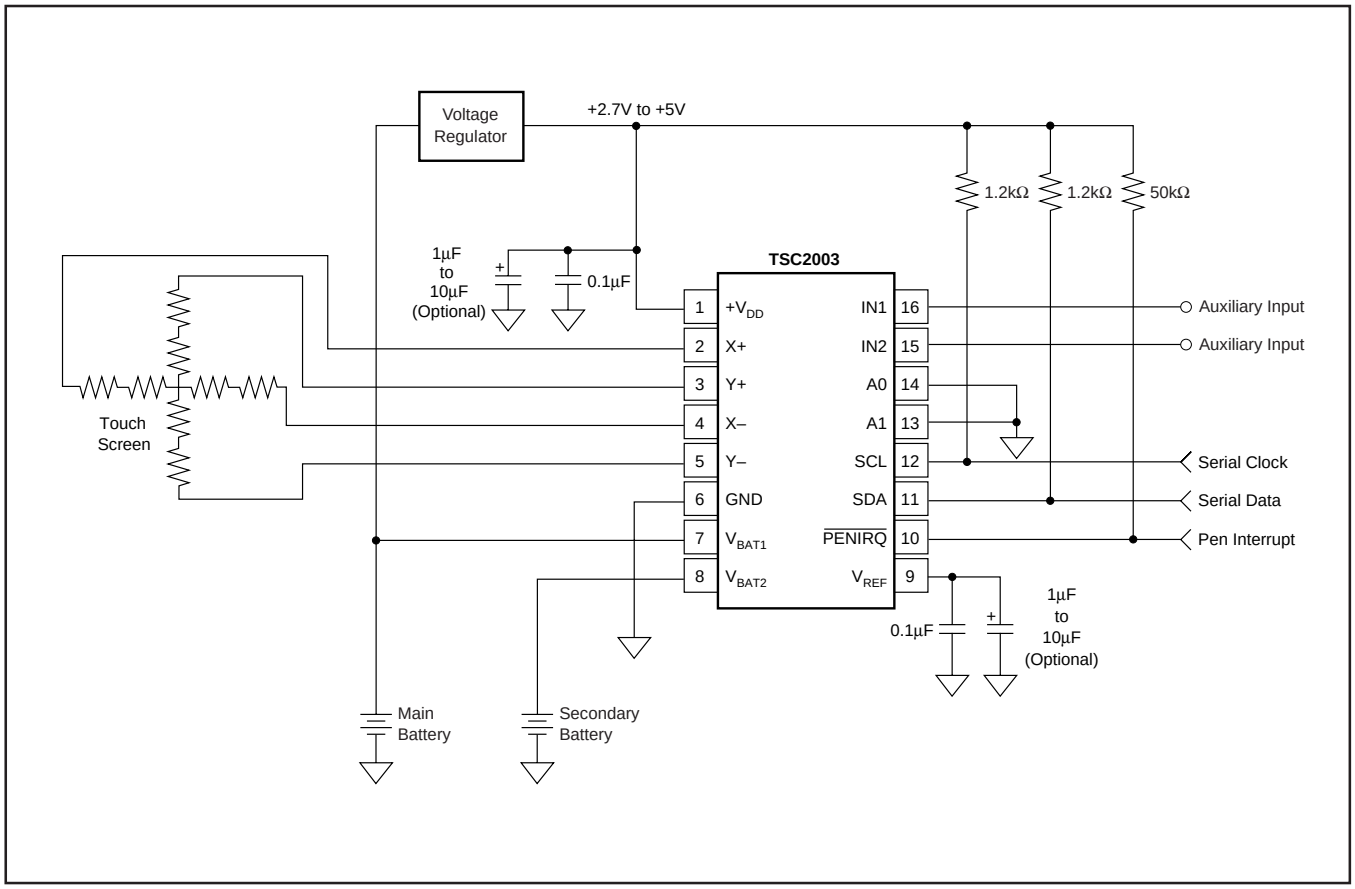


FIGURE 1. Basic Operation of the TSC2003.

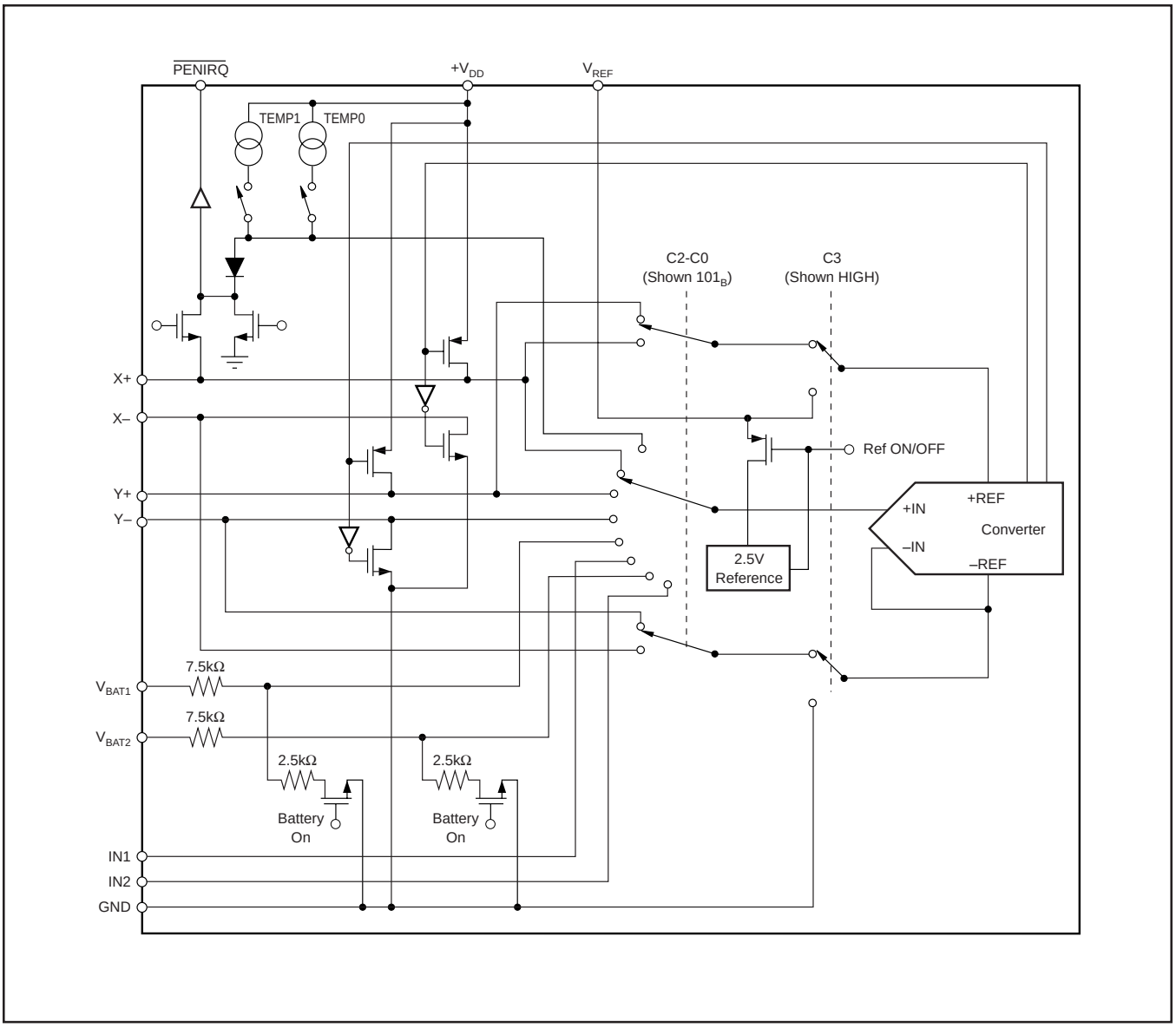


FIGURE 2. Simplified Diagram of the Analog Input.

INTERNAL REFERENCE

The TSC2003 has an internal 2.5V voltage reference that can be turned ON or OFF with the power-down control bits, PD0 and PD1 (see Table II and Figure 3). The internal reference is powered down when power is first applied to the device.

The internal reference voltage is only used in the single-ended reference mode for battery monitoring, temperature measurement, and for measuring the auxiliary input. Optimal touch screen performance is achieved when using a ratiometric conversion; thus, all touch screen measurements are done automatically in the differential mode.

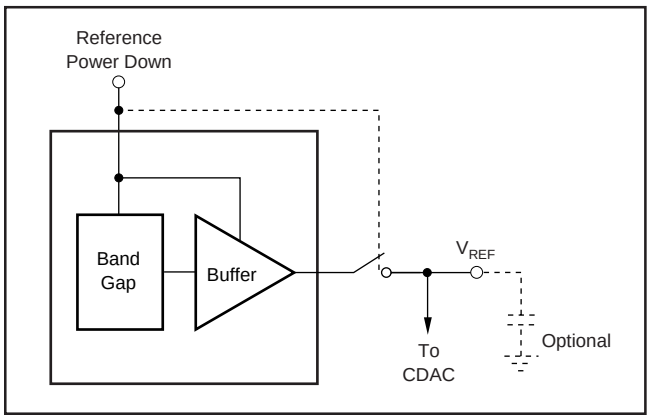


FIGURE 3. Simplified Diagram of the Internal Reference.

REFERENCE INPUT

The voltage difference between +REF and –REF (see Figure 2) sets the analog input range. The TSC2003 will operate with a reference in the range of 2V to $+V_{DD}$. There are several critical items concerning the reference input and its wide-voltage range. As the reference voltage is reduced, the analog voltage weight of each digital output code is also reduced. This is often referred to as the LSB (Least Significant Bit) size, and is equal to the reference voltage divided by 4096 (256 if in 8-bit mode). Any Offset or Gain error inherent in the A/D converter will appear to increase, in terms of LSB size, as the reference voltage is reduced. For example, if the offset of a given converter is 2LSBs with a 2.5V reference, it will typically be 2.5LSBs with a 2V reference. In each case, the actual offset of the device is the same, 1.22mV. With a lower reference voltage, more care must be taken to provide a clean layout including adequate bypassing, a clean (low-noise, low-ripple) power supply, a low-noise reference (if an external reference is used), and a low-noise input signal.

The voltage into the V_{REF} input is not buffered, and directly drives the Capacitor Digital-to-Analog Converter (CDAC) portion of the TSC2003. Therefore, the input current is very low, typically < 6µA.

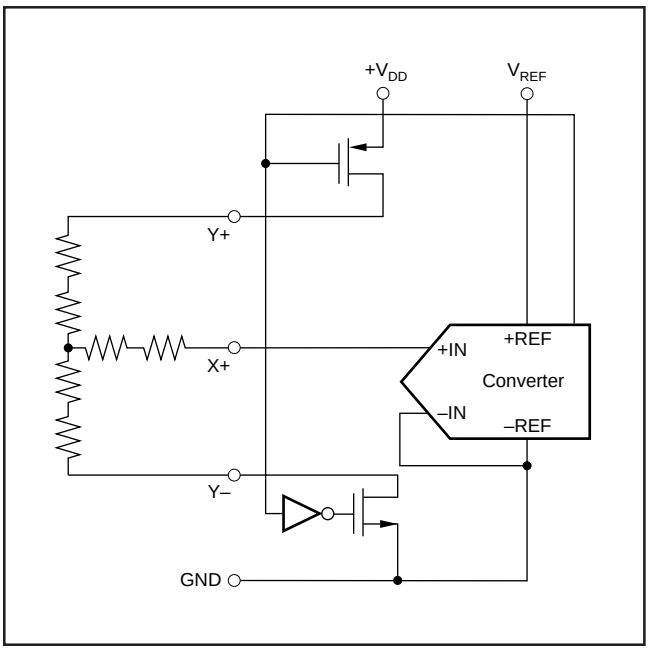


FIGURE 4. Simplified Diagram of Single-Ended Reference.

REFERENCE MODE

There is a critical item regarding the reference when making measurements while the switch drivers are ON. For this discussion, it is useful to consider the basic operation of the TSC2003 (see Figure 1). This particular application shows the device being used to digitize a resistive touch screen. A measurement of the current Y position of the pointing device is made by connecting the X+ input to the A/D converter, turning on the Y+ and Y– drivers, and digitizing the voltage on X+, as shown in Figure 4. For this measurement, the resistance in the X+ lead does not affect the conversion; it does, however, affect the settling time, but the resistance is usually small enough that this is not a concern. However, since the resistance between Y+ and Y– is fairly low, the on-resistance of the Y drivers does make a small difference. Under the situation outlined so far, it would not be possible to achieve a 0V input or a full-scale input regardless of where the pointing device is on the touch screen because some voltage is lost across the internal switches. In addition, the internal switch resistance is unlikely to track the resistance of the touch screen, providing an additional source of error.

This situation is remedied, as shown in Figure 5, by using the differential mode: the +REF and –REF inputs are connected directly to Y+ and Y–, respectively. This makes the A/D converter ratiometric. The result of the conversion is always a percentage of the external reference, regardless of how it changes in relation to the on-resistance of the internal switches.

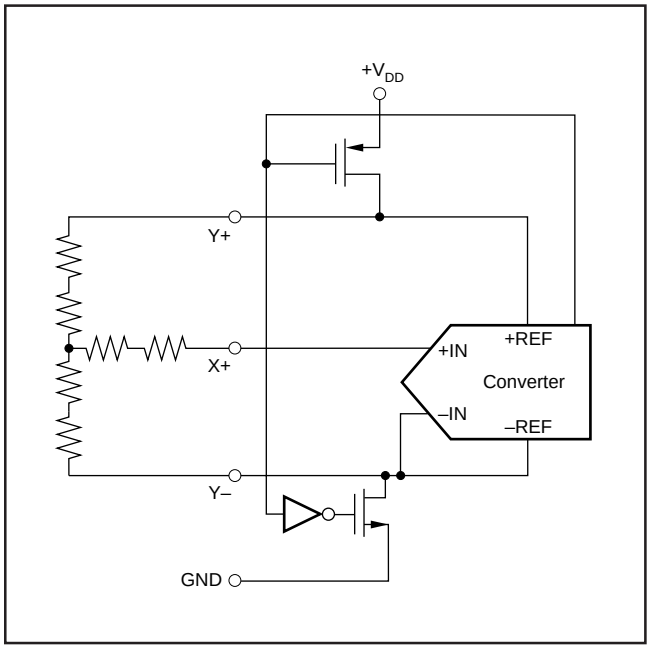


FIGURE 5. Simplified Diagram of Differential Reference (Y Switches Enabled, X+ is Analog Input).

Differential reference mode always uses the supply voltage, through the drivers, as the reference voltage for the A/D converter. V_{REF} cannot be used as the reference voltage in differential mode.

It is possible to use a high-precision reference on V_{REF} in single-ended reference mode for measurements which do not need to be ratiometric (i.e., battery voltage, temperature measurement, etc.). In some cases, it could be possible to power the converter directly from a precision reference. Most references can provide enough power for the TSC2003, but they might not be able to supply enough current for the external load, such as a resistive touch screen.

TOUCH SCREEN SETTLING

In some applications, external capacitors may be required across the touch screen for filtering noise picked up by the touch screen (i.e., noise generated by the LCD panel or backlight circuitry). These capacitors will provide a low-pass filter to reduce the noise, but they will also cause a settling time requirement when the panel is touched. The settling time will typically show up as a gain error. The problem is that the input and/or reference has not settled to its final steady-state value prior to the A/D converter sampling the input(s), and providing the digital output. Additionally, the reference voltage may still be changing during the measurement cycle.

To resolve these settling time problems, the TSC2003 can be commanded to turn on the drivers only without performing a conversion (see Table I). Time can then be allowed before the command is issued to perform a conversion. Generally, the time it takes to communicate the conversion command over the I^2C bus is adequate for the touch screen to settle.

TEMPERATURE MEASUREMENT

In some applications, such as battery recharging, a measurement of ambient temperature is required. The temperature measurement technique used in the TSC2003 relies on the characteristics of a semiconductor junction operating at a fixed current level to provide a measurement of the temperature of the TSC2003 chip. The forward diode voltage (V_{BE}) has a well-defined characteristic versus temperature. The temperature can be predicted in applications by knowing the 25°C value of the V_{BE} voltage and then monitoring the delta of that voltage as the temperature changes. The TSC2003 offers two modes of temperature measurement.

The first mode requires calibrations at a known temperature, but only requires a single reading to predict the ambient temperature. A diode is used during this measurement cycle. The voltage across the diode is connected through the MUX for digitizing the diode forward bias voltage by the A/D converter with an address of C3 = 0, C2 = 0, C1 = 0, and C0 = 0 (see Table I and Figure 6 for details). This voltage is typically 600mV at +25°C, with a 20µA current through it. The absolute value of this diode voltage can vary a few millivolts; the Temperature Coefficient (TC) of this voltage is very consistent at –2.1mV/°C. During the final test of the end product, the diode voltage would be stored at a known room temperature, in memory, for calibration purposes by the user. The result is an equivalent temperature measurement resolution of 0.3°C/LSB.

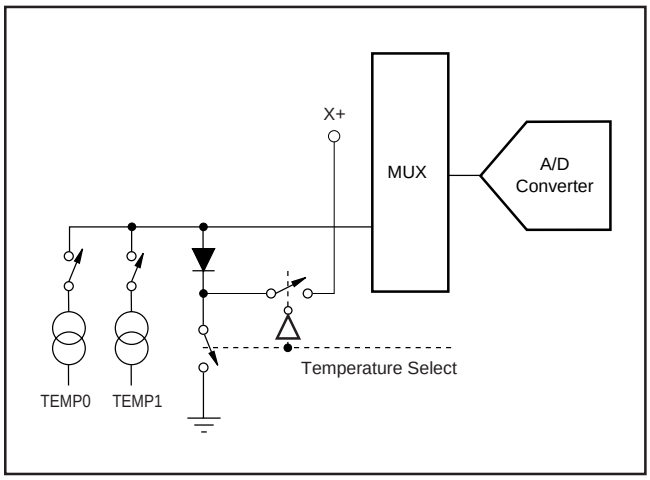


FIGURE 6. Functional Block Diagram of Temperature Measurement Mode.

The second mode does not require a test temperature calibration, but uses a two-measurement method to eliminate the need for absolute temperature calibration and for achieving 2°C/LSB accuracy. This mode requires a second conversion with an address of C3 = 0, C2 = 1, C1 = 0, and C0 = 0, with an 91 times larger current. The voltage difference between the first and second conversion using 91 times the bias current will be represented by kT/q • 1n (N), where N is the current ratio = 91, k = Boltzmann's constant (1.38054 • 10^{-23} electrons volts/degrees Kelvin), q = the electron charge (1.602189 • 10^{-19} C), and T = the temperature in degrees Kelvin. This mode can provide improved absolute temperature measurement over the first mode, but at the cost of less resolution (1.6°C/LSB). The equation to solve for °K is:

$$°K = \frac{q \bullet \Delta V}{k \bullet 1n(N)} \quad (1)$$

where:

$$\Delta V = V(I_{91}) - V(I_1) \text{ (in mV)}$$

$$\therefore {}^{\circ}K = 2.573 \Delta V {}^{\circ}K/mV$$

$${}^{\circ}C = 2.573 \bullet \Delta V(mV) - 273^{\circ}K$$

NOTE: The bias current for each diode temperature measurement is only turned ON during the acquisition mode, and, therefore, does not add any noticeable increase in power, especially if the temperature measurement only occurs occasionally.

BATTERY MEASUREMENT

An added feature of the TSC2003 is the ability to monitor the battery voltage on the other side of the voltage regulator (DC/DC converter), as shown in Figure 7. The battery voltage can vary from 0.5V to 6V, while the voltage regulator maintains the voltage to the TSC2003 at 2.7V, 3.3V, etc. The input voltage (V_{BAT1} or V_{BAT2}) is divided down by 4 so that a 6.0V battery voltage is represented as 1.5V to the A/D converter. The simplifies the multiplexer and control logic. In order to minimize the power consumption, the divider is only ON during the sample period which occurs after control bits C3 = 0, C2 = 0, C1 = 0, and C0 = 1 (V_{BAT1}) or C3 = 0, C2 = 1, C1 = 0, and C0 = 1 (V_{BAT2}) are received. See Tables I and II for the relationship between the control bits and configuration of the TSC2003.

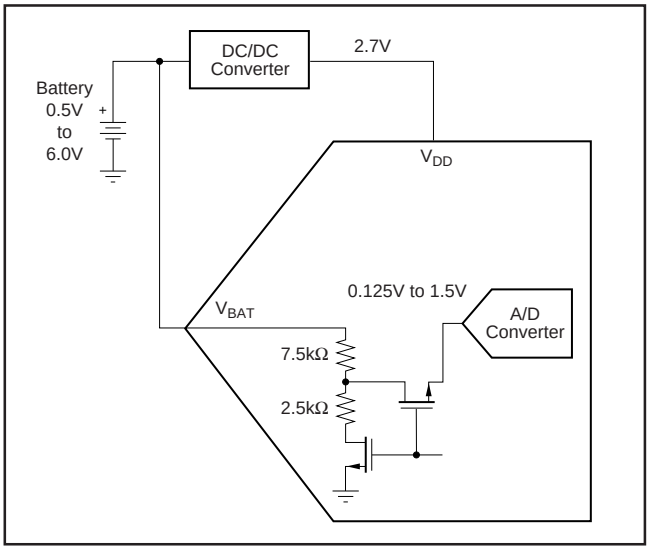


FIGURE 7. Battery Measurement Functional Block Diagram.

PRESSURE MEASUREMENT

Measuring touch pressure can also be done with the TSC2003. To determine pen or finger touch, the pressure of the "touch" needs to be determined. Generally, it is not necessary to have high accuracy for this test, therefore, the 8-bit resolution mode is recommended. However, calculations will be shown with the 12-bit resolution mode. There are several different ways of performing this measurement—the TSC2003 supports two methods.

The first method requires knowing the X-Plate resistance, measurement of the X-Position, and two additional cross-panel measurements (Z_2 and Z_1) of the touch screen, as shown in Figure 8. Using Equation 2 will calculate the touch resistance:

$$R_{TOUCH} = R_{X-Plate} \bullet \frac{X-Position}{4096}\left(\frac{Z_2}{Z_1} - 1\right) \qquad (2)$$

The second method requires knowing both the X-Plate and Y-Plate resistance, measurement of X-Position and Y-Position, and Z_1. Equation 3 calculates the touch resistance using the second method:

$$R_{TOUCH} = \frac{R_{X-Plate} \bullet X-Position}{4096}\left(\frac{4096}{Z_1} - 1\right) - R_{Y-Plate} \bullet \left(1 - \frac{Y-Position}{4096}\right) \qquad (3)$$

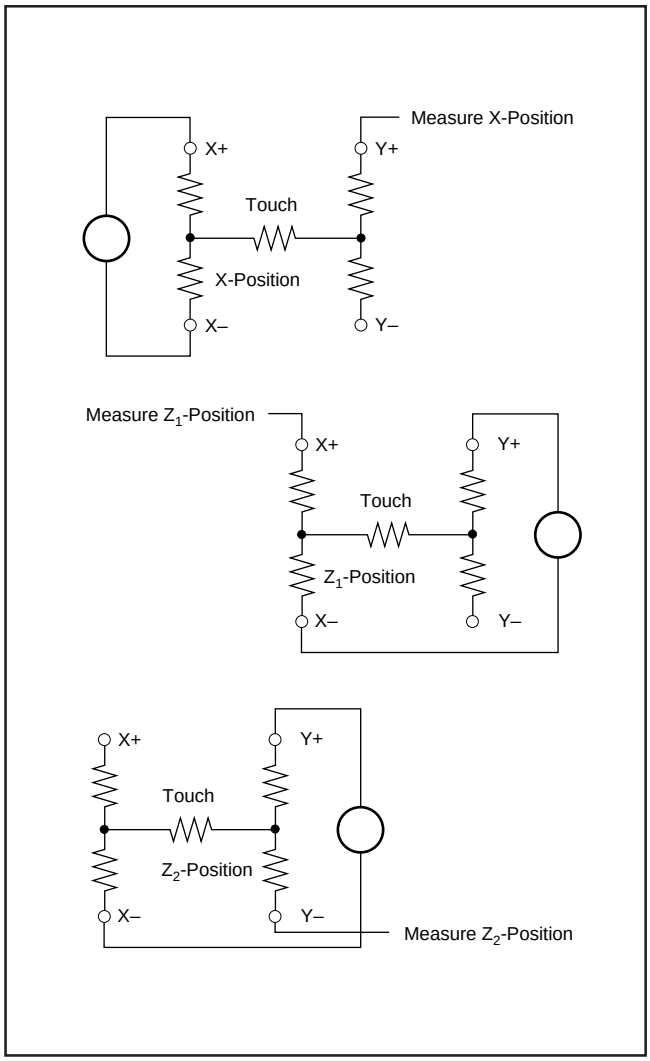


FIGURE 8. Pressure Measurement Block Diagrams.

DIGITAL INTERFACE

The TSC2003 supports the I^2C serial bus and data transmission protocol in all three defined modes: standard, fast, and high-speed. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a *master*. The devices that are controlled by the master are *slaves*. The bus must be controlled by a master device which generates the

serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The TSC2003 operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O lines SDA and SDL.

The following bus protocol has been defined, as shown in Figure 9:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy: Both data and clock lines remain HIGH.

Start Data Transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH defines a START condition.

Stop Data Transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH defines a STOP condition.

Data Valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise, and each receiver acknowledges with a ninth-bit.

Within the I²C bus specifications, a standard mode (100kHz clock rate), a fast mode (400kHz clock rate), and a high-speed mode (3.4MHz clock rate) are defined. The TSC2003 works in all three modes.

Acknowledge: Each receiving device, when accessed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse, which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Figure 9 details how data transfer is accomplished on the I²C bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

- **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after the slave address and each received byte.
- **Data transfer from a slave transmitter to a master receiver.** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next, a number of data bytes are transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last one. At the end of the last received byte, a 'not acknowledge' is returned.

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The TSC2003 may operate in the following two modes:

- **Slave Receiver Mode:** Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.
- **Slave Transmitter Mode:** The first byte (the slave address) is received and handled as in the slave receiver mode. However, in this mode the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the TSC2003 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

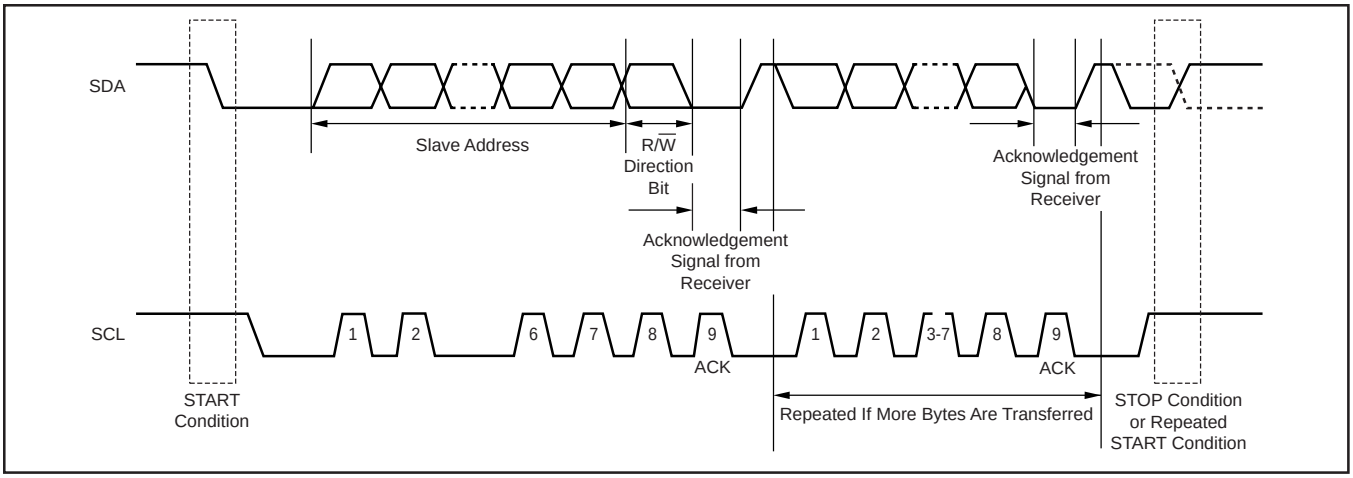


FIGURE 9. I²C Bus Protocol.

Address Byte

The address byte, as shown in Figure 10, is the first byte received following the START condition from the master device. The first five bits (MSBs) of the slave address are factory preset to 10010. The next two bits of the address byte are the device select bits: A1 and A0. Input pins (A1-A0) on the TSC2003 determine these two bits of the device address for a particular TSC2003. Therefore, a maximum of four devices with the same preset code can be connected on the same bus at one time.

MSB							LSB
1	0	0	1	0	A1	A0	R/$\overline{W}$

FIGURE 10. Address Byte.

The A1-A0 Address Inputs can be connected to V_{DD} or digital ground. The last bit of the address byte (R/$\overline{W}$) defines the operation to be performed. When set to a “1”, a read operation is selected; when set to a “0”, a write operation is selected. Following the START condition, the TSC2003 monitors the SDA bus and checks the device type identifier being transmitted. Upon receiving the 10010 code, the appropriate device select bits, and the R/$\overline{W}$ bit, the slave device outputs an acknowledge signal on the SDA line.

Command Byte

The TSC2003’s operating mode is determined by a command byte, which is shown in Figure 11.

MSB							LSB
C3	C2	C1	C0	PD1	PD0	M	X

FIGURE 11. Command Byte.

The bits in the device command byte are defined as follows:

- **C3-C0:** Configuration bits. These bits set the input multiplexer address and functions that the TSC2003 will perform, as shown in Table I.
- **PD1-PD0:** Power-down bits. These two bits select the power-down mode that the TSC2003 will be in after the current command completes, as shown in Table II.

The internal reference voltage can be turned ON or OFF independently of the A/D converter. This can allow extra time for the internal reference voltage to settle to its final value prior to making a conversion. Make sure to allow this extra wake-up time if the internal reference was powered down. Also note that the status of the internal reference power down is latched into the part (internally) when a STOP or repeated START occurs at the end of a command byte (see Figures 12 and 14). Therefore, in order to turn the internal reference OFF, an additional write to the TSC2003, with PD1 = 0, is required after the channel has been converted.

It is recommended to set PD0 = 0 in each command byte to get the lowest power consumption possible. If multiple X-, Y-, and Z-position measurements will be done one right after another, such as when averaging, PD0 =1 will leave the touch screen drivers on at the end of each conversion cycle.

- **M**: Mode bit. If M is 0, the TSC2003 is in 12-bit mode. If M is 1, 8-bit mode is selected.
- **X:** Don’t care.

PD1	PD0	$\overline{\text{PENIRQ}}$	DESCRIPTION
0	0	Enabled	Power-Down Between Conversions
0	1	Disabled	Internal reference OFF, ADC(1) ON
1	0	Enabled	Internal reference ON, ADC(1) OFF
1	1	Disabled	Internal reference ON, ADC(1) ON
NOTE: (1) ADC = Analog-to Digital Converter.			

TABLE II. Power-Down Bit Functions.

When the TSC2003 powers up, the power-down mode bits need to be written to ensure that the part is placed into the desired mode to achieve lowest power. Therefore, immediately after power-up, a command byte should be sent which sets PD1 = PD0 = 0, so that the device will be in the lowest power mode, powering down between conversions.

Start A Conversion/Write Cycle

A Conversion/Write Cycle begins when the master issues the address byte containing the slave address of the TSC2003, with the eighth bit equal to a 0 (R/$\overline{W}$ = 0), as shown in Figure 10. Once the eighth bit has been received, and the address matches the A1-A0 address input pin setting, the TSC2003 issues an acknowledge.

C3	C2	C1	C0	FUNCTION	INPUT to ADC	X-DRIVERS	Y-DRIVERS	REFERENCE MODE
0	0	0	0	Measure TEMP0	TEMP0	OFF	OFF	Single-Ended
0	0	0	1	Measure V_{BAT1}	V_{BAT1}	OFF	OFF	Single-Ended
0	0	1	0	Measure IN1	IN1	OFF	OFF	Single-Ended
0	0	1	1	Reserved	–	–	–	Single-Ended
0	1	0	0	Measure TEMP1	TEMP1	OFF	OFF	Single-Ended
0	1	0	1	Measure V_{BAT2}	V_{BAT2}	OFF	OFF	Single-Ended
0	1	1	0	Measure IN2	IN2	OFF	OFF	Single-Ended
0	1	1	1	Reserved	–	–	–	Single-Ended
1	0	0	0	Activate X– Drivers	–	ON	OFF	Differential
1	0	0	1	Activate Y– Drivers	–	OFF	ON	Differential
1	0	1	0	Activate Y+, X– Drivers	–	X– ON	Y+ ON	Differential
1	0	1	1	Reserved	–	–	–	Differential
1	1	0	0	Measure X Position	Y+	ON	OFF	Differential
1	1	0	1	Measure Y Position	X+	OFF	ON	Differential
1	1	1	0	Measure Z_1 Position	X+	X– ON	Y+ ON	Differential
1	1	1	1	Measure Z_2 Position	Y–	X– ON	Y+ ON	Differential

TABLE I. Possible Input Configurations.

Once the master receives the acknowledge bit from the TSC2003, the master writes the command byte to the slave (see Figure 11). After the command byte is received by the slave, the slave issues another acknowledge bit. The master then ends the Write Cycle by issuing a repeated START or a STOP condition, as shown in Figure 12.

If the master sends additional command bytes after the initial byte, before sending a STOP or repeated START condition, the TSC2003 will not acknowledge those bytes.

The input multiplexer for the A/D converter has its channel selected when bits C3 through C0 are clocked in. If the selected channel is an X-,Y-, or Z-position measurement, the appropriate drivers will turn on once the acquisition period begins.

When R/$\overline{W}$ = 0, the input sample acquisition period starts on the falling edge of SCL once the C0 bit of the command byte has been latched, and ends when a STOP or repeated START condition has been issued. A/D conversion starts immediately after the acquisition period. The multiplexer inputs to the A/D converter are disabled once the conversion period starts. However, if an X-, Y-, or Z-position is being measured, the respective touch screen drivers remain on during the conversion period. A complete Write Cycle is shown in Figure 12.

Read A Conversion/Read Cycle

For best performance, the I^{2}C bus should remain in an idle state while an A/D conversion is taking place. This prevents digital clock noise from affecting the bit decisions being made by the TSC2003. The master should wait for at least 10µs before attempting to read data from the TSC2003 to realize this best performance. However, the master does not need to wait for a completed conversion before beginning a read from the slave, if full 12-bit performance is not necessary.

Data access begins with the master issuing a START condition followed by the address byte (see Figure 10) with R/$\overline{W}$ = 1. Once the eighth bit has been received, and the address matches, the slave issues an acknowledge. The first byte of serial data will follow (D11-D4, MSB first).

After the first byte has been sent by the slave, it releases the SDA line for the master to issue an acknowledge. The slave responds with the second byte of serial data upon receiving the acknowledge from the master (D3-D0, followed by four 0 bits). The second byte is followed by a NOT acknowledge bit (ACK = 1) from the master to indicate that the last data byte has been received. If the master acknowledges the second data byte, then the data will repeat on subsequent reads with ACKs between bytes. This is true in both 12-bit and 8-bit mode. The master will then issue a STOP condition, which ends the Read Cycle, as shown in Figure 13.

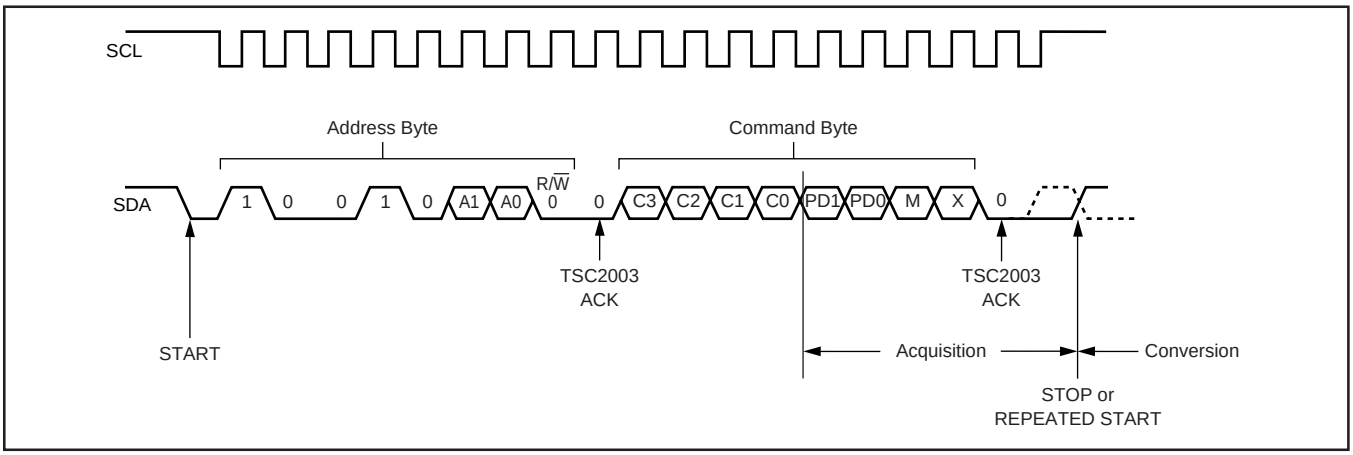


FIGURE 12. Complete I^{2}C Serial Write Transmission.

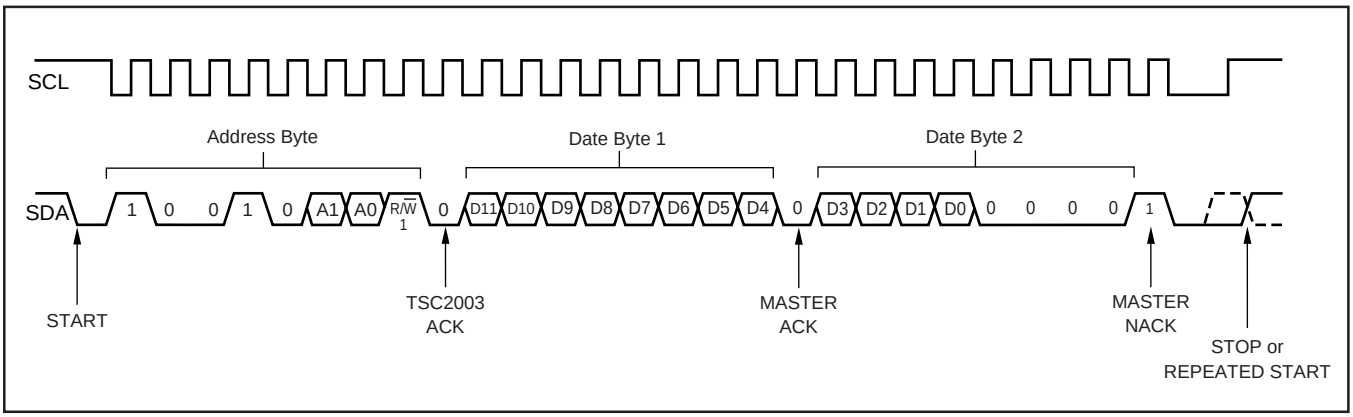


FIGURE 13. Complete I^{2}C Serial Read Transmission.

I²C High-Speed Operation

The TSC2003 can operate with high-speed I²C masters. To do so, the simple resistor pull-up on SCL must be changed to the active pull-up, as recommended in the I²C specification.

The I²C bus will be operating in standard or fast mode initially. Following a START condition, the master will send the code 00001xxx, which the slave will not acknowledge. At this point, the bus is now operating in high-speed mode. The bus will remain in high-speed mode until a STOP condition occurs. Therefore, to maximize throughput only repeated STARTs should be used to separate transactions.

Since the TSC2003 may not have completed a conversion before a read to the part can be requested, the TSC2003 is capable of stretching the clock until the converted data is stored in its internal shift register. Once the data is latched, the TSC2003 will release the clock line so that the master can receive the converted data. A complete high-speed Conversion Cycle is shown in Figure 14.

Data Format

The TSC2003 output data is in Straight Binary format, as shown in Figure 15. This shows the ideal output code for the given input voltage, and does not include the effects of offset, gain, or noise.

8-Bit Conversion

The TSC2003 provides an 8-bit conversion mode (M = 1) that can be used when faster throughput is needed, and the digital result is not as critical (for example, measuring pressure). By switching to the 8-bit mode, a conversion result can be read by transferring only one data byte.

This shortens each conversion by four bits and reduces data transfer time which results in fewer clock cycles and provides lower power consumption.

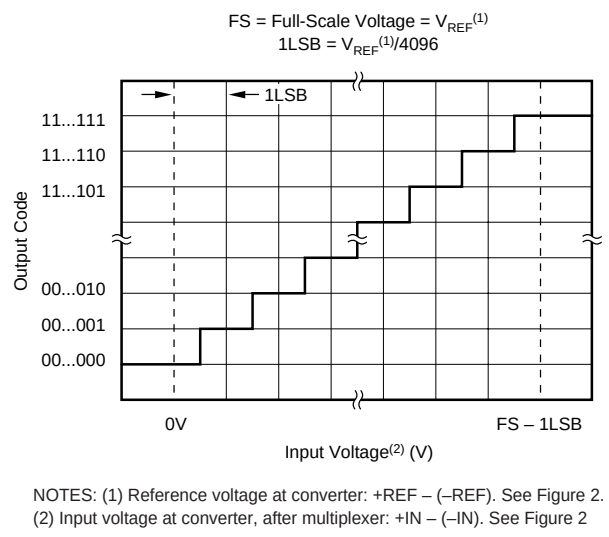


FIGURE 15. Ideal Input Voltages and Output Codes.

LAYOUT

The following layout suggestions should provide optimum performance from the TSC2003. However, many portable applications have conflicting requirements concerning power, cost, size, and weight. In general, most portable devices have fairly “clean” power and grounds because most of the internal components are very low power. This situation would mean less bypassing for the converter's power, and less concern regarding grounding. Still, each situation is unique, and the following suggestions should be reviewed carefully.

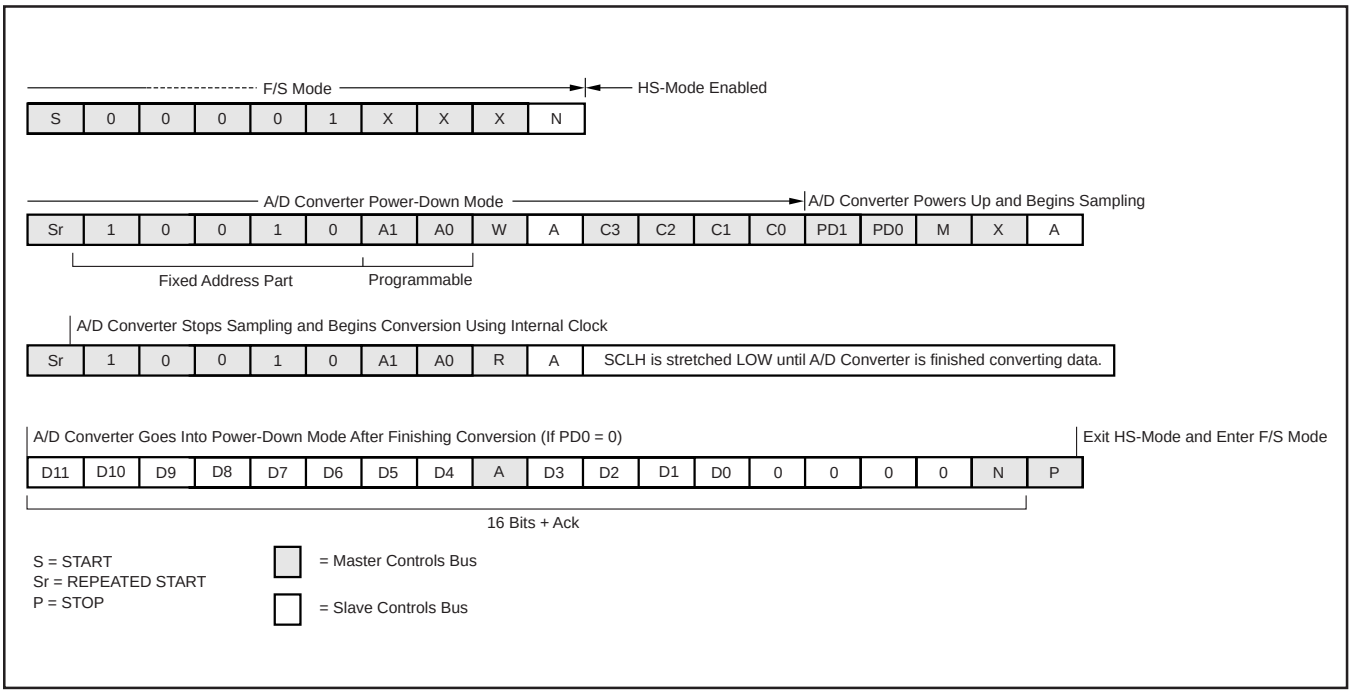


FIGURE 14. High-Speed I²C Mode Conversion Cycle.

For optimum performance, care should be taken with the physical layout of the TSC2003 circuitry. The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Therefore, during any single conversion for an n-bit SAR converter, there are n "windows" in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high-power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. The error can change if the external event changes in time with respect to the SCL input.

With this in mind, power to the TSC2003 should be clean and well bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1µF to 10µF capacitor may also be needed if the impedance of the connection between $+V_{DD}$ and the power supply is high.

A bypass capacitor is generally not needed on the V_{REF} pin because the internal reference is buffered by an internal op amp. If an external reference voltage originates from an op amp, make sure that it can drive any bypass capacitor that is used without oscillation.

The TSC2003 architecture offers no inherent rejection of noise or voltage variation in regards to using an external reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply will appear directly in the digital results. While high-frequency noise can be filtered out, voltage variation due to line frequency (50Hz or 60Hz) can be difficult to remove.

The GND pin should be connected to a clean ground point. In many cases, this will be the "analog" ground. Avoid connections which are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power-supply entry point. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.

In the specific case of use with a resistive touch screen, care should be taken with the connection between the converter and the touch screen. Since resistive touch screens have fairly low resistance, the interconnection should be as short and robust as possible. Longer connections will be a source of error, much like the on-resistance of the internal switches. Likewise, loose connections can be a source of error when the contact resistance changes with flexing or vibrations.

As indicated previously, noise can be a major source of error in touch screen applications (e.g., applications that require a backlit LCD panel). This EMI noise can be coupled through the LCD panel to the touch screen and cause "flickering" of the converted data. Several things can be done to reduce this error, such as utilizing a touch screen with a bottom-side metal layer connected to ground. This will couple the majority of noise to ground. Additionally, filtering capacitors from Y+, Y–, X+, and X– to ground can also help.

$\overline{\text{PENIRQ}}$ OUTPUT

The pen-interrupt output function is shown in Figure 16. By connecting a pull-up resistor to V_{DD} (typically 100kΩ), the $\overline{\text{PENIRQ}}$ output is HIGH. While in the power-down mode, with PD0 = 0, the Y– driver is ON and connected to GND, and the $\overline{\text{PENIRQ}}$ output is connected to the X+ input. When the panel is touched, the X+ input is pulled to ground through the touch screen, and $\overline{\text{PENIRQ}}$ output goes LOW due to the current path through the panel to GND, initiating an interrupt to the processor. During the measurement cycle for X-, Y-, and Z-Position, the X+ input will be disconnected from the $\overline{\text{PENIRQ}}$ pull-down transistor to eliminate any leakage current from the pull-up resistor to flow through the touch screen, thus causing no errors.

In addition to the measurement cycles for X-, Y-, and Z-position, commands which activate the X-drivers, Y-drivers, Y+ and X-drivers without performing a measurement also disconnect the X+ input from the $\overline{\text{PENIRQ}}$ pull-down transistor and disable the pen-interrupt output function regardless of the value of the PD0 bit. Under these conditions, the $\overline{\text{PENIRQ}}$ output will be forced LOW. Furthermore, if the last command byte written to the TSC2003 contains PD0 = 1, the pen-interrupt output function will be disabled and will not be able to detect when the panel is touched. In order to re-enable the pen-interrupt output function under these circumstances, a command byte needs to be written to the TSC2003 with PD0 = 0.

Once the bus master sends the address byte with R/$\overline{\text{W}}$ = 0 (see Figure 10) and the TSC2003 sends an acknowledge, the pen-interrupt function is disabled. If the command which follows the address byte has PD0 = 0, then the pen-interrupt function will be enabled at the end of a conversion. This is approximately 10µs (12-bit mode) or 7µs (8-bit mode) after the TSC2003 receives a STOP/START condition following the reception of a command byte (see Figures 12 and 14 for further details of when the conversion cycle begins).

In both cases listed above, it is recommended that the master processor mask the interrupt which the $\overline{\text{PENIRQ}}$ is associated with whenever the host writes to the TSC2003. This will prevent false triggering of interrupts when the $\overline{\text{PENIRQ}}$ line is disabled in the cases listed above.

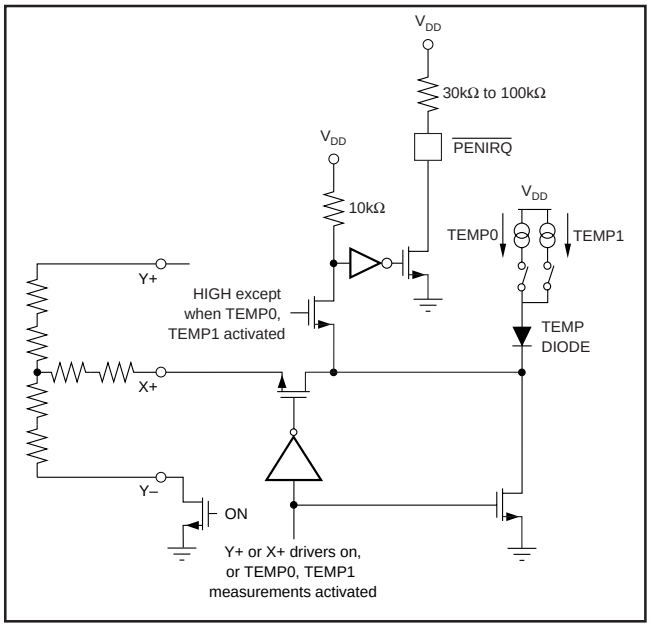


FIGURE 16. $\overline{\text{PENIRQ}}$ Functional Block Diagram.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
6/07	G	6	Timing	Added *Power-On Sequence Timing* section.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
TSC2003IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TSC2003IPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TSC2003IPWR	ACTIVE	TSSOP	PW	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TSC2003IPWRG4	ACTIVE	TSSOP	PW	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TSC2003IZQCR	ACTIVE	BGA MICROSTAR JUNIOR	ZQC	48	2500	Pb-Free (RoHS)	SNAGCU	Level-2-260C-1 YEAR	

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF TSC2003 :

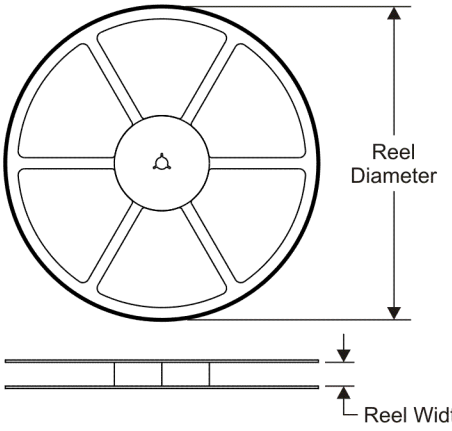
- Automotive: TSC2003-Q1

NOTE: Qualified Version Definitions:

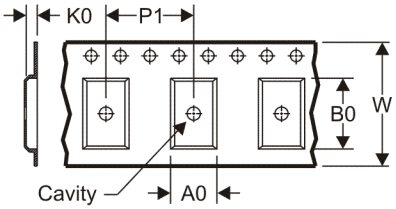
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

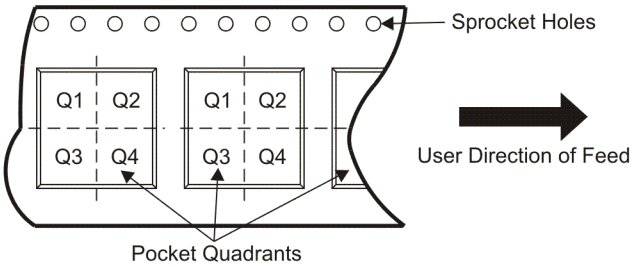


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

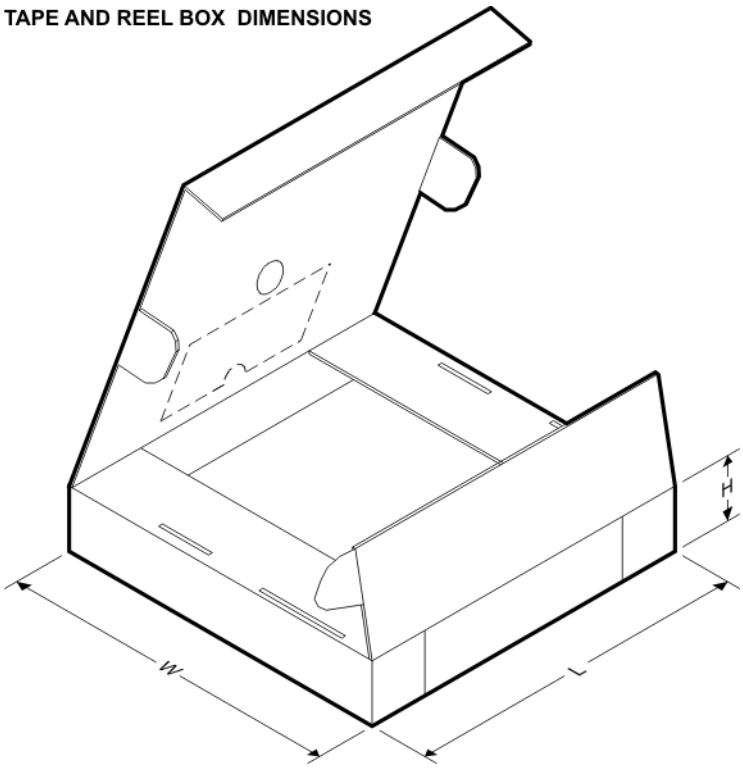
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSC2003IPWR	TSSOP	PW	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TSC2003IZQCR	BGA MICROSTAR JUNIOR	ZQC	48	2500	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q1

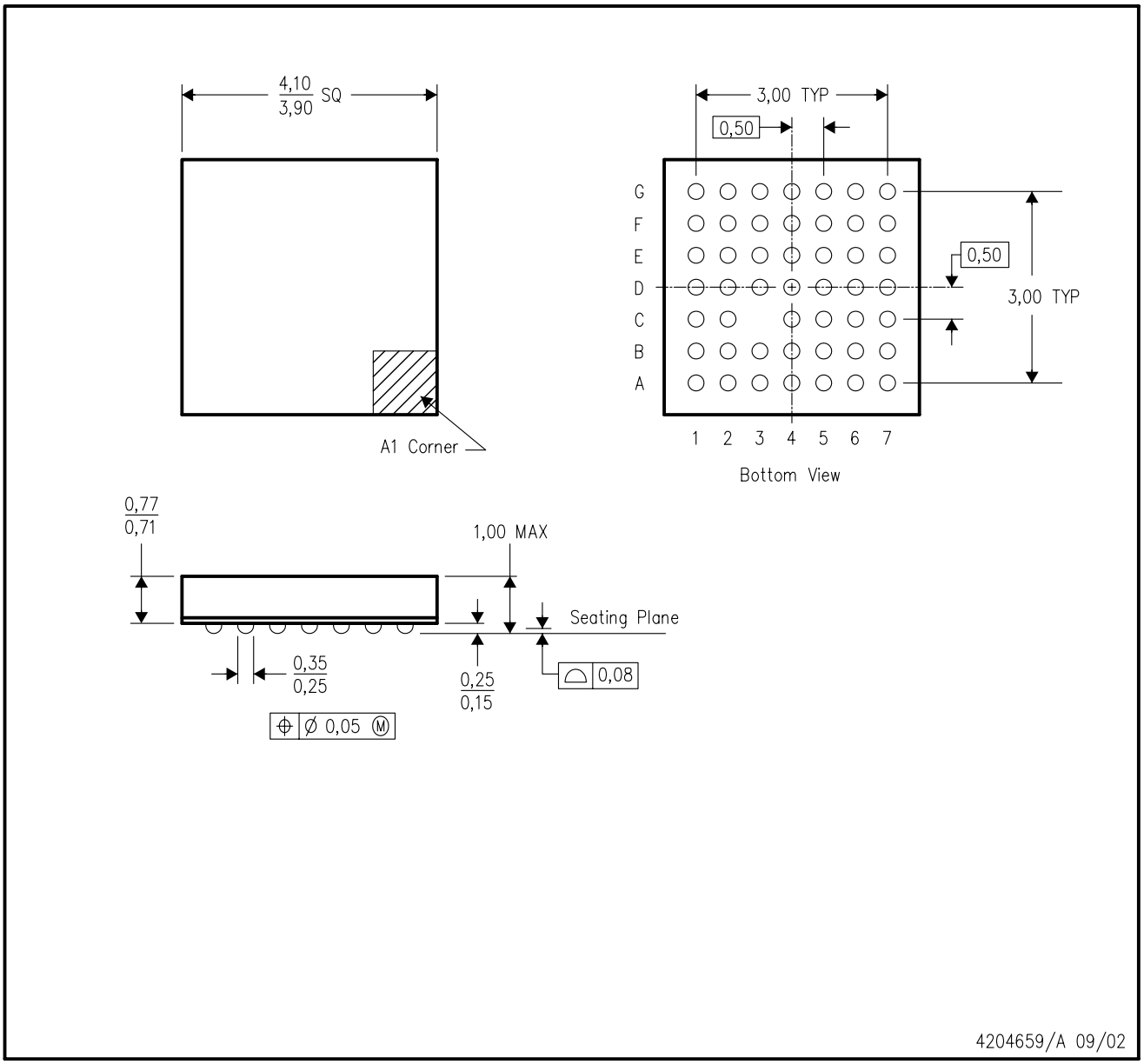
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSC2003IPWR	TSSOP	PW	16	2500	346.0	346.0	29.0
TSC2003IZQCR	BGA MICROSTAR JUNIOR	ZQC	48	2500	340.5	333.0	20.6

ZQC (S–PBGA–N48) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior™ BGA configuration
D. Falls within JEDEC MO–225
E. This package is lead–free.

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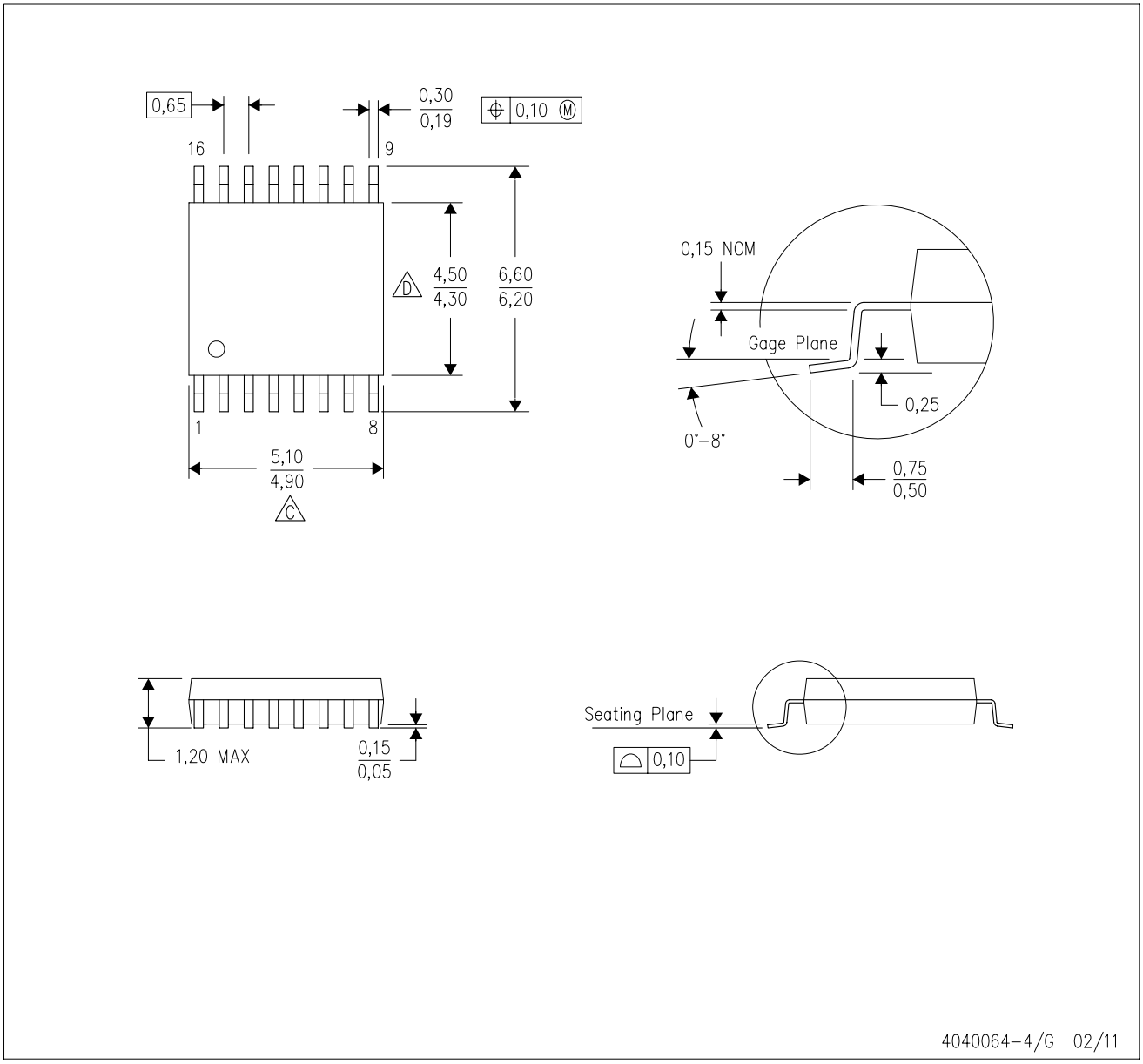
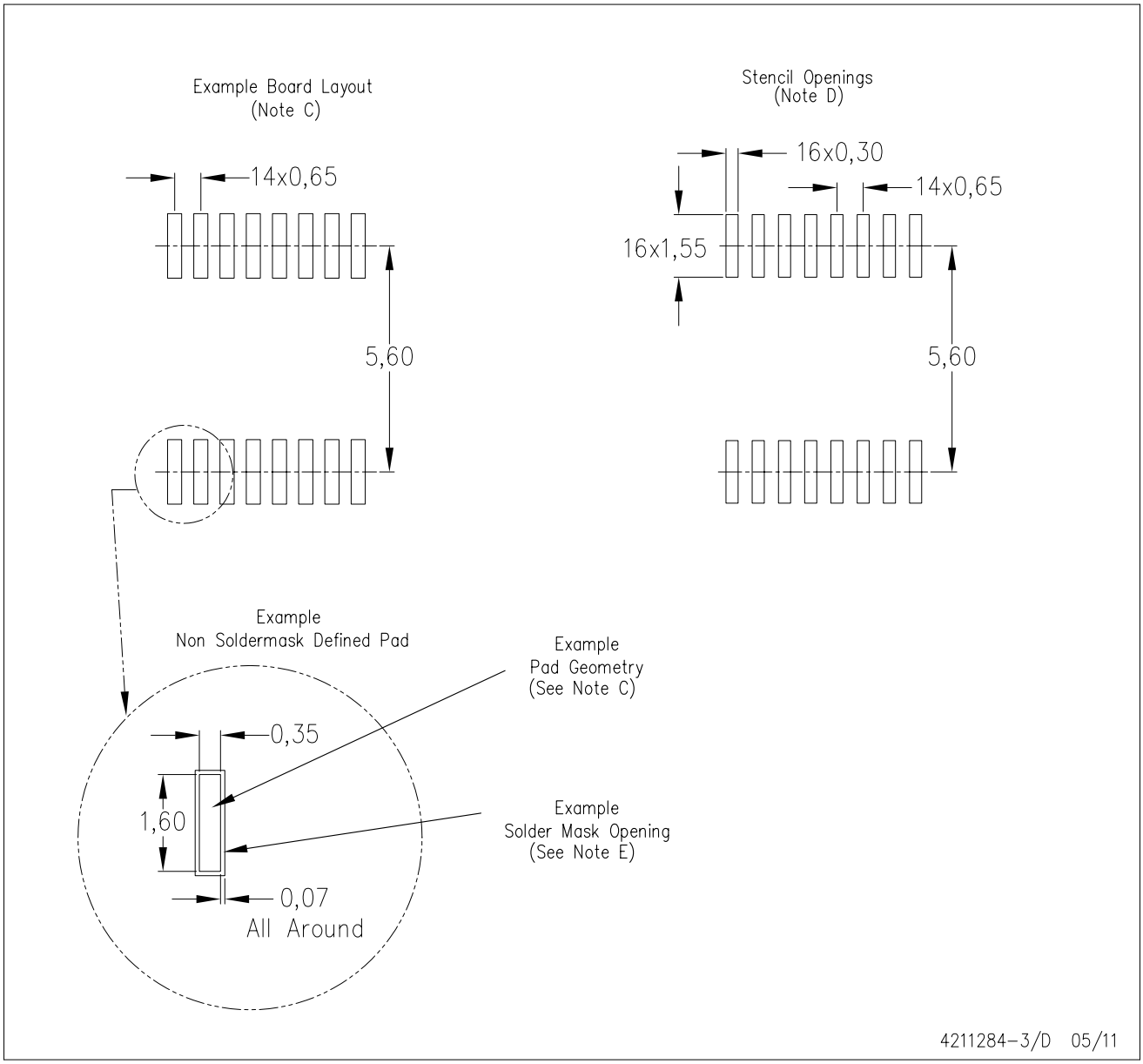
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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