FULLY INTEGRATED 13.56-MHz RFID READER/WRITER IC FOR ISO14443A,B/NFC STANDARDS

Check for Samples: TRF7963A

1 Introduction

1.1 Features

- **Completely Integrated Protocol Handling for ISO14443A/B, NFC Forum Device Types 1 to 4, and FeliCa**
- **Input Voltage Range: 2.7 VDC to 5.5 VDC**
- **Programmable Output Power: +20 dBm (100 mW) or +23 dBm (200 mW)**
- **Programmable I/O Voltage Levels: 1.8 VDC to 5.5 VDC**
- **Programmable System Clock Frequency Output (RF, RF/2, RF/4)**
- **Programmable Modulation Depth**
- **Dual Receiver Architecture With RSSI for Elimination of "Read Holes" and Adjacent Reader System/Ambient In-Band Noise Detection**
- **Programmable Power Modes for Ultra-Low Power System Design (Power Down <0.5 µA)**
- **Parallel or SPI Interface**
- **Integrated Voltage Regulator for Microcontroller Supply**
- **Temperature Range: -25°C to 85°C**
- **32-Pin QFN Package (5 mm x 5 mm) (RHB)**

1.2 Applications

- **Secure Access Control**
- **Digital Door Lock**
- **Contactless Payment Systems**
- **Transport Ticketing**
- **ePassport Reader Systems**

1.3 Description

The TRF7963A is an integrated analog front end and data-framing device for a 13.56-MHz RFID reader/writer system. Built-in programming options make it suitable for a wide range of applications for proximity identification systems.

The reader is configured by selecting the desired protocol in the control registers. Direct access to all control registers allows fine tuning of various reader parameters as needed.

Comprehensive documentation, reference designs, evaluation modules, and TI microcontrollers (based on MSP430™ or ARM™ technology) source code are available.

The TRF7963A is a high-performance 13.56-MHz HF RFID reader IC comprising an integrated analog front end (AFE) and a built-in data framing engine for ISO14443A/B and FeliCa. It supports data rates up to 848 kbps for ISO14443 with all framing and synchronization tasks on board (in ISO Mode, default). The TRF7963A also supports NFC Forum Tag Types 1, 2, 3, and 4 operations (as reader/writer only). This architecture enables the customer to build a complete and cost-effective yet high-performance HF RFID/NFC reader/writer using a low-cost microcontroller (for example, an MSP430).

Other standards and even custom protocols can be implemented by using two of the Direct Modes the device offers. These Direct Modes (0 and 1) allow the user to fully control the analog front end (AFE) and also gain access to the raw subcarrier data or the unframed, but already ISO formatted data and the associated (extracted) clock signal.

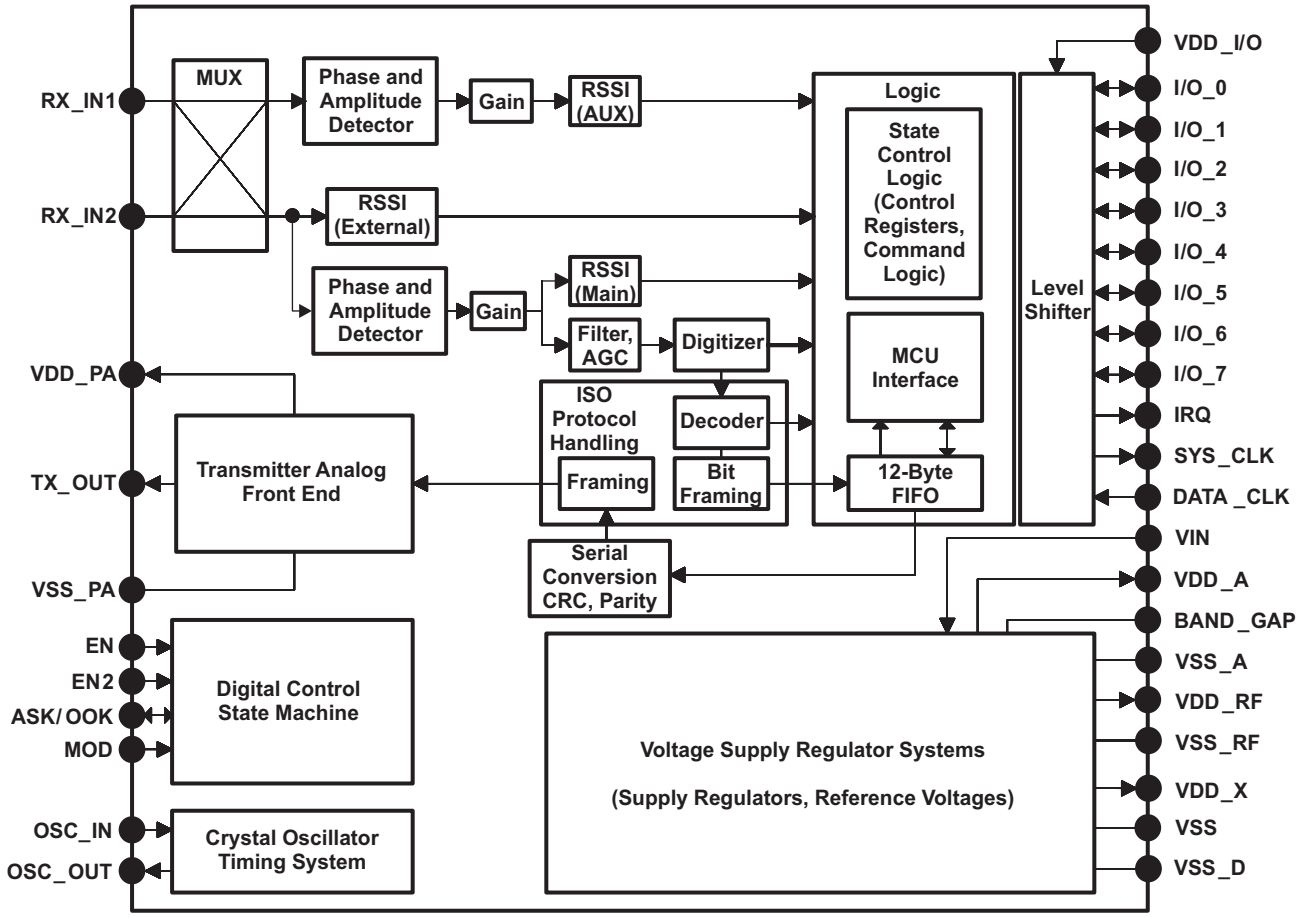


Figure 1-1. Block Diagram

The receiver system has a dual-input receiver architecture. The receivers also include various automatic and manual gain control options. The received input bandwidth can be selected to cover a broad range of input subcarrier signal options.

The received signal strength from transponders, ambient sources or internal levels is available via the RSSI register. The receiver output is selectable among a digitized subcarrier signal and any of the integrated subcarrier decoders. The selected subcarrier decoder delivers the data bit stream and the data clock as outputs.

The TRF7963A includes a receiver framing engine. This receiver framing engine performs the CRC and/or parity check, removes the EOF and SOF settings, and organizes the data in bytes for ISO14443A/B and NFC Forum protocols. Framed data is then accessible to the microcontroller (MCU) via a 12-byte FIFO register.

A parallel or serial interface (SPI) can be used for the communication between the MCU and the TRF7963A reader. When the built-in hardware encoders and decoders are used, transmit and receive functions use a 12-byte FIFO register. For direct transmit or receive functions, the encoders or decoders can be bypassed so the MCU can process the data in real time. The TRF7963A supports data communication levels from 1.8 V to 5.5 V for the MCU I/O interface. The transmitter has selectable output power levels of 100 mW (+20 dBm) or 200 mW (+23 dBm) equivalent into a 50-Ω load when using a 5-V supply.

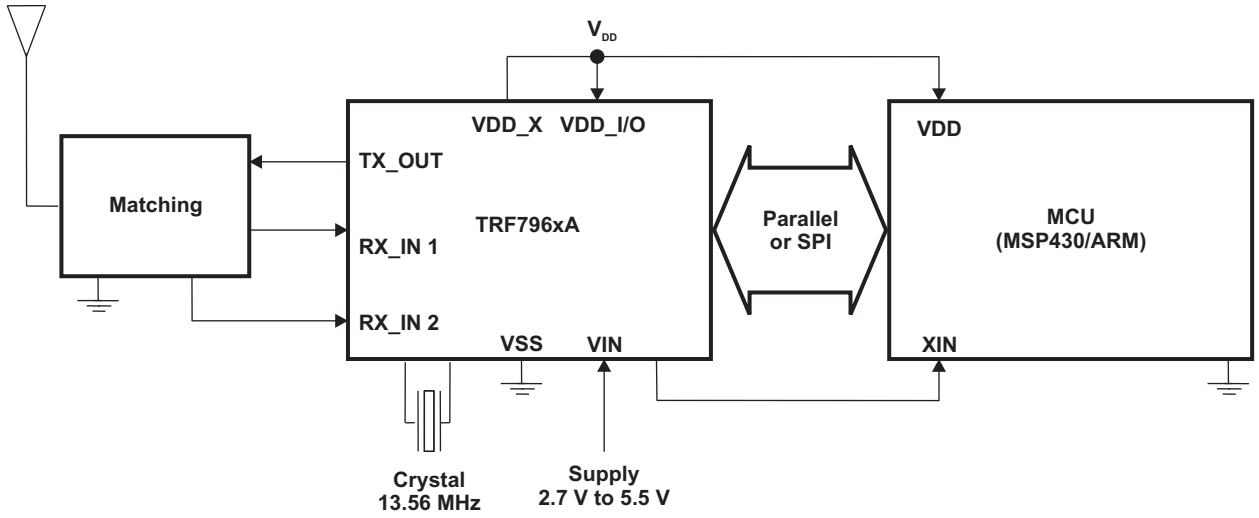


Figure 1-2. Application Block Diagram

The transmitter supports OOK and ASK modulation with selectable modulation depth. The TRF7963A includes a data transmission engine that supports modified Miller encoding for ISO14443A/B and FeliCa. Included with the transmit data coding is the automatic generation of Start Of Frame (SOF), End Of Frame (EOF), Cyclic Redundancy Check (CRC), and parity bits. Several integrated voltage regulators ensure a proper power-supply noise rejection for the complete reader system. The built-in programmable auxiliary voltage regulator VDD_X (pin 32) delivers up to 20 mA to supply a microcontroller and additional external circuits within the reader system.

Table 1-1. Supported Protocols

Device	Supported Protocols				
	ISO14443A/B				NFC Forum Types 1 to 4
	106 kbps	212 kbps	424 kbps	848 kbps	
TRF7963A	✓	✓	✓	✓	✓

1.4 Ordering Information

Packaged Devices(1)	Package Type(2)	Transport Media	Quantity
TRF7963ARHBT	RHB-32	Tape and Reel	250
TRF7963ARHBR			3000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

2 Physical Characteristics

2.1 Device Pinout

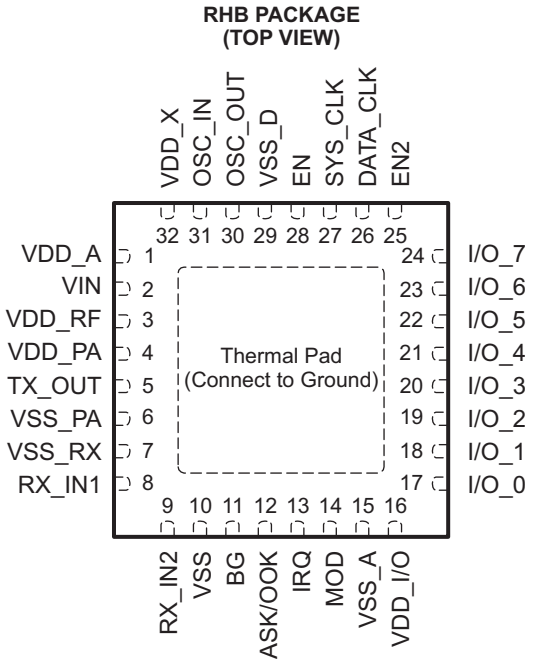


Figure 2-1. TRF7963A Pin Assignment

2.2 Terminal Functions

Table 2-1. Terminal Functions

Terminal		Type (1)	Description
Name	No.		
VDD_A	1	OUT	Internal regulated supply (2.7 V to 3.4 V) for analog circuitry
VIN	2	SUP	External supply input to chip (2.7 V to 5.5 V)
VDD_RF	3	OUT	Internal regulated supply (2.7 V to 5 V); normally connected to VDD_PA (pin 4)
VDD_PA	4	INP	Supply for PA; normally connected externally to VDD_RF (pin 3)
TX_OUT	5	OUT	RF output (selectable output power: 100 mW or 200 mW, with V_{DD} = 5 V)
VSS_PA	6	SUP	Negative supply for PA; normally connected to circuit ground
VSS_RX	7	SUP	Negative supply for receive inputs; normally connected to circuit ground
RX_IN1	8	INP	Main receive input
RX_IN2	9	INP	Auxiliary receive input
VSS	10	SUP	Chip substrate ground
BAND_GAP	11	OUT	Bandgap voltage (V_{BG} = 1.6 V); internal analog voltage reference
ASK/OOK	12	BID	Selection between ASK and OOK modulation (0 = ASK, 1 = OOK) for Direct Mode 0 and 1. It can be configured as an output to provide the received analog signal output.
IRQ	13	OUT	Interrupt request
MOD	14	INP	External data modulation input for Direct Mode 0 or 1
		OUT	Subcarrier digital data output (see register 0x1A and 0x1B definitions)
VSS_A	15	SUP	Negative supply for internal analog circuits; connected to GND
VDD_I/O	16	INP	Supply for I/O communications (1.8 V to VIN) level shifter. VIN should be never exceeded.

(1) SUP = Supply, INP = Input, BID = Bidirectional, OUT = Output

Table 2-1. Terminal Functions (continued)

Terminal		Type (1)	Description
Name	No.		
I/O_0	17	BID	I/O pin for parallel communication
I/O_1	18	BID	I/O pin for parallel communication
I/O_2	19	BID	I/O pin for parallel communication
I/O_3	20	BID	I/O pin for parallel communication
I/O_4	21	BID	I/O pin for parallel communication Slave select signal in SPI mode
I/O_5	22	BID	I/O pin for parallel communication Data clock output in Direct Mode 1
I/O_6	23	BID	I/O pin for parallel communication MISO for serial communication (SPI) Serial bit data output in Direct Mode 1 or subcarrier signal in Direct Mode 0
I/O_7	24	BID	I/O pin for parallel communication. MOSI for serial communication (SPI)
EN2	25	INP	Selection of power down mode. If EN2 is connected to VIN, then VDD_X is active during power down mode 2 (for example, to supply the MCU).
DATA_CLK	26	INP	Data clock input for MCU communication (parallel and serial)
SYS_CLK	27	OUT	If EN = 1 (EN2 = don't care) the system clock for the MCU is configured with register 0x09 (off, 3.39 MHz, 6.78 MHz, or 13.56 MHz). If EN = 0 and EN2 = 1, the system clock is set to 60 kHz
EN	28	INP	Chip enable input (If EN = 0, then the chip is in sleep or power-down mode)
VSS_D	29	SUP	Negative supply for internal digital circuits
OSC_OUT	30	OUT	Crystal or oscillator output
OSC_IN	31	INP	Crystal or oscillator input
VDD_X	32	OUT	Internally regulated supply (2.7 V to 3.4 V) for digital circuit and external devices (for example, an MCU)
PAD	PAD	SUP	Chip substrate ground

3 Electrical Characteristics

3.1 Absolute Maximum Ratings (1)

over operating free-air temperature range (unless otherwise noted) (2)

VIN	Input voltage range		-0.3 V to 6 V
I_{IN}	Maximum current		150 mA
ESD	Electrostatic discharge rating	Human-body model (HBM)	2 kV
		Charged-device model (CDM)	500 V
		Machine model (MM)	200 V
T_J	Maximum operating virtual junction temperature (3)	Any condition	140°C
		Continuous operation, long-term reliability	125°C
T_{STG}	Storage temperature range		-55°C to 150°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Operating Conditions are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to substrate ground terminal VSS.
(3) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

3.2 Dissipation Ratings

PACKAGE	θ_{JC}	θ_{JA} (1)	POWER RATING (2)	
			$T_A \le 25°C$	$T_A \le 85°C$
RHB (32)	31°C/W	36.4°C/W	2.7 W	1.1 W

(1) This data was taken using the JEDEC standard high-K test PCB.
(2) Power rating is determined with a junction temperature of 125°C. This is the point where distortion starts to increase substantially. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long-term reliability.

3.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
VIN	Operating input voltage	2.7	5	5.5	V
T_A	Operating ambient temperature	-25	25	85	°C
T_J	Operating virtual junction temperature	-25	25	125	°C

3.4 Electrical Characteristics

Typical operating conditions are T_A = 25°C, VIN = 5 V, full-power mode (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
I_{PD1}	Supply current in Power Down Mode 1	All building blocks disabled, including supply-voltage regulators; measured after 500-ms settling time (EN = 0, EN2 = 0)		<0.5	5	µA
I_{PD2}	Supply current in Power Down Mode 2 (Sleep Mode)	The SYS_CLK generator and VDD_X remain active to support external circuitry, measured after 100-ms settling time (EN = 0, EN2 = 1)		120	200	µA
I_{STBY}	Supply current in stand-by mode	Oscillator running, supply-voltage regulators in low-consumption mode (EN = 1, EN2 = x)		1.9	3.5	mA
I_{ON1}	Supply current without antenna driver current	Oscillator, regulators, RX, and AGC are active, TX is off		10.5	14	mA
I_{ON2}	Supply current – TX (half power)	Oscillator, regulators, RX, AGC, and TX active, P_{OUT} = 100 mW		70	78	mA
I_{ON3}	Supply current – TX (full power)	Oscillator, regulators, RX, AGC, and TX active, P_{OUT} = 200 mW		130	170	mA
V_{POR}	Power-on reset voltage	Input voltage at VIN	1.4	2	2.6	V
V_{BG}	Bandgap voltage (pin 11)	Internal analog reference voltage	1.5	1.6	1.7	V
VDD_A	Regulated output voltage for analog circuitry (pin 1)	VIN = 5 V	3.1	3.5	3.8	V
VDD_X	Regulated supply for external circuitry	Output voltage pin 32, VIN = 5 V	3.1	3.4	3.8	V
I_{VDD_Xmax}	Maximum output current of VDD_X	Output current pin 32, VIN = 5 V			20	mA
R_{RFOUT}	Antenna driver output resistance (1)	Half power mode, VIN = 2.7 V to 5.5 V		8	12	Ω
		Full power mode, VIN = 2.7 V to 5.5 V		4	6	Ω
R_{RFIN}	RX_IN1 and RX_IN2 input resistance		4	10	20	kΩ
V_{RF_INmax}	Maximum RF input voltage at RX_IN1, RX_IN2	V_{RF_INmax} should not exceed VIN		3.5		V_{pp}
V_{RF_INmin}	Minimum RF input voltage at RX_IN1, RX_IN2 (input sensitivity) (2)	$f_{SUBCARRIER}$ = 424 kHz		1.4	2.5	mV_{pp}
		$f_{SUBCARRIER}$ = 848 kHz		2.1	3	mV_{pp}
f_{SYS_CLK}	SYS_CLK frequency	In power mode 2, EN = 0, EN2 = 1	25	60	120	kHz
f_C	Carrier frequency	Defined by external crystal		13.56		MHz
$t_{CRYSTAL}$	Crystal run-in time	Time until oscillator stable bit is set (register 0x0F) (3)		5		ms
f_{D_CLKmax}	Maximum DATA_CLK frequency (4)	Depends on capacitive load on the I/O lines, recommendation is 2 MHz (4)	2	8	10	MHz
V_{IL}	Input voltage, logic low	I/O lines, IRQ, SYS_CLK, DATA_CLK, EN, EN2			0.2 × VDD_I/O	V
V_{IH}	Input voltage threshold, logic high	I/O lines, IRQ, SYS_CLK, DATA_CLK, EN, EN2			0.8 × VDD_I/O	V
R_{OUT}	Output resistance, I/O_0 to I/O_7			500	800	Ω
R_{SYS_CLK}	Output resistance R_{SYS_CLK}			200	400	Ω

(1) Antenna driver output resistance
(2) Measured with subcarrier signal at RX_IN1/2 and measured the digital output at MOD pin with register 0x1A bit 6 = 1
(3) Depending on the crystal parameters and components
(4) Recommended DATA_CLK speed is 2 MHz; higher data clock depends on the capacitive load. Maximum SPI clock speed should not exceed 10 MHz. This clock speed is acceptable only when external capacitive load is less than 30 pF. MISO driver has a typical output resistance of 400 Ω (12-ns time constant when 30-pF load is used).

3.5 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
$t_{LO/HI}$	DATA_CLK time, high or low (one half of DATA_CLK at 50% duty cycle)	Depends on capacitive load on the I/O lines (1)	50	62.5	250	ns
$t_{STE,LEAD}$	Slave select lead time, slave select low to clock			200		ns
$t_{STE,LAG}$	Slave select lag time, last clock to slave select high			200		ns
$t_{SU,SI}$	MOSI input data setup time		15			ns
$t_{HD,SI}$	MOSI input data hold time		15			ns
$t_{SU,SO}$	MISO input data setup time		15			ns
$t_{HD,SO}$	MISO input data hold time		15			ns
$t_{VALID,SO}$	MISO output data valid time	DATA_CLK edge to MISO valid, C_L = <30 pF	30	50	75	ns

(1) Recommended DATA_CLK speed is 2 MHz; higher data clock depends on the capacitive load. Maximum SPI clock speed should not exceed 10 MHz. This clock speed is acceptable only when external capacitive load is less than 30 pF. MISO driver has a typical output resistance of 400 Ω (12-ns time constant when 30-pF load is used).

4 Application Schematic and Layout Considerations

4.1 TRF7963A Reader System Using Parallel Microcontroller Interface

4.1.1 General Application Considerations

Figure 4-1 shows the most flexible TRF7963A application. Due to the low clock frequency on the DATA_CLK line, the parallel interface is the most robust way to connect the TRF7963A with the MCU.

This schematic shows matching to a 50-Ω port, which allows connection to a properly matched 50-Ω antenna circuit or RF measurement equipment (for example, a spectrum analyzer or power meter).

4.1.2 Schematic

Figure 4-1 shows a sample application schematic with a parallel interface to the MCU.

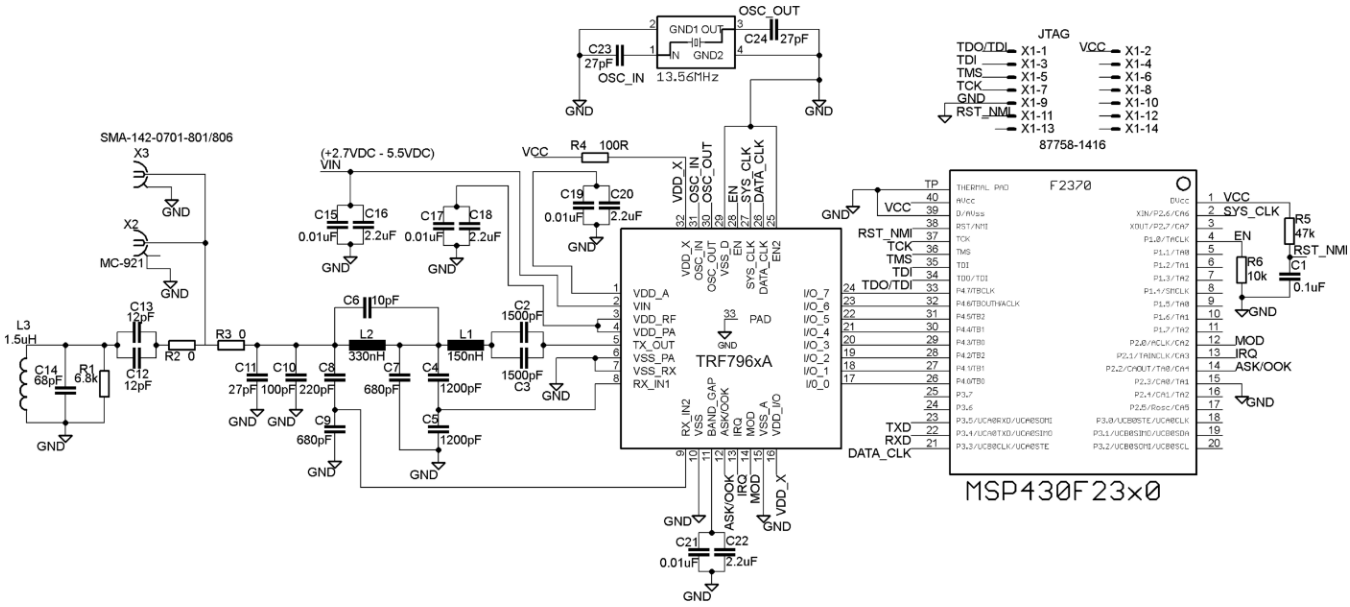


Figure 4-1. Application Schematic, Parallel MCU Interface

The MSP430F2370 (32kB flash, 2kB RAM) is shown in Figure 4-1. Minimum MCU requirements depend on application requirements and coding style. If only one ISO protocol and/or a limited command set of a protocol must be supported, MCU flash and RAM requirements can be significantly reduced. For example, current reference firmware for ISO14443A/B (with host interface) is approximately 8kB, using 1kB RAM. An MCU that is capable of running a GPIO at 13.56 MHz is required for Direct Mode 0 operations with nonstandard transponders.

4.2 TRF7963A Reader System Using SPI With SS Mode

4.2.1 General Application Considerations

Figure 4-2 shows the TRF7963A application schematic using the Serial Port Interface (SPI). Short SPI lines, proper isolation to radio frequency lines, and a proper ground area are essential to avoid interference. The recommended clock frequency on the DATA_CLK line is 2 MHz.

This schematic shows matching to a 50-Ω port, which allows connection to a properly matched 50-Ω antenna circuit or RF measurement equipment (for example, a spectrum analyzer or power meter).

4.2.2 Schematic

Figure 4-2 shows a sample application schematic with a serial interface to the MCU.

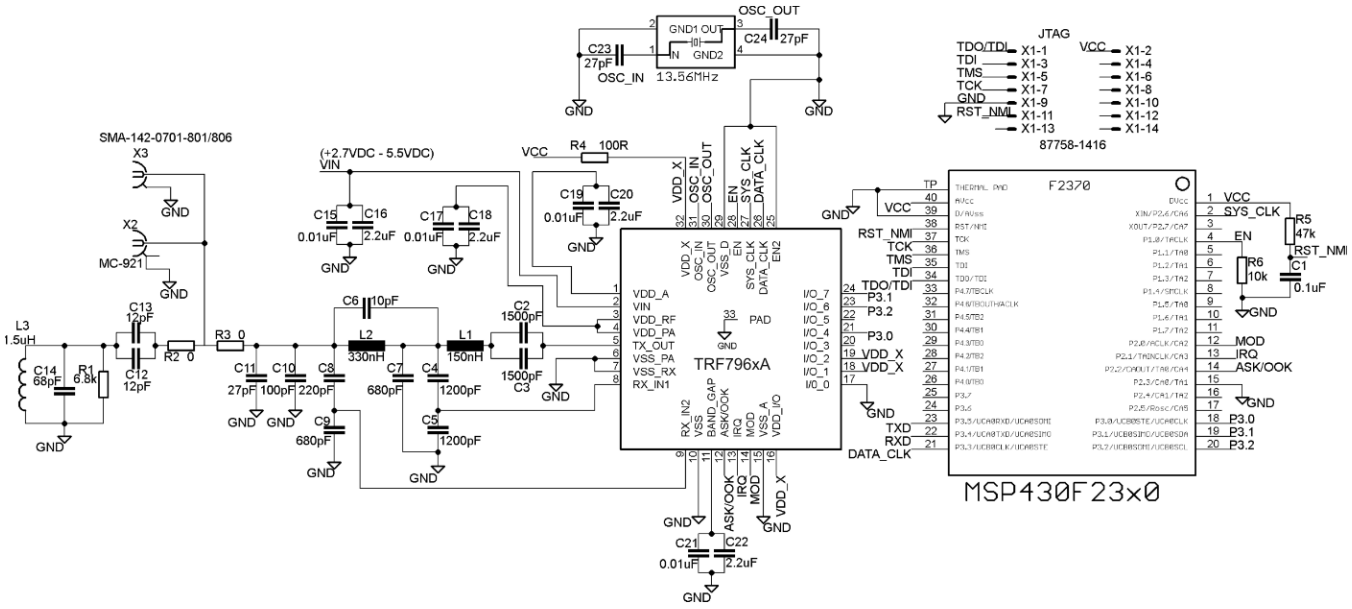


Figure 4-2. Application Schematic, SPI With SS Mode MCU Interface

The MSP430F2370 (32kB flash, 2kB RAM) is shown in Figure 4-2. Minimum MCU requirements depend on application requirements and coding style. If only one ISO protocol and/or a limited command set of a protocol must be supported, MCU flash and RAM requirements can be significantly reduced. For example, current reference firmware for ISO14443A/B (with host interface) is approximately 8kB, using 1kB RAM. An MCU that is capable of running a GPIO at 13.56 MHz is required for Direct Mode 0 operations with nonstandard transponders.

5 Detailed System Description

5.1 System Block Diagram

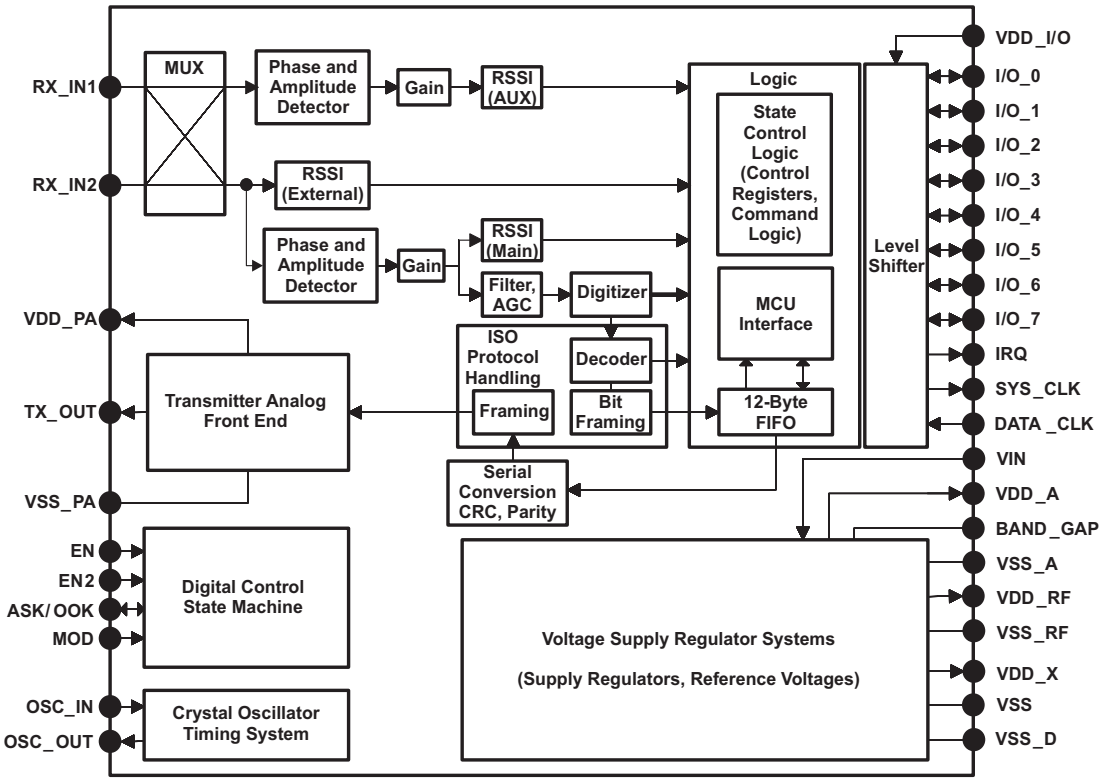


Figure 5-1. System Block Diagram

5.2 Power Supplies

The TRF7963A positive supply input VIN (pin 2) sources three internal regulators with output voltages VDD_RF, VDD_A, and VDD_X. All regulators require external bypass capacitors for supply noise filtering and must be connected as indicated in reference schematics. These regulators provide a high power supply reject ratio (PSRR) as required for RFID reader systems. All regulators are supplied via VIN (pin 2).

The regulators are not independent and have common control bits in register 0x0B for output voltage setting. The regulators can be configured to operate in either automatic or manual mode (register 0x0B, bit 7). The automatic regulator setting mode ensures an optimal compromise between PSRR and the highest possible supply voltage for RF output (to ensure maximum RF power output). The manual mode allows the user to manually configure the regulator settings.

5.3 Supply Arrangements

Regulator Supply Input: VIN

The positive supply at VIN (pin 2) has an input voltage range of 2.7 V to 5.5 V. VIN provides the supply input sources for three internal regulators with the output voltages VDD_RF, VDD_A, and VDD_X. External bypass capacitors for supply noise filtering must be used (per reference schematics).

NOTE

VIN must be the highest voltage supplied to the TRF7963A.

RF Power Amplifier Regulator: VDD_RF

The VDD_RF (pin 3) regulator is supplying the RF power amplifier. The voltage regulator can be set for either 5V or 3V operation. External bypass capacitors for supply noise filtering must be used (per reference schematics). When configured for 5V manual-operation, the VDD_RF output voltage can be set from 4.3 V to 5 V in 100-mV steps. In 3-V manual operation, the output can be programmed from 2.7 V to 3.4 V in 100-mV steps (see Table 5-2). The maximum output current capability for 5-V operation is 150 mA and for 3-V operation is 100 mA.

Analog Supply Regulator: VDD_A

Regulator VDD_A (pin 1) supplies the analog circuits of the device. The output voltage setting depends on the input voltage and can be set for 5-V and 3-V operation. When configured for 5-V manual operation, the output voltage is fixed at 3.4 V. External bypass capacitors for supply noise filtering must be used (per reference schematics). When configured for 3-V manual operation, the VDD_A output can be set from 2.7 V to 3.4 V in 100-mV steps (see Table 5-2).

NOTE

The configuration of VDD_A and VDD_X regulators are not independent from each other. The VDD_A output current should not exceed 20 mA.

Digital Supply Regulator: VDD_X

The Digital Supply Regulator VDD_X (pin 32) provides the power for the internal digital building blocks and can also be used to supply external electronics within the reader system. When configured for 3-V operation, the output voltage can be set from 2.7 to 3.4 V in 100-mV steps. External bypass capacitors for supply noise filtering must be used (per reference schematics).

NOTE

The configuration of the VDD_A and VDD_X regulators are not independent from each other. The VDD_X output current should not exceed 20 mA.

The RF power amplifier regulator (VDD_RF), analog supply regulator (VDD_A), and digital supply regulator (VDD_X) can be configured to operate in either automatic or manual mode described in Table 5-1. The automatic regulator setting mode ensures an optimal compromise between PSRR and the highest possible supply voltage to ensure maximum RF power output.

By default, the regulators are set in automatic regulator setting mode. In this mode, the regulators are automatically set every time the system is activated by setting EN input High or each time the automatic regulator setting bit, B7 in register 0x0B is set to a 1. The action is started on the 0 to 1 transition. This means that, if the user wants to re-run the automatic setting from a state in which the automatic setting bit is already high, the automatic setting bit (B7 in register 0x0B) should be changed: 1-0-1.

By default, the regulator setting algorithm sets the regulator outputs to a "Delta Voltage" of 250 mV below VIN, but not higher than 5 V for VDD_RF and 3.4 V for VDD_A and VDD_A. The "Delta Voltage" in automatic regulator mode can be increased up to 400 mV (for more details, see bits B0 to B2 in register 0x0B).

Power Amplifier Supply: VDD_PA

The power amplifier of the TRF7963A is supplied through VDD_PA (pin 4). The positive supply pin for the RF power amplifier is externally connected to the regulator output VDD_RF (pin 3).

I/O Level Shifter Supply: VDD_I/O

The TRF7963A has a separate supply input VDD_I/O (pin 16) for the build in I/O level shifter. The supported input voltage ranges from 1.8 V to VIN, however not exceeding 5.5 V. Pin 16 is used to supply the I/O interface pins (I/O_0 to I/O_7), IRQ, SYS_CLK, and DATA_CLK pins of the reader. In typical applications, VDD_I/O is directly connected to VDD_X while VDD_X also supplies the MCU. This ensures that the I/O signal levels of the MCU match with the logic levels of the TRF7963A.

Negative Supply Connections: VSS, VSS_RX, VSS_A, VSS_PA

The negative supply connections VSS_X of each functional block are all externally connected to GND.

The substrate connection is VSS (pin 10), the analog negative supply is VSS_A (pin 15), the logic negative supply is VSS_D (pin 29), the RF output stage negative supply is VSS_PA (pin 6), and the negative supply for the RF receiver VSS_RX (pin 7).

5.4 Supply Regulator Settings

The input supply voltage mode of the reader must be selected. This is done in the Chip Status Control register (0x00). Bit 0 in register 0x00 selects between 5-V or 3-V input supply voltage. The default configuration is 5 V, which reflects an operating supply voltage range of 4.3 V to 5.5 V. If the supply voltage is below 4.3 V, the 3-V configuration should be used.

The various regulators can be configured to operate in automatic or manual mode. This is done in the

Regulator and I/O Control register (0x0B) as shown in Table 5-1.

Table 5-1. Supply Regulator Setting: 5-V System

Register Address	Option Bits Setting in Regulator Control Register(1)								Comments
	B7	B6	B5	B4	B3	B2	B1	B0	
Automatic Mode (default)									
0B	1	x	x	x	x	x	1	1	Automatic regulator setting 250-mV difference
0B	1	x	x	x	x	x	1	0	Automatic regulator setting 350-mV difference
0B	1	x	x	x	x	x	0	0	Automatic regulator setting 400-mV difference
Manual Mode									
0B	0	x	x	x	x	1	1	1	VDD_RF = 5 V, VDD_A = 3.4 V, VDD_X = 3.4 V
0B	0	x	x	x	x	1	1	0	VDD_RF = 4.9 V, VDD_A = 3.4 V, VDD_X = 3.4 V
0B	0	x	x	x	x	1	0	1	VDD_RF = 4.8 V, VDD_A = 3.4 V, VDD_X = 3.4 V
0B	0	x	x	x	x	1	0	0	VDD_RF = 4.7 V, VDD_A = 3.4 V, VDD_X = 3.4 V
0B	0	x	x	x	x	0	1	1	VDD_RF = 4.6 V, VDD_A = 3.4 V, VDD_X = 3.4 V
0B	0	x	x	x	x	0	1	0	VDD_RF = 4.5 V, VDD_A = 3.4 V, VDD_X = 3.4 V
0B	0	x	x	x	x	0	0	1	VDD_RF = 4.4 V, VDD_A = 3.4 V, VDD_X = 3.4 V
0B	0	x	x	x	x	0	0	0	VDD_RF = 4.3 V, VDD_A = 3.4 V, VDD_X = 3.4 V

(1) x = don't care

Table 5-2. Supply Regulator Setting: 3-V System

Register Address	Option Bits Setting in Regulator Control Register (1)								Comments
	B7	B6	B5	B4	B3	B2	B1	B0	
Automatic Mode (default)									
0B	1	x	x	x	x	x	1	1	Automatic regulator setting 250-mV difference
0B	1	x	x	x	x	x	1	0	Automatic regulator setting 350-mV difference
0B	1	x	x	x	x	x	0	0	Automatic regulator setting 400-mV difference
Manual Mode									
0B	0	x	x	x	x	1	1	1	VDD_RF = 3.4 V, VDD_A = 3.4 V, VDD_X = 3.4 V
0B	0	x	x	x	x	1	1	0	VDD_RF = 3.3 V, VDD_A = 3.3 V, VDD_X = 3.3 V
0B	0	x	x	x	x	1	0	1	VDD_RF = 3.2 V, VDD_A = 3.2 V, VDD_X = 3.2 V
0B	0	x	x	x	x	1	0	0	VDD_RF = 3.1 V, VDD_A = 3.1 V, VDD_X = 3.1 V
0B	0	x	x	x	x	0	1	1	VDD_RF = 3.0 V, VDD_A = 3.0 V, VDD_X = 3.0 V
0B	0	x	x	x	x	0	1	0	VDD_RF = 2.9 V, VDD_A = 2.9 V, VDD_X = 2.9 V
0B	0	x	x	x	x	0	0	1	VDD_RF = 2.8 V, VDD_A = 2.8 V, VDD_X = 2.8 V
0B	0	x	x	x	x	0	0	0	VDD_RF = 2.7 V, VDD_A = 2.7 V, VDD_X = 2.7 V

(1) x = don't care

The regulator configuration function adjusts the regulator outputs by default to 250 mV below VIN level, but not higher than 5 V for VDD_RF, 3.4 V for VDD_A and VDD_X. This ensures the highest possible supply voltage for the RF output stage while maintaining an adequate PSRR (power supply rejection ratio).

To further improve the PSRR, it is possible to increase the target voltage difference across VDD_X and VDD_A from its default to 350 mV or even 400 mV (for details, see Regulator and I/O Control register 0x0B definition and Table 5-2.)

5.5 Power Modes

The chip has several power states, which are controlled by two input pins (EN and EN2) and several bits in the Chip Status Control register (0x00).

Table 5-3 is a consolidated table showing the configuration for the different power modes when using a 5-V or 3-V system supply. The main reader enable signal is pin EN. When EN is set high, all of the reader regulators are enabled, the 13.56-MHz oscillator is running and the SYS_CLK (output clock for external microcontroller) is also available.

The Regulator Control register settings shown are for optimized power out. The automatic setting (normally 0x87) is optimized for best PSRR and noise reduction.

Table 5-3. Power Modes (1)

Mode	EN2	EN	Chip Status Control Register (0x00)	Regulator Control Register (0x0B)	Trans-mitter	Receiver	SYS_CLK (13.56 MHz)	SYS_CLK (60 kHz)	VDD_X	Typical Current (mA)	Typical Power Out (dBm)	Time (From Previous State)
Mode 4 (Full Power) 5 VDC	x	1	21	07	On	On	On	x	On	130	23	~20-25 µs
Mode 4 (Full Power) 3.3 VDC	x	1	20	07	On	On	On	x	On	67	18	
Mode 3 (Half Power) 5 VDC	x	1	31	07	On	On	On	x	On	70	20	~20-25 µs
Mode 3 (Half Power) 3.3 VDC	x	1	30	07	On	On	On	x	On	53	15	

(1) x = don't care

Table 5-3. Power Modes[(1)] (continued)

Mode	EN2	EN	Chip Status Control Register (0x00)	Regulator Control Register (0x0B)	Trans-mitter	Receiver	SYS_CLK (13.56 MHz)	SYS_CLK (60 kHz)	VDD_X	Typical Current (mA)	Typical Power Out (dBm)	Time (From Previous State)
Mode 2 5 VDC	x	1	03	07	Off	On	On	x	On	10.5	—	~20-25 µs
Mode 2 3.3 VDC	x	1	02	00	Off	On	On	x	On	9	—	
Mode 1 5 VDC	x	1	01	07	Off	Off	On	x	On	5	—	~20-25 µs
Mode 1 3.3 VDC	x	1	00	00	Off	Off	On	x	On	3		
Standby Mode 5 VDC	x	1	81	07	Off	Off	On	x	On	3	—	4.8 ms
Standby Mode 3.3 VDC	x	1	80	00	Off	Off	On	x	On	2	—	
Sleep Mode	1	0	x	x	Off	Off	Off	On	On	0.120	—	1.5 ms
Power Down	0	0	x	x	Off	Off	Off	Off	Off	<0.001	—	Start

The input pin EN2 has two functions:

- A direct connection from EN2 to VIN to ensure the availability of the regulated supply VDD_X and an auxiliary clock signal (60 kHz, SYS_CLK) for an external MCU. This mode (EN = 0, EN2 = 1) is intended for systems in which the MCU is also being supplied by the reader supply regulator (VDD_X) and the MCU clock is supplied by the SYS_CLK output of the reader. This allows the MCU supply and clock to be available during sleep mode.
- EN2 enables the start-up of the reader system from complete power down (EN = 0, EN2 = 0). In this case, the EN input is being controlled by the MCU (or other system device) that is without supply voltage during complete power down (thus unable to control the EN input). A rising edge applied to the EN2 input (which has an approximately 1-V threshold level) starts the reader supply system and 13.56-MHz oscillator (identical to condition EN = 1).

When user MCU is controlling EN and EN2, a delay of 5 ms between EN and EN2 must be used. In cases where MCU is only controlling EN, EN2 is recommended to be connected to either VIN or GND, depending on the application MCU requirements/needs for VDD_X and SYS_CLK.

NOTE

Using EN=1 and EN2=1 in parallel at start up should not be done as it may cause incorrect operation.

This start-up mode lasts until all of the regulators have settled and the 13.56-MHz oscillator has stabilized. If the EN input is set high (EN = 1) by the MCU (or other system device), the reader stays active. If the EN input is not set high (EN = 0) within 100 µs after the SYS_CLK output is switched from auxiliary clock (60 kHz) to high-frequency clock (derived from the crystal oscillator), the reader system returns to complete Power-Down Mode 1. This option can be used to wake the reader system from complete Power Down (PD Mode 1) by using a pushbutton switch or by sending a single pulse.

After the reader EN line is high, the other power modes are selected by control bits within the Chip Status Control register (0x00). The power mode options and states are listed in Table 5-3.

When EN is set high (or on rising edge of EN2 and then confirmed by EN = 1) the supply regulators are activated and the 13.56-MHz oscillator started. When the supplies are settled and the oscillator frequency is stable, the SYS_CLK output is switched from the auxiliary frequency of 60 kHz to the 13.56-MHz frequency derived from the crystal oscillator. At this time, the reader is ready to communicate and perform the required tasks. The MCU can then program the Chip Status Control register 0x00 and select the operation mode by programming the additional registers.

- Stand-by Mode (bit 7 = 1 of register 0x00), the reader is capable of recovering to full operation in 100 µs.
- Mode 1 (active mode with RF output disabled, bit 5 = 0 and bit 1 = 0 of register 0x00) is a low-power mode that allows the reader to recover to full operation within 25 µs.
- Mode 2 (active mode with only the RF receiver active, bit 1 = 1 of register 0x00) can be used to measure the external RF field (as described in RSSI measurements paragraph) if reader-to-reader anticollision is implemented.
- Mode 3 and Mode 4 (active modes with the entire RF section active, bit 5 = 1 of register 0x00) are the normal modes used for normal transmit and receive operations.

5.6 Receiver - Analog Section

5.6.1 Main and Auxiliary Receiver

The TRF7963A has two receiver inputs: RX_IN1 (pin 8) and RX_IN2 (pin 9). Each of the inputs is connected to an external capacitive voltage divider to ensure that the modulated signal from the tag is available on at least one of the two inputs. This architecture eliminates any possible communication holes that may occur from the tag to the reader.

The two RX inputs (RX_IN1 and RX_IN2) are multiplexed into two receivers–the main receiver and the auxiliary receiver. Only the main receiver is used for reception; the auxiliary receiver is used for signal quality monitoring. Receiver input multiplexing is controlled by bit B3 in the Chip Status Control register (address 0x00).

After startup, RX_IN1 is multiplexed to the main receiver which is composed of an RF envelope detection, first gain and band-pass filtering stage, second gain and filtering stage with AGC. Only the main receiver is connected to the digitizing stage which output is connected to the digital processing block. The main receiver also has an RSSI measuring stage, which measures the strength of the demodulated signal (subcarrier signal).

The primary function of the auxiliary receiver is to monitor the RX signal quality by measuring the RSSI of the demodulated subcarrier signal (internal RSSI). After startup, RX_IN2 is multiplexed to the auxiliary receiver. The auxiliary receiver has an RF envelope detection stage, first gain and filtering with AGC stage and finally the auxiliary RSSI block.

The default MUX setting is RX_IN1 connected to the main receiver and RX_IN2 connected to the auxiliary receiver. To determine the signal quality, the response from the tag is detected by the "main" (pin RX_IN1) and "auxiliary" (pin RX_IN2) RSSI. Both values measured and stored in the RSSI level register (address 0x0F). The MCU can read the RSSI values from the TRF7963A RSSI register and decide if swapping the input signals is preferable or not. Setting B3 in the Chip Status Control register (address 0x00) to 1 connects RX_IN1 (pin 8) to the auxiliary receiver and RX_IN2 (pin 9) to the main receiver. This mechanism must be used to avoid reading holes.

The main and auxiliary receiver input stages are RF envelope detectors. The RF amplitude at RX_IN1 and RX_IN2 should be approximately 3 V_{PP} for a VIN supply level greater than 3.3 V. If the VIN level is lower, the RF input peak-to-peak voltage level should not exceed the VIN level.

5.6.2 Receiver Gain and Filter Stages

The first gain and filtering stage has a nominal gain of 15 dB with an adjustable band-pass filter. The band-pass filter has programmable 3-dB corner frequencies between 110 kHz to 450 kHz for the high-pass filter and between 570 kHz to 1500 kHz for the low-pass filter. After the band-pass filter, there is another gain-and-filtering stage with a nominal gain of 8 dB and with frequency characteristics identical to the first band-pass stage.

The internal filters are configured automatically depending on the selected ISO communication standard in the ISO Control register (address 0x01). If required, additional fine tuning can be done by writing directly to the RX special setting registers (address 0x0A).

The main receiver also has a second receiver gain and digitizer stage which is included in the AGC loop. The AGC loop is activated by setting the bit B2 = 1 in the Chip Status Control register (address 0x00). When activated, the AGC continuously monitors the input signal level. If the signal level is significantly higher than an internal threshold level, gain reduction is activated.

By default, the AGC is frozen after the first four pulses of the subcarrier signal. This prevents the AGC from interfering with the reception of the remaining data packet. In certain situations, this "AGC freeze" is not optimal, so it can be removed by setting B0 = 1 in the RX Special Setting register (address 0x0A).

Table 5-4 shows the various settings for the receiver analog section. It is important to note that setting B4, B5, B6, and B7 to 0 results in a band-pass characteristic of 240 kHz to 1.4 MHz, which is appropriate for ISO14443B 106 kbps, ISO14443A/B data-rates of 212 kbps and 424 kbps, and FeliCa 424 kbps.

Table 5-4. RX Special Setting Register (0x0A)

Bit	Function	Comments
B7	Bandpass from 110 kHz to 570 kHz	Appropriate for any 212-kHz subcarrier systems like FeliCa
B6	Bandpass from 200 kHz to 900 kHz	
B5	Bandpass from 450 kHz to 1.5 MHz	Appropriate for Manchester-coded 106-kbps 848-kHz subcarrier systems (for example, used in ISO14443A).
B4	Bandpass from 100 kHz to 1.5 MHz	Appropriate for highest bit rate (848 kbps) used in high-bit-rate ISO14443B. Gain is reduced by 7 dB.
B3 B2	00 = no gain reduction 01 = gain reduction for 5 dB 10 = gain reduction for 10 dB 11 = gain reduction for 15 dB	Sets the RX digital gain reduction (changing the window of the digitizing comparator).
B1	0 = 5 times minimum digitizing level 1 = 3 times minimum digitizing level	AGC activation level change. From five times higher to the minimum RX digitizing level to three times the minimum digitizing level. The minimum RX digitizing level can be adjusted by B2 and B3 (gain reduction).
B0	0 = AGC freeze after 16 subcarrier edges 1 = AGC always on during receive	AGC action is not limited in time or to the start of receive. AGC action can be done any time during receive process. The AGC can only increase and, hence, clips on the peak RX level during the enable period. AGC level is reset automatically at the beginning of each receive start frame.

5.7 Receiver - Digital Section

The output of the TRF7963A analog receiver block is a digitized subcarrier signal and is the input to the digital receiver block. This block includes a Protocol Bit Decoder section and the Framing Logic section.

The protocol bit decoders convert the subcarrier coded signal into a serial bit stream and a data clock. The decoder logic is designed for maximum error tolerance. This enables the decoder section to successfully decode even partly corrupted subcarrier signals that otherwise would be lost due to noise or interference.

In the framing logic section, the serial bit stream data is formatted in bytes. Special signals such as the start of frame (SOF), end of frame (EOF), start of communication, and end of communication are automatically removed. The parity bits and CRC bytes are also checked and removed. This "clean" data is then sent to the 12-byte FIFO register where it can be read by the external microcontroller system. Providing the data this way, in conjunction with the timing register settings of the TRF7963A, means the firmware developer has to know about much less of the finer details of the ISO protocols to create a very robust application, especially in low-cost platforms where code space is at a premium and high performance is still required.

The start of the receive operation (successfully received SOF) sets the IRQ flags in the IRQ and Status register (0x0C). The end of the receive operation is signaled to the external system MCU by setting pin 13 (IRQ) high. If the receive data packet is longer than 8 bytes, an interrupt is sent to the MCU as the received data occupies 75% of the FIFO capacity. The data should be immediately removed from the FIFO.

Any error in the data format, parity, or CRC is detected and notified to the external system by an interrupt request pulse. The source condition of the interrupt request pulse is available in the IRQ Status register (0x0C). The main register controlling the digital part of the receiver is the ISO Control register (0x01). By writing to this register, the user selects the protocol to be used. With each new write in this register, the default presets are reloaded in all related registers, so no further adjustments in other registers are needed for proper operation.

NOTE

If register setting changes are needed for fine tuning the system, they must be done after setting the ISO Control register (0x01).

The framing section also supports the bit-collision detection as specified in ISO14443A (0x01). When a bit collision is detected, an interrupt request is sent and a flag is set in the IRQ and Status register (0x0C). The position of the bit collision is written in two registers: Collision Position register (0x0E) and partly in Collision Position and Interrupt Mask register (0x0D) (bits B6 and B7).

The collision position is presented as sequential bit number, where the count starts immediately after the start bit. This means a collision in the first bit of a UID would give the value 00 0001 0000 in these registers when their contents are combined after being read. (the count starts with 0 and the first 16 bits are the command code and the Number of Valid Bits (NVB) byte)

The receive section also includes two timers. The RX wait time timer is controlled by the value in the RX Wait Time register (0x08). This timer defines the time interval after the end of the transmit operation in which the receive decoders are not active (held in reset state). This prevents false detections resulting from transients following the transmit operation. The value of the RX Wait Time register (0x08) defines the time in increments of 9.44 µs. This register is preset at every write to ISO Control register (0x01) according to the minimum tag response time defined by each standard.

The RX no response timer is controlled by the RX No Response Wait Time register (0x07). This timer measures the time from the start of slot in the anticollision sequence until the start of tag response. If there is no tag response in the defined time, an interrupt request is sent and a flag is set in the IRQ Status register (0x0C). This enables the external controller to be relieved of the task of detecting empty slots. The wait time is stored in the register in increments of 37.76 µs. This register is also automatically preset for every new protocol selection.

5.7.1 Received Signal Strength Indicator (RSSI)

The TRF7963A incorporates in total three independent RSSI building blocks: Internal Main RSSI, Internal Auxiliary RSSI, and External RSSI. The internal RSSI blocks are measuring the amplitude of the subcarrier signal, and the external RSSI block measures the amplitude of the RF carrier signal at the receiver input.

5.7.1.1 Internal RSSI – Main and Auxiliary Receivers

Each receiver path has its own RSSI block to measure the envelope of the demodulated RF signal (subcarrier). Internal Main RSSI and Internal Auxiliary RSSI are identical except that they are connected to different RF input pins. The Internal RSSI is intended for diagnostic purposes to set the correct RX path conditions.

The Internal RSSI values can be used to adjust the RX gain settings and/or decide which RX path (main or auxiliary) provides the greater amplitude and, hence, to decide if the MUX may need to be reprogrammed to swap the RX input signal. The measuring system latches the peak value, so the RSSI level can be read after the end of each receive packet. The RSSI register values are reset with every transmission (TX) by the reader. This guarantees an updated RSSI measurement for each new tag response.

The Internal RSSI has 7 steps (3 bit) with a typical increment of about 4 dB. The operating range is between 600 mVp and 4.2 Vpp with a typical step size of about 600 mV. Both RSSI values "Internal Main" and "Internal Aux" RSSI are stored in the RSSI Levels and Oscillator Status register (0x0F).

The nominal relationship between the input RF peak level and the RSSI value is shown in Figure 5-2.

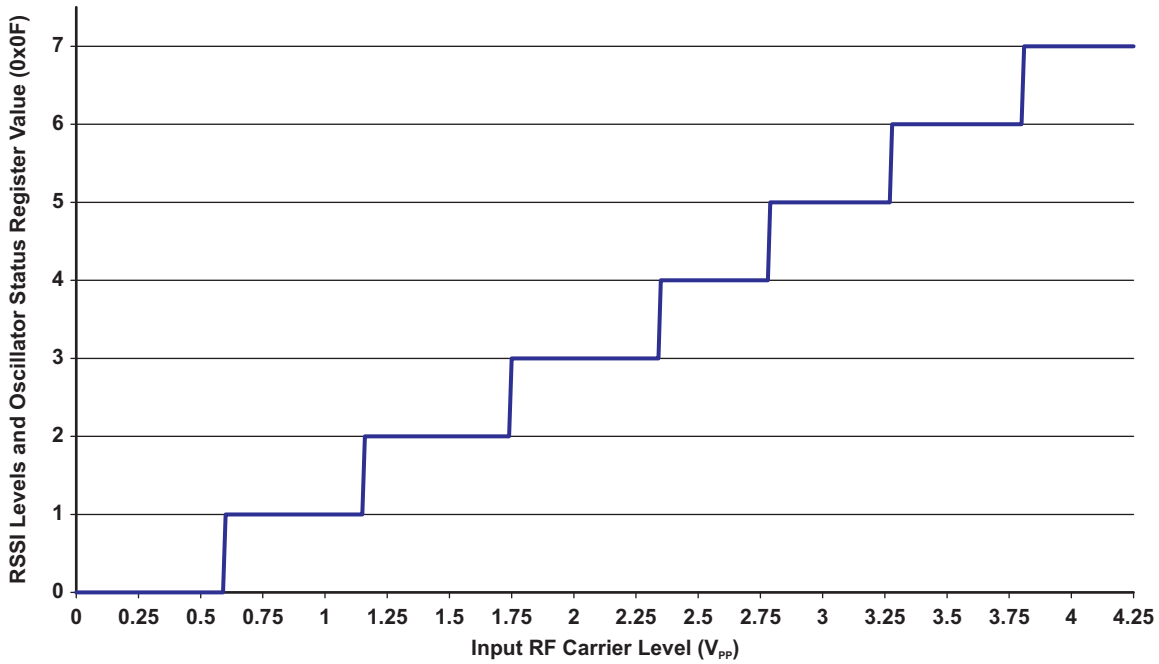


Figure 5-2. Digital Internal RSSI (Main and Auxiliary) Value vs RF Input Level

This RSSI measurement is done during the communication to the Tag; this means the TX must be on. Bit 1 in the Chip Status Control register (0x00) defines if internal RSSI or the external RSSI value is stored in the RSSI Levels and Oscillator Status register 0x0F. Direct command 0x18 is used to trigger an internal RSSI measurement.

5.7.1.2 External RSSI

The external RSSI is mainly used for test and diagnostic in order to sense the amplitude of any 13.56-MHz signal at the receivers RX_IN1 input. The external RSSI measurement is typically done in active mode when the receiver is on but transmitter output is off. The level of the RF signal received at the antenna is measured and stored in the RSSI Levels and Oscillator Status Register 0x0F.

The relationship between the voltage at the RX_IN1 input and the 3-bit code is shown in Figure 5-3.

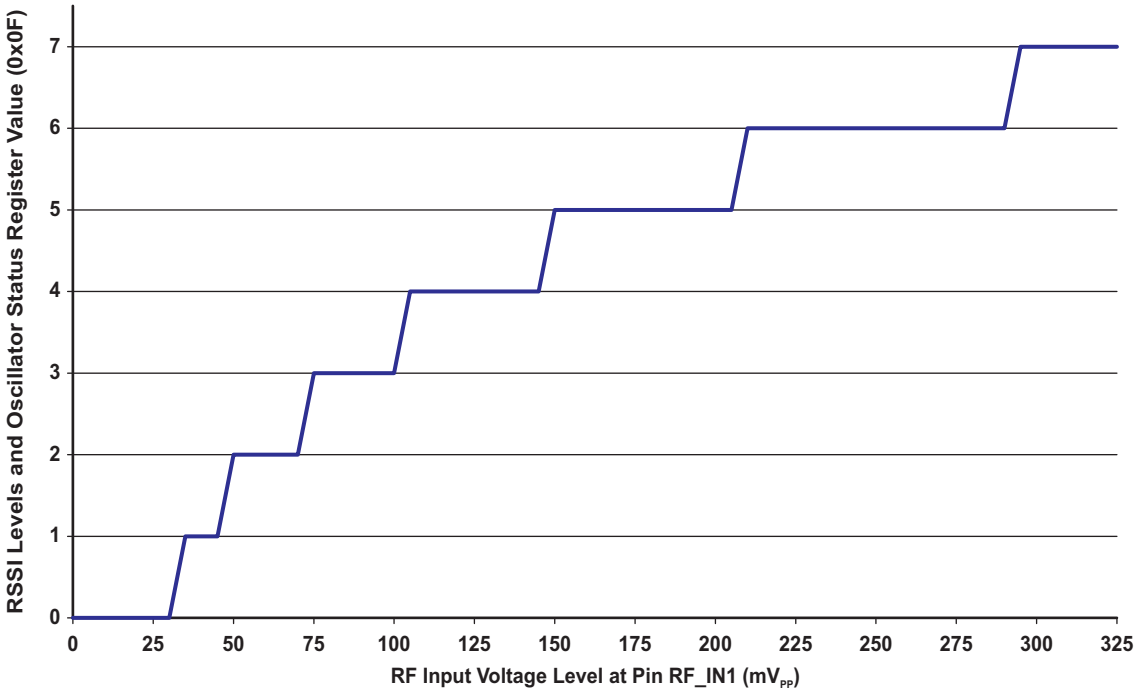


Figure 5-3. Digital External RSSI Value vs RF Input Level

The relation between the 3-bit code and the external RF field strength (A/m) sensed by the antenna must be determined by calculation or by experiments for each antenna design. The antenna Q-factor and connection to the RF input influence the result. Direct command 0x19 is used to trigger an internal RSSI measurement.

To check the internal or external RSSI value independent of any other operation, the user must:

1. Set transmitter to desired state (on or off) using Bit 5 of Chip Status Control register (0x00)
2. Set the receiver using direct command 0x17.
3. Check internal or external RSSI using direct commands 0x18 or 0x19, respectively.

   This action latches/places RSSI value in RSSI register
4. Read RSSI register using direct command 0x0F, values range from 0x40 to 0x7F.
5. Repeat steps 1-4 as desired, as register is reset after read.

5.8 Oscillator Section

The 13.56-MHz oscillator is controlled via the Chip Status Control register (0x00) and the EN and EN2 signals. The oscillator generates the RF frequency for the RF output stage and the clock source for the digital section. The buffered clock signal is available at pin 27 (SYS_CLK) for external circuits. B4 and B5 inside the Modulation and SYS_CLK register (0x09) can be used to divide the external SYS_CLK signal at pin 27 by 1, 2, or 4.

Typical start-up time from complete power down is in the range of 3.5 ms.

During Power Down Mode 2 (EN = 0, EN2 = 1) the frequency of SYS_CLK is switched to 60 kHz (typical).

The 13.56-MHz crystal must be connected between pin 31 and pin 32. The external shunt capacitors values for C_1 and C_2 must be calculated based on the specified load capacitance of the crystal being used. The external shunt capacitors are calculated as two identical capacitors in series plus the stray capacitance of the TRF7963A and parasitic PCB capacitance in parallel to the crystal.

The parasitic capacitance (C_S , stray and parasitic PCB capacitance) can be estimated at 4 to 5 pF (typical).

As an example, using a crystal with a required load capacitance (C_L) of 18 pF, the calculation is as follows (see Figure 5-4):

$C_1 = C_2 = 2 \times (C_L - C_S) = 2 \times (18\ pF - 4.5\ pF) = 27\ pF$

A 27-pF capacitor must be placed on pins 30 and 31 to ensure proper crystal oscillator operation.

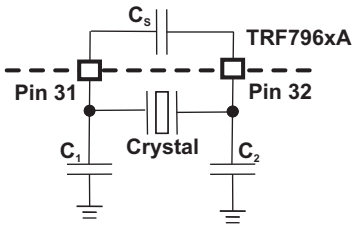


Figure 5-4. Crystal Block Diagram

Table 5-5 shows the minimum characteristics required for any crystal used with TRF7963A.

Table 5-5. TRF7963A Minimum Crystal Requirements

Parameter	Specification
Frequency	13.56 MHz
Mode of operation	Fundamental
Type of resonance	Parallel
Frequency tolerance	± 20 ppm
Aging	<5 ppm/year
Operation temperature range	-40°C to 85°C
Equivalent series resistance	50 Ω

As an alternative, an external clock oscillator source can be connected to pin 31 to provide the system clock, and pin 32 can be left open.

5.9 Transmitter - Analog Section

The 13.56-MHz oscillator generates the RF signal for the PA stage. The power amplifier consists of a driver with selectable output resistance of 4 Ω or 8 Ω (typical). The transmit power levels are selectable between 100 mW (half power) or 200 mW (full power) when configured for 5-V automatic operation. Selection of the transmit power level is set by bit B4 in the Chip Status Control register (0x00). When configured for 3-V automatic operation, the transmit power level is typically in the range of 33 mW (half power) or 70 mW (full power).

The ASK modulation depth is controlled by bits B0, B1, and B2 in the Modulator and SYS_CLK Control register (0x09). The ASK modulation depth range can be adjusted between 7% to 30% or 100% (OOK).

External control of the transmit modulation depth is possible by setting the ISO Control register (0x01) to Direct Mode. While operating the TRF7963A in Direct Mode, the transmit modulation is made possible by selecting the modulation type ASK or OOK at pin 12. External control of the modulation type is made possible only if enabled by setting B6 in the Modulator and SYS_CLK Control register (0x09) to 1.

In normal operation mode, the length of the modulation pulse is defined by the protocol selected in the ISO Control register (0x01). In case of a high-Q antenna, the modulation pulse is typically prolonged, and the tag detects a longer pulse than intended. For such cases, the modulation pulse length must be corrected by using the TX Pulse Length register (0x06).

If the register contains all zeros, then the pulse length is governed by the protocol selection. If the register contains a value other than 0x00, the pulse length is equal to the value of the register multiplied by 73.7 ns. This means the pulse length can be adjusted between 73.7 ns and 18.8 µs in 73.7-ns increments.

5.10 Transmitter - Digital Section

The digital part of the transmitter is a mirror of the receiver. The settings controlled the ISO Control register (0x01) are applied to the transmitter just like the receiver. In the TRF7963A default mode (ISO Mode), the TRF7963A automatically adds all the special signals like start of communication, end of communication, SOF, EOF, parity bits and CRC bytes.

The data is then coded to modulation pulse levels and sent to the RF output stage modulation control unit. Just like with the receiver, this means that the external system MCU only has to load the FIFO with data and all the micro-coding is done automatically, again saving the firmware developer code space and time. Additionally, all the registers used for transmit parameter control are automatically preset to optimum values when a new selection is entered into the ISO Control register (0x01).

NOTE

The FIFO must be reset before starting any transmission with Direct Command 0x0F.

There are two ways to start the transmit operation:

- It can be started by loading the number of bytes to be sent (address 0x1D and 0x1E) and data to be loaded in the FIFO (address 0x1F) followed by a transmit command (described in direct commands section). In this case, the transmission then starts exactly on the transmit command.
- It is also possible to send the transmit command and information on the number of bytes to be transmitted first and then start to send the data to FIFO. In this case, the transmission starts when first data byte is written into the FIFO.

NOTE

If the data length is longer than the FIFO, the external system MCU is warned when the majority of data from the FIFO was already transmitted by sending and interrupt request with flag in IRQ register to indicate a FIFO low/high status. The external system should respond by loading next data packet into the FIFO.

At the end of a transmit operation, the external system MCU is notified by interrupt request (IRQ) with a flag in IRQ register (0x0C) indicating TX is complete (example value = 0x80).

The TX Length registers also support incomplete byte transmission. The high two nibbles in register 0x1D and the nibble composed of bits B4 through B7 in register 0x1E store the number of complete bytes to be transmitted. Bit B0 in register 0x1E is a flag indicating that there are also additional bits to be transmitted which do not form a complete byte. The number of bits is stored in bits B1 through B3 of the same register (0x1E).

Some protocols have options so there are two sub-level configuration registers to select the TX protocol options.

- ISO14443B TX Options register (0x02). It controls the SOF and EOF selection and EGT selection for the ISO14443B protocol.
- ISO14443A High-Bit-Rate and Parity Options register (0x03). This register enables the use of different bit rates for RX and TX operations in ISO14443 high bit rate protocol. Besides that, it also selects the parity method in case of ISO14443A high bit rate.

5.11 Transmitter – External Power Amplifier / Subcarrier detector

The TRF7963A can be used in conjunction with an external TX power amplifier and/or external subcarrier detector for the receiver path. If this is the case, certain registers must be programmed as shown here:

- Bit B6 of the Regulator and I/O Control register (0x0B) must be set to 1.

  This setting has two functions: First, to provide a modulated signal for the transmitter, if needed. Second, to configure the TRF7963A receiver inputs for an external demodulated subcarrier input.
- Bit B3 of the Modulation and SYS_CLK Control register (0x09) to 1 (see Section 6.1.2.6).

This function configures the ASK/OOK pin for either a digital or analog output (B3 = 0 enables a digital output, and B3 = 1 enables an analog output). The design of an external power amplifier requires detailed RF knowledge. There are also readily designed and certified high-power HF reader modules on the market.

5.12 TRF7963A Communication Interface

5.12.1 General Introduction

The communication interface to the reader can be configured in two ways: with a eight line parallel interface (D0:D7) plus DATA_CLK, or with a three or four wire Serial Peripheral Interface (SPI). The SPI interface uses traditional Master Out/Slave In (MOSI), Master In, Slave Out (MISO), IRQ, and DATA_CLK lines. The SPI can be operated with or without using the Slave Select line.

These communication modes are mutually exclusive; meaning, only one mode can be used at a time in the application.

When the SPI interface is selected, the unused I/O_2, I/O_1, and I/O_0 pins must be hard-wired according to Table 5-6. At power up, the TRF7963A IC samples the status of these three pins. If they are not the same (all High or all Low) it enters one of the possible SPI modes.

The TRF7963A always behaves as the slave, while the microcontroller (MCU) behaves as the master device. The MCU initiates all communications with the TRF7963A. The TRF7963A makes use of the Interrupt Request (IRQ) pin in both parallel and SPI modes to prompt the MCU for servicing attention.

Table 5-6. Pin Assignment in Parallel and Serial Interface Connection or Direct Mode

Pin	Parallel	Parallel Direct	SPI With SS	SPI Without SS
DATA_ CLK	DATA_CLK	DATA_CLK	DATA_CLK from master	DATA_CLK from master
I/O_7	A/D[7]		MOSI (1) = data in (reader in)	MOSI (1) = data in (reader in)
I/O_6	A/D[6]	Direct mode, data out (subcarrier or bit stream)	MISO (2) = data out (MCU out)	MISO (2) = data out (MCU out)
I/O_5 (3)	A/D[5]	Direct mode, strobe (bit clock out)	See (3)	See (3)
I/O_4	A/D[4]		SS (slave select) (4)	–
I/O_3	A/D[3]	–	–	–
I/O_2	A/D[2]	–	At VDD	At VDD
I/O_1	A/D[1]	–	At VDD	At VSS
I/O_0	A/D[0]	–	At VSS	At VSS
IRQ	IRQ interrupt	IRQ interrupt	IRQ interrupt	IRQ interrupt

(1) MOSI = Master Out, Slave In
(2) MISO = Master In, Slave Out
(3) The I/O_5 pin is used only for information when data is put out of the chip (for example, reading 1 byte from the chip). It is necessary first to write in the address of the register (8 clocks) and then to generate another 8 clocks for reading out the data. The I/O_5 pin goes high during the second 8 clocks. But for normal SPI operations I/O_5 pin is not used.
(4) The slave select pin is active low.

Communication is initialized by a start condition, which is expected to be followed by an Address/Command word (Adr/Cmd). The Adr/Cmd word is 8 bits long, and its format is shown in Table 5-7.

Table 5-7. Address/Command Word Bit Distribution

Bit	Description	Bit Function	Address	Command
B7	Command control bit	0 = address 1 = command	0	1
B6	Read/Write	1 = read 0 = write	R/W	0
B5	Continuous address mode	1 = continuous mode	R/W	0
B4	Address/command bit 4		Adr 4	Cmd 4
B3	Address/command bit 3		Adr 3	Cmd 3
B2	Address/command bit 2		Adr 2	Cmd 2
B1	Address/command bit 1		Adr 1	Cmd 1
B0	Address/command bit 0		Adr 0	Cmd 0

The MSB (bit 7) determines if the word is to be used as a command or as an address. The last two columns of Table 5-7 show the function of the separate bits if either address or command is written. Data is expected once the address word is sent. In continuous address mode (continuous mode = 1), the first data that follows the address is written (or read) to (from) the given address. For each additional data, the address is incremented by one. Continuous mode can be used to write to a block of control registers in a single stream without changing the address; for example, setup of the predefined standard control registers from the MCU non-volatile memory to the reader. In non-continuous address mode (simple addressed mode), only one data word is expected after the address.

Address Mode is used to write or read the configuration registers or the FIFO. When writing more than 12 bytes to the FIFO, the Continuous Address Mode should be set to 1.

The Command Mode is used to enter a command resulting in reader action (for example, initialize transmission, enable reader, and turn reader on/off).

Examples of expected communications between an MCU and the TRF7963A are shown.

Table 5-8. Continuous Address Mode

Start	Adr x	Data(x)	Data(x+1)	Data(x+2)	Data(x+3)	Data(x+4)	...	Data(x+n)	StopCont

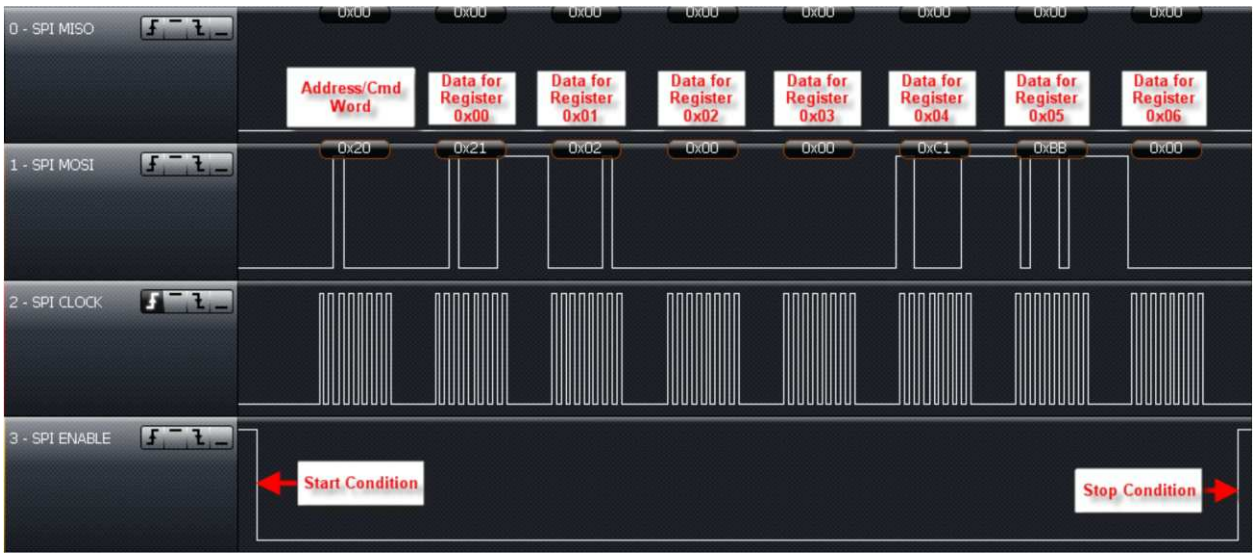


Figure 5-5. Continuous Address Register Write Example Starting With Register 0x00 (Using SPI With SS Mode)

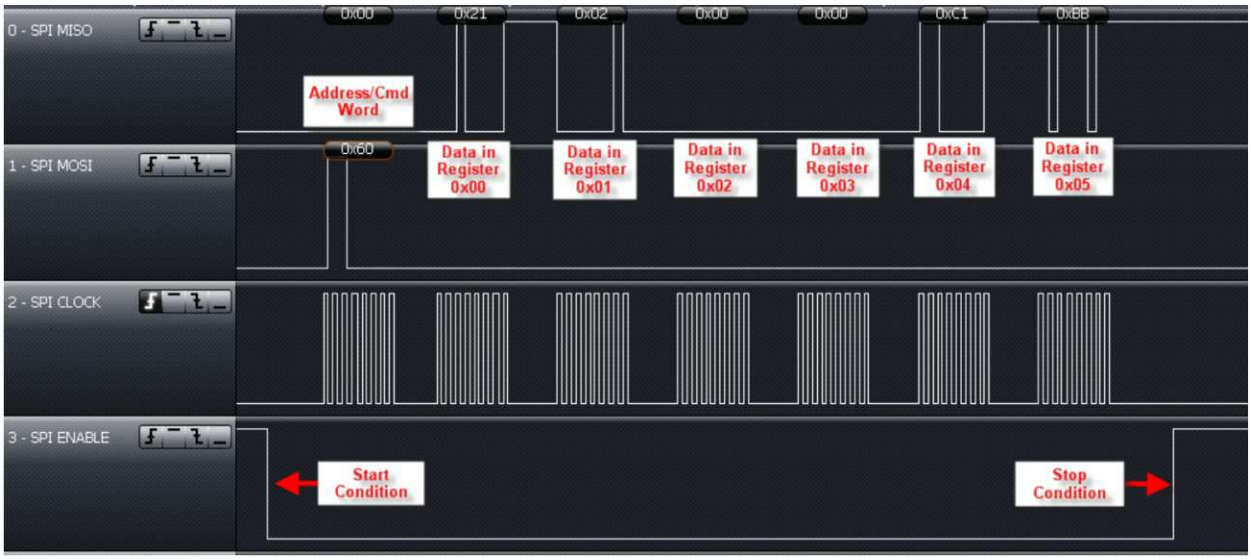


Figure 5-6. Continuous Address Register Read Example Starting With Register 0x00 (Using SPI With SS Mode)

Table 5-9. Non-Continuous Address Mode (Single Address Mode)

Start	Adr x	Data(x)	Adr y	Data(y)	...	Adr z	Data(z)	StopSgl

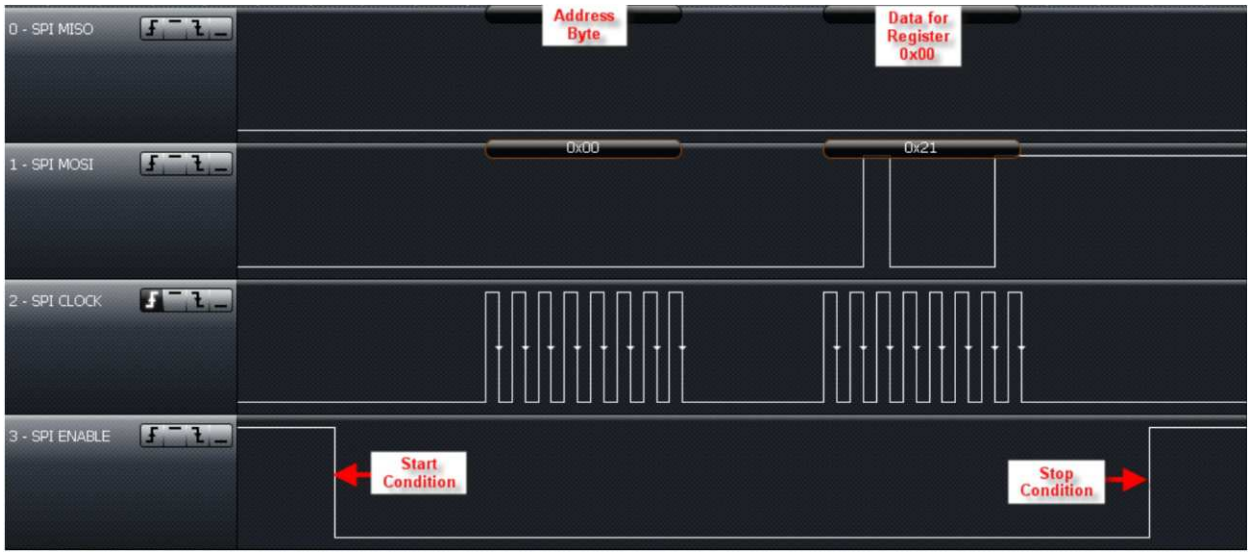


Figure 5-7. Single Address Register Write Example of Register 0x00 (Using SPI With SS Mode)

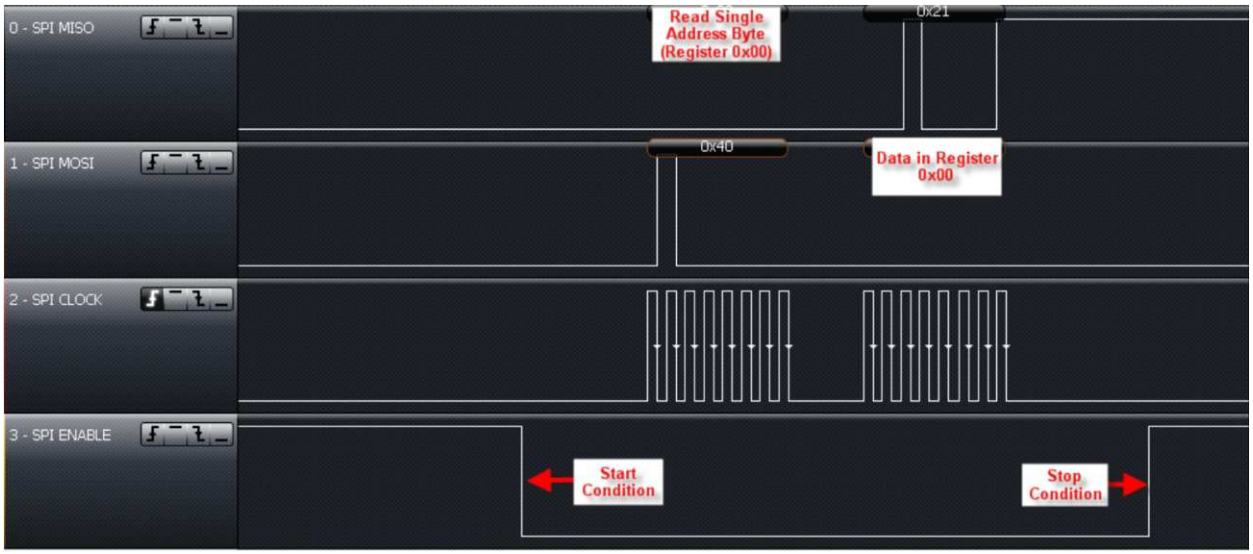


Figure 5-8. Single Address Register Read Example of Register 0x00 (Using SPI With SS Mode)

Table 5-10. Direct Command Mode

Start	Cmd x	(Optional data or command)	Stop

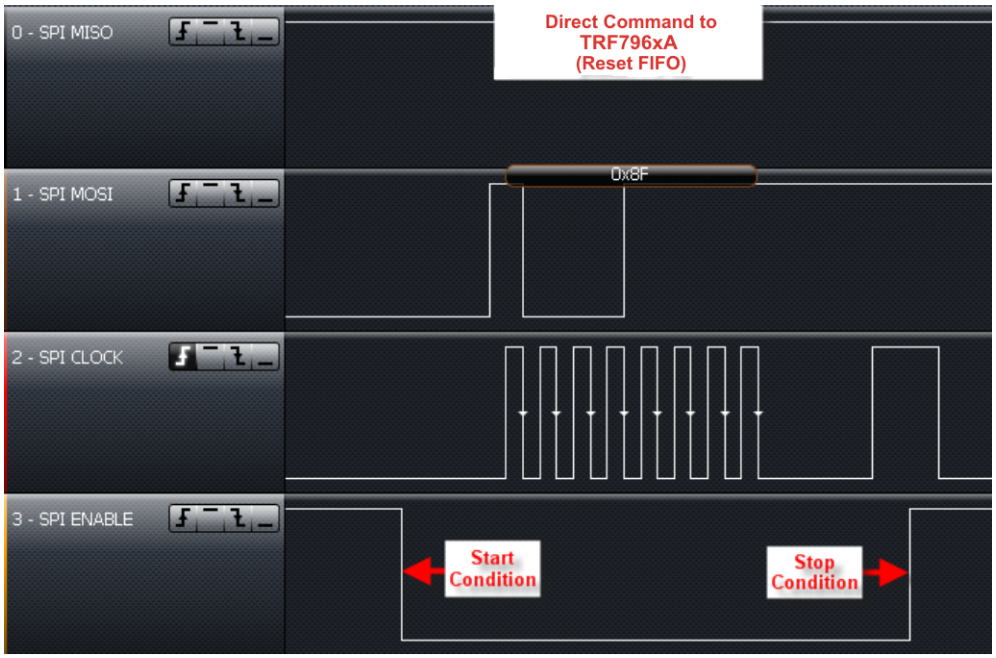


Figure 5-9. Direct Command Example of Sending 0x0F (Reset) (Using SPI With SS Mode)

The other Direct Command Codes from MCU to TRF7963A are described in Section 5.13.

5.12.2 FIFO Operation

The FIFO is a 12-byte register at address 0x1F with byte storage locations 0 to 11. FIFO data is loaded in a cyclical manner and can be cleared by a reset command (0x0F, see graphic above showing this Direct Command).

Associated with the FIFO are two counters and three FIFO status flags. The first counter is a 4-bit FIFO byte counter (bits B0 to B3 in register 0x1C) that keeps track of the number of bytes loaded into the FIFO. If the number of bytes in the FIFO is n, the register value is n – 1 (number of bytes in FIFO register). If 8 bytes are in the FIFO, the FIFO counter (bits B0 to B3 in register 0x1C) has the value 7.

A second counter (12 bits wide) indicates the number of bytes being transmitted (registers 0x1D and 0x1E) in a data frame. An extension to the transmission-byte counter is a 4-bit broken-byte counter also provided in register 0x1E (bits B0 to B3). Together these counters make up the TX length value that determines when the reader generates the EOF byte.

FIFO status flags are as follows:

1. **FIFO overflow** (bit B4 of register 0x1C): Indicates that the FIFO was loaded too soon
2. **FIFO level too low** (bit B5 of register 0x1C): Indicates that only three bytes are left to be transmitted (Can be used during transmission.)
3. **FIFO level high** (bit B6 of register 0x1C): Indicates that nine bytes are already loaded into the FIFO (Can be used during reception to generate a FIFO reception IRQ. This is to notify the MCU to service the reader in time to ensure a continuous data stream.)

During transmission, the FIFO is checked for an almost-empty condition, and during reception for an almost-full condition. The maximum number of bytes that can be loaded into the FIFO in a single sequence is 12 bytes.

NOTE

The number of bytes in a frame, transmitted or received, can be greater than 12 bytes.

During transmission, the MCU loads the TRF7963A FIFO (or, during reception, the MCU removes data from the FIFO), and the FIFO counter counts the number of bytes being loaded into the FIFO. Meanwhile, the byte counter keeps track of the number of bytes being transmitted. An interrupt request is generated if the number of bytes in the FIFO is less than 3 or greater than 9, so that MCU can send new data or remove the data as necessary. The MCU also checks the number of data bytes to be sent, so as to not surpass the value defined in TX length bytes. The MCU also signals the transmit logic when the last byte of data is sent or was removed from the FIFO during reception. Transmission starts automatically after the first byte is written into FIFO.

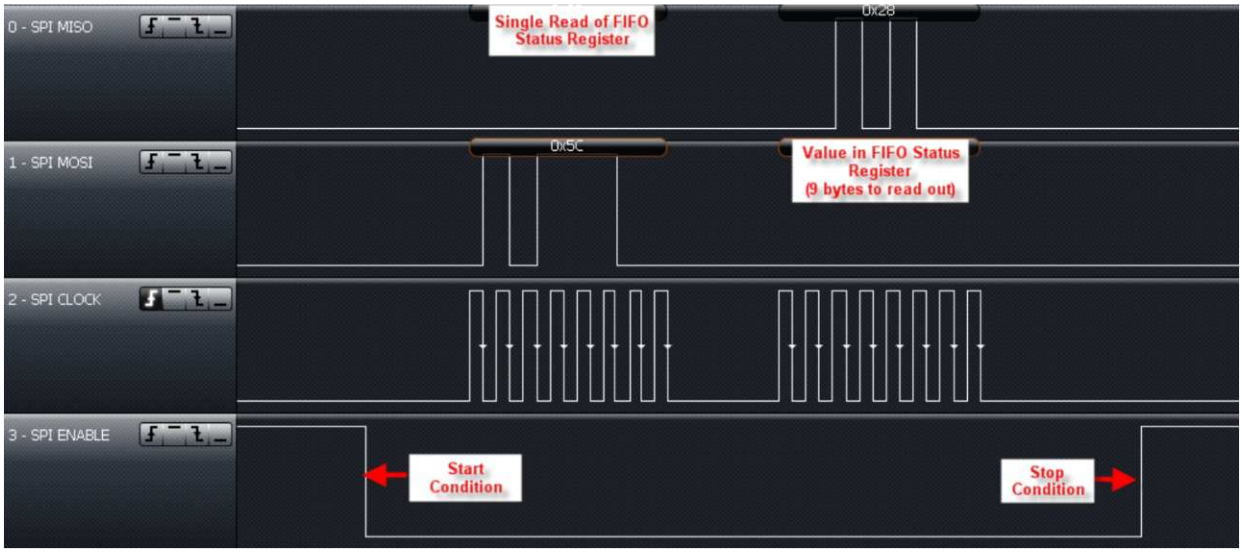


Figure 5-10. Checking the FIFO Status Register (Using SPI With SS Mode)

5.12.3 Parallel Interface Mode

In parallel mode, the start condition is generated on the rising edge of the I/O_7 pin while the CLK is high.

This is used to reset the interface logic. Figure 5-11 shows the sequence of the data, with an 8-bit address word first, followed by data.

Communication is ended by:

- The StopSmpl condition, where a falling edge on the I/O_7 pin is expected while CLK is high
- The StopCont condition, where the I/O_7 pin must have a successive rising and falling edge while CLK is low in order to reset the parallel interface and be ready for the new communication sequence
- The StopSmpl condition is also used to terminate the Direct Mode.

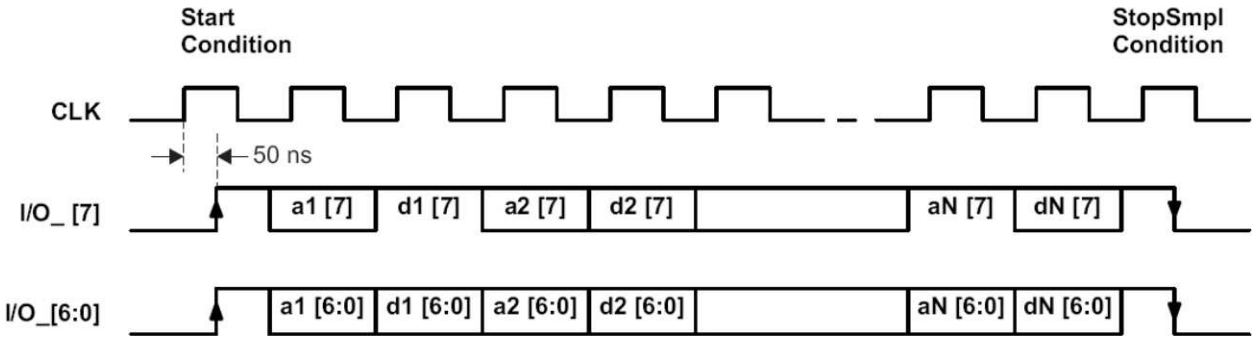


Figure 5-11. Parallel Interface Communication With Simple Stop Condition (StopSmpl)

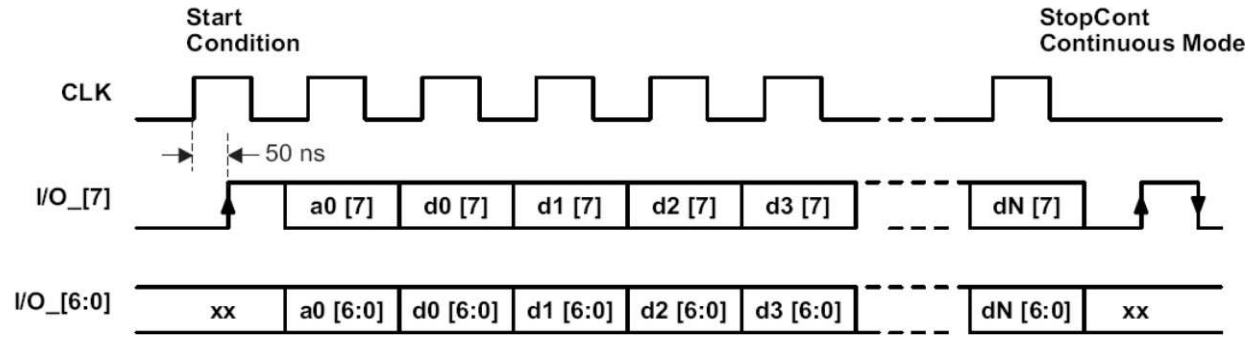


Figure 5-12. Parallel Interface Communication With Continuous Stop Condition (StopCont)

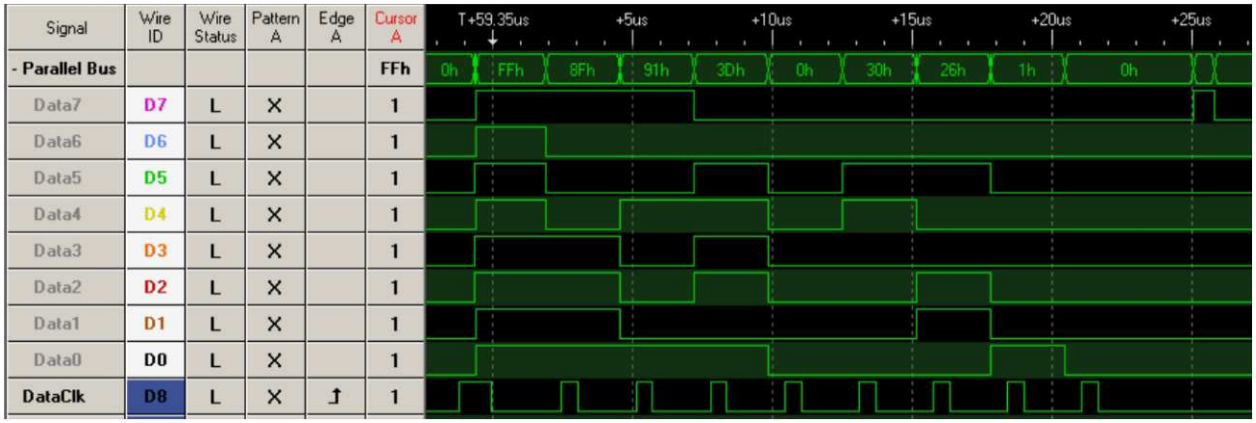


Figure 5-13. Parallel Interface Communication With Continuous Stop Condition

5.12.3.1 Reception of Air Interface Data

At the start of a receive operation (when SOF is successfully detected), B6 is set in the IRQ Status register. An interrupt request is sent to the MCU at the end of the receive operation if the receive data string was shorter than or equal to 8 bytes. The MCU receives the interrupt request, then checks to determine the reason for the interrupt by reading the IRQ Status register (address 0x0C), after which the MCU reads the data from the FIFO.

If the received packet is longer than 8 bytes, the interrupt is sent before the end of the receive operation when the ninth byte is loaded into the FIFO (75% full). The MCU should again read the content of the IRQ Status register to determine the cause of the interrupt request. If the FIFO is 75% full (as marked with flag B5 in IRQ Status register and by reading the FIFO Status register), the MCU should respond by reading the data from FIFO to make room for new incoming receive data. When the receive operation is finished, the interrupt is sent and the MCU must check how many words are still present in the FIFO before it finishes reading.

If the reader detects a receive error, the corresponding error flag is set (framing error, CRC error) in the IRQ Status register, indicating to the MCU that reception was not completed correctly.

5.12.3.2 Data Transmission to MCU

Before beginning data transmission, the FIFO should always be cleared with a reset command (0x0F). Data transmission is initiated with a selected command (see Section 5.13). The MCU then commands the reader to do a continuous write command (0x3D) (see Table 5-7) starting from register 0x1D. Data written into register 0x1D is the TX length byte 1 (upper and middle nibbles), while the following byte in register 0x1E is the TX length byte 2 (lower nibble and broken byte length). Note that the TX byte length determines when the reader sends the EOF byte. After the TX length bytes are written, FIFO data is loaded in register 0x1F with byte storage locations 0 to 11. Data transmission begins automatically after the first byte is written into the FIFO. The loading of TX length bytes and the FIFO can be done with a continuous write command, as the addresses are sequential.

At the start of transmission, the flag B7 (IRQ_TX) is set in the IRQ Status register. If the transmit data is shorter than or equal to 4 bytes, the interrupt is sent only at the end of the transmit operation. If the number of bytes to be transmitted is higher or equal to 5, then the interrupt is generated. This occurs also when the number of bytes in the FIFO reaches 3. The MCU should check the IRQ Status register and FIFO Status register and then load additional data to the FIFO, if needed. At the end of the transmit operation, an interrupt is sent to inform the MCU that the task is complete.

5.12.4 Serial Interface Communication (SPI)

When an SPI interface is utilized, I/O pins, I/O_2, I/O_1, and I/O_0, must be hard wired according to Table 5-7. On power up, the TRF7963A looks for the status of these pins; if they are not the same (not all high, or not all low), the reader enters into one of two possible SPI modes:

- SPI with slave select

  or
- SPI without slave select

The choice of one of these modes over the other should be made based on the available GPIOs and the desired control of the system.

The serial communications work in the same manner as the parallel communications with respect to the FIFO, except for the following condition. On receiving an IRQ from the reader, the MCU reads the TRF7963A IRQ Status register to determine how to service the reader. After this, the MCU must to do a dummy read to clear the reader's IRQ Status register. The dummy read is required in SPI mode, because the reader's IRQ Status register needs an additional clock cycle to clear the register. This is not required in parallel mode, because the additional clock cycle is included in the Stop condition.

A procedure for a dummy read is as follows:

1. Starting the dummy read
   (a) When using slave select (SS): set SS bit low
   (b) When not using SS: start condition is when SCLK is high
2. Send address word to IRQ Status register (0x0C) with read and continuous address mode bits set to 1
3. Read 1 byte (8 bits) from IRQ Status register (0x0C)
4. Dummy-read 1 byte from register 0Dh (collision position and interrupt mask)
5. Stopping the dummy read
   (a) When using slave select (SS): set SS bit high
   (b) When not using SS: stop condition when SCLK is high

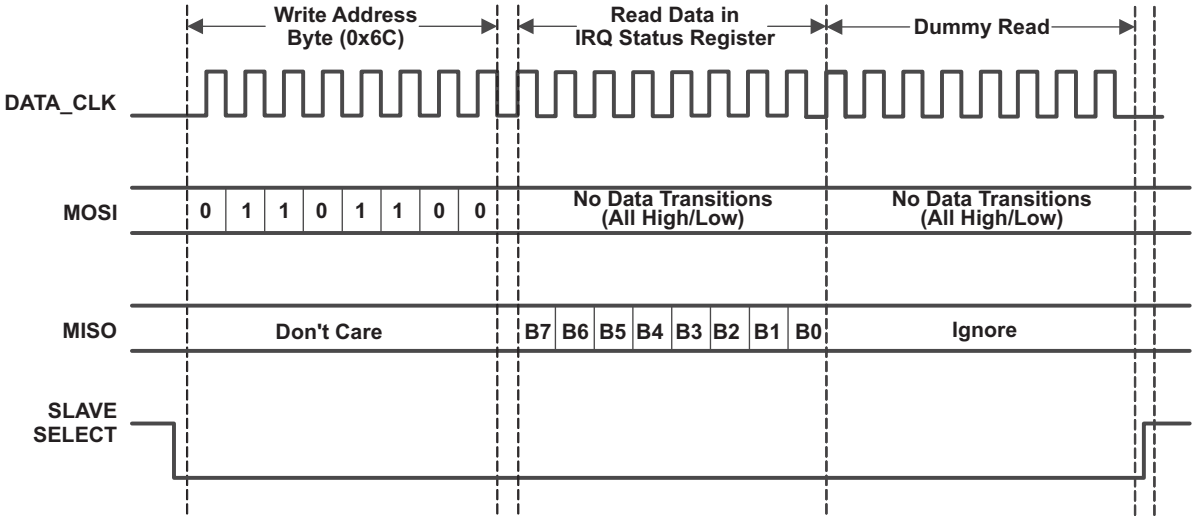


Figure 5-14. Procedure for Dummy Read

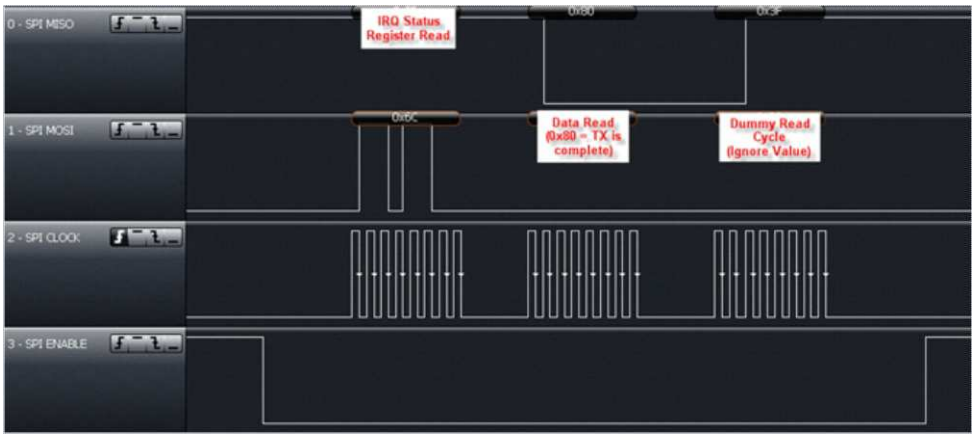


Figure 5-15. Dummy Read Using SPI With SS

5.12.4.1 Serial Interface Mode Without Slave Select (SS)

The serial interface without the slave select pin must use delimiters for the start and stop conditions. Between these delimiters, the address, data, and command words can be transferred. All words must be 8 bits long with MSB transmitted first (see Figure 5-16).

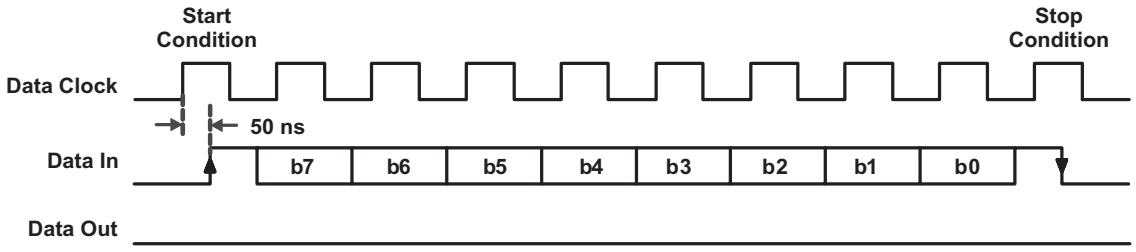


Figure 5-16. SPI Without Slave Select Timing

In this mode, a rising edge on data in (I/O_7, pin 24) while SCLK is high resets the serial interface and prepares it to receive data. Data in can change only when SCLK is low, and it is read by the reader on the SCLK rising edge. Communication is terminated by the stop condition when the data in falling edge occurs during a high SCLK period.

5.12.4.2 Serial Interface Mode With Slave Select (SS)

The serial interface is in reset while the Slave Select signal is high. Serial data in (MOSI) changes on the falling edge, and is validated in the reader on the rising edge, as shown in Figure 5-17. Communication is terminated when the Slave Select signal goes high.

All words must be 8 bits long with the MSB transmitted first.

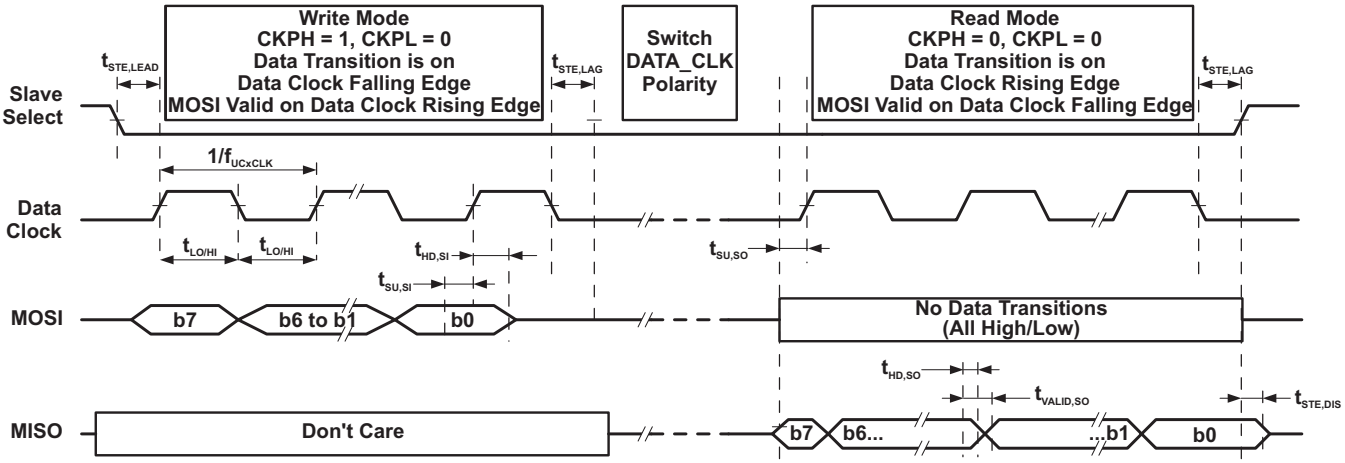


Figure 5-17. SPI With Slave Select Timing

The read command is sent out on the MOSI pin, MSB first, in the first eight clock cycles. MOSI data changes on the falling edge, and is validated in the reader on the rising edge, as shown in Figure 5-17. During the write cycle, the serial data out (MISO) is not valid. After the last read command bit (B0) is validated at the eighth rising edge of SCLK, after half a clock cycle, valid data can be read on the MISO pin at the falling edge of SCLK. It takes eight clock edges to read out the full byte (MSB first).

When using the hardware SPI (for example, an MSP430 hardware SPI) to implement this feature, care must be taken to switch the SCLK polarity after write phase for proper read operation. The example clock polarity for the MSP430-specific environment is shown in the write-mode and read-mode boxes of Figure 5-17. See the USART-SPI chapter for any specific microcontroller family for further information on the setting the appropriate clock polarity. This clock polarity switch must be done for all read (single, continuous) operations. The MOSI (serial data out) should not have any transitions (all high or all low) during the read cycle. The Slave Select should be low during the whole write and read operation.

See Section 3.5, Switching Characteristics, for the timing values shown in Figure 5-17.

The continuous read operation is shown in Figure 5-18.

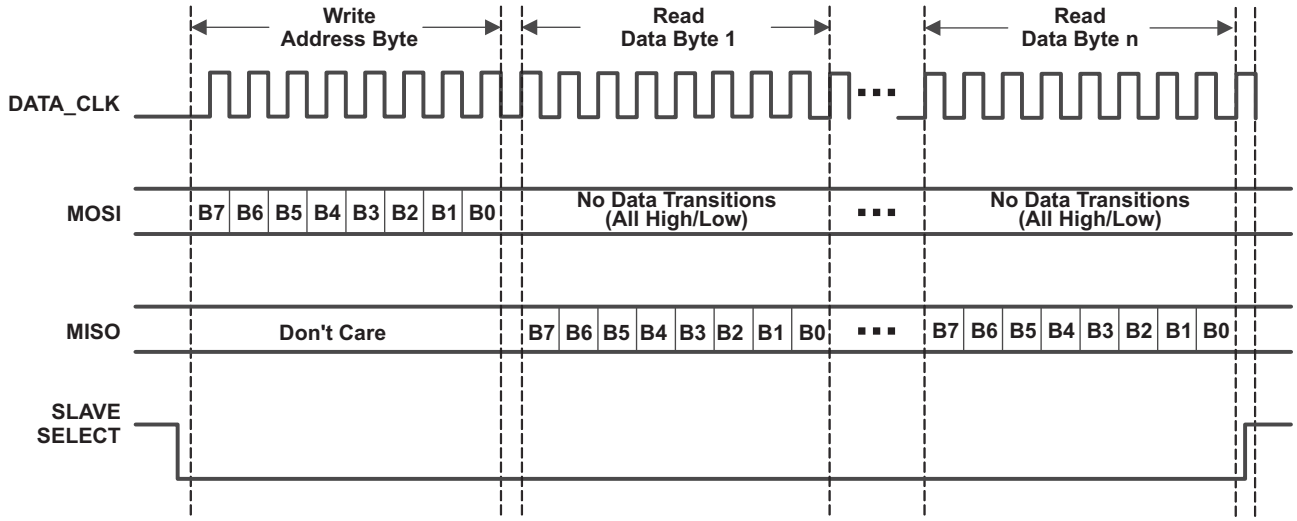


Figure 5-18. Continuous Read Operation Using SPI With Slave Select

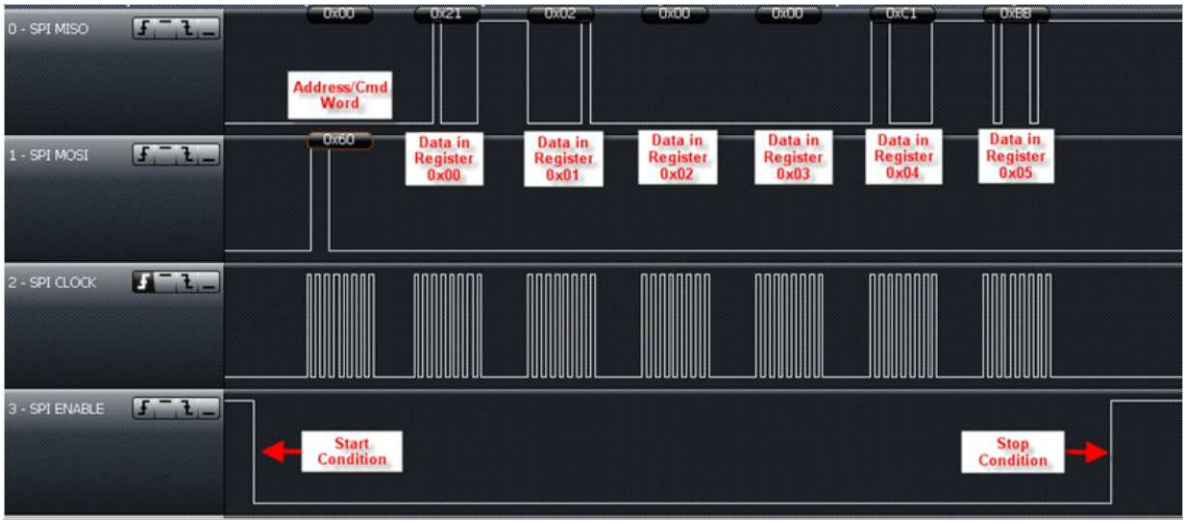


Figure 5-19. Continuous Read of Registers 0x00 Through 0x05 Using SPI With SS

5.12.5 Direct Mode

Direct mode allows the reader to be configured in one of two ways.

Direct Mode 0 (bit 6 = 0, as defined in ISO Control register) allows the application to use only the front-end functions of the reader, bypassing the protocol implementation in the reader. For transmit functions, the application has direct access to the transmit modulator through the MOD pin (pin 14). On the receive side, the application has direct access to the subcarrier signal (digitized RF envelope signal) on I/O_6 (pin 23).

Direct Mode 1 (bit 6 = 1, as defined in ISO Control register) uses the subcarrier signal decoder of the selected protocol (as defined in ISO Control register). This means that the receive output is not the subcarrier signal but the decoded serial bit stream and bit clock signals. The serial data is available on I/O_6 (pin 23), and the bit clock is available on I/O_5 (pin 22). The transmit side is identical; the application has direct control over the RF modulation through the MOD input. This mode is provided so that the application can implement a protocol that has the same bit coding as one of the protocols implemented in the reader, but needs a different framing format.

To select Direct Mode, first choose which Direct Mode to enter by writing B6 in the ISO Control register. This bit determines if the receive output is the direct subcarrier signal (B6 = 0) or the serial data of the selected decoder. If B6 = 1, then the application must also define which protocol should be used for bit decoding by writing the appropriate setting in the ISO Control register.

The reader actually enters the Direct Mode when B6 (direct) is set to 1 in the Chip Status Control register. Direct mode starts immediately. The write command should not be terminated with a stop condition (see communication protocol), because the stop condition terminates the Direct Mode and clears B6. This is necessary as the Direct Mode uses one or two I/O pins (I/O_6 and I/O_5). Normal parallel communication is not possible in Direct Mode. Sending a stop condition terminates Direct Mode.

Figure 5-20 shows the different configurations available in Direct Mode.

- In mode 0, the reader is used as an AFE only, and protocol handling is bypassed.
- In mode 1, framing is not done, but SOF and EOF are present. This allows for a user-selectable framing level based on an existing ISO standard.
- In mode 2, data is ISO standard formatted. SOF, EOF, and error checking are removed, so the microprocessor receives only bytes of raw data via a 12-byte FIFO.

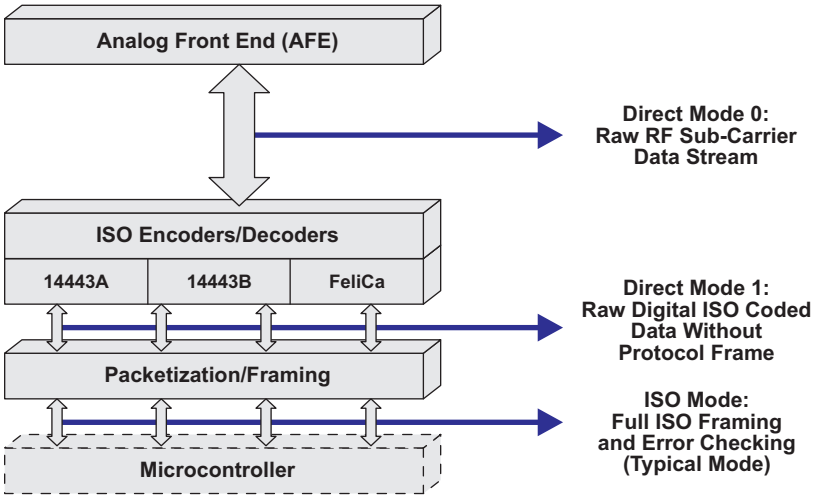


Figure 5-20. User-Configurable Modes

The steps to enter Direct Mode are listed below, using SPI with SS communication method only as one example, as Direct Mode(s) are also possible with parallel and SPI without SS. The application must enter Direct Mode 0 to accommodate non-ISO standard compliant card type communications. Direct Mode can be entered at any time, so that if a card type started with ISO standard communications, then deviated from the standard after being identified and selected, the ability to go into Direct Mode 0 becomes very useful.

Step 1: Configure pins I/O_0 to I/O_2 for SPI with SS

Step 2: Set pin 12 of the TRF7963A (ASK/OOK pin) to 0 for ASK or 1 for OOK

Step 3: Program the TRF7963A registers

The following registers need to be explicitly set before going into Direct Mode.

1. ISO Control register (0x01) to the appropriate standard:
   - 0x08 for ISO14443A (106 kbps)
   - 0x1A for FeliCa 212 kbps
   - 0x1B for FeliCa 424 kbps
2. Modulator and SYS_CLK Register (0x09) to the appropriate clock speed and modulation:
   - 0x21 for 6.78-MHz clock and OOK (100%) modulation
   - 0x20 for 6.78-MHz clock and ASK 10% modulation
   - 0x22 for 6.78-MHz clock and ASK 7% modulation
   - 0x23 for 6.78-MHz clock and ASK 8.5% modulation
   - 0x24 for 6.78-MHz clock and ASK 13% modulation
   - 0x25 for 6.78-MHz clock and ASK 16% modulation

   See register 0x09 definition for all other possible values.

   Example register setting for ISO14443A at 106 kbps:
   - ISO Control register (0x01) to 0x08
   - RX No Response Wait Time register (0x07) to 0x0E
   - RX Wait Time register (0x08) to 0x07
   - Modulator Control register (0x09) to 0x21 (or any custom modulation)
   - RX Special Settings register (0x0A) to 0x20

Step 4: Enter Direct Mode

The following registers must be reprogrammed to enter Direct Mode:

a. Set bit B6 of the Modulator and SYS_CLK Control register (0x09) to 1.

b. Set bit B6 of the ISO Control register (0x01) to 0 for Direct Mode 0 (default its 0)

c. Set bit B6 of the Chip Status Control register (0x00) to 1 to enter Direct Mode (do not send a Stop condition after this command)

NOTE

- It is important that the last write be NOT terminated with Stop condition. For SPI, this means that Slave Select (I/O_4) continues to stay low.
- Sending a Stop condition terminates the Direct Mode and clears bit B6 in the Chip Status Control register (0x00).

NOTE

Access to registers, FIFO, and IRQ is not available during Direct Mode 0.

Remember that the reader enters Direct Mode 0 when bit 6 of the Chip Status Control register (0x00) is set to a 1, and it stays in Direct Mode 0 until a Stop condition is sent from the microcontroller.

NOTE

The write command should not be terminated with a Stop condition (for example, in SPI mode this is done by bringing the SS line high after the register write), because the Stop condition terminates the Direct Mode and clears bit 6 of the Chip Status Control register (0x00), making it a 0.

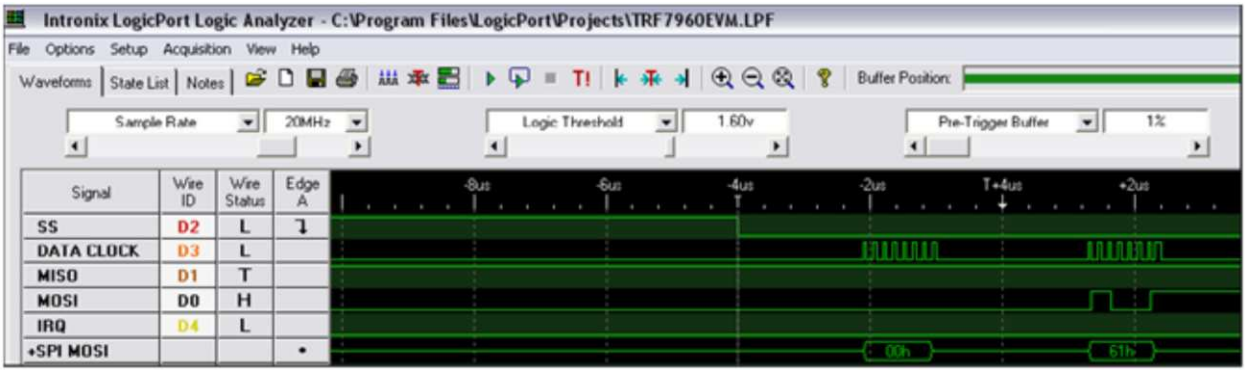


Figure 5-21. Entering Direct Mode 0

Step 5: Transmit data using Direct Mode

The user now has direct control over the RF modulation through the MOD input.

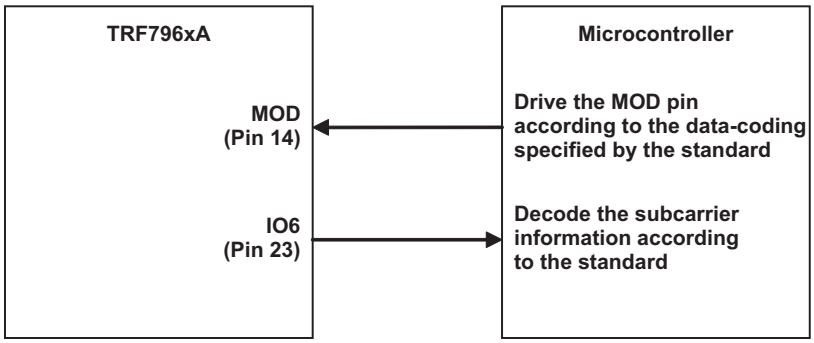


Figure 5-22. Control of RF Modulation Using MOD

The microcontroller is responsible for generating data according to the coding specified by the particular standard. The microcontroller must generate SOF, EOF, data, and CRC. In Direct Mode, the FIFO is not used and no IRQs are generated. See the applicable ISO standard to understand bit and frame definitions.

Step 6: Receive data using Direct Mode

After the TX operation is complete, the tag responds to the request and the subcarrier data is available on pin I/O_6. The microcontroller must decode the subcarrier signal according to the standard. This includes decoding the SOF, data bits, CRC, and EOF. The CRC then must be checked to verify data integrity. The receive data bytes must be buffered locally.

As an example of the receive data bits and framing level according to the ISO14443A standard is shown in Figure 5-23 (taken from ISO14443 specification and TRF7963A air interface).

- 128/fc = 9.435 µs = t_b (106-kbps data rate)
- 64/fc = 4.719 µs = t_x time
- 32/fc = 2.359 µs = t_1 time

Table 7 — Parameters for sequences

Parameter	Bit rate			
	fc/128	fc/64	fc/32	fc/16
t_b	128/fc	64/fc	32/fc	16/fc
t_x	64/fc	32/fc	16/fc	8/fc
t_1	see t_1 of Table 3	see t_1 of Table 5		

Figure 10 together with the timing parameters in Table 7 illustrate sequences X, Y and Z.

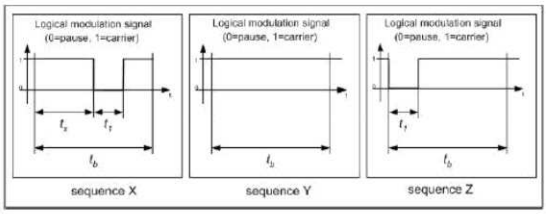


Figure 10 — Sequences for Type A communication PCD to PICC

The above sequences shall be used to code the following information:

— logic "1": sequence X,

— logic "0": sequence Y with the following two exceptions:

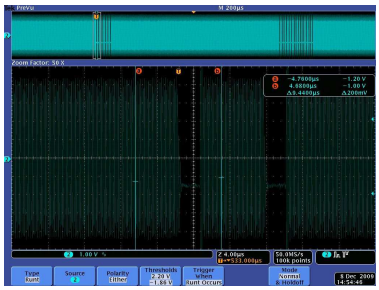
i) If there are two or more contiguous "0"s, sequence Z shall be used from the second "0" on,

ii) If the first bit after a "start of frame" is "0", sequence Z shall be used to represent this and any "0"s which follow directly thereafter,

— start of communication: sequence Z,

— end of communication: logic "0" followed by sequence Y,

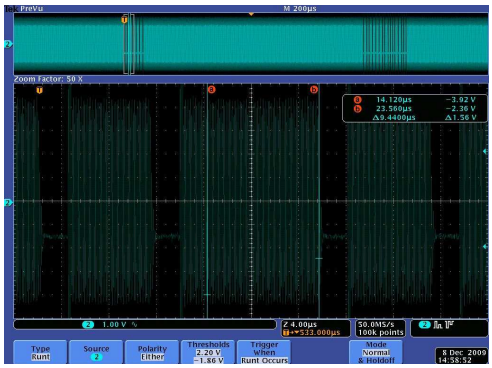
— no information: at least two sequences Y.



t_b = 9.44 µs

t_x = 4.72 µs

t_1 = 2.48 µs



Sequence Y = Carrier for 9.44 µs

Sequence Z = Pause for 2 to 3 µs,
Carrier for Remainder of 9.44 µs

Figure 5-23. Receive Data Bits and Framing Level (ISO14443A)

Step 7: Exit Direct Mode 0

When an EOF is received, data transmission is over, and Direct Mode 0 can be terminated by sending a Stop condition (the SS signal goes high). The TRF7963A returns to ISO Mode (normal mode).

5.13 Direct Commands from MCU to Reader

5.13.1 Command Codes

Table 5-11 lists the valid commands that the MCU can send to the reader.

Table 5-11. Command Codes

Command Code	Command	Comments
0x00	Idle	
0x03	Software Initialization	Same as power on reset
0x0F	Reset	
0x10	Transmission without CRC	
0x11	Transmission with CRC	
0x16	Block Receiver	
0x17	Enable Receiver	
0x18	Test external RF (RSSI at RX input with TX on)	
0x19	Test internal RF (RSSI at RX input with TX off)	
0x1A	Receiver Gain Adjust	

The command code values from Table 5-11 are substituted in Table 5-12, Bits 0 through 4. Also, the most-significant bit (MSB) in Table 5-12 must be set to 1.

Table 5-12. Address/Command Word Bit Distribution

Bit	Description	Bit Function	Address	Command
B7	Command control bit	0 = address 1 = command	0	1
B6	Read/Write	0 = write 1 = read	R/W	0
B5	Continuous address mode		Continuous mode	Not used
B4	Address/Command bit 4		Adr 4	Cmd 4
B3	Address/Command bit 3		Adr 3	Cmd 3
B2	Address/Command bit 2		Adr 2	Cmd 2
B1	Address/Command bit 1		Adr 1	Cmd 1
B0	Address/Command bit 0		Adr 0	Cmd 0

The MSB determines if the word is to be used as a command or address. The last two columns of Table 5-12 show the function of separate bits depending on whether address or command is written. Command mode is used to enter a command resulting in reader action (for example, initialize transmission, enable reader, or turn the reader on or off).

5.13.2 Reset (0x0F)

The reset command clears the FIFO contents and FIFO Status register (0x1C). It also clears the register storing the collision error location (0x0E).

5.13.3 Transmission With CRC (0x11)

The transmission command must be sent first, followed by transmission length bytes, and FIFO data. The reader starts transmitting after the first byte is loaded into the FIFO. The CRC byte is included in the transmitted sequence.

5.13.4 Transmission Without CRC (0x10)

The transmission command must be sent first, followed by transmission length bytes, and FIFO data. The reader starts transmitting after the first byte is loaded into the FIFO. This is the same as the previous section (Section 5.13.3), except that the CRC is not included.

5.13.5 Block Receiver (0x16)

The block receiver command puts the digital part of receiver (bit decoder and framer) in reset mode. This is useful in an extremely noisy environment, where the noise level could otherwise cause a constant switching of the subcarrier input of the digital part of the receiver. The receiver (if not in reset) would try to catch a SOF signal, and if the noise pattern matched the SOF pattern, an interrupt would be generated, falsely signaling the start of an receive operation. A constant flow of interrupt requests can be a problem for the external system (MCU), so the external system can stop this by putting the receive decoders in reset mode.

The reset mode can be terminated in two ways:

The external system can send the enable receiver command (see Section 5.13.6).

The reset mode is automatically terminated at the end of a transmit operation.

The receiver can stay in reset after end of transmit if the RX Wait Time register (0x08) is set. In this case, the receiver is enabled at the end of the wait time following the transmit operation.

5.13.6 Enable Receiver (0x17)

This command clears the reset mode in the digital part of the receiver if the reset mode was entered by the block receiver command.

5.13.7 Test Internal RF (RSSI at RX Input With TX On) (0x18)

The level of the RF carrier at RF_IN1 and RF_IN2 inputs is measured. Operating range between 300 mV_P and 2.1 V_P (step size is 300 mV). The two values are reported in the RSSI Levels register (0x0F). The command is intended for diagnostic purposes to set correct RF_IN levels. Optimum RFIN input level is approximately 1.6 V_P or code 5 to 6. The nominal relationship between the RF peak level and RSSI code is described in Table 5-13 and in Section 5.7.1.1.

NOTE

If the command is executed immediately after power-up and before any communication with tag was performed, the command must be preceded by the Enable RX command. The Check RF commands require full operation, so the receiver must be activated by enable receive or by a normal tag communication for the Check RF command to work properly.

Table 5-13. Test Internal RF

RF_IN1 (mV_P):	300	600	900	1200	1500	1800	2100
Decimal Code:	1	2	3	4	5	6	7
Binary Code:	001	010	011	001	101	011	111

5.13.8 Test External RF (RSSI at RX Input With TX Off) (0x19)

This command can be used in active mode when the RF receiver is on but RF output is off. This means bit B1 = 1 in the Chip Status Control register. The level of RF signal received on the antenna is measured and reported in the RSSI Levels register (0x0F). The relation between the 3-bit code and the external RF field strength [A/m] must be determinate by calculation or by experiments for each antenna type, because the antenna Q and connection to the RF input influence the result. The nominal relation between the RF peak to peak voltage in the RF_IN1 input and RSSI code is shown in Table 5-14 and in Section 5.7.1.2.

NOTE

If the command is executed immediately after power-up and before any communication with tag was performed, the command must be preceded by the Enable RX command. The Check RF commands require full operation, so the receiver must be activated by enable RX or by a normal tag communication for the Check RF command to work properly.

Table 5-14. Test External RF

RF_IN1 (mV_P):	40	60	80	100	140	180	300
Decimal Code:	1	2	3	4	5	6	7
Binary Code:	001	010	011	001	101	011	111

5.13.9 Receiver Gain Adjust (0x1A)

This command should be executed when the MCU determines that no tag response is detected and when the RF and receivers are on. When this command is received, the reader observes the digitized receiver output. If more than two edges are observed in 100 ms, the window comparator voltage is increased. The procedure is repeated until the number of edges (changes of logical state) of the digitized reception signal is less than 2 (in 100 ms). The command can reduce the input sensitivity in 5-dB increments up to 15 dB. This command ensures better operation in a noisy environment. The gain setting is reset to maximum gain at EN = 0, POR = 1.

5.13.10 Register Preset

After power-up and the EN pin low-to-high transition, the registers are in a default mode, which must be changed by writing the desired ISO protocol settings to the ISO Control register. The low-level option registers (0x02 to 0x0B) are automatically configured to the new protocol parameters. After selecting the protocol, it is possible to change some low-level register contents if needed. However, changing to another protocol and then back reloads the default settings; therefore, the custom settings must be reloaded.

The Clo0 and Clo1 bits in the Modulator and SYS_CLK Control register (0x09), which define the microcontroller frequency available on the SYS_CLK pin, are the only two bits in the configuration registers that are not cleared during protocol selection.

6 Register Description

6.1 Register Overview

Table 6-1 lists the registers available in the TRF7963A. These registers are described in the following sections.

Table 6-1. Register Overview

Address (hex)	Register	Read/Write	Section
Main Control Registers			
0x00	Chip Status Control	R/W	Section 6.1.1.1
0x01	ISO Control	R/W	Section 6.1.1.2
Protocol Sub-Setting Registers			
0x02	ISO14443B TX Options	R/W	Section 6.1.2.1
0x03	ISO14443A High Bit Rate Options	R/W	Section 6.1.2.2
0x06	TX Pulse-Length Control	R/W	Section 6.1.2.3
0x07	RX No Response Wait	R/W	Section 6.1.2.4
0x08	RX Wait Time	R/W	Section 6.1.2.5
0x09	Modulator and SYS_CLK Control	R/W	Section 6.1.2.6
0x0A	RX Special Setting	R/W	Section 6.1.2.7
0x0B	Regulator and I/O Control	R/W	Section 6.1.2.8
Status Registers			
0x0C	IRQ Status	R	Section 6.1.3.1
0x0D	Collision Position and Interrupt Mask Register	R/W	Section 6.1.3.2
0x0E	Collision Position	R	Section 6.1.3.2
0x0F	RSSI Levels and Oscillator Status	R	Section 6.1.3.3
FIFO Registers			
0x1A	Test	R/W	Section 6.1.4.1
0x1B	Test	R/W	Section 6.1.4.2
0x1C	FIFO Status	R	Section 6.1.5.1
0x1D	TX Length Byte1	R/W	Section 6.1.5.2
0x1E	TX Length Byte2	R/W	Section 6.1.5.2
0x1F	FIFO I/O Register	R/W	

6.1.1 Main Configuration Registers

6.1.1.1 Chip Status Control Register (0x00)

Table 6-2. Chip Status Control Register (0x00)

Function: Control of power mode, RF on/off, AGC, AM/PM, Direct Mode			
Default Settings: Register default is 0x01. It is preset at EN = L or POR = H			
Bit No.	**Bit Name**	**Function**	**Description**
B7	stby	1 = Standby Mode	Standby mode keeps all supply regulators and the 13.56-MHz SYS_CLK oscillator running (typical start-up time to full operation is 100 µs).
		0 = Active Mode	Active Mode (default)
B6	direct	1 = Direct Mode 0/1	Provides user direct access to AFE (Direct Mode 0) or allows user to add their own framing (Direct Mode 1). Bit 6 of ISO Control register must be set by user before entering Direct Mode 0 or 1.
		0 = ISO Mode (default)	Uses SPI or parallel communication with automatic framing and ISO decoders
B5	rf_on	1 = RF output active	Transmitter on, receivers on
		0 = RF output not active	Transmitter off
B4	rf_pwr	1 = Half output power	TX_OUT (pin 5) = 8-Ω output impedance P = 100 mW (+20 dBm) at 5 V, P = 33 mW (+15 dBm) at 3.3 V
		0 = Full output power	TX_OUT (pin 5) = 4-Ω output impedance P = 200 mW (+23 dBm) at 5 V, P = 70 mW (+18 dBm) at 3.3 V
B3	pm_on	1 = Selects Main RX input	RX_IN1 input is used
		0 = Selects Aux RX input	RX_IN2 input is used
B2	agc_on	1 = AGC on	Enables AGC (AGC gain can be set in register 0x0A)
		0 = AGC off	AGC block is disabled
B1	rec_on	1 = Receiver activated for external field measurement	Forces enabling of receiver and TX oscillator. Used for external field measurement.
		0 = Automatic enable	Allows enable of the receiver via bit 5 of this register
B0	vrs5_3	1 = 5-V operation	Selects the VIN voltage range
		0 = 3-V operation	

6.1.1.2 ISO Control Register (0x01)

Table 6-3. ISO Control Register (0x01)

Function: Controls the selection of ISO standard protocol, Direct Mode, and receive CRC			
Default Settings: Register default is 0x02 . It is reset at EN = L or POR = H.			
Bit No.	**Bit Name**	**Function**	**Description**
B7	rx_crc_n	CRC receive selection	1 = no RX CRC (CRC not present in the response) 0 = RX CRC (CRC is present in the response)
B6	dir_mode	Direct mode type selection	0 = Direct Mode 0 1 = Direct Mode 1
B5	rfid	RFID / Reserved	0 = RFID mode 1 = Reserved (should be set to 0)
B4	iso_4	RFID	See Table 6-4 for B0:B4 settings based on the ISO protocol that the application requires
B3	iso_3	RFID	
B2	iso_2	RFID	
B1	iso_1	RFID	
B0	iso_0	RFID	

Table 6-4. ISO Control Register: ISO_4 to ISO_0

ISO_4	ISO_3	ISO_2	ISO_1	ISO_0	Protocol	Remarks
0	1	0	0	0	ISO14443A RX bit rate, 106 kbps	RX bit rate(1)
0	1	0	0	1	ISO14443A RX high bit rate, 212 kbps	
0	1	0	1	0	ISO14443A RX high bit rate, 424 kbps	
0	1	0	1	1	ISO14443A RX high bit rate, 848 kbps	
0	1	1	0	0	ISO14443B RX bit rate, 106 kbps	RX bit rate(1)
0	1	1	0	1	ISO14443B RX high bit rate, 212 kbps	
0	1	1	1	0	ISO14443B RX high bit rate, 424 kbps	
0	1	1	1	1	ISO14443B RX high bit rate, 848 kbps	
1	1	0	1	0	FeliCa 212 kbps	
1	1	0	1	1	FeliCa 424 kbps	

(1) For ISO14443A/B, when bit rate of TX is different from RX, settings can be done in REG (0x02 or 0x03)

6.1.2 Protocol Sub-Setting Registers

6.1.2.1 ISO14443B TX Options Register (0x02)

Table 6-5. ISO14443B TX Options Register (0x02)

Function: Selects the ISO subsets for ISO14443B – TX			
Default Settings: 0x00 at POR = H or EN = L			
Bit No.	**Bit Name**	**Function**	**Description**
B7	egt2	TX EGT time select MSB	Three bit code defines the number of etu (0 to 7) that separate two characters. ISO14443B TX only.
B6	egt1	TX EGT time select	
B5	egt0	TX EGT time select LSB	
B4	eof_l0	1 = EOF → 0 length 11 etu 0 = EOF → 0 length 10 etu	ISO14443B TX only
B3	sof_l1	1 = SOF → 1 length 03 etu 0 = SOF → 1 length 02 etu	
B2	sof _l0	1 = SOF → 0 length 11 etu 0 = SOF → 0 length 10 etu	
B1	l_egt	1 = EGT after each byte 0 = EGT after last byte is omitted	
B0	Unused		

6.1.2.2 ISO14443A High-Bit-Rate and Parity Options Register (0x03)

Table 6-6. ISO14443A High-Bit-Rate and Parity Options Register (0x03)

Function: Selects the ISO subsets for ISO14443A – TX			
Default Settings: 0x00 at POR = H or EN = L, and at each write to ISO Control register			
Bit No.	**Bit Name**	**Function**	**Description**
B7	dif_tx_br	TX bit rate different than RX bit rate enable	Valid for ISO14443A/B high bit rate
B6	tx_br1	TX bit rate	tx_br1 = 0, tx_br = 0: 106 kbps tx_br1 = 0, tx_br = 1: 212 kbps tx_br1 = 1, tx_br = 0: 424 kbps tx_br1 = 1, tx_br = 1: 848 kbps
B5	tx_br0		
B4	parity-2tx	1 = parity odd except last byte, which is even for TX	For ISO14443A high bit rate coding and decoding
B3	parity-2rx	1 = parity odd except last byte, which is even for RX	
B2	Unused		
B1	Unused		
B0	Unused		

6.1.2.3 TX Pulse Length Control Register (0x06)

The length of the modulation pulse is defined by the protocol selected in the ISO Control register (0x01). With a high-Q antenna, the modulation pulse is typically prolonged, and the tag detects a longer pulse than intended. For such cases, the modulation pulse length can be corrected by using the TX pulse length register 0x06. If the register contains all zeros, then the pulse length is governed by the protocol selection. If the register contains a value other than 0x00, the pulse length is equal to the value of the register in 73.7-ns increments. This means the range of adjustment can be 73.7 ns to 18.8 µs.

Table 6-7. TX Pulse Length Control Register (0x06)

Function: Controls the length of TX pulse			
Default Settings: Default is set to 0x00 at POR = H or EN = L and at each write to ISO Control register.			
Bit No.	**Bit Name**	**Function**	**Description**
B7	Pul_p2	Pulse length MSB	The pulse range is 73.7 ns to 18.8 µs (1 to 255), step size 73.7 ns All bits low (00): pulse length control is disabled The following default timings are preset by the ISO Control register (0x01): 2.36 µs → ISO14443A at 106 kbps 1.4 µs → ISO14443A at 212 kbps 737 ns → ISO14443A at 424 kbps 442 ns → ISO14443A at 848 kbps; pulse length control disabled
B6	Pul_p1		
B5	Pul_p0		
B4	Pul_c4		
B3	Pul_c3		
B2	Pul_c2		
B1	Pul_c1		
B0	Pul_c0	Pulse length LSB	

6.1.2.4 RX No Response Wait Time Register (0x07)

The RX no response timer is controlled by the RX No Response Wait Time register. This timer measures the time from the start of slot in the anticollision sequence until the start of tag response. If there is no tag response in the defined time, an interrupt request is sent and a flag is set in IRQ Status Control register (0x0C). This enables the external controller to be relieved of the task of detecting empty slots. The wait time is stored in the register in increments of 37.76 µs. This register is also preset, automatically, for every new protocol selection.

Table 6-8. RX No Response Wait Time Register (0x07)

Function: Defines the time when "no response" interrupt is sent			
Default Settings: Default is set to 0x0E at POR = H or EN = L and at each write to ISO Control register.			
Bit No.	**Bit Name**	**Function**	**Description**
B7	NoResp7	No response MSB	Defines the time when *no response* interrupt is sent. It starts from the end of TX EOF. RX no response wait range is 37.76 µs to 9628 µs (1 to 255). Step size is 37.76 µs. The following default timings are preset by the ISO Control register (0x01): 529 µs → for all protocols
B6	NoResp6		
B5	NoResp5		
B4	NoResp4		
B3	NoResp3		
B2	NoResp2		
B1	NoResp1		
B0	NoResp0	No response LSB	

6.1.2.5 RX Wait Time Register (0x08)

The RX wait time timer is controlled by the value in the RX Wait Time register. This timer defines the time after the end of the transmit operation in which the receive decoders are not active (held in reset state). This prevents incorrect detections resulting from transients following the transmit operation. The value of the RX wait time register defines this time in increments of 9.44 µs. This register is preset at every write to ISO Control register according to the minimum tag response time defined by each standard.

Table 6-9. RX Wait Time Register (0x08)

Function: Defines the time after TX EOF when the RX input is disregarded; for example, to block out electromagnetic disturbance generated by the responding card.			
Default Settings: Default is set to 0x1F at POR = H or EN = L and at each write to the ISO control register.			
Bit No.	**Bit Name**	**Function**	**Description**
B7	Rxw7	RX wait time	Defines the time after the TX EOF during which the RX input is ignored. Time starts from the end of TX EOF. RX wait range is 9.44 µs to 2407 µs (1 to 255). Step size is: 9.44 µs. The following default timings are preset by the ISO Control register (0x01): 9.44 µs → FeliCa 66 µs → ISO14443A and B
B6	Rxw6		
B5	Rxw5		
B4	Rxw4		
B3	Rxw3		
B2	Rxw2		
B1	Rxw1		
B1	Rxw0		

6.1.2.6 Modulator and SYS_CLK Control Register (0x09)

The frequency of SYS_CLK (pin 27) is programmable by the bits B4 and B5 of this register. The frequency of the TRF7963A system clock oscillator is divided by 1, 2 or 4 resulting in available SYS_CLK frequencies of 13.56 MHz or 6.78 MHz or 3.39 MHz.

The ASK modulation depth is controlled by bits B0, B1 and B2. The range of ASK modulation is 7% to 30% or 100% (OOK). The selection between ASK and OOK (100%) modulation can also be done using direct input OOK (pin 12). The direct control of OOK/ASK using OOK pin is only possible if the function is enabled by setting B6 = 1 (en_ook_p) in this register (0x09) and the ISO Control register (0x01, B6 = 1). When configured this way, the MOD (pin 14) is used as input for the modulation signal.

Table 6-10. Modulator and SYS_CLK Control Register (0x09)

Function: Controls the modulation input and depth, ASK / OOK control and clock output to an external system (an MCU)						
Default Settings: Default is set to 0x11 at POR = H or EN = L, and at each write to the ISO Control register, except Clo1 and Clo0.						
Bit No.	**Bit Name**	**Function**	**Description**			
B7	Unused					
B6	en_ook_p	1 = enables external selection of ASK or OOK modulation 0 = default operation as defined in bits B0 to B2 of this register	Enable ASK/OOK pin (pin 12) for "on the fly change" between any pre-selected ASK modulation as defined by B0 to B2 and OOK modulation. If B6 is set to 1, pin 12 is configured as follows: 1 = OOK modulation 0 = Modulation as defined in B0 to B2 (0x09)			
B5	Clo1	SYS_CLK output frequency MSB	**Clo1**	**Clo0**	**SYS_CLK Output**	
			0	0	Disabled	
			0	1	3.39 MHz	
B4	Clo0	SYS_CLK output frequency LSB	1	0	6.78 MHz	
			1	1	13.56 MHz	
B3	en_ana	1 = sets pin 12 (ASK/OOK) as an analog output 0 = default	For test and measurement purpose. ASK/OOK pin 12 can be used to monitor the analog subcarrier signal before the digitizing with DC level equal to AGND.			
B2	Pm2	Modulation depth MSB	**Pm2**	**Pm1**	**Pm0**	**Modulation Type and Percentage**
			0	0	0	ASK 10%
			0	0	1	OOK (100%)
B1	Pm1	Modulation depth	0	1	0	ASK 7%
			0	1	1	ASK 8.5%
			1	0	0	ASK 13%
B0	Pm0	Modulation depth LSB	1	0	1	ASK 16%
			1	1	0	ASK 22%
			1	1	1	ASK 30%

6.1.2.7 RX Special Setting Register (0x0A)

Table 6-11. RX Special Setting Register (0x0A)

Function: Sets the gains and filters directly			
Default Settings: Default is set to 0x40 at POR = H or EN = L, and at each write to the ISO Control register (0x01). When bits B7, B6, B5 and B4 are all zero, the filters are set for ISO14443B (240 kHz to 1.4 MHz).			
Bit No.	**Bit Name**	**Function**	**Description**
B7	C212	Bandpass 110 kHz to 570 kHz	Appropriate for 212-kHz subcarrier system (FeliCa)
B6	C424	Bandpass 200 kHz to 900 kHz	
B5	M848	Bandpass 450 kHz to 1.5 MHz	Appropriate for Manchester-coded 848-kHz subcarrier used in ISO14443A
B4	hbt	Bandpass 100 kHz to 1.5 MHz Gain reduced for 18 dB	Appropriate for highest bit rate (848 kbps) used in high-bit-rate ISO14443
B3	gd1	00 = gain reduction 0 dB 01 = gain reduction for 5 dB 10 = gain reduction for 10 dB 11 = gain reduction for 15 dB	Sets the RX gain reduction and reduces sensitivity
B2	gd2		
B1	agcr	AGC activation level change	AGC activation level changed from five times the digitizing level to three times the digitizing level. 1 = 3x 0 = 5x
B0	no-lim	AGC action is not limited in time	AGC action can be done any time during receive process. It is not limited to the start of receive ("max hold"). 1 = continuously, no time limit 0 = 8 subcarrier pulses

The first four steps of the AGC control are comparator adjustment. The second three steps are gain reduction done automatically by AGC control. The AGC is turned on after TX.

The first gain and filtering stage following the RF envelope detector has a nominal gain of 15, and the 3-dB band-pass frequencies are adjustable in the range from 100 kHz to 400 kHz for high pass and 600 kHz to 1.5 MHz for low pass. The next gain and filtering stage has a nominal gain of 8, and the frequency characteristic identical to first stage. The filter setting is done automatically with internal preset for each new selection of communication standard in the ISO Control register. Additional corrections can be done by directly writing into the RX Special Setting register.

The second receiver gain stage and digitizer stage are included in the AGC loop. The AGC loop can be activated by setting the bit B2 = 1 (agc-on) in the Chip Status Control register. If activated the AGC monitors the signal level at the input of digitizing stage. If the signal level is significantly higher than the digitizing threshold level, the gain reduction is activated. The signal level, at which the action is started, is by default five times the digitizing threshold level. It can be reduced to three times the digitizing level by setting bit B1 = 1 (agcr) in the RX Special Setting register.

The AGC action typically finishes after four subcarrier pulses. By default, the AGC action is blocked after first few pulses of subcarrier signal so AGC cannot interfere with signal reception during rest of data packet. In certain cases, this is not optimal, so this blocking can be removed by setting B0 = 1 (no_lim) in the RX Special Setting register.

NOTE

The setting of bits b4, b5, b6, and b7 to zero selects bandpass characteristic of 240 kHz to 1.4 MHz. This is appropriate for ISO14443B, FeliCa protocol, and ISO14443A higher bit rates 212 kbps and 424 kbps.

6.1.2.8 Regulator and I/O Control Register (0x0B)

Table 6-12. Regulator and I/O Control Register (0x0B)

Function: Control the three voltage regulators			
Default Settings: Default is set to 0x87 at POR = H or EN = L			
Bit No.	**Bit Name**	**Function**	**Description**
B7	auto_reg	0 = Manual system 1 = Automatic system	Automatic system settings: VDD_RF = VIN – 250 mV VDD_A = VIN – 250 mV VDD_X = VIN – 250 mV, but not higher than 3.4 V Manual system settings: See B2 to B0
B6	en_ext_pa	Support for external power amplifier	Internal peak detectors are disabled, receiver inputs (RX_IN1 and RX_IN2) accept externally demodulated subcarrier. At the same time, the ASK/OOK pin becomes modulation output for external TX amplifier.
B5	io_low	1 = Enable low peripheral communication voltage	When B5 = 1, maintains the output driving capabilities of the I/O pins connected to the level shifter under low-voltage operation. Should be set 1 when VDD_I/O voltage is between 1.8 V and 2.7 V.
B4	Unused	No function	Default is 0.
B3	Unused	No function	Default is 0.
B2	vrs2	Voltage set MSB	vrs3_5 = L: VDD_RF, VDD_A, VDD_X range 2.7 V to 3.4 V. See Table 6-13 through Table 6-16.
B1	vrs1		
B0	vrs0	Voltage set LSB	

Table 6-13. Supply Regulator Setting, Manual 5-V System

Register	**Option Bits Setting in Control Register**								**Action**
	B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	
00								1	5-V system
0B	0								Manual regulator setting
0B	0					1	1	1	VDD_RF = 5 V, VDD_A = 3.5 V, VDD_X = 3.4 V
0B	0					1	1	0	VDD_RF = 4.9 V, VDD_A = 3.5 V, VDD_X = 3.4 V
0B	0					1	0	1	VDD_RF = 4.8 V, VDD_A = 3.5 V, VDD_X = 3.4 V
0B	0					1	0	0	VDD_RF = 4.7 V, VDD_A = 3.5 V, VDD_X = 3.4 V
0B	0					0	1	1	VDD_RF = 4.6 V, VDD_A = 3.5 V, VDD_X = 3.4 V
0B	0					0	1	0	VDD_RF = 4.5 V, VDD_A = 3.5 V, VDD_X = 3.4 V
0B	0					0	0	1	VDD_RF = 4.4 V, VDD_A = 3.5 V, VDD_X = 3.4 V
0B	0					0	0	0	VDD_RF = 4.3 V, VDD_A = 3.5 V, VDD_X = 3.4 V

Table 6-14. Supply Regulator Setting, Manual 3-V System

Register	Option Bits Setting in Control Register								Action
	B7	B6	B5	B4	B3	B2	B1	B0	
00								0	3-V system
0B	0								Manual regulator setting
0B	0					1	1	1	VDD_RF = 3.4 V, VDD_A = 3.4 V, VDD_X = 3.4 V
0B	0					1	1	0	VDD_RF = 3.3 V, VDD_A = 3.3 V, VDD_X = 3.3 V
0B	0					1	0	1	VDD_RF = 3.2 V, VDD_A = 3.2 V, VDD_X = 3.2 V
0B	0					1	0	0	VDD_RF = 3.1 V, VDD_A = 3.1 V, VDD_X = 3.1 V
0B	0					0	1	1	VDD_RF = 3.0 V, VDD_A = 3.0 V, VDD_X = 3.0 V
0B	0					0	1	0	VDD_RF = 2.9 V, VDD_A = 2.9 V, VDD_X = 2.9 V
0B	0					0	0	1	VDD_RF = 2.8 V, VDD_A = 2.8 V, VDD_X = 2.8 V
0B	0					0	0	0	VDD_RF = 2.7 V, VDD_A = 2.7 V, VDD_X = 2.7 V

Table 6-15. Supply Regulator Setting, Automatic 5-V System

Register	Option Bits Setting in Control Register								Action
	B7	B6	B5	B4	B3	B2 (1)	B1	B0	
00								1	5-V system
0B	1					x	1	1	Automatic regulator setting 250-mV difference
0B	1					x	1	0	Automatic regulator setting 350-mV difference
0B	1					x	0	0	Automatic regulator setting 400-mV difference

(1) x = don't care

Table 6-16. Supply Regulator Setting, Automatic 3-V System

Register	Option Bits Setting in Control Register								Action
	B7	B6	B5	B4	B3	B2 (1)	B1	B0	
00								0	3-V system
0B	1					x	1	1	Automatic regulator setting 250-mV difference
0B	1					x	1	0	Automatic regulator setting 350-mV difference
0B	1					x	0	0	Automatic regulator setting 400-mV difference

(1) x = don't care

6.1.3 Status Registers

6.1.3.1 IRQ Status Register (0x0C)

Table 6-17. IRQ Status Register (0x0C)

Function: Information available about TRF7963A IRQ and TX/RX status			
Default Settings: Default is set to 0x00 at POR = H or EN = L, and at each write to the ISO Control Register 0x01. It is also automatically reset at the end of a read phase. The reset also removes the IRQ flag.			
Bit No.	**Bit Name**	**Function**	**Description**
B7	Irq_tx	IRQ set due to end of TX	Signals that TX is in progress. The flag is set at the start of TX but the interrupt request (IRQ = 1) is sent when TX is finished.
B6	Irg_srx	IRQ set due to RX start	Signals that RX SOF was received and RX is in progress. The flag is set at the start of RX but the interrupt request (IRQ = 1) is sent when RX is finished.
B5	Irq_fifo	FIFO is high or low	Signals when the FIFO is high or low (more than 8 bits during RX or less than 4 bits during TX). See Section 5.12.2 for details.
B4	Irq_err1	CRC error	Indicates receive CRC error only if B7 (no RX CRC) of ISO Control register is set to 0.
B3	Irq_err2	Parity error	Indicates parity error for ISO14443A
B2	Irq_err3	Byte framing or EOF error	Indicates framing error
B1	Irq_col	Collision error	Collision error for ISO14443A . Bit is set if more then 6 or 7 (as defined in register 0x01) are detected inside one bit period of ISO14443A 106 kbit/s. Collision error bit can also be triggered by external noise.
B0	Irq_noresp	No-response time interrupt	No response within the "No-response time" defined in RX No-response Wait Time register (0x07).

To reset (clear) the register 0x0C and the IRQ line, the register must be read. During transmit, the decoder is disabled, and only bits B5 and B7 can be changed. During receive, only bit B6 can be changed, but does not trigger the IRQ line immediately. The IRQ signal is set at the end of the transmit or receive phase.

6.1.3.2 Collision Position and Interrupt Mask Registers (0x0D and 0x0E)

Table 6-18. Collision Position and Interrupt Mask Register (0x0D)

Default Settings: Default is set to 0x3E at POR = H and EN = L. Collision bits reset automatically after read operation.			
Bit No.	**Bit Name**	**Function**	**Description**
B7	Col9	Bit position of collision MSB	Supports ISO14443A
B6	Col8	Bit position of collision	
B5	En_irq_fifo	Interrupt enable for FIFO	Default = 1
B4	En_irq_err1	Interrupt enable for CRC	Default = 1
B3	En_irq_err2	Interrupt enable for Parity	Default = 1
B2	En_irq_err3	Interrupt enable for Framing error or EOF	Default = 1
B1	En_irq_col	Interrupt enable for collision error	Default = 1
B0	En_irq_noresp	Enables no-response interrupt	Default = 0

Table 6-19. Collision Position Register (0x0E)

Function: Displays the bit position of collision or error			
Default Settings: Default is set to 0x00 at POR = H and EN = L. Automatically reset after read operation.			
Bit No.	**Bit Name**	**Function**	**Description**
B7	Col7	Bit position of collision MSB	ISO14443A mainly supported; in the other protocols, this register shows the bit position of error. Either frame, SOF/EOF, parity, or CRC error.
B6	Col6		
B5	Col5		
B4	Col4		
B3	Col3		
B2	Col2		
B1	Col1		
B0	Col0	Bit position of collision LSB	

6.1.3.3 RSSI Levels and Oscillator Status Register (0x0F)

Table 6-20. RSSI Levels and Oscillator Status Register (0x0F)

Function: Displays the signal strength on both reception channels and RF amplitude during RF-off state. The RSSI values are valid from reception start until the start of the next transmission.			
Bit No.	**Bit Name**	**Function**	**Description**
B7	Unused		
B6	osc_ok	Crystal oscillator stable indicator	13.56-MHz frequency stable (approximately 200 µs)
B5	rssi_x2	MSB RSSI value of auxiliary RX (RX_IN2)	Auxiliary channel is by default RX_IN2. The input can be swapped by B3 = 1 (Chip State Control register). If "swapped", the auxiliary channel is connected to RX_IN1 and the auxiliary RSSI represents the signal level at RX_IN1.
B4	rssi_x1	Auxiliary channel RSSI	
B3	rssi_x0	MSB RSSI value of auxiliary RX (RX_IN2)	
B2	rssi_2	MSB RSSI value of Main RX (RX_IN1)	Active channel is the default and can be set with option bit B3 = 0 of the Chip Status Control register (0x00).
B1	rssi_1	Main channel RSSI	
B0	rssi_0	LSB RSSI value of Main RX (RX_IN1)	

RSSI measurement block is measuring the demodulated envelope signal (except in case of direct command for RF amplitude measurement described later in direct commands section). The measuring system is latching the peak value, so the RSSI level can be read after the end of receive packet. The RSSI value is reset during next transmit action of the reader, so the new tag response level can be measured. The RSSI levels calculated to the RF_IN1 and RF_IN2 are shown in Section 5.7.1.1 and Section 5.7.1.2. The RSSI has 7 steps (3 bits) with 4-dB increment. The input level is the peak to peak modulation level of RF signal measured on one side envelope (positive or negative).

6.1.4 Test Registers

6.1.4.1 Test Register (0x1A)

Table 6-21. Test Register (0x1A) (for Test or Direct Use)

Default Settings: Default is set to 0x00 at POR = H and EN = L.			
Bit No.	**Bit Name**	**Function**	**Description**
B7	OOK_Subc_In	Subcarrier input	OOK Pin becomes decoder digital input
B6	MOD_Subc_Out	Subcarrier output	MOD Pin becomes receiver subcarrier output
B5	MOD_Direct	Direct TX modulation and RX reset	MOD Pin becomes receiver subcarrier output
B4	o_sel	First stage output selection	0 = First stage output used for analog out and digitizing 1 = Second stage output used for analog out and digitizing
B3	low2	Second stage gain -6 dB, HP corner frequency/2	
B2	low1	First stage gain -6 dB, HP corner frequency/2	
B1	zun	Input followers test	
B0	Test_AGC	AGC test, AGC level is seen on rssi_210 bits	

6.1.4.2 Test Register (0x1B)

Table 6-22. Test Register (0x1B) (for Test or Direct Use)

Default Settings: Default is set to 0x00 at POR = H and EN = L. When a test_dec or test_io is set, IC is switched to test mode. Test Mode persists until a stop condition arrives. At stop condition the test_dec and test_io bits are cleared.			
Bit No.	**Bit Name**	**Function**	**Description**
B7	test_rf_level	RF level test	
B6			
B5			
B4			
B3	test_io1	I/O test	Not implemented
B2	test_io0		
B1	test_dec	Decoder test mode	
B0	clock_su	Coder clock 13.56 MHz	For faster test of coders

6.1.5 FIFO Control Registers

6.1.5.1 FIFO Status Register (0x1C)

Table 6-23. FIFO Status Register (0x1C)

Function: Low nibbles of complete bytes to be transferred through FIFO. Information about a broken byte and number of bits to be transferred from it			
Bit No.	**Bit Name**	**Function**	**Description**
B7	RFU	B7 = 0	Reserved for future use (RFU)
B6	Fhil	FIFO level high	Indicates that 9 bytes are already in the FIFO (for RX) (also see register 0x0C bit 5)
B5	Flol	FIFO level low	Indicates that only 3 bytes are in the FIFO (for TX) (also see register 0x0C bit 5)
B4	Fove	FIFO overflow error	Too many bytes were written to the FIFO
B3	Fb3	FIFO bytes fb[3]	Bits B0:B3 indicate how many bytes that are loaded in FIFO were not read out yet (displays N – 1 number of bytes). If 8 bytes are in the FIFO, this number is 7 (also see register 0x0C bit 6).
B2	Fb2	FIFO bytes fb[2]	
B1	Fb1	FIFO bytes fb[1]	
B0	Fb0	FIFO bytes fb[0]	

6.1.5.2 TX Length Byte1 Register (0x1D) and TX Length Byte2 Register (0x1E)

Table 6-24. TX Length Byte1 Register (0x1D)

Function: High two nibbles of complete intended bytes to be transferred through FIFO			
Default Settings: Default is set to 0x00 at POR and EN = 0. It is also automatically reset at TX EOF.			
Bit No.	**Bit Name**	**Function**	**Description**
B7	Txl11	Number of complete byte bn[11]	High nibble of complete intended bytes to be transmitted
B6	Txl10	Number of complete byte bn[10]	
B5	Txl9	Number of complete byte bn[9]	
B4	Txl8	Number of complete byte bn[8]	
B3	Txl7	Number of complete byte bn[7]	High nibble of complete intended bytes to be transmitted
B2	Txl6	Number of complete byte bn[6]	
B1	Txl5	Number of complete byte bn[5]	
B0	Txl4	Number of complete byte bn[4]	

Table 6-25. TX Length Byte2 Register (0x1E)

Function: Low nibbles of complete bytes to be transferred through FIFO. Information about a broken byte and number of bits to be transferred from it.			
Default Settings: Default is set to 0x00 at POR and EN = 0. It is also automatically reset at TX EOF.			
Bit No.	**Bit Name**	**Function**	**Description**
B7	Txl3	Number of complete byte bn[3]	High nibble of complete intended bytes to be transmitted
B6	Txl2	Number of complete byte bn[2]	
B5	Txl1	Number of complete byte bn[1]	
B4	Txl0	Number of complete byte bn[0]	
B3	Bb2	Broken byte number of bits bb[2]	Number of bits in the last broken byte to be transmitted. It is taken into account only when broken byte flag is set.
B2	Bb1	Broken byte number of bits bb[1]	
B1	Bb0	Broken byte number of bits bb[0]	
B0	Bbf	Broken byte flag	B0 = 1 indicates that last byte is not complete 8 bits wide.

7 System Design

7.1 Layout Considerations

Keep all decoupling capacitors as close to the IC as possible, with the high-frequency decoupling capacitors (10 nF) closer than the low-frequency decoupling capacitors (2.2 µF).

Place ground vias as close as possible to the ground side of the capacitors and reader IC pins to minimize any possible ground loops.

It is not recommend using any inductor sizes below 0603 as the output power can be compromised. If smaller sized inductors are absolutely necessary, the designer must confirm output performance.

Pay close attention to the required load capacitance of the used crystal and adjust the two external shunt capacitors accordingly. Follow the recommendations of the crystal manufacturer for those values.

There should be a common ground plane for the digital and analog sections. The multiple ground sections or "islands" should have vias that tie the different sections of the planes together.

Ensure that the exposed thermal pad at the center of the IC is properly laid out. It should be tied to ground to help dissipate heat from the package.

Trace line lengths should be minimized whenever possible, particularly the RF output path, crystal connections, and control lines from the reader to the microprocessor. Proper placement of the TRF7963A, microprocessor, crystal, and RF connection/connector help facilitate this.

Avoid crossing of digital lines under RF signal lines. Also, avoid crossing of digital lines with other digital lines whenever possible. If the crossings are unavoidable, 90° crossings should be used to minimize coupling of the lines.

Depending on the production test plan, the designer should consider possible implementations of test pads and/or test vias for use during testing. The necessary pads/vias should be placed in accordance with the proposed test plan to help enable easy access to those test points.

If the system implementation is complex (for example, if the RFID reader module is a subsystem of a larger system with other modules such as Bluetooth, WiFi, microprocessors, and clocks), special considerations should be taken to ensure that there is no noise coupling into the supply lines. If needed, special filtering or regulator considerations should be used to minimize or eliminate noise in these systems.

For more information/details on layout considerations, see the *TRF796x HF-RFID Reader Layout Design Guide* (SLOA139).

7.2 Impedance Matching TX_Out (Pin 5) to 50 Ω

The output impedance of the TRF7963A when operated at full power out setting is nominally 4 + j0 (4 Ω real). This impedance must be matched to a resonant circuit and TI recommends matching circuit from 4 Ω to 50 Ω, as commercially available test equipment (for example, spectrum analyzers, power meters, and network analyzers) are 50-Ω systems. See Figure 7-1 and Figure 7-2 for an impedance match reference circuit. This section explains how the values were calculated.

Starting with the 4-Ω source, Figure 7-1 and Figure 7-2 shows the process of going from 4 Ω to 50 Ω by showing it represented on a Smith Chart simulator (available from http://www.fritz.dellsperger.net/). The elements are grouped together where appropriate.

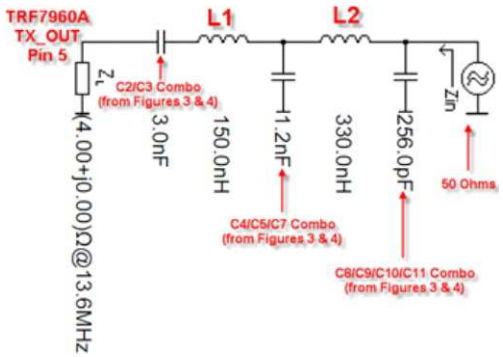


Figure 7-1. Impedance Matching Circuit

This yields the following Smith Chart Simulation:

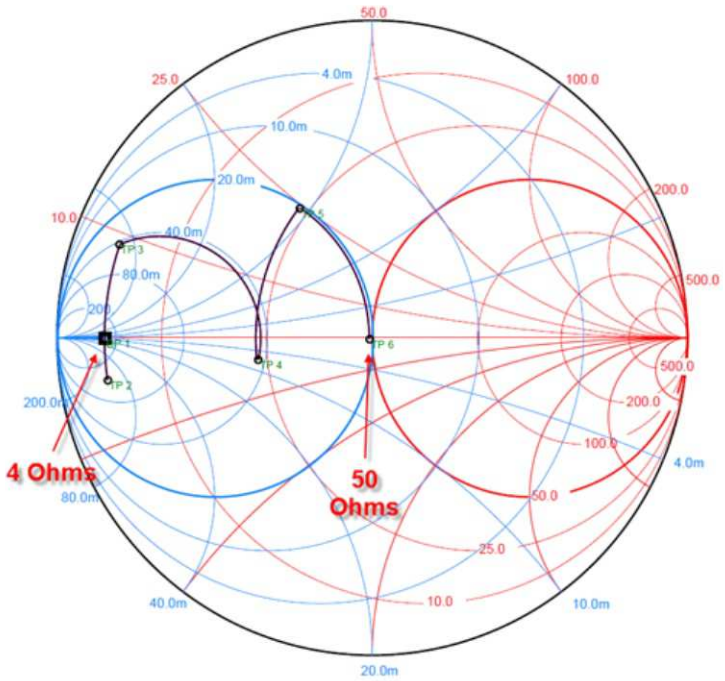


Figure 7-2. Impedance Matching Smith Chart

Resulting power out can be measured with power meter/spectrum analyzer with power meter function or other equipment capable of making a "hot" measurement. Take care to observe maximum power input levels on test equipment and use attenuators whenever available to avoid any possibility of damage to expensive equipment. Expected output power levels under various operating conditions are shown in Table 5-3.

7.3 Reader Antenna Design Guidelines

For HF antenna design considerations using the TRF7963A, see the following documentation:

Antenna Matching for the TRF7960 RFID Reader (SLOA135)

TRF7960TB HF RFID Reader Module User's Guide, with antenna details at end of manual (SLOU297)

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision	Description
SLOS758	Production Data release
SLOS758A	Section 3.2, Corrected Power Rating for $T_A \leq 25°C$.
SLOS758B	Section 3.1, Corrected T_{STG} value. Section 3.2, Corrected typo on θ_{JA}. Section 3.4, Added "Typical operating conditions are" to table-level conditions.

PACKAGING INFORMATION

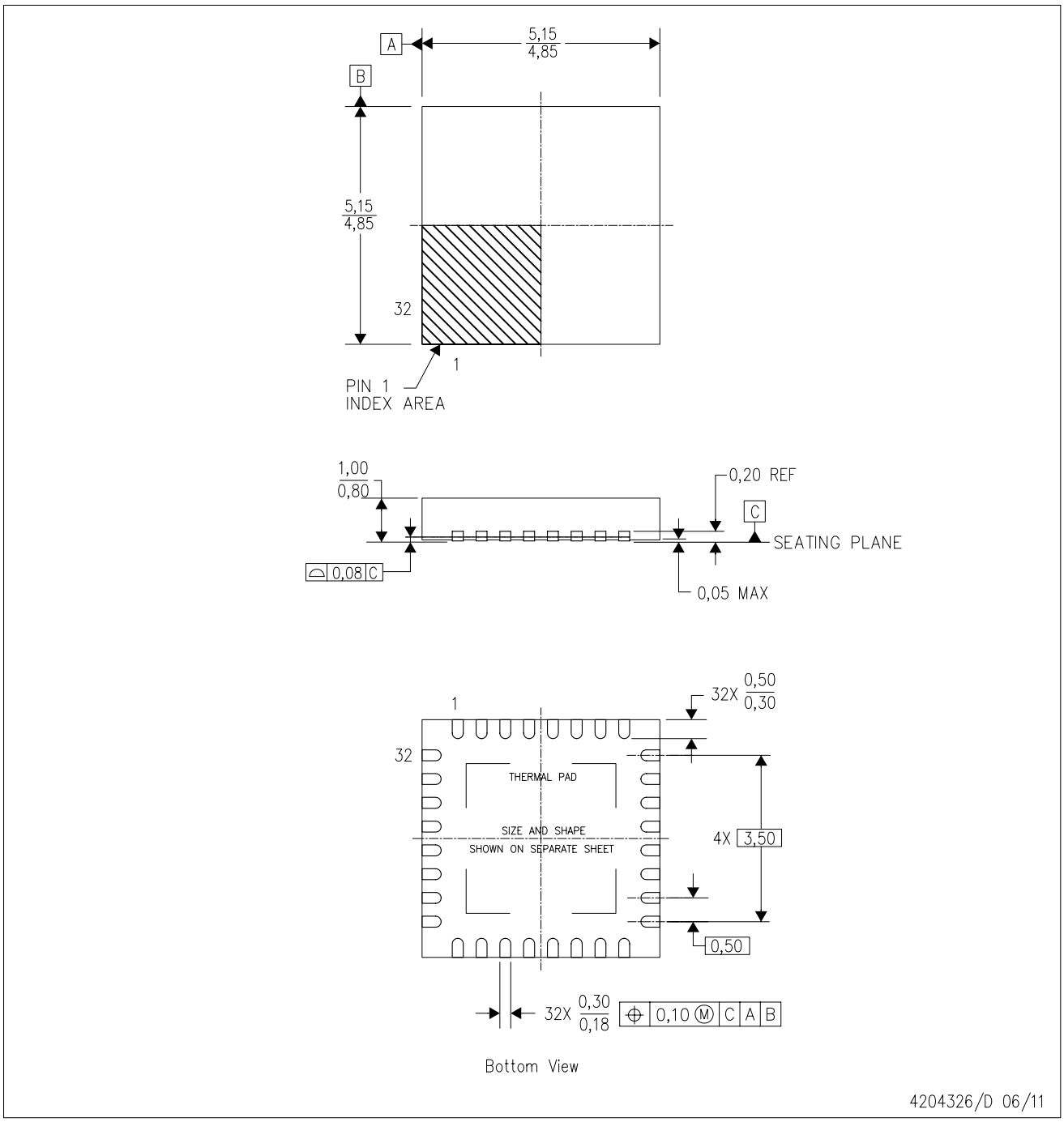
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TRF7963ARHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TRF7963ARHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

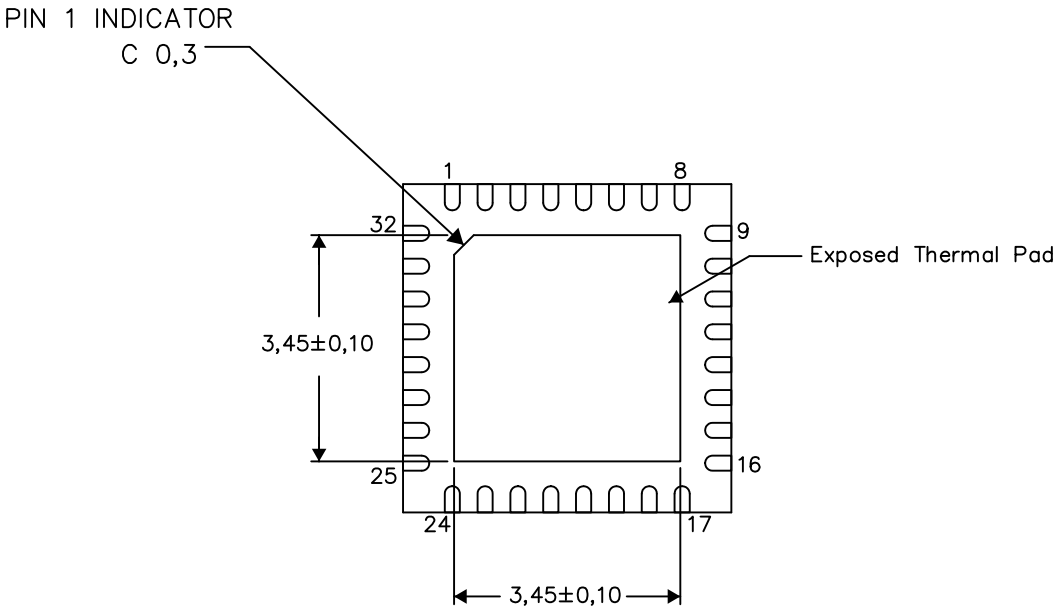
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



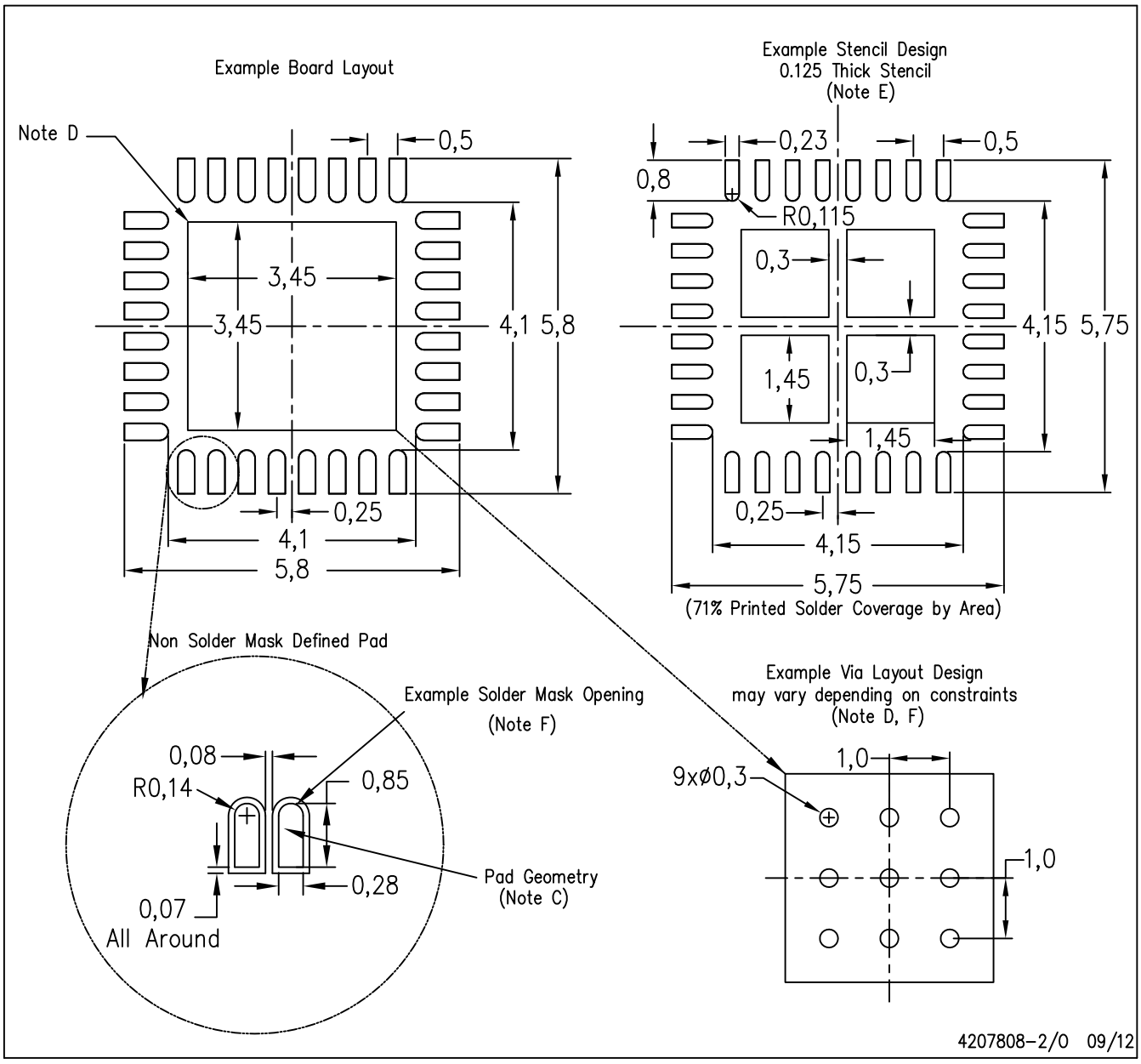
Bottom View

Exposed Thermal Pad Dimensions

4206356–2/W 09/12

NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

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