TEXAS INSTRUMENTS

TPS7A6601-Q1, TPS7A6633-Q1
TPS7A6650-Q1, TPS7A6933-Q1, TPS7A6950-Q1

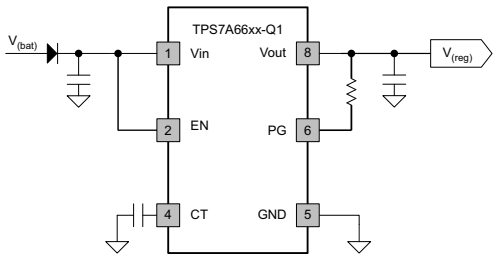
SLVSBL0D – DECEMBER 2012 – REVISED OCTOBER 2014

TPS7A6xxx-Q1 High-Voltage Ultralow-$I_{(q)}$ Low-Dropout Regulator

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C4
- 4-V to 40-V Wide Vin Input Voltage Range With up to 45-V Transient
- Output Current 150 mA
- Low Quiescent Current, $I_{(q)}$:
  - 2 µA when EN = Low (Shutdown Mode)
  - 12 µA Typical at Light Loads
- Low ESR Ceramic Output Stability Capacitor (2.2 µF–100 µF)
- 300-mV Dropout Voltage at 150 mA (Typical, $V_{(Vin)}$ = 4 V)
- Fixed (3.3-V and 5-V) and Adjustable (1.5-V to 5-V) Output Voltages (Adjustable for TPS7A66xx-Q1 Only)
- Low Input Voltage Tracking
- Integrated Power-On Reset
  - Programmable Reset-Pulse Delay
  - Open-Drain Reset Output
- Integrated Fault Protection
  - Thermal Shutdown
  - Short-Circuit Protection
- Input Voltage Sense Comparator (TPS7A69xx-Q1 Only)
- Packages
  - 8-Pin SOIC-D for TPS7A69xx-Q1
  - 8-Pin MSOP-DGN for TPS7A66xx-Q1

Hardware-Enable Option



2 Applications

- Infotainment Systems With Sleep Mode
- Body Control Modules
- Always-On Battery Applications
  - Gateway Applications
  - Remote Keyless Entry Systems
  - Immobilizers

3 Description

The TPS7A66xx-Q1 and TPS7A69xx-Q1 are low-dropout linear regulators designed for up to 40-V Vin operations. With only 12-µA quiescent current at no load, they are quite suitable for standby microprocessor control-unit systems, especially in automotive applications.

The devices feature integrated short-circuit and overcurrent protection. The devices implement reset delay on power up to indicate the output voltage is stable and in regulation. One can program the delay with an external capacitor. A low-voltage tracking feature allows for a smaller input capacitor and can possibly eliminate the need of using a boost converter during cold-crank conditions.

The devices operate in the –40°C to 125°C temperature range. These features suit the devices well for power supplies in various automotive applications.

Device Information(1)

DEVICE NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7A6601-Q1	MSOP (8)	3.00 mm × 3.00 mm
TPS7A6633-Q1		
TPS7A6650-Q1		
TPS7A6933-Q1	SOIC (8)	4.90 mm × 3.91 mm
TPS7A6950-Q1		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Input-Voltage-Sensing Option

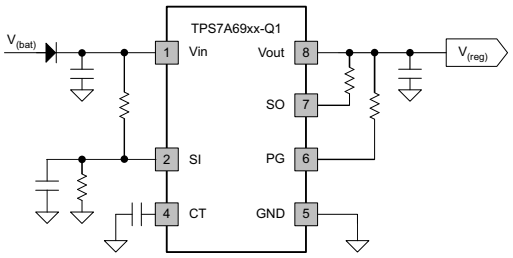


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (December 2013) to Revision D — **Page**

- Changed CDM ESC classification level ... 1
- Changed FB/NC pin to FB/NU in Pin Functions table. Added NC and NU notes to pinout drawings ... 4
- Removed ESD and T_{stg} specifications from the *Absolute Maximum Ratings* table ... 4
- Added *Handling Ratings* table ... 5
- Numerous changes throughout the *Electrical Characteristics* table ... 6
- Added *Switching Characterisitcs* table ... 7
- Moved an oscilloscope trace to the Applications Information section ... 9
- Changed de-glitch time in *Power-On Reset (PG) section* ... 12
- Changed reset delay timer default delay to 290 µs from 150 µs ... 12
- Changed voltage at which Power-on reset initializes to 91.6% of $V_{(Vout)}$ ... 12
- Changed selectable output voltage range and calculation for FB resistor divideer ... 13

Changes from Revision B (August 2013) to Revision C — **Page**

- Corrected part number in the Description section by adding -Q1 ... 1
- Changed Operating ambient temperature to Operating junction temperature ... 4
- Added PSRR graph to Typical Characteristics ... 8
- Deleted a paragraph from the Thermal Protection section ... 14

Changes from Revision A (March 2013) to Revision B — **Page**

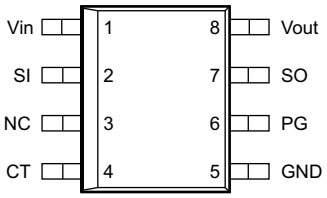
- Added two conditions to $V_{dropout}$ in the Electrical Characteristics table ... 6

Changes from Original (December 2012) to Revision A **Page**

- Deleted the ORDERING INFORMATION table 4
- Changed From: T_A Operating ambient temperature range –40 to 125°C To: T_J Operating ambient temperature range –40 to 150°C 4

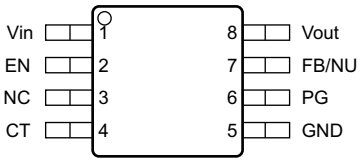
5 Pin Configuration and Functions

8-Pin SOIC (TPS7A69xx-Q1)
D Package
(Top View)



NC - No internal connection

8-Pin MSOP (TPS7A66xx-Q1)
DGN Package
(Top View)



NC - No internal connection
NU - Make no external connection

Pin Functions

PIN NAME	PIN NO.		TYPE	DESCRIPTION
	SOIC-D	MSOP-DGN		
CT	4	4	O	Reset-pulse delay adjustment. Connecting this pin via a capacitor to GND
EN		2	I	Enable pin. The device enters the standby state when the enable pin becomes lower than the threshold.
FB/NU		7	I	Feedback pin when using external resistor divider or NU pin when using internal resistor divider
GND	5	5	G	Ground reference
NC	3	3	—	Not-connected pin
PG	6	6	O	Output ready. This open-drain pin must connect to Vout via an external resistor. The output voltage going below threshold pulls it down.
SI	2		I	Sense input pin to supervise input voltage. Connect via an external voltage divider to Vin and GND
SO	7		O	Sense output. This open-drain pin must connect to Vout via an external resistor. The SI voltage becoming lower than the threshold pulls it down.
Vin	1	1	P	Input power-supply voltage
Vout	8	8	O	Output voltage
		—	—	Thermal pad for MSOP-DGN package

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Vin, EN	Unregulated input (2) (3)	–0.3	45	V
Vout	Regulated output	–0.3	7	V
SI	See (2)	–0.3	Vin	V
CT		–0.3	25	V
FB, SO, PG		–0.3	Vout	V
T_J	Operating junction temperature range	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND
(3) Absolute maximum voltage, withstand 45 V for 200 ms

6.2 Handling Ratings

				MIN	MAX	UNIT
T_{stg}	Storage temperature range			–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)		0	4	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 4, 5, and 8)	0	1	
			Other pins	0	1	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Vin	Unregulated input	4	40	V
EN, SI		0	40	V
CT		0	20	V
Vout		1.5	5.5	V
PG, SO, FB	Low voltage (I/O)	0	5.5	V
T_J	Operating junction temperature	–40	150	°C

6.4 Thermal Information

THERMAL METRIC (1)		TPS7A66xx-Q1	TPS7A69xx-Q1	UNIT
		MSOP (8 PINS)	SOIC (8 PINS)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.4	113.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.0	59.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance (2)	37.4	59.57	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.7	12.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.1	52.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	13.5	NA	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

6.5 Electrical Characteristics

$V_{(Vin)}$ = 14 V, 1 mΩ < ESR < 2 Ω, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT (Vin)						
$V_{(Vin)}$	Input voltage	Fixed 5-V output, I_O = 1 mA	5.5		40	V
		Fixed 3.3-V output, I_O = 1 mA	4		40	V
$I_{(q)}$	Quiescent current	$V_{(Vin)}$ = 5.5 V to 40 V, EN = ON, I_O = 0.2 mA		12	20	µA
$I_{(Sleep)}$	Input sleep current	No load current and EN = OFF			4	µA
$I_{(EN)}$	EN pin current	$V_{(EN)}$ = 40 V			1	µA
$V_{(bg)}$	Band gap	Reference voltage for FB	1.199	1.223	1.247	V
$V_{(VinUVLO)}$	Undervoltage detection	Ramp $V_{(Vin)}$ down until output turns OFF			2.6	V
$V_{(UVLOhys)}$	Undervoltage hysteresis			1		V
ENABLE INPUT (EN)						
V_{IL}	Logic input low level		0		0.4	V
V_{IH}	Logic input high level		1.7			V
REGULATED OUTPUT (Vout)						
$V_{(Vout)}$	Regulated output	I_O = 1 mA, T_J = 25°C	–1%		1%	
		$V_{(Vin)}$ = 6 V to 40 V, I_O = 1 mA to 150 mA, fixed 5-V version	–2%		2%	
		$V_{(Vin)}$ = 4 V to 40 V, I_O = 1 mA to 150 mA, fixed 3.3-V version	–2%		2%	
		$V_{(Vin)}$ = $V_{(Vout)}$ + 0.45 V and Vin ≥ 4 V, I_O = 1 mA to 150 mA, adjustable version[1]	–2%		2%	
$V_{(line-reg)}$	Line regulation	$V_{(Vin)}$ = 5.5 V to 40 V, I_O = 50 mA			5	mV
$V_{(load-reg)}$	Load regulation	I_O = 1 mA to 150 mA			20	mV
$V_{(dropout)}$	Dropout voltage	$V_{(dropout)}$ = $V_{(Vin)}$ – $V_{(Vout)}$, I_{OUT} = 80 mA		180	240	mV
		$V_{(Vin)}$ – $V_{(Vout)}$, I_{OUT} = 150 mA		300	450	
		$V_{(Vin)}$ = 3 V, $V_{(dropout)}$ = $V_{(Vin)}$ – $V_{(Vout)}$, I_O = 5 mA	12	27.5	58	
		$V_{(Vin)}$ = 3 V, $V_{(dropout)}$ = $V_{(Vin)}$ – $V_{(Vout)}$, I_O = 30 mA	44	80	145	
I_O	Output current	$V_{(Vout)}$ in regulation	0		150	mA
$I_{(lreg-CL)}$	Output current limit	$V_{(Vout)}$ short to ground		500	800	mA
PSRR	Power supply ripple rejection[2]	$V_{(Vin)}$ = 12 V, I_L = 10 mA, output capacitance = 2.2 µF				
		Frequency = 100 Hz		60		dB
		Frequency = 100 kHz		40		dB
VOLTAGE SENSING PRE-WARNING						
$V_{I(S-th)}$	Sense low threshold	$V_{(SI)}$ decreasing	1.089	1.123	1.157	V
$V_{I(S-th,hys)}$	Sense threshold hysteresis		50	100	150	mV
$V_{OL(S)}$	Sense output low voltage	($V_{(SI)}$ ≤ 1.06 V, $V_{(Vin)}$ ≥ 4 V, $R_{(SO)}$ = 10 kΩ to $V_{(Vout)}$			0.4	V
$I_{OH(S)}$	Sense output leakage	($V_{(SO)}$ = 5 V, $V_{(SI)}$ ≥ 1.5 V)			1	µA
$I_{I(S)}$	Sense input current		–1	0.1	1	µA
RESET (PG)						
V_{OL}	Reset output, low voltage	I_{OL} = 0.5 mA			0.4	V
I_{lkg}	Leakage current	Reset pulled Vout through 10-kΩ resistor			1	µA
$V_{(TH-POR)}$	Power-on-reset threshold	$V_{(Vout)}$ increasing	89.6	91.6	93.6	% of Vout
$V_{(Thres)}$	Hysteresis			2		% of Vout
RESET DELAY (CT)						
$I_{(Chg)}$	Delay-capacitor charging current	$V_{(CT)}$ = 0 V		1.4		µA
$V_{(th)}$	Threshold to release PG high			1		V
OPERATING TEMPERATURE RANGE						
T_J	Junction temperature		–40		150	°C
$T_{(shutdown)}$	Junction shutdown temperature			175		°C
$T_{(hyst)}$	Hysteresis of thermal shutdown			20		°C

(1) Adjustable version with precision external feedback resistor with tolerance of less than ±1%.
(2) Design information – Not tested

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(SDeglitch,rise)}$	SI or SO rising deglitch time		50		260	µs
$t_{(SDeglitch,drop)}$	SI or SO falling deglitch time		30		240	µs
TIMING FOR RESET (PG)						
$t_{(POR)}$	Power-on-reset delay	Where C = delay capacitor value; capacitance C = 100 nF(1)	50	100	180	ms
$t_{(POR-fixed)}$		No capacitor on pin	100	290	650	µs
$t_{(Deglitch)}$	Reset deglitch time		20	250		µs

(1) This information only is not tested in production and equation basis is (C × 1) / 1 × 10^{-6} = t_d (delay time).
Where C = Delay capacitor value. Capacitance C range = 100 pF to 100 nF.

6.7 Typical Characteristics

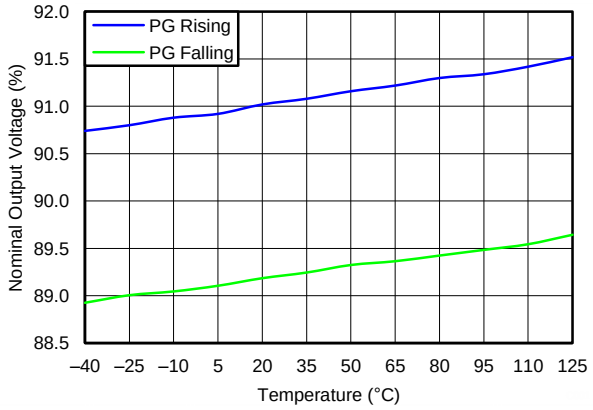


Figure 1. Power-Good Threshold Voltage vs Temperature (Vin = 14 V, No Load)

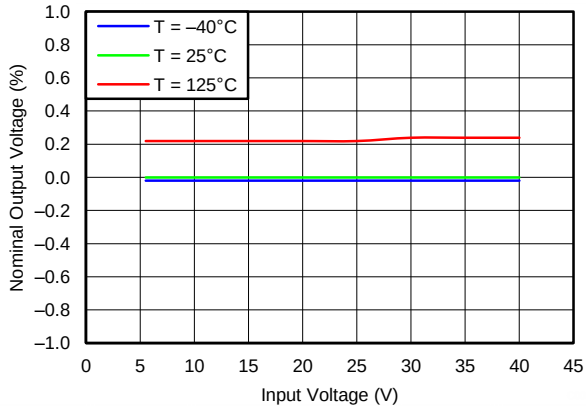


Figure 2. Line Regulation (Vin = 14 V, I_L = 1 mA)

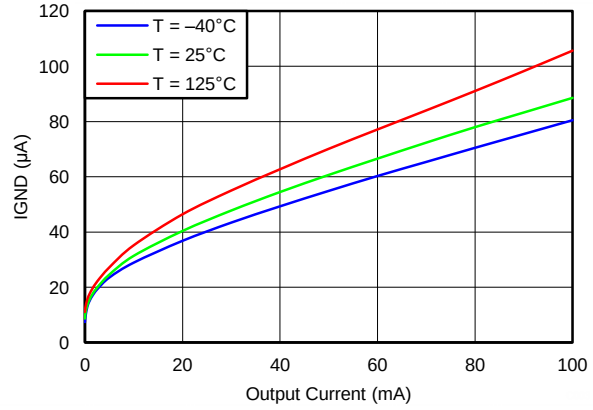


Figure 3. Ground Current vs Output Current (Vin = 14 V)

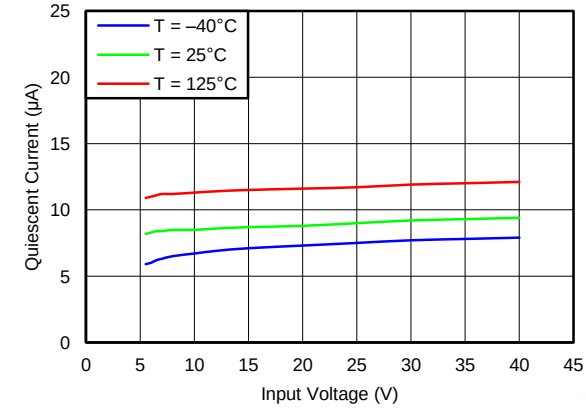


Figure 4. Quiescent Current vs Input Voltage (I_L = 0)

Typical Characteristics (continued)

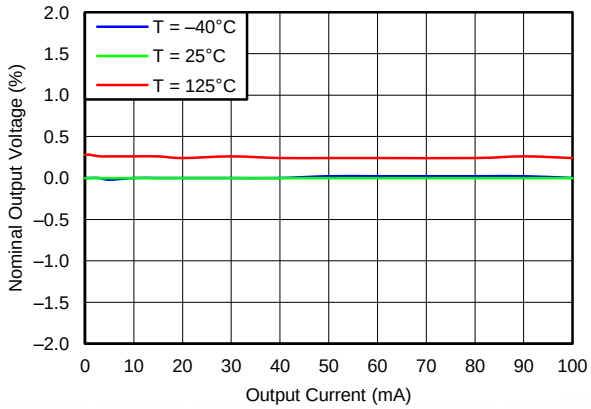


Figure 5. Load Regulation (Vin = 14 V)

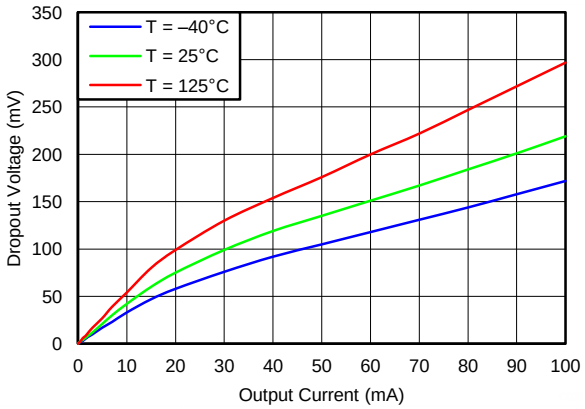


Figure 6. Dropout Voltage vs Output Current (Vin = 4 V)

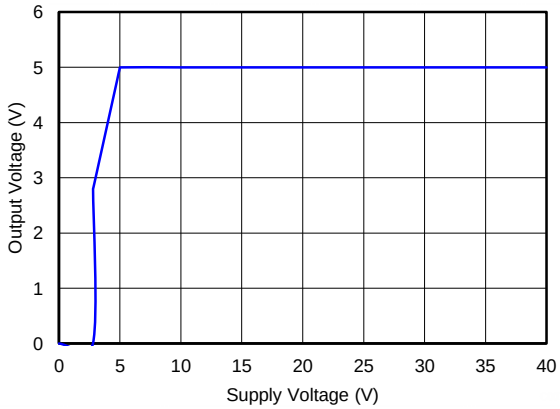


Figure 7. Output Voltage vs Supply Voltage (Fixed 5-V Version, I_L = 0)

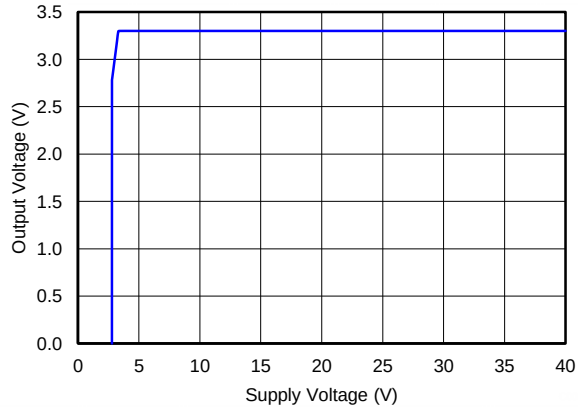


Figure 8. Output Voltage vs Supply Voltage (Fixed 3.3-V Version, I_L = 0)

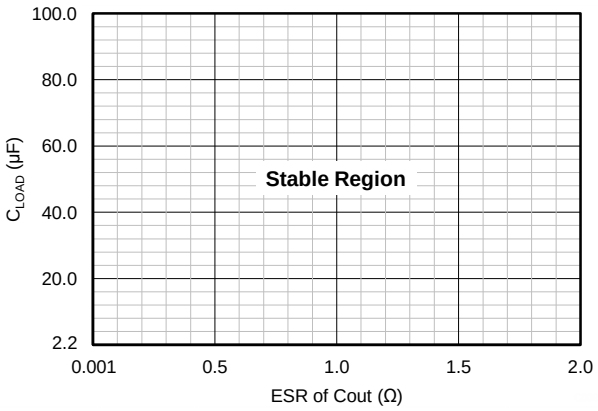


Figure 9. Load Capacitance vs ESR Stability

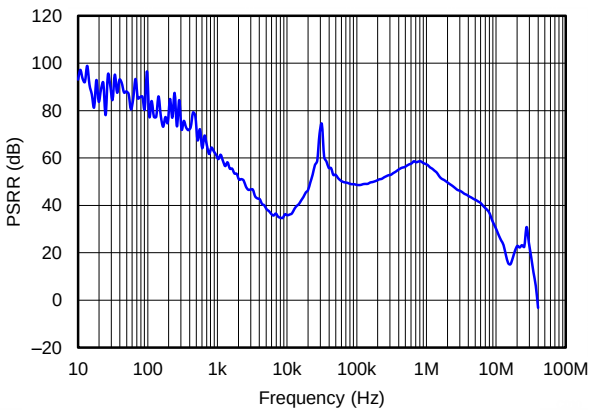


Figure 10. Power-Supply Rejection Ratio vs Frequency

Typical Characteristics (continued)

All oscilloscope waveforms were taken at room temperature.

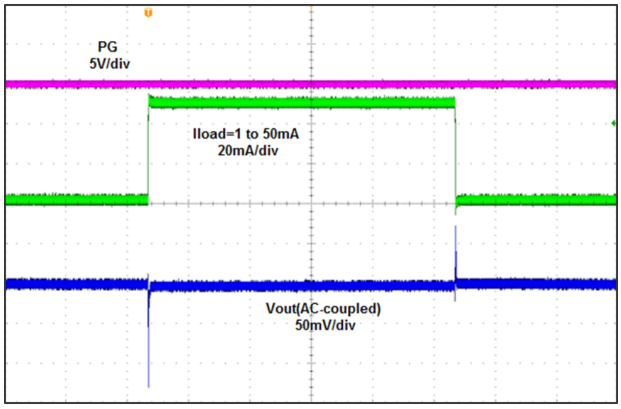


Figure 11. Load Transient Response, 10 ms/div

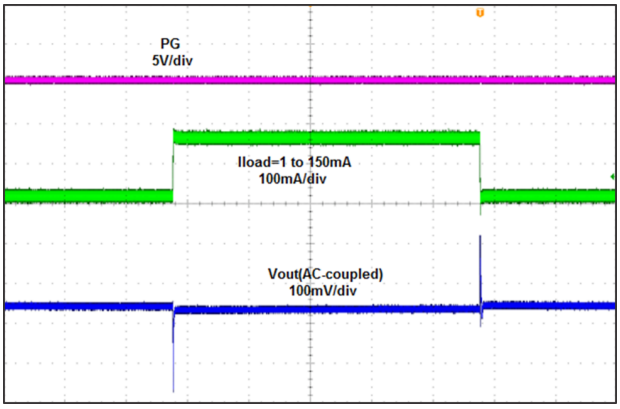


Figure 12. Load Transient Response, 10 ms/div

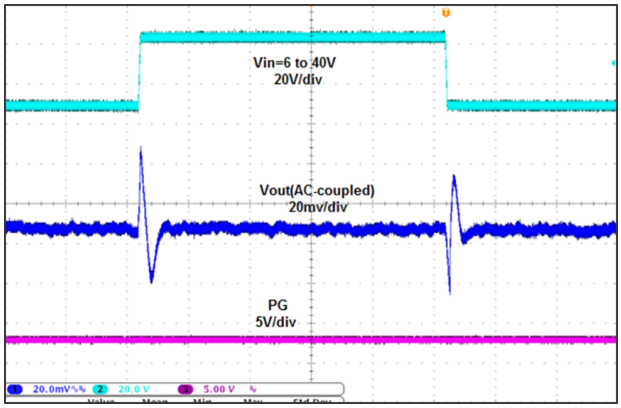


Figure 13. Line Transient Response, I_L = 1 mA, 1 V/µs

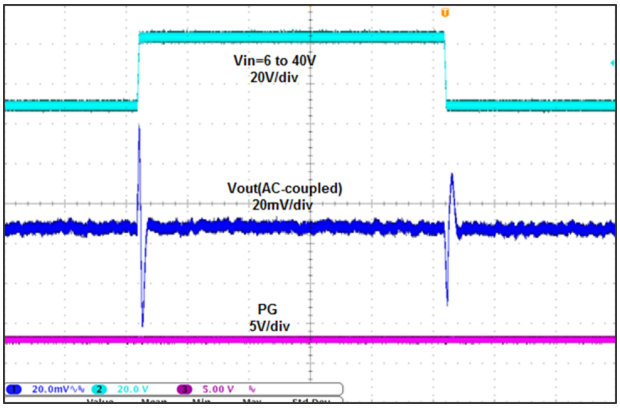


Figure 14. Line Transient Response, I_L = 10 mA, 1 V/µs

7 Detailed Description

7.1 Overview

This product is a combination of a low-dropout linear regulator with reset function. The power-on reset initializes once the Vout output exceeds 91.6% of the target value. The power-on-reset delay is a function of the value set by an external capacitor on the CT pin before releasing the PG pin high.

7.2 Functional Block Diagrams

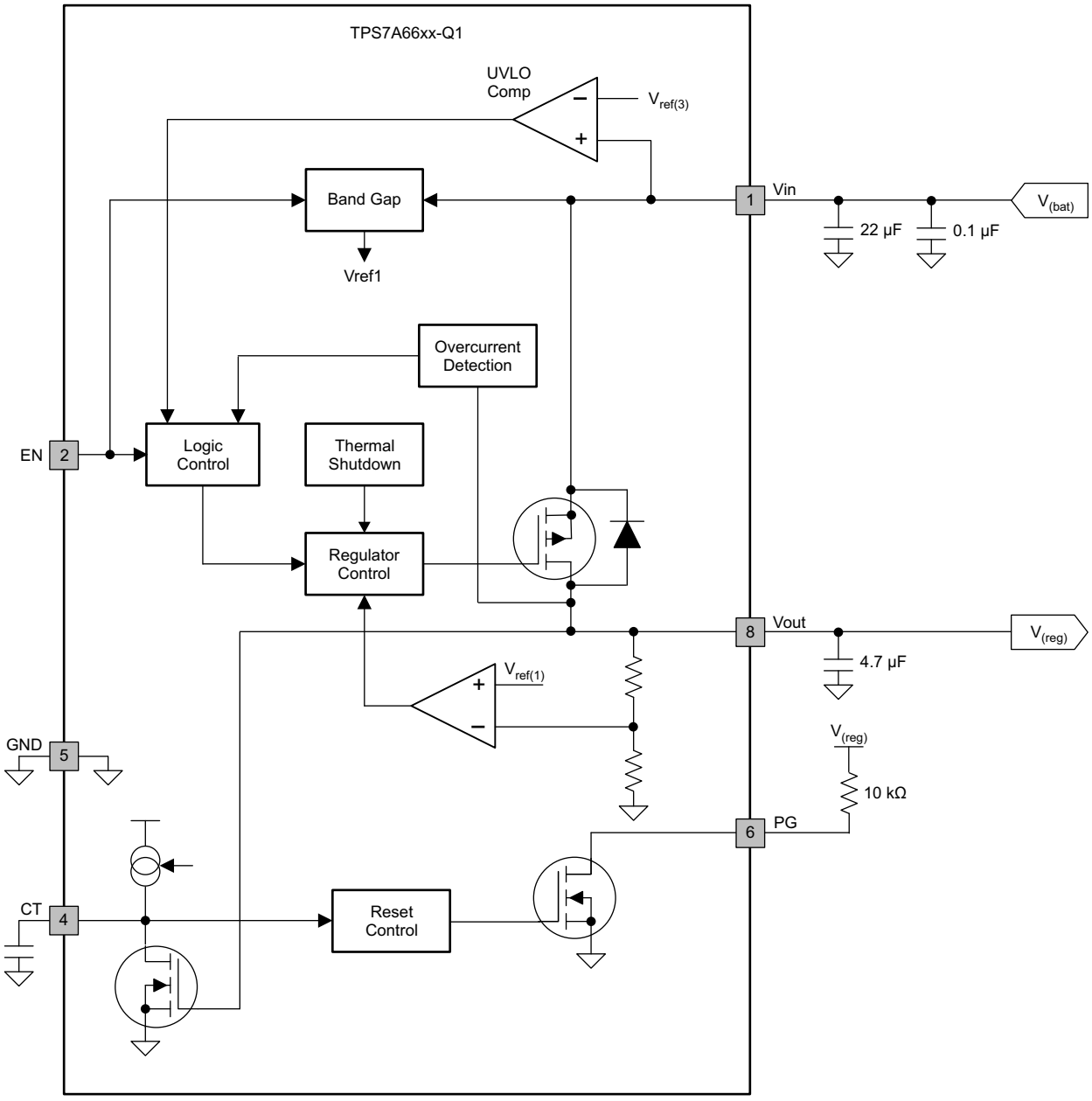


Figure 15. TPS7A66xx-Q1 Functional Block Diagram

Functional Block Diagrams (continued)

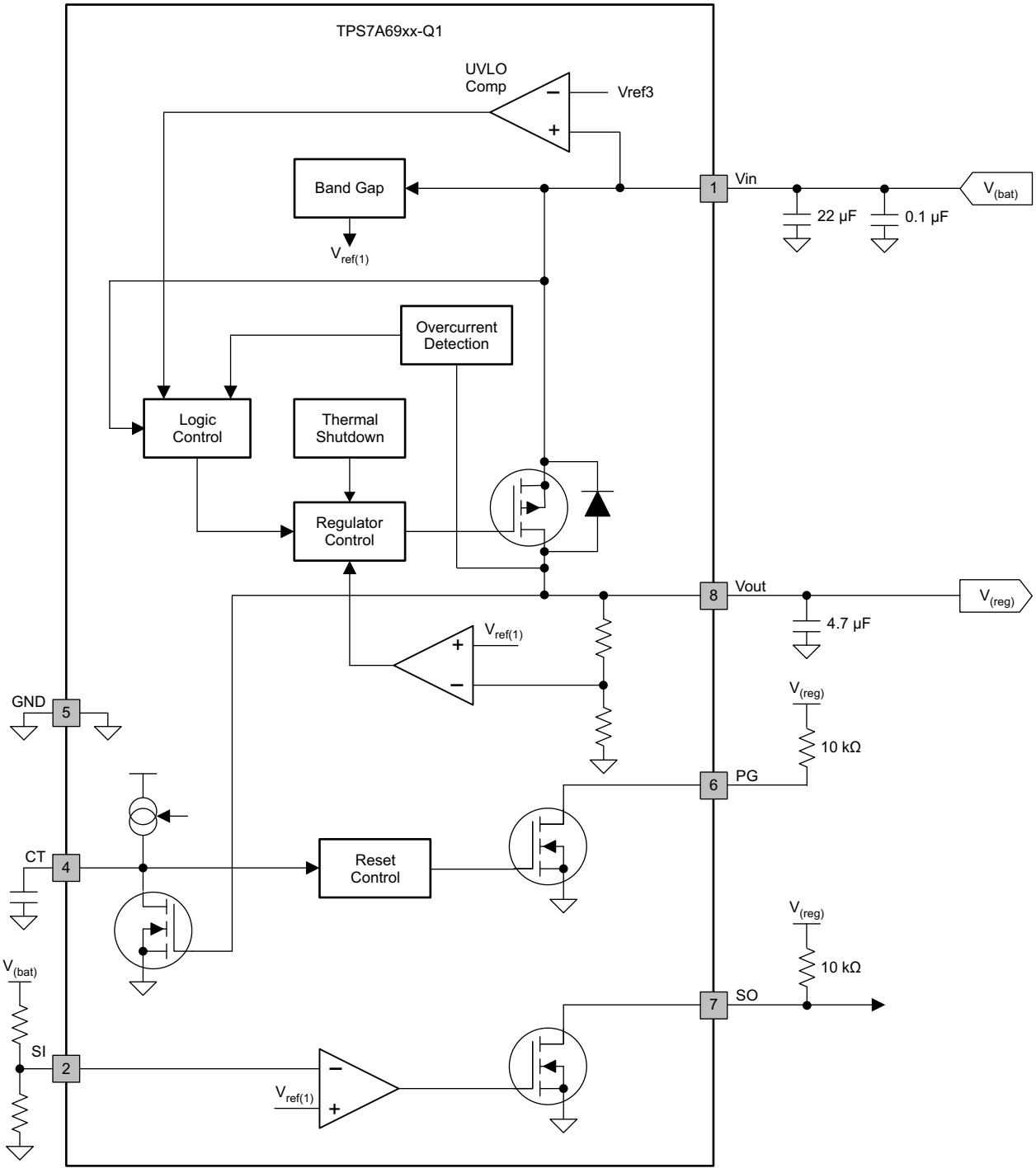


Figure 16. TPS7A69xx-Q1 Functional Block Diagram

7.3 Feature Description

7.3.1 Enable (EN)

This is a high-voltage-tolerant pin; high input activates the device and turns the regulator ON. One can connect this input to the Vin pin for self-bias applications.

Feature Description (continued)

7.3.2 Regulated Output (Vout)

This is the regulated output based on the required voltage. The output has current limitation. During initial power up, the regulator has a soft start incorporated to control initial current through the pass element and the output capacitor.

In the event the regulator drops out of regulation, the output tracks the input minus a drop based on the load current. When the input voltage drops below the UVLO threshold, the regulator shuts down until the input voltage recovers above the minimum start-up level.

7.3.3 Power-On Reset (PG)

This is an output with an external pullup resistor to the regulated supply. The output remains low until the regulated Vout has exceeded approximately 90% of the set value and the power-on-reset delay has expired. The on-chip oscillator presets the delay. The regulated output falling below the 90% level asserts this output low after a short de-glitch time of approximately 250 µs (typical).

7.3.4 Reset Delay Timer (CT)

An external capacitor on this pin sets the timer delay before the reset pin is asserted high. The constant output current charges an external capacitor until the voltage exceeds a threshold to trip an internal comparator. If this pin is open, the default delay time is 290 µs (typ). After releasing the PG pin high, the capacitor on this pin discharges, thus allowing the capacitor to charge from approximately 0.2 V for the next power-on-reset delay-timer function.

An external capacitor, CT, defines the reset-pulse delay time, $t_{(POR)}$, with the charge time of:

$$t_{(POR)} = \frac{C_{(CT)} \times 1\,V}{1\,\mu A} \quad (1)$$

The power-on reset initializes once the output $V_{(Vout)}$ exceeds 91.6% of the programmed value. The power-on-reset delay is a function of the value set by an external capacitor on the CT pin before the releasing of the PG pin high.

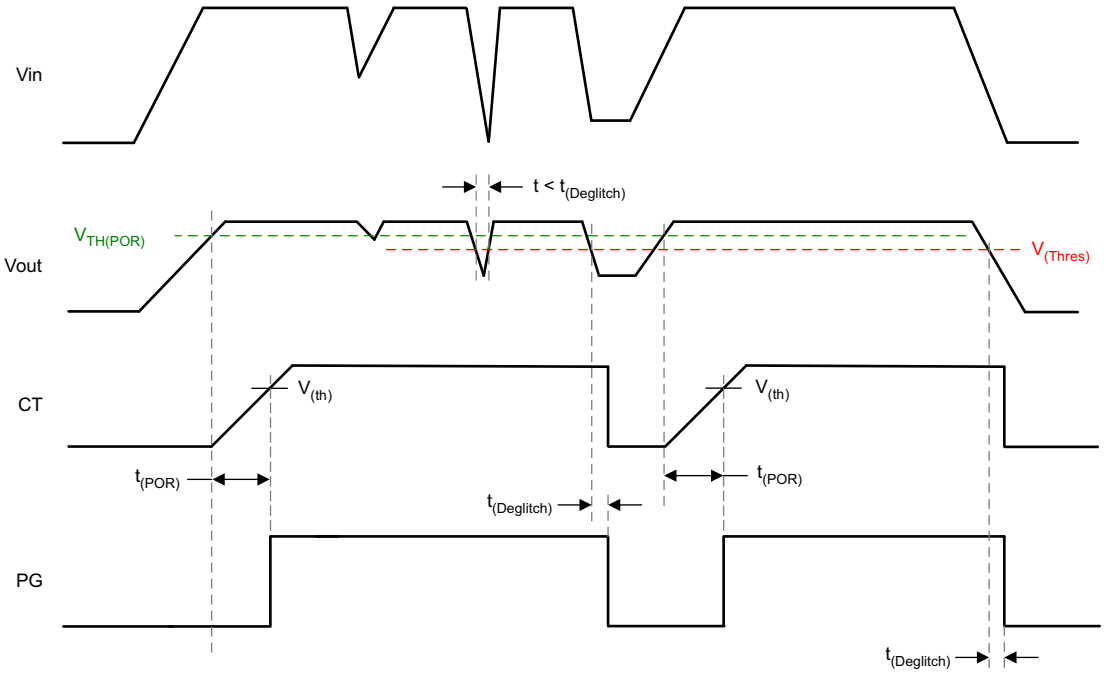


Figure 17. Conditions for Activation of Reset

Feature Description (continued)

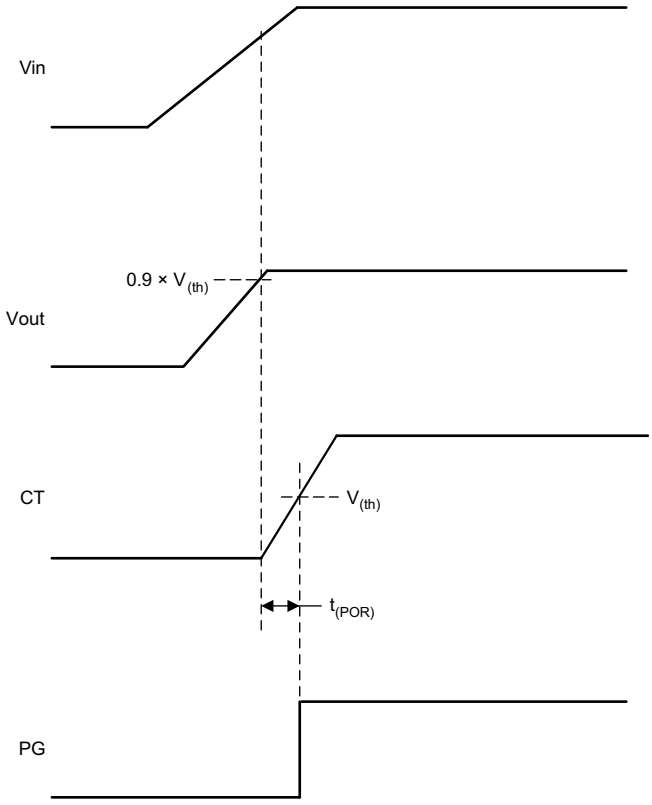


Figure 18. External Programmable Reset Delay

7.3.5 Sense Comparator (SI and SO for TPS7A69xx-Q1)

The sense comparator compares the input signal with an internal voltage reference of 1.223 V for rising and 1.123 V for falling threshold. The use of an external voltage divider makes this comparator very flexible in the application.

The device can supervise the input voltage either before or after the protection diode and give additional information to the microprocessor, like low-voltage warnings.

The regulator operates in low-power mode when the output load is below 2 mA (typical, 1-mA to 10-mA range). In this mode, the regulator output tolerance is approximately $V_{(Vout)}$ ± 1%.

7.3.6 Adjustable Output Voltage (FB for TPS7A6601-Q1)

One can select an output voltage between 1.5 V and 5 V by using an external resistor divider. Calculate the output voltage using the following equation, where $V_{(FB)}$ = 1.223 V. The recommendation for R1 and R2 is that both be less than 100 kΩ.

$$V_{(Vout)} = V_{(FB)} \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

Feature Description (continued)

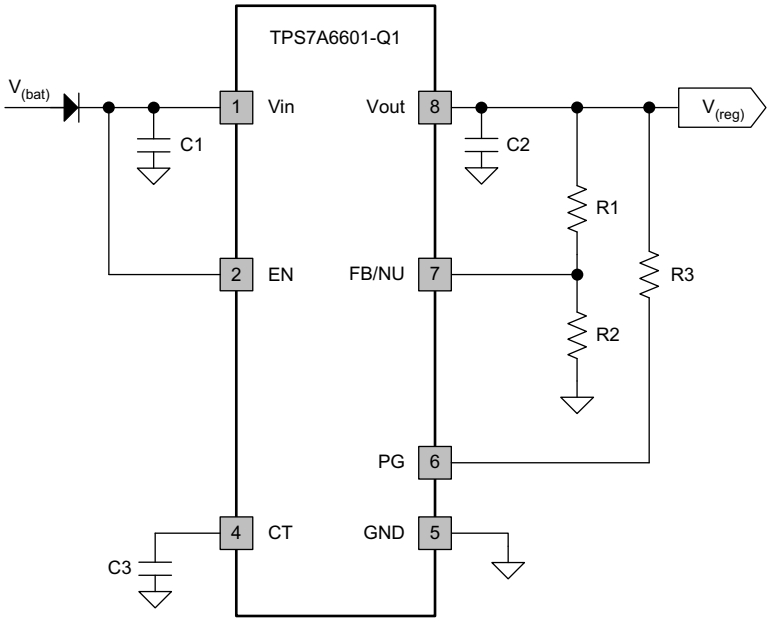


Figure 19. External Feedback Resistor Divider

7.3.7 Undervoltage Shutdown

There is an internally fixed undervoltage shutdown threshold. Undervoltage shutdown activates when the input voltage on Vin drops below $V_{(VinUVLO)}$. This ensures the regulator is not latched into an unknown state during low input supply voltage. If the input voltage has a negative transient which drops below the UVLO threshold and recovers, the regulator shuts down and powers up with a normal power-up sequence once the input voltage is above the required levels.

7.3.8 Low-Voltage Tracking

At low input voltages, the regulator drops out of regulation and the output voltage tracks input minus a voltage based on the load current (I_O) and switch resistance ($R_{(SW)}$). This allows for a smaller input capacitor and can possibly eliminate the need of using a boost convertor during cold-crank conditions.

7.3.9 Thermal Shutdown

These devices incorporate a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the TSD trip point. If the junction temperature exceeds the TSD trip point, the output turns off. When the junction temperature falls below the TSD trip point, the output turns on again.

Thermal protection disables the output when the junction temperature rises to approximately 170°C, allowing the device to cool. Cooling of the junction temperature to approximately 150°C enables the output circuitry. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

The purpose of the design of the internal protection circuitry of the TPS7A66/69xx-Q1 is for protection against overload conditions, not as a replacement for proper heat-sinking. Continuously running the TPS7A66xx-Q1 or TPS7A69xx-Q1 into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Operation With $V_{(VIN)}$ < 4 V

The devices operate with input voltages above 4 V. The maximum UVLO voltage is 2.6 V, and the devices operate at an input voltage above 4 V. The devices can also operate at lower input voltages; no minimum UVLO voltage is specified. At input voltages below the actual UVLO voltage, the devices do not operate.

7.4.2 Operation With EN Control (TPS7A66xx-Q1)

The enable rising edge threshold voltage is 1.7 V (maximum). With the EN pin held above that voltage and the input voltage above 4 V, the device becomes active. The enable falling edge is 0.4 V (minimum). Holding the EN pin below that voltage disables the device, thus reducing the IC quiescent current.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7A66xx-Q1 and TPS7A69xx-Q1 devices are 150-mA low-dropout linear regulators designed for up to 40-V Vin operation with only 12 µA quiescent current at no load. One can use the Pspice transient model, which is downloadable from the product folder (see *Related Links*), for evaluating the base function of the devices. in addition, there are specific EVMs designed for these devices. Both the EVM and its user guide are available on the product folder as well.

8.2 Typical Applications

Figure 20 and Figure 22 show typical application circuits for the TPS7A66xx-Q1 and TPS7A69xx-Q1, respectively. One may use different values of external components, depending on the end application. An application may require a larger output capacitor during fast load steps in order to prevent reset from occurring. TI recommends a low-ESR ceramic capacitor with dielectric of type X5R or X7R.

8.2.1 TPS7A66xx-Q1 Typical Application

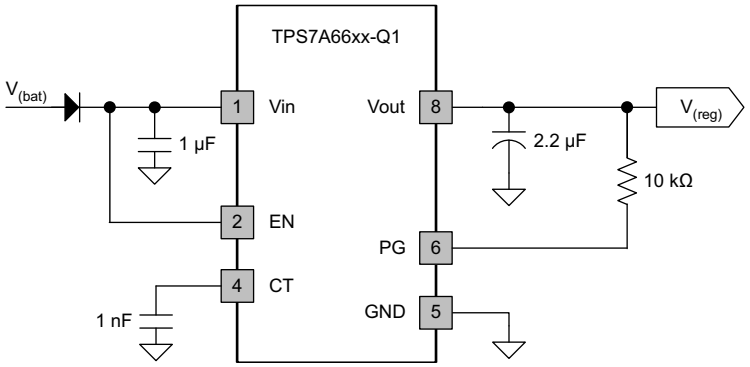


Figure 20. Typical Application Schematic for TPS7A66xx-Q1

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the design parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	4 V to 40 V
Output voltage	3.3 V
Output current rating	150 mA
Output capacitor range	2.2 µF to 100 µF
Output capacitor ESR range	1 mΩ to 2 Ω
CT capacitor range	100 pF to 100 nF

8.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current rating
- Input capacitor
- Output capacitor
- Power-up-reset delay time

8.2.1.2.1 Input Capacitor

The device requires an input decoupling capacitor, the value of which depends on the application. The typical recommended value for the decoupling capacitor is 10 µF. The voltage rating must be greater than the maximum input voltage.

8.2.1.2.2 Output Capacitor

The device requires an output capacitor to stablize the output voltage. The capacitor value should be between 2.2 µF and 100 µF. The ESR range should be between 1 mΩ and 2 Ω. TI recommends to selecting a ceramic capacitor with low ESR to improve the load transient response.

8.2.1.3 Application Performance Plots

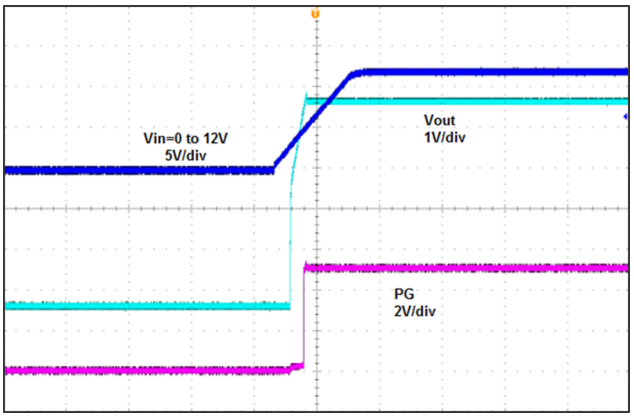


Figure 21. Power Up (5 V), 20 ms/div, I_L = 20 mA

8.2.2 TPS7A69xx-Q1 Typical Application

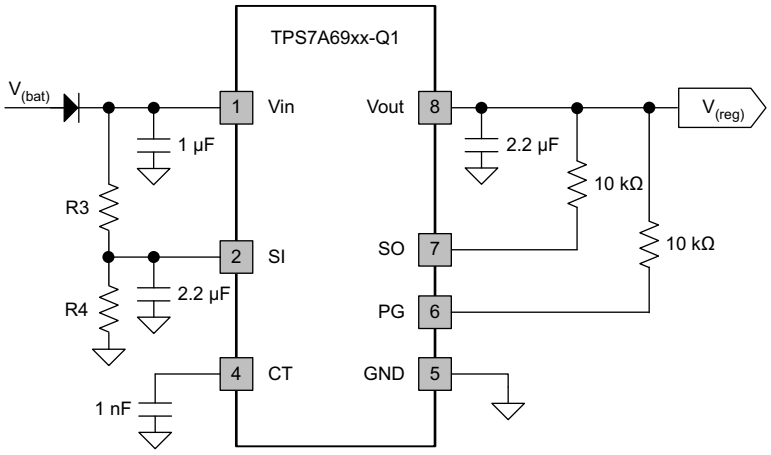


Figure 22. Typical Application Schematic for TPS7A69xx-Q1

8.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	4 V to 40 V
Output voltage	3.3 V
Output current rating	150 mA
Output capacitor range	2.2 µF to 100 µF
Output capacitor ESR range	1 mΩ to 2 Ω
CT capacitor range	100 pF to 100 nF
Low-voltage tracking threshold	6 V to 9 V

8.2.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current rating
- Input capacitor
- Output capacitor
- Power-up-reset delay time
- Low-voltage tracking threshold

8.2.2.2.1 Low-Voltage Tracking Threshold

After determining the low-voltage tracking threshold, calculate the ratio of the resistor divider connected to Vin, SI, and GND by the following equation:

$$\frac{R3}{R4} = \frac{V_{(LT)}}{1.223} - 1 \quad (3)$$

TI recommends that the values of both R3 and R4 be less than 100 kΩ.

8.2.2.3 Application Performance Plots

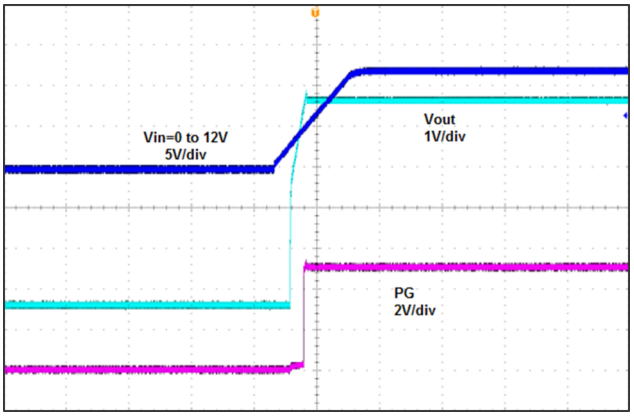


Figure 23. Power Up (5 V), 20 ms/div, I_L = 20 mA

9 Power Supply Recommendations

Design of the device is for operation from an input voltage supply with a range between 4 V and 28 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7A66xx-Q1 or TPS7A69xx-Q1 device, TI recommends adding an electrolytic capacitor with a value of 22 µF and a ceramic bypass capacitor at the input.

10 Layout

10.1 Layout Guidelines

The high impedance of the FB pin makes the regulator sensitive to parasitic capacitances that may couple undesirable signals from nearby components (especially from logic and digital ICs, such as microcontrollers and microprocessors); these capacitive-coupled signals may produce undesirable output voltage transients. In these cases, TI recommends the use of a fixed-voltage version of the TPS7A66xx-Q1, or isolation of the FB node by flooding the local PCB area with ground-plane copper to minimize any undesirable signal coupling.

10.1.1 Package Mounting

Solder pad footprint recommendations for the TPS7A66xx-Q1 and TPS7A69xx-Q1 are available at the end of this product data sheet and at www.ti.com.

10.1.2 Board Layout Recommendations to Improve PSRR and Noise Performance

For the layout of TPS7A66xx-Q1 and TPS7A69xx-Q1, place the input and output capacitors close to the devices as shown in Figure 24 and Figure 25, respectively. In order to enhance the thermal performance, TI recommends surrounding the device with some vias.

To improve ac performance such as PSRR, output noise, and transient response, TI recommends a board design with separate ground planes for Vin and Vout, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device.

Minimize equivalent series inductance (ESL) and ESR in order to maximize performance and ensure stability. Place every capacitor as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. TI strongly discourages the use of vias and long traces because they may impact system performance negatively and even cause instability.

If possible, and to ensure the maximum performance specified in this product data sheet, use the same layout pattern used for the TPS7A66xx-Q1 and TPS7A69xx-Q1 evaluation board, available at www.ti.com.

10.2 Layout Examples

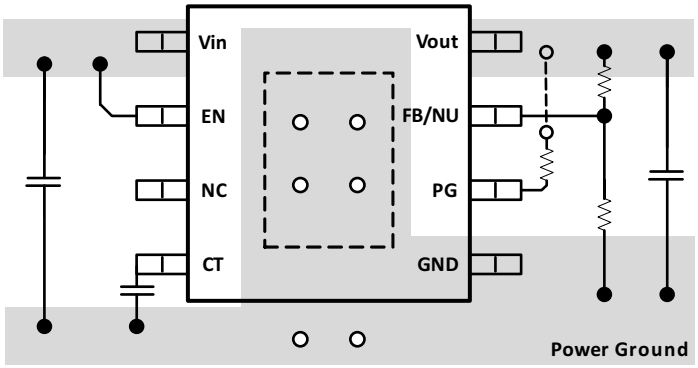


Figure 24. TPS7A66xx-Q1 Board Layout Diagram

Layout Examples (continued)

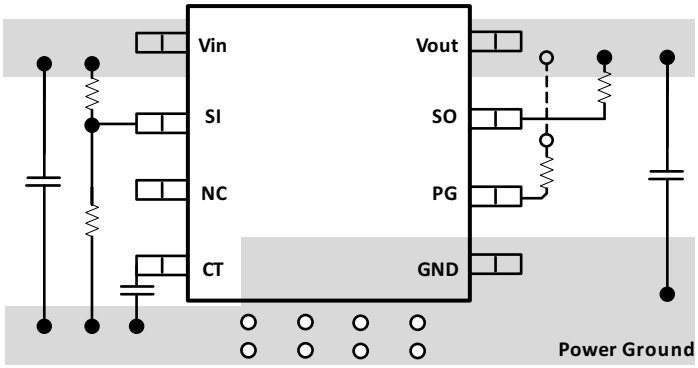


Figure 25. TPS7A69xx-Q1 Board Layout Diagram

10.3 Power Dissipation and Thermal Considerations

Calculate power dissipated in the device using Equation 4.

$$P_D = I_O \times (V_{(Vin)} - V_{(Vout)}) + I_{(q)} \times V_{(Vin)} \quad (4)$$

where:

P_D = continuous power dissipation
I_O = output current
$V_{(Vin)}$ = input voltage
$V_{(Vout)}$ = output voltage

As $I_{(q)} << I_O$, therefore ignore the term $I_{(q)} \times V_{(Vin)}$ in Equation 4.

For a device under operation at a given ambient air temperature (T_A), calculate the junction temperature (T_J) using Equation 5.

$$T_J = T_A + (R_{\theta JA} \times P_{D)}) \quad (5)$$

where:

$R_{\theta JA}$ = junction-to-ambient air thermal impedance

$$\Delta T = T_J - T_A = (R_{\theta JA} \times P_{D)}) \quad (6)$$

11 Device and Documentation Support

11.1 Related Links

The table below lists quick-access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PART	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS7A6601-Q1	Click here	Click here	Click here	Click here	Click here
TPS7A6633-Q1	Click here	Click here	Click here	Click here	Click here
TPS7A6650-Q1	Click here	Click here	Click here	Click here	Click here
TPS7A6933-Q1	Click here	Click here	Click here	Click here	Click here
TPS7A6950-Q1	Click here	Click here	Click here	Click here	Click here

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A6601QDGNRQ1	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PA4Q	Samples
TPS7A6633QDGNRQ1	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PA2Q	Samples
TPS7A6650QDGNRQ1	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PA1Q	Samples
TPS7A6933QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	6933	Samples
TPS7A6950QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	6950	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

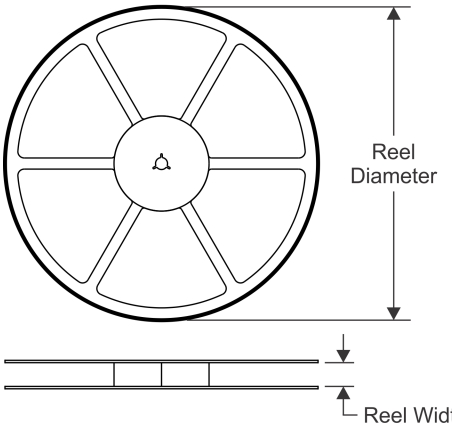
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

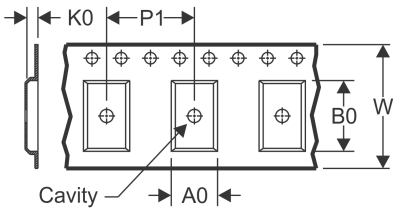
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

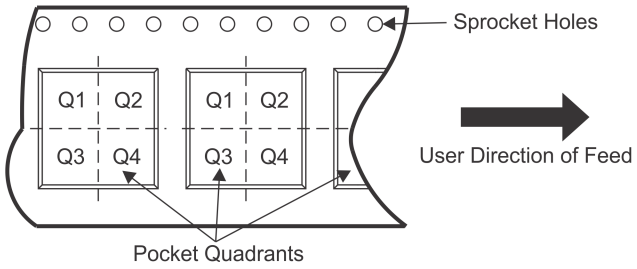


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

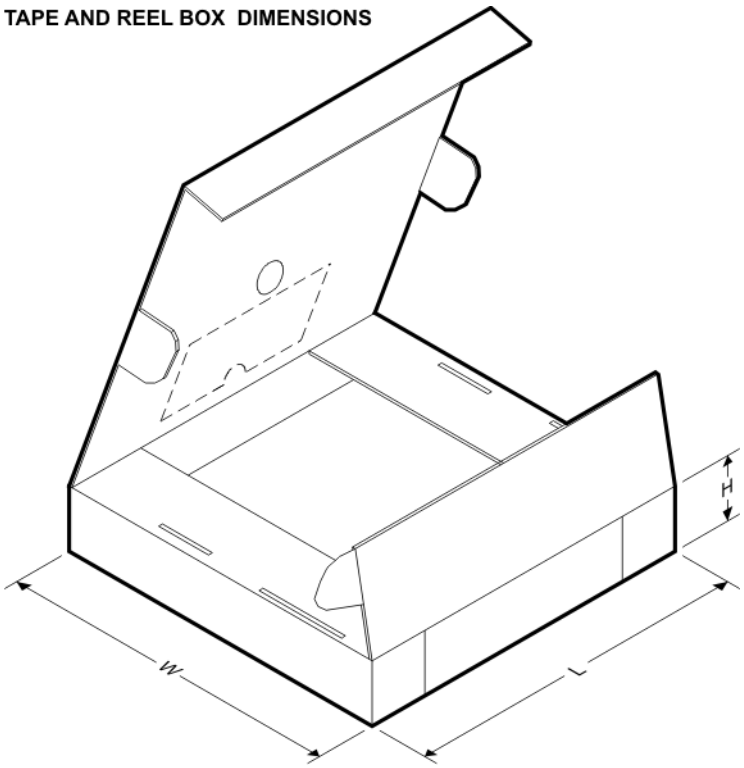
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A6601QDGNRQ1	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7A6633QDGNRQ1	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7A6650QDGNRQ1	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7A6933QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS7A6950QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

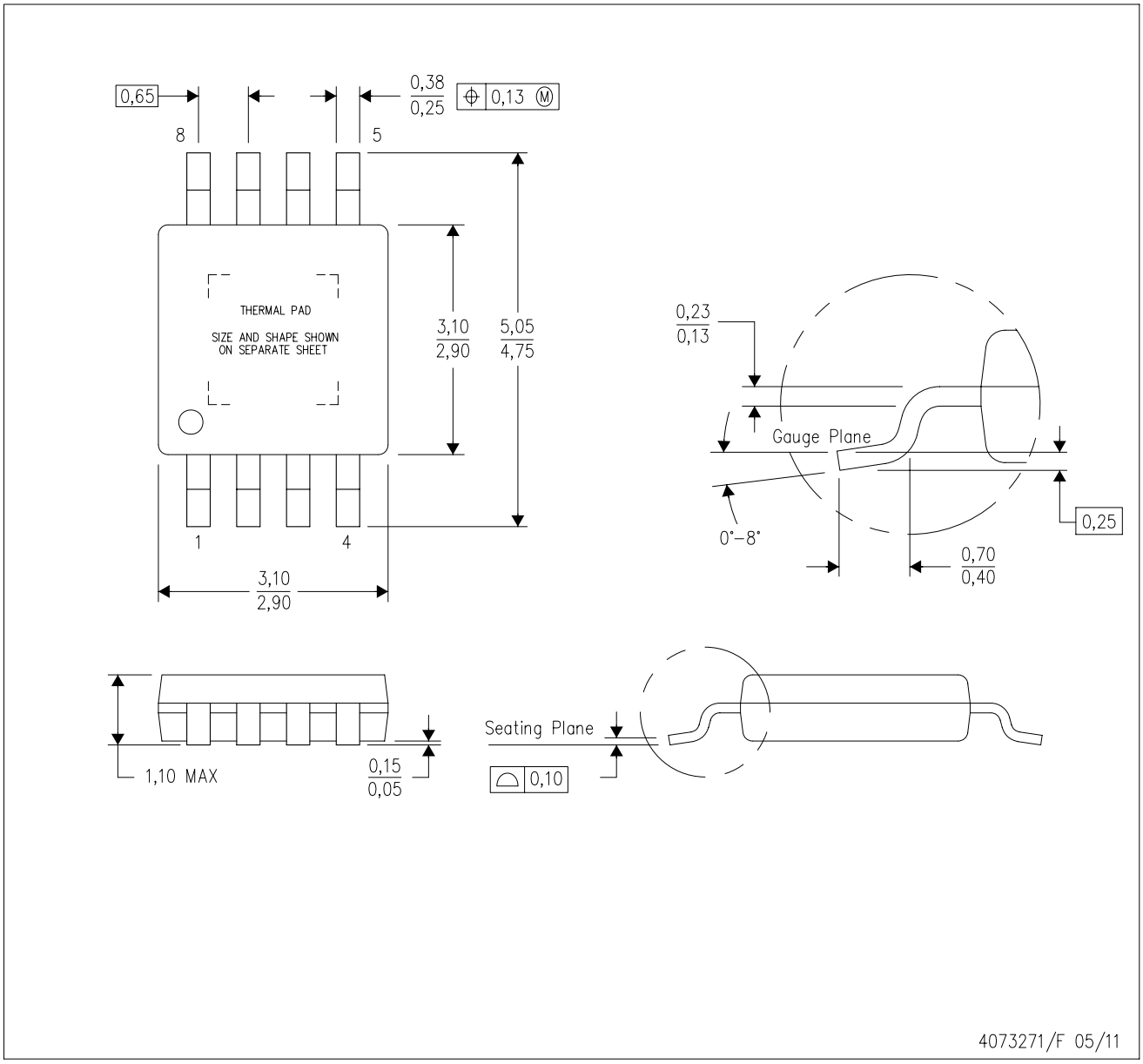
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A6601QDGNRQ1	MSOP-PowerPAD	DGN	8	2500	366.0	364.0	50.0
TPS7A6633QDGNRQ1	MSOP-PowerPAD	DGN	8	2500	366.0	364.0	50.0
TPS7A6650QDGNRQ1	MSOP-PowerPAD	DGN	8	2500	366.0	364.0	50.0
TPS7A6933QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0
TPS7A6950QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation AA–T

PowerPAD is a trademark of Texas Instruments.

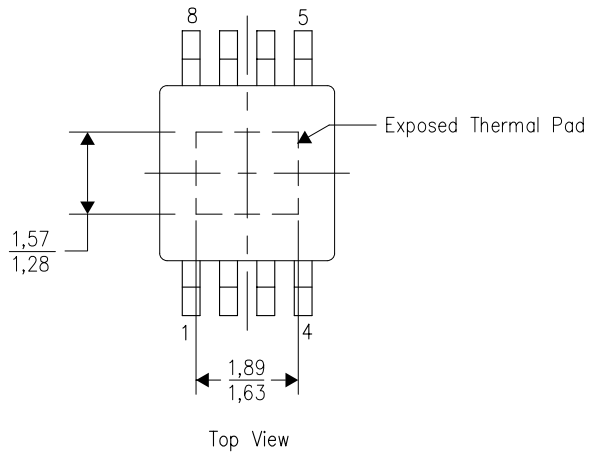
DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

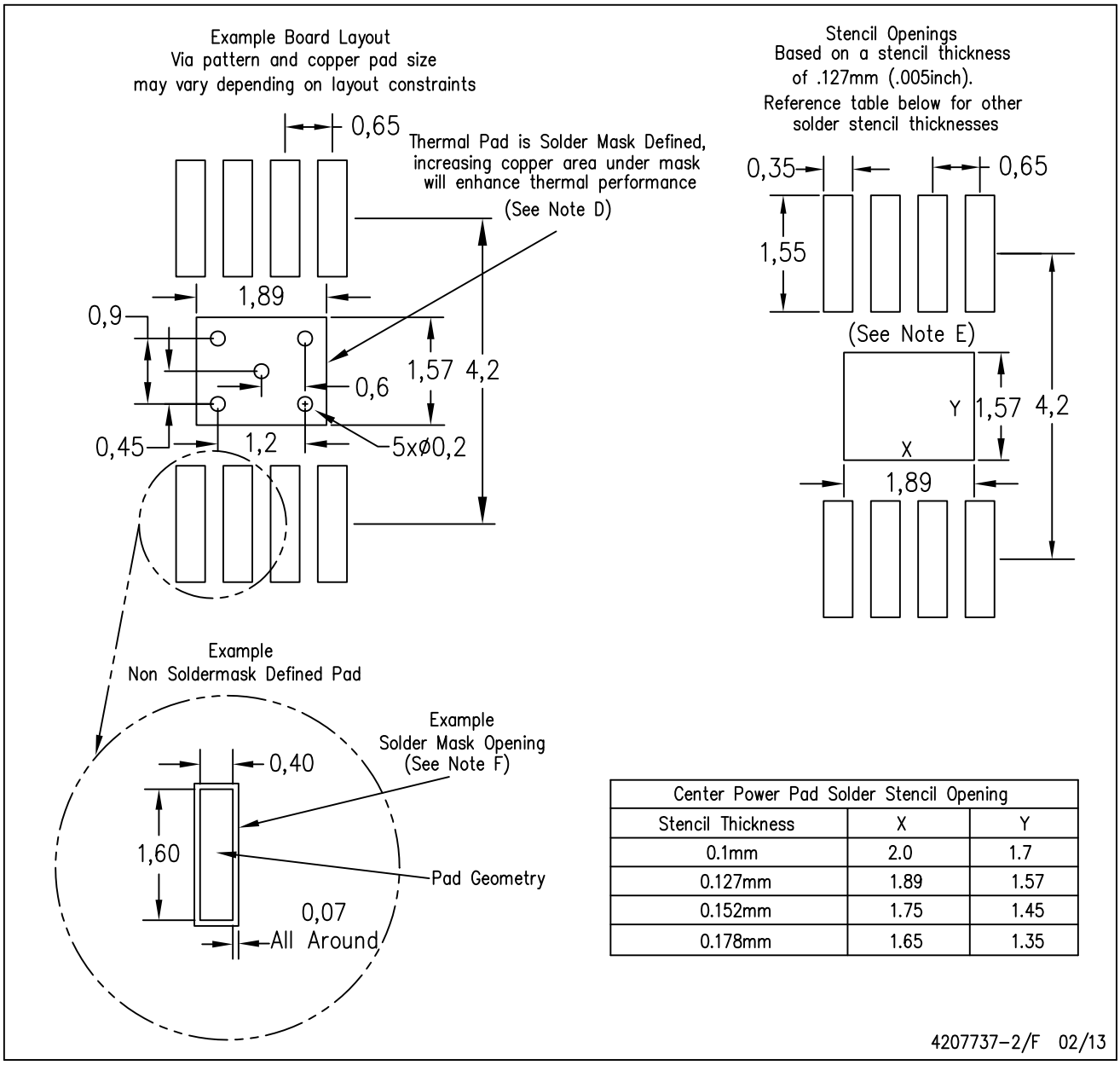
Exposed Thermal Pad Dimensions

4206323–2/I 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGN (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

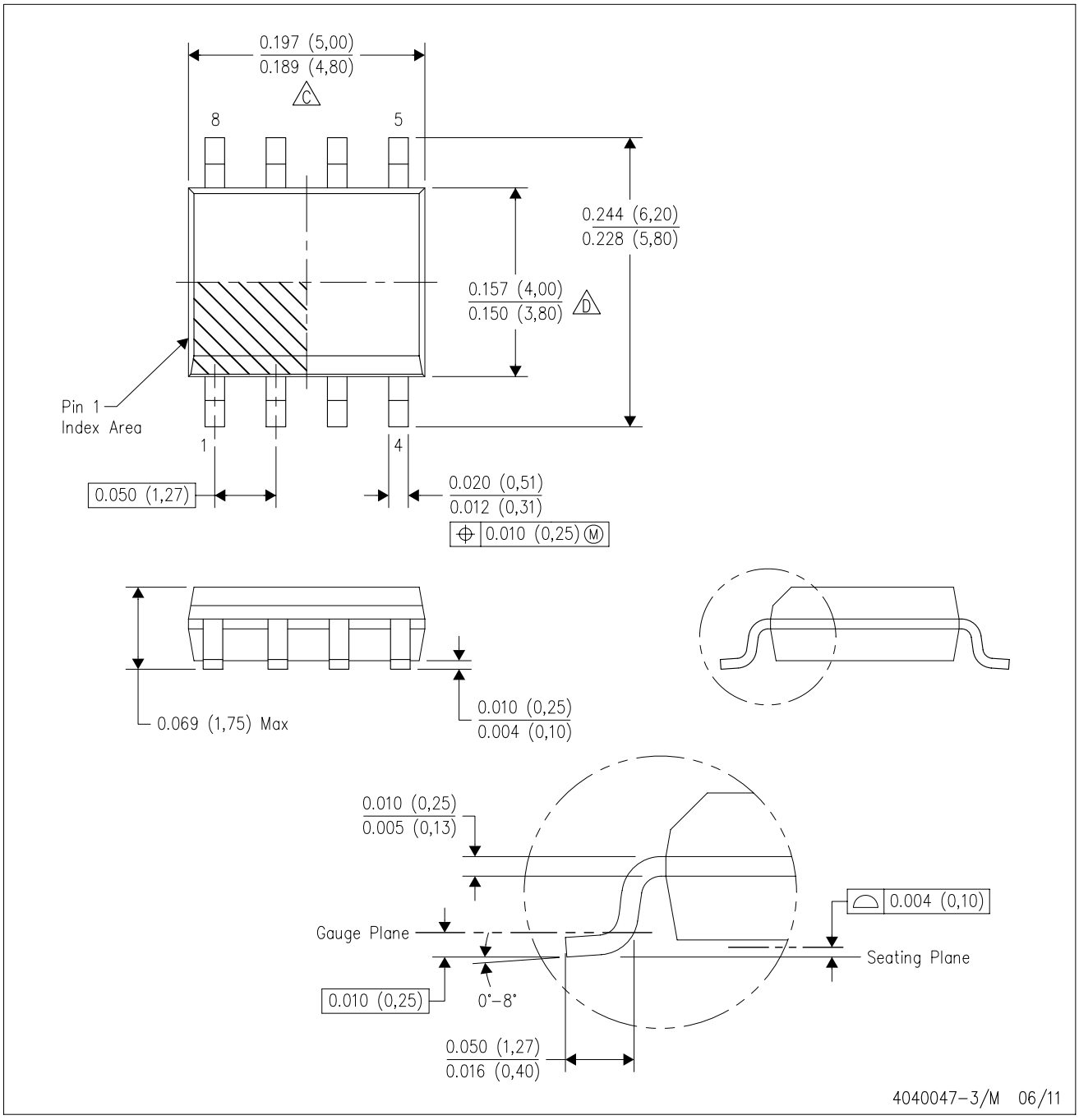


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

4207737–2/F 02/13

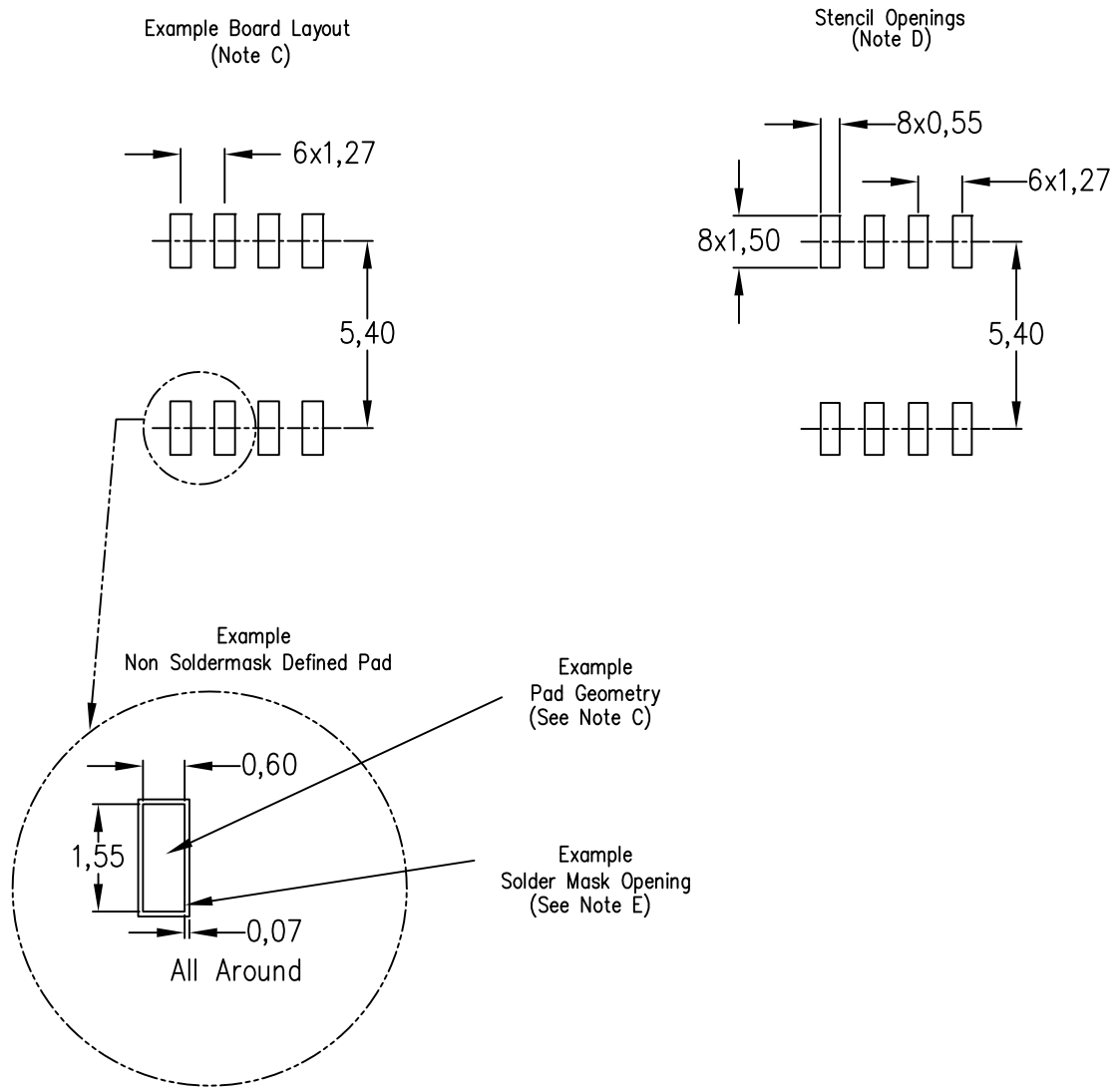
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

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