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Jameco Part Number 1123336

ULTRALOW-NOISE, HIGH PSRR, FAST RF 200mA LOW-DROPOUT LINEAR REGULATORS IN NanoStar™ WAFER CHIP SCALE AND SOT23

FEATURES

- 200mA RF Low-Dropout Regulator With Enable
- Available in Fixed Voltage Versions from 1.8V to 4.75V and Adjustable (1.22V to 5.5V)
- High PSRR (70dB at 10kHz)
- Ultralow-Noise (32 μ V_{RMS}, TPS79328)
- Fast Start-Up Time (50 μ s)
- Stable With a 2.2 μ F Ceramic Capacitor
- Excellent Load/Line Transient Response
- Very Low Dropout Voltage (112mV at 200mA, TPS79330)
- 5- and 6-Pin SOT23 (DBV) and NanoStar Wafer Chip Scale (YEQ, YZQ) Packages

APPLICATIONS

- RF: VCOs, Receivers, ADCs
- Audio
- Cellular and Cordless Telephones
- Bluetooth®, Wireless LAN
- Handheld Organizers, PDAs

DESCRIPTION

The TPS793xx family of low-dropout (LDO) low-power linear voltage regulators features high power-supply rejection ratio (PSRR), ultralow-noise, fast start-up, and excellent line and load transient responses in NanoStar wafer chip scale and SOT23 packages. NanoStar packaging gives an ultrasmall footprint as well as an ultralow profile and package weight, making it ideal for portable applications such as handsets and PDAs. Each device in the family is stable, with a small 2.2 μ F ceramic capacitor on the output. The TPS793xx family uses an advanced, proprietary BiCMOS fabrication process to yield extremely low dropout voltages (for example, 112mV at 200mA, TPS79330). Each device achieves fast start-up times (approximately 50 μ s with a 0.001 μ F bypass capacitor) while consuming very low quiescent current (170 μ A typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than 1 μ A. The TPS79328 exhibits approximately 32 μ V_{RMS} of output voltage noise at 2.8V output with a 0.1 μ F bypass capacitor. Applications with analog components that are noise-sensitive, such as portable RF electronics, benefit from the high PSRR and low-noise features as well as the fast response time.

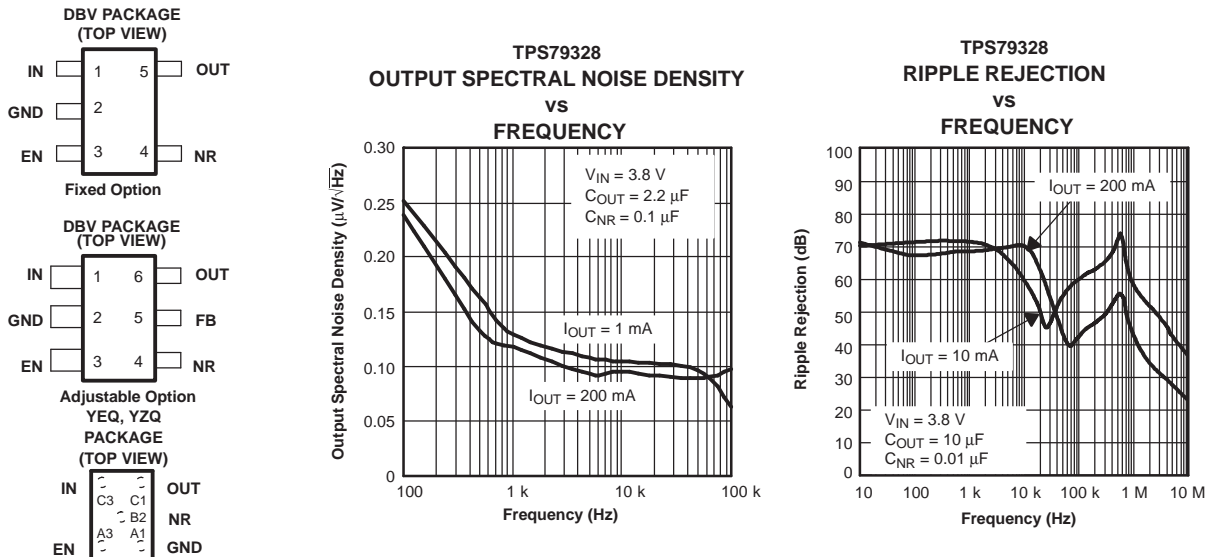


Figure 1.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

PRODUCT	V _{OUT} ⁽²⁾
TPS793xxyyyz	XX is nominal output voltage (for example, 28 = 2.8V, 285 = 2.85V, 01 = Adjustable). YYY is package designator. Z is package quantity.

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (2) Output voltages from 1.2V to 4.8V in 50mV increments are available; minimum order quantities may apply. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS

Over operating temperature range (unless otherwise noted)⁽¹⁾

	UNIT
V _{IN} range	–0.3V to 6V
V _{EN} range	–0.3V to 6V
V _{OUT} range	–0.3V to 6V
Peak output current	Internally limited
ESD rating, HBM	2kV
ESD rating, CDM	500V
Continuous total power dissipation	See Dissipation Ratings Table
Junction temperature range, DBV package	–40°C to +150°C
Junction temperature range, YEQ package	–40°C to +125°C
Storage temperature range, T _{stg}	–65°C to +150°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS TABLE

BOARD	PACKAGE	R _{θJC}	R _{θJA}	DERATING FACTOR ABOVE T _A = +25°C	T _A ≤ +25°C POWER RATING	T _A = +70°C POWER RATING	T _A = +85°C POWER RATING
Low-K ⁽¹⁾	DBV	65°C/W	255°C/W	3.9mW/°C	390mW	215mW	155mW
High-K ⁽²⁾	DBV	65°C/W	180°C/W	5.6mW/°C	560mW	310mW	225mW
Low-K ⁽¹⁾	YEQ	27°C/W	255°C/W	3.9mW/°C	390mW	215mW	155mW
High-K ⁽²⁾	YEQ	27°C/W	190°C/W	5.3mW/°C	530mW	296mW	216mW

- (1) The JEDEC low-K (1s) board design used to derive this data was a 3-inch x 3-inch, two layer board with 2 ounce copper traces on top of the board.
- (2) The JEDEC high-K (2s2p) board design used to derive this data was a 3-inch x 3-inch, multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.

ELECTRICAL CHARACTERISTICS

Over recommended operating temperature range $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{\text{EN}} = V_{\text{IN}}$, $V_{\text{IN}} = V_{\text{OUT(nom)}} + 1\text{V}^{(1)}$, $I_{\text{OUT}} = 1\text{mA}$, $C_{\text{OUT}} = 10\mu\text{F}$, $C_{\text{NR}} = 0.01\mu\text{F}$ (unless otherwise noted). Typical values are at $+25^{\circ}\text{C}$.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} Input voltage ⁽¹⁾				2.7		5.5	V
I_{OUT} Continuous output current				0		200	mA
V_{FB} Internal reference (TPS79301)				1.201	1.225	1.250	V
Output voltage range (TPS79301)				V_{FB}		$5.5 - V_{\text{DO}}$	V
Output voltage	TPS79318	$0\mu\text{A} < I_{\text{OUT}} < 200\text{mA}$,	$2.8\text{V} < V_{\text{IN}} < 5.5\text{V}$	1.764	1.8	1.836	V
	TPS79325	$0\mu\text{A} < I_{\text{OUT}} < 200\text{mA}$,	$3.5\text{V} < V_{\text{IN}} < 5.5\text{V}$	2.45	2.5	2.55	V
	TPS79328	$0\mu\text{A} < I_{\text{OUT}} < 200\text{mA}$,	$3.8\text{V} < V_{\text{IN}} < 5.5\text{V}$	2.744	2.8	2.856	V
	TPS793285	$0\mu\text{A} < I_{\text{OUT}} < 200\text{mA}$,	$3.85\text{V} < V_{\text{IN}} < 5.5\text{V}$	2.793	2.85	2.907	V
	TPS79330	$0\mu\text{A} < I_{\text{OUT}} < 200\text{mA}$,	$4\text{V} < V_{\text{IN}} < 5.5\text{V}$	2.94	3	3.06	V
	TPS79333	$0\mu\text{A} \leq I_{\text{OUT}} < 200\text{mA}$,	$4.3\text{V} < V_{\text{IN}} < 5.5\text{V}$	3.234	3.3	3.366	V
	TPS793475	$0\mu\text{A} < I_{\text{OUT}} < 200\text{mA}$,	$5.25\text{V} < V_{\text{IN}} < 5.5\text{V}$	4.655	4.75	4.845	V
Line regulation ($\Delta V_{\text{OUT}}\%/\Delta V_{\text{IN}}$) ⁽¹⁾		$V_{\text{OUT}} + 1\text{V} < V_{\text{IN}} \leq 5.5\text{V}$			0.05	0.12	%/V
Load regulation ($\Delta V_{\text{OUT}}\%/\Delta I_{\text{OUT}}$)		$0\mu\text{A} < I_{\text{OUT}} < 200\text{mA}$, $T_J = +25^{\circ}\text{C}$			5		mV
Dropout voltage ⁽²⁾ ($V_{\text{IN}} = V_{\text{OUT(nom)}} - 0.1\text{V}$)	TPS79328	$I_{\text{OUT}} = 200\text{mA}$			120	200	mV
	TPS793285	$I_{\text{OUT}} = 200\text{mA}$			120	200	
	TPS79330	$I_{\text{OUT}} = 200\text{mA}$			112	200	
	TPS79333	$I_{\text{OUT}} = 200\text{mA}$			102	180	
	TPS793475	$I_{\text{OUT}} = 200\text{mA}$			77	125	
Output current limit		$V_{\text{OUT}} = 0\text{V}$		285		600	mA
GND pin current		$0\mu\text{A} < I_{\text{OUT}} < 200\text{mA}$			170	220	μA
Shutdown current ⁽³⁾		$V_{\text{EN}} = 0\text{V}$, $2.7\text{V} < V_{\text{IN}} < 5.5\text{V}$			0.07	1	μA
FB pin current		$V_{\text{FB}} = 1.8\text{V}$				1	μA
Power-supply ripple rejection	TPS79328	$f = 100\text{Hz}$, $T_J = +25^{\circ}\text{C}$, $I_{\text{OUT}} = 10\text{mA}$			70		dB
		$f = 100\text{Hz}$, $T_J = +25^{\circ}\text{C}$, $I_{\text{OUT}} = 200\text{mA}$			68		
		$f = 10\text{kHz}$, $T_J = +25^{\circ}\text{C}$, $I_{\text{OUT}} = 200\text{mA}$			70		
		$f = 100\text{kHz}$, $T_J = +25^{\circ}\text{C}$, $I_{\text{OUT}} = 200\text{mA}$			43		
Output noise voltage (TPS79328)		BW = 200Hz to 100kHz, $I_{\text{OUT}} = 200\text{mA}$	$C_{\text{NR}} = 0.001\mu\text{F}$		55		μV_{RMS}
			$C_{\text{NR}} = 0.0047\mu\text{F}$		36		
			$C_{\text{NR}} = 0.01\mu\text{F}$		33		
			$C_{\text{NR}} = 0.1\mu\text{F}$		32		
Time, start-up (TPS79328)		$R_L = 14\Omega$, $C_{\text{OUT}} = 1\mu\text{F}$	$C_{\text{NR}} = 0.001\mu\text{F}$		50		μs
			$C_{\text{NR}} = 0.0047\mu\text{F}$		70		
			$C_{\text{NR}} = 0.01\mu\text{F}$		100		
High level enable input voltage		$2.7\text{V} < V_{\text{IN}} < 5.5\text{V}$		1.7		V_{IN}	V
Low level enable input voltage		$2.7\text{V} < V_{\text{IN}} < 5.5\text{V}$		0		0.7	V
EN pin current		$V_{\text{EN}} = 0\text{V}$		-1		1	μA
UVLO threshold		V_{CC} rising		2.25		2.65	V
UVLO hysteresis					100		mV

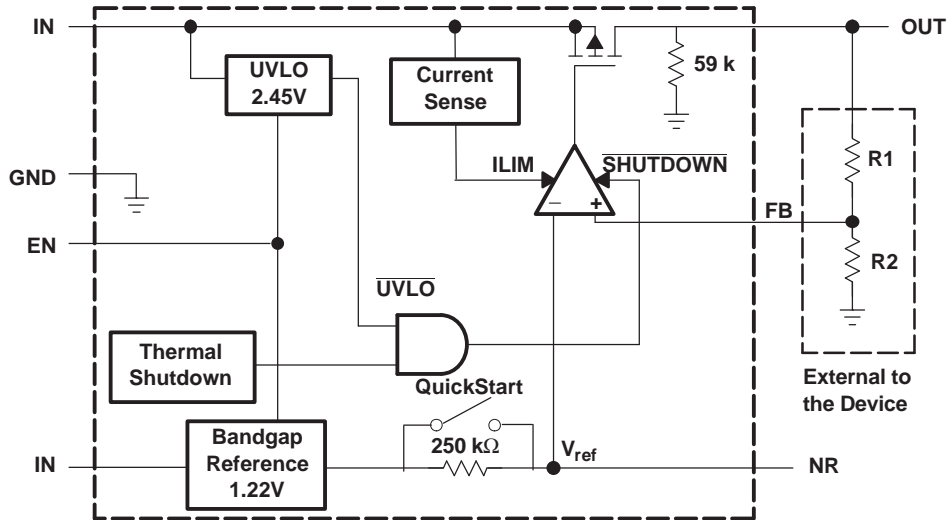
(1) Minimum V_{IN} is 2.7V or $V_{\text{OUT}} + V_{\text{DO}}$, whichever is greater.

(2) Dropout is not measured for the TPS79318 and TPS79325 since minimum $V_{\text{IN}} = 2.7\text{V}$.

(3) For adjustable versions, this parameter applies only after V_{IN} is applied; then V_{EN} transitions high to low.

FUNCTIONAL BLOCK DIAGRAMS

ADJUSTABLE VERSION



FIXED VERSION

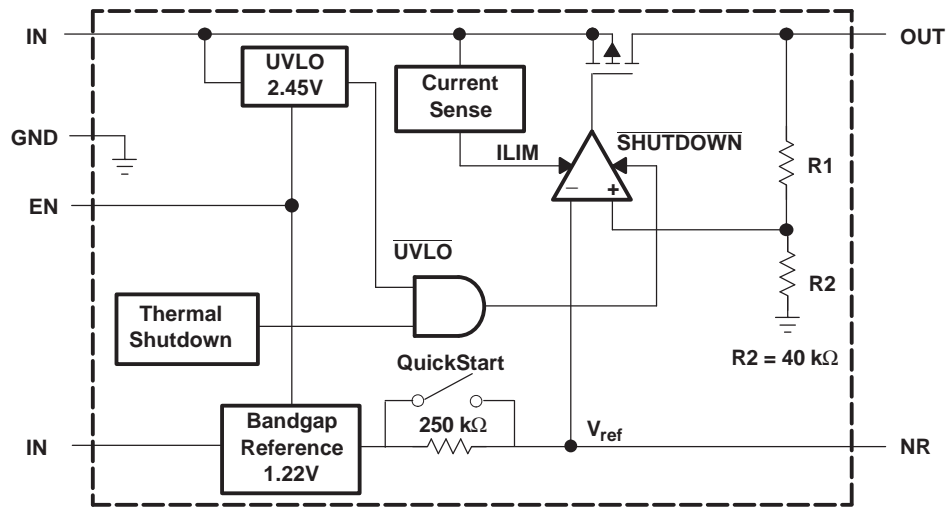


Table 1. Terminal Functions

TERMINAL				DESCRIPTION
NAME	SOT23 ADJ	SOT23 FIXED	WCSP FIXED	
NR	4	4	B2	Connecting an external capacitor to this pin bypasses noise generated by the internal bandgap. This improves power-supply rejection and reduces output noise.
EN	3	3	A3	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used.
FB	5	N/A	N/A	This terminal is the feedback input voltage for the adjustable device.
GND	2	2	A1	Regulator ground
IN	1	1	C3	Input to the device.
OUT	6	5	C1	Output of the regulator.

TYPICAL CHARACTERISTICS (SOT23 PACKAGE)

TPS79328
OUTPUT VOLTAGE
VS
OUTPUT CURRENT

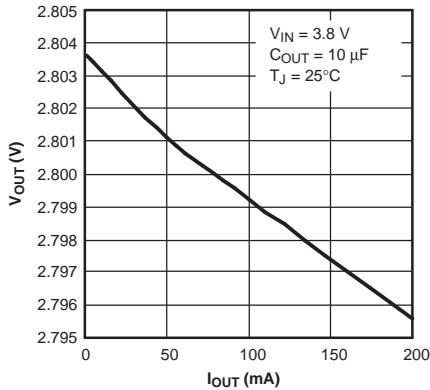


Figure 2.

TPS79328
OUTPUT VOLTAGE
VS
JUNCTION TEMPERATURE

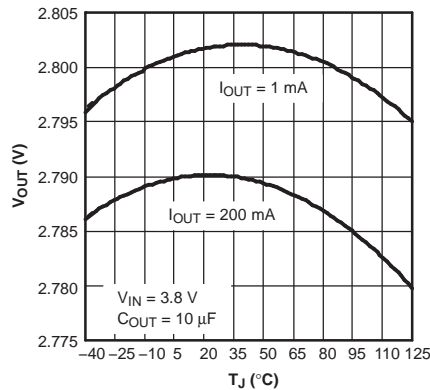


Figure 3.

TPS79328
GROUND CURRENT
VS
JUNCTION TEMPERATURE

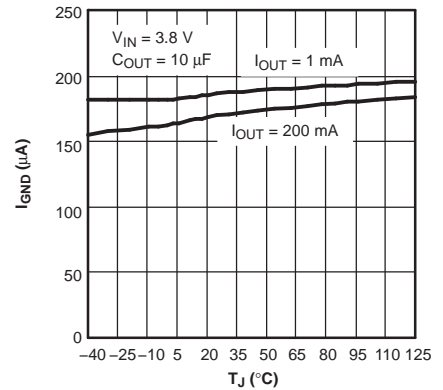


Figure 4.

TPS79328 OUTPUT SPECTRAL
NOISE DENSITY
VS
FREQUENCY

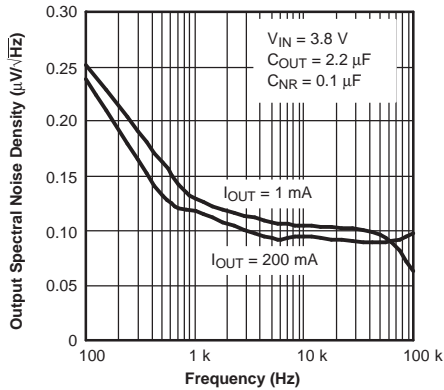


Figure 5.

TPS79328 OUTPUT SPECTRAL
NOISE DENSITY
VS
FREQUENCY

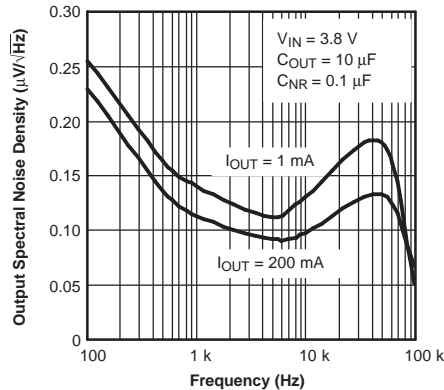


Figure 6.

TPS79328 OUTPUT SPECTRAL
NOISE DENSITY
VS
FREQUENCY

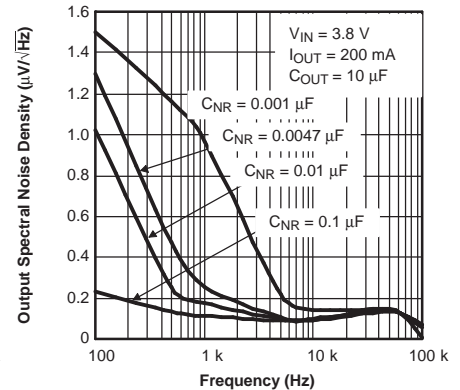


Figure 7.

ROOT MEAN SQUARE OUTPUT
NOISE
VS
CNR

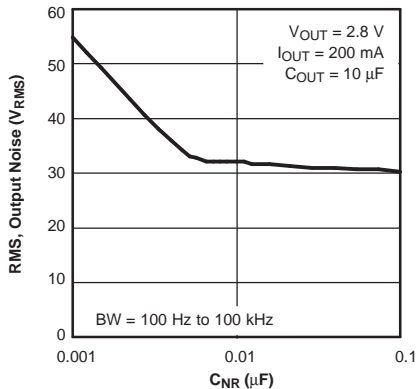


Figure 8.

OUTPUT IMPEDANCE
VS
FREQUENCY

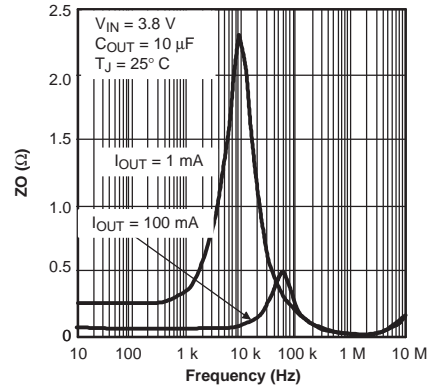


Figure 9.

TPS79328
DROPOUT VOLTAGE
VS
JUNCTION TEMPERATURE

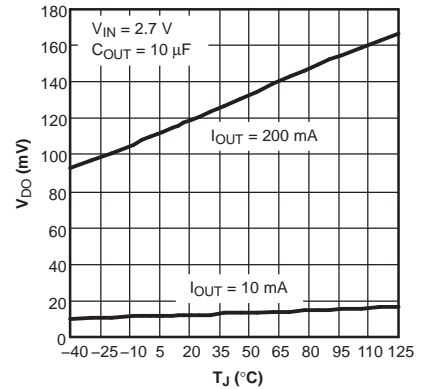


Figure 10.

TYPICAL CHARACTERISTICS (SOT23 PACKAGE) (continued)

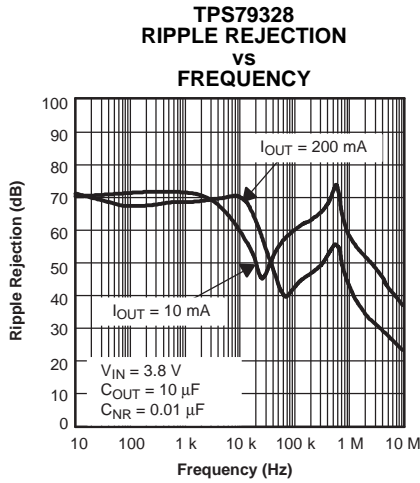


Figure 11.

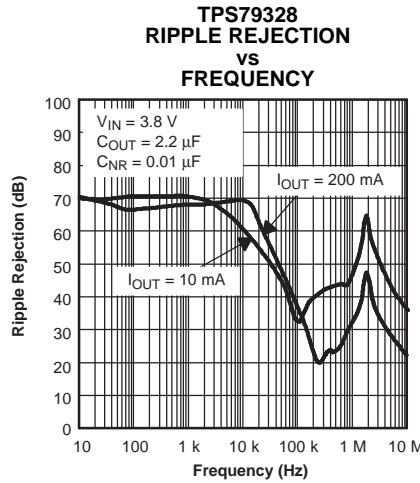


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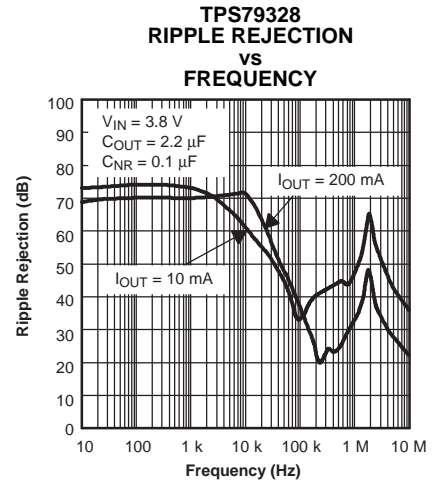


Figure 13.

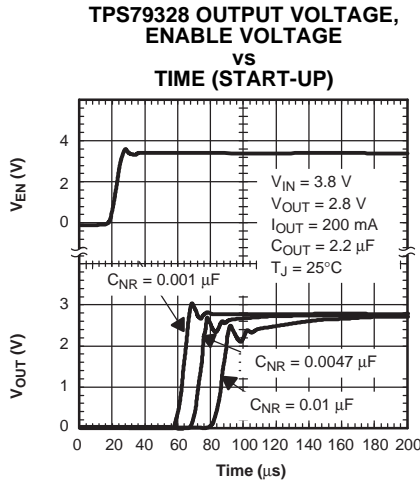


Figure 14.

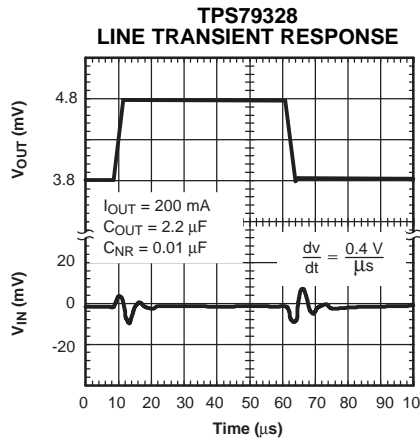


Figure 15.

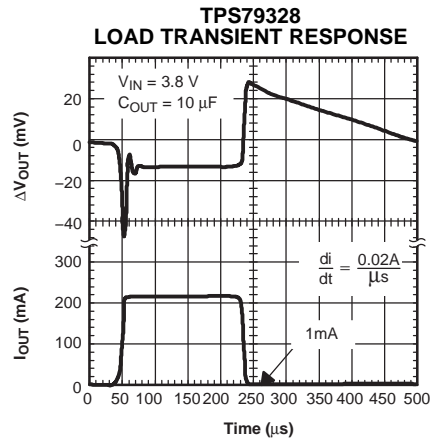


Figure 16.

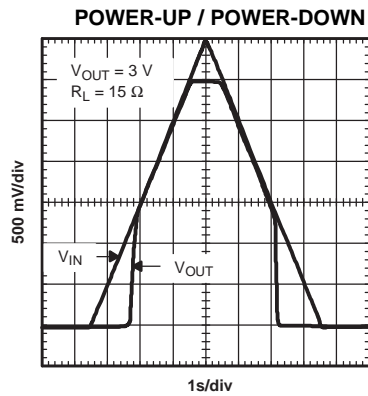


Figure 17.

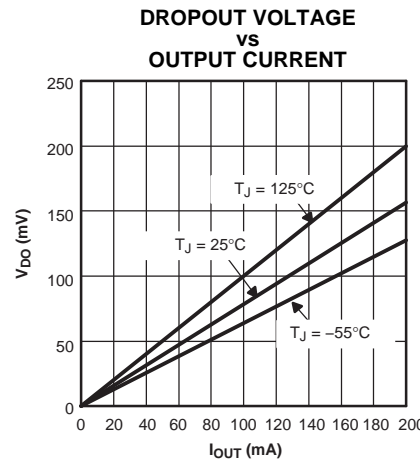


Figure 18.

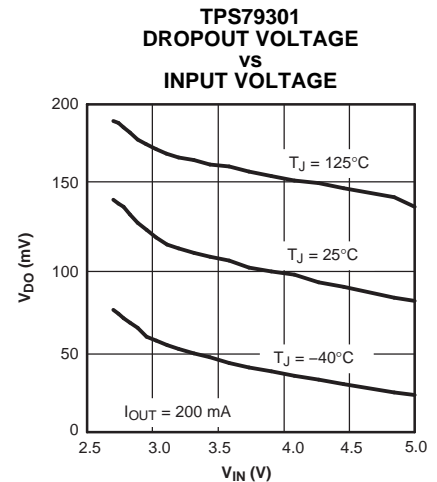


Figure 19.

TYPICAL CHARACTERISTICS (SOT23 PACKAGE) (continued)

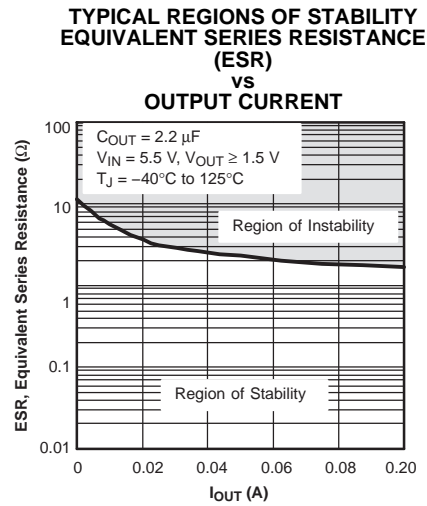


Figure 20.

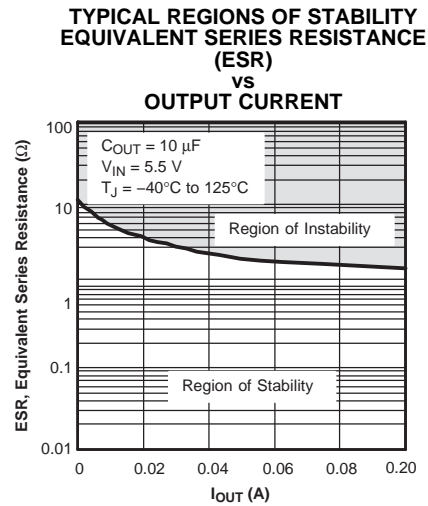


Figure 21.

APPLICATION INFORMATION

The TPS793xx family of low-dropout (LDO) regulators has been optimized for use in noise-sensitive battery-operated equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current (170 μ A typically), and enable-input to reduce supply currents to less than 1 μ A when the regulator is turned off.

A typical application circuit is shown in [Figure 22](#).

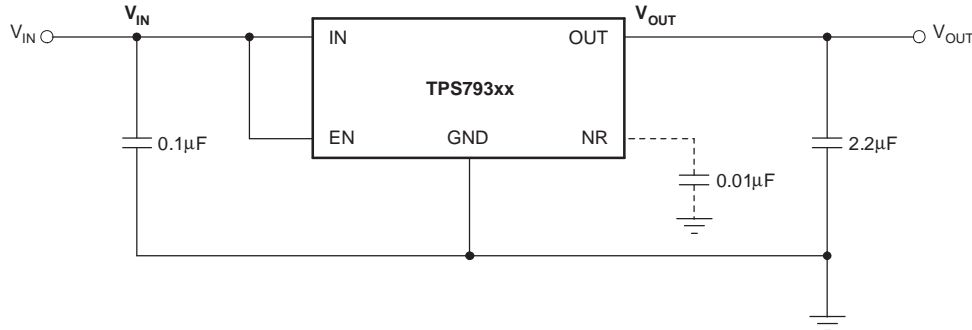


Figure 22. Typical Application Circuit

External Capacitor Requirements

A 0.1 μ F or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS793xx, is required for stability and improves transient response, noise rejection, and ripple rejection. A higher-value input capacitor may be necessary if large, fast-rise-time load transients are anticipated or the device is located several inches from the power source.

Like most low-dropout regulators, the TPS793xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 2.2 μ F. Any 2.2 μ F or larger ceramic capacitor is suitable, provided the capacitance does not vary significantly over temperature. If load current is not expected to exceed 100mA, a 1.0 μ F ceramic capacitor can be used.

The internal voltage reference is a key source of noise in an LDO regulator. The TPS793xx has an NR pin which is connected to the voltage reference through a 250k Ω internal resistor. The 250k Ω internal resistor, in conjunction with an external bypass capacitor connected to the NR pin, creates a low-pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. In order for the regulator to operate properly, the current flow out of the NR pin must be at a minimum, because any leakage current creates an IR drop across the internal resistor, thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current. The bypass capacitor should be no more than 0.1 μ F to ensure that it is fully charged during the quickstart time provided by the internal switch shown in the [Functional Block Diagrams](#).

As an example, the TPS79328 exhibits only 32 μ V_{RMS} of output voltage noise using a 0.1 μ F ceramic bypass capacitor and a 2.2 μ F ceramic output capacitor. Note that the output starts up slower as the bypass capacitance increases due to the RC time constant at the NR pin that is created by the internal 250k Ω resistor and external capacitor.

Board Layout Recommendation to Improve PSRR and Noise Performance

To improve ac measurements like PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT} , with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

Power Dissipation and Junction Temperature

Specified regulator operation is assured to a junction temperature of +125°C; the maximum junction temperature should be restricted to +125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D , which must be less than or equal to $P_{D(max)}$.

The maximum power dissipation limit is determined using [Equation 1](#):

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}} \quad (1)$$

Where:

- T_{Jmax} is the maximum allowable junction temperature.
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package (see the [Dissipation Ratings Table](#)).
- T_A is the ambient temperature.

The regulator dissipation is calculated using [Equation 2](#):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

Programming the TPS79301 Adjustable LDO Regulator

The output voltage of the TPS79301 adjustable regulator is programmed using an external resistor divider as shown in [Figure 23](#). The output voltage is calculated using [Equation 3](#):

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2} \right) \quad (3)$$

Where:

- $V_{REF} = 1.2246V$ typ (the internal reference voltage)

Resistors R_1 and R_2 should be chosen for approximately 50µA divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Higher resistor values should be avoided as leakage current into/out of FB across R_1/R_2 creates an offset voltage that artificially increases/decreases the feedback voltage and thus erroneously decreases/increases V_{OUT} . The recommended design procedure is to choose $R_2 = 30.1k\Omega$ to set the divider current at 50µA, $C_1 = 15pF$ for stability, and then calculate R_1 using [Equation 4](#):

$$R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \times R_2 \quad (4)$$

In order to improve the stability of the adjustable version, it is suggested that a small compensation capacitor be placed between OUT and FB. For voltages less than 1.8V, the value of this capacitor should be 100pF. For voltages greater than 1.8V, the approximate value of this capacitor can be calculated as shown in [Equation 5](#):

$$C_1 = \frac{(3 \times 10^{-7}) \times (R_1 + R_2)}{(R_1 \times R_2)} \quad (5)$$

The suggested value of this capacitor for several resistor ratios is shown in the table below. If this capacitor is not used (such as in a unity-gain configuration) or if an output voltage less than 1.8V is chosen, then the minimum recommended output capacitor is 4.7µF instead of 2.2µF.

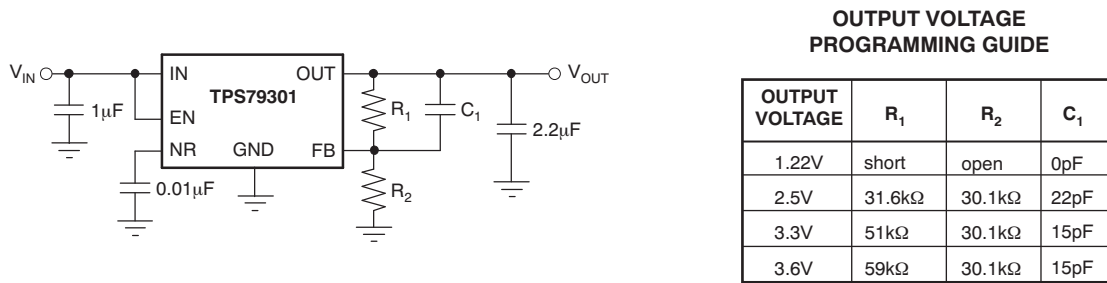


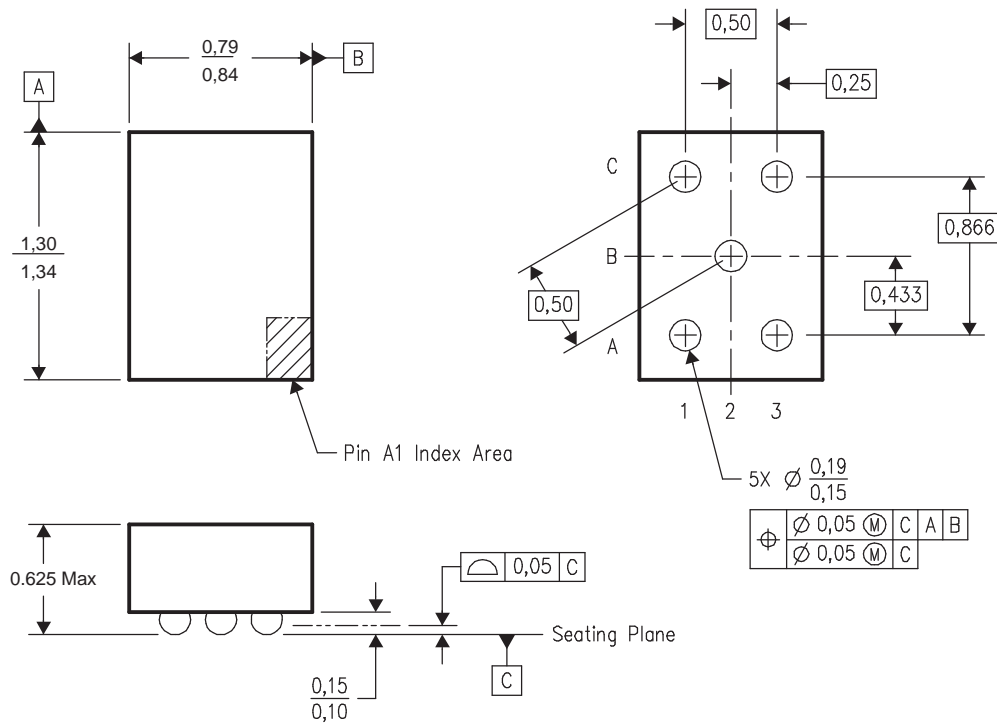
Figure 23. TPS79301 Adjustable LDO Regulator Programming

Regulator Protection

The TPS793xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power-down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS793xx features internal current limiting and thermal protection. During normal operation, the TPS793xx limits output current to approximately 400mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package or the absolute maximum voltage ratings of the device. If the temperature of the device exceeds approximately +165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately +140°C, regulator operation resumes.

TPS793xxYEQ, YZQ NanoStar™ Wafer Chip Scale Information



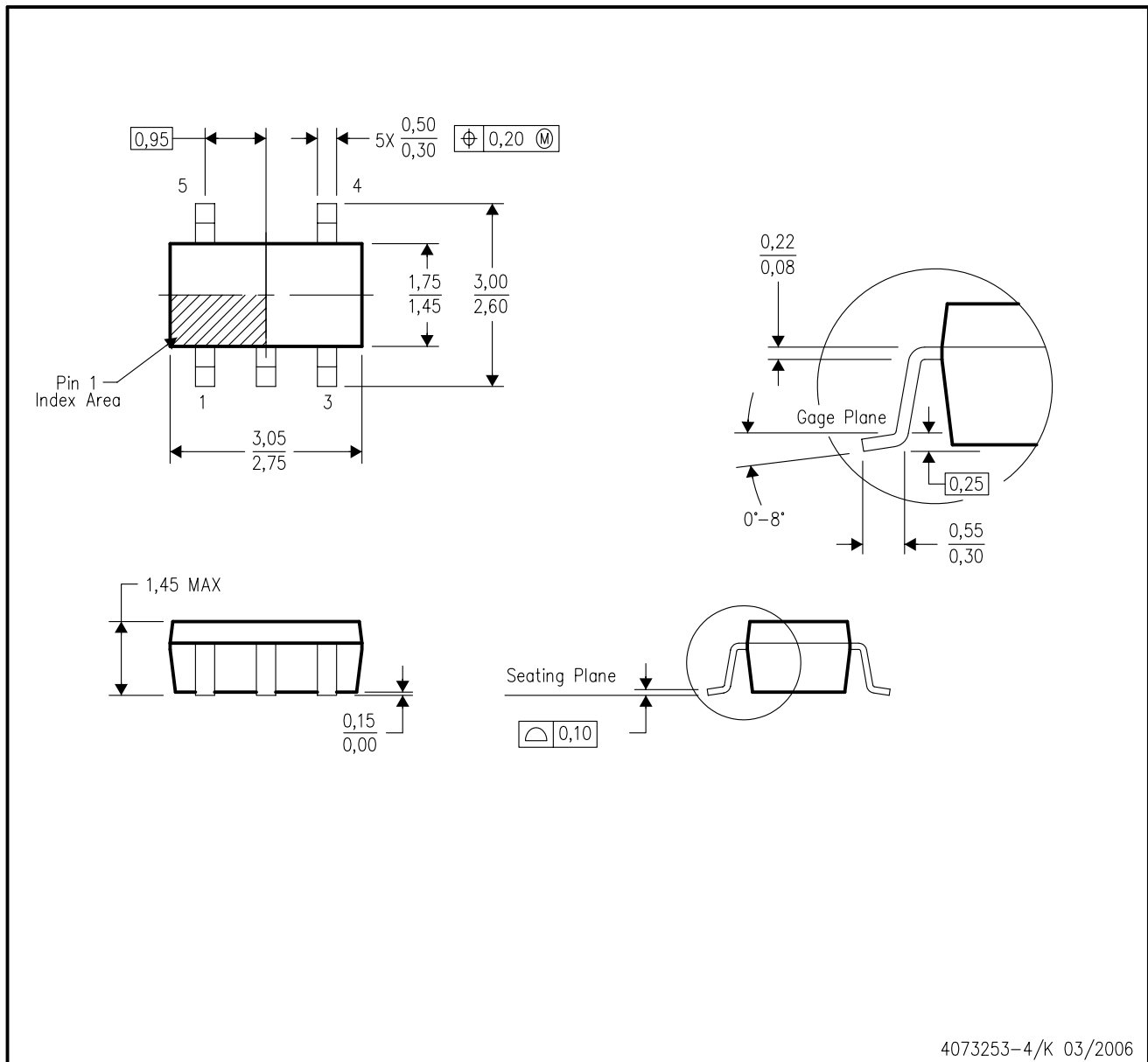
- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. NanoStar™ package configuration.

NanoStar is a trademark of Texas Instruments.

Figure 24. NanoStar™ Wafer Chip Scale Package

DBV (R-PDSO-G5)

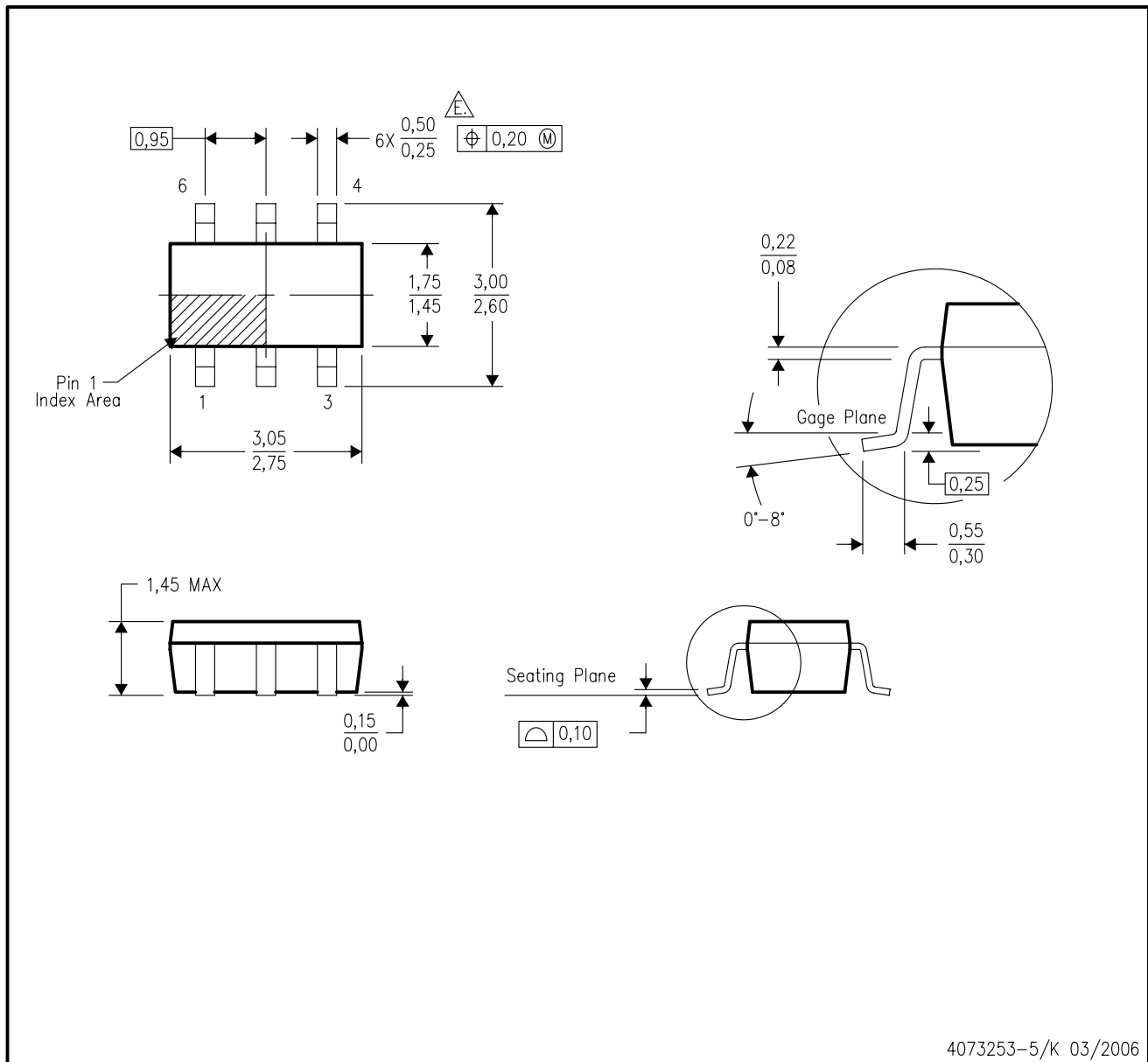
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- $\triangle E$ Falls within JEDEC MO-178 Variation AB, except minimum lead width.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPS79301DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79301DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79318DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79318DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79318DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79318DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79318YEQR	ACTIVE	DSBGA	YEQ	5	3000	Green (RoHS & no Sb/Br)	SNPB	Level-1-260C-UNLIM
TPS79318YEQT	NRND	DSBGA	YEQ	5	250	Green (RoHS & no Sb/Br)	SNPB	Level-1-260C-UNLIM
TPS79318YZQR	ACTIVE	DSBGA	YZQ	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79318YZQT	ACTIVE	DSBGA	YZQ	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79325DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79325DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79325YEQR	ACTIVE	DSBGA	YEQ	5	3000	Green (RoHS & no Sb/Br)	SNPB	Level-1-260C-UNLIM
TPS79325YEQT	NRND	DSBGA	YEQ	5	250	Green (RoHS & no Sb/Br)	SNPB	Level-1-260C-UNLIM
TPS79325YZQR	ACTIVE	DSBGA	YZQ	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79325YZQT	ACTIVE	DSBGA	YZQ	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS793285DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS793285DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS793285DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS793285DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS793285YEQR	NRND	DSBGA	YEQ	5	3000	Green (RoHS & no Sb/Br)	SNPB	Level-1-260C-UNLIM
TPS793285YEQT	NRND	DSBGA	YEQ	5	250	Green (RoHS & no Sb/Br)	SNPB	Level-1-260C-UNLIM
TPS793285YZQR	ACTIVE	DSBGA	YZQ	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS793285YZQT	ACTIVE	DSBGA	YZQ	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79328DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPS79328DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79328YEQR	NRND	DSBGA	YEQ	5	3000	Green (RoHS & no Sb/Br)	SNPB	Level-1-260C-UNLIM
TPS79328YEQT	NRND	DSBGA	YEQ	5	250	Green (RoHS & no Sb/Br)	SNPB	Level-1-260C-UNLIM
TPS79328YZQR	ACTIVE	DSBGA	YZQ	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79328YZQT	ACTIVE	DSBGA	YZQ	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79330DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79330DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79330YEQR	NRND	DSBGA	YEQ	5	3000	Green (RoHS & no Sb/Br)	SNPB	Level-1-260C-UNLIM
TPS79330YEQT	NRND	DSBGA	YEQ	5	250	Green (RoHS & no Sb/Br)	SNPB	Level-1-260C-UNLIM
TPS79330YZQR	ACTIVE	DSBGA	YZQ	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79330YZQT	ACTIVE	DSBGA	YZQ	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TPS79333DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79333DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS793475DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS793475DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

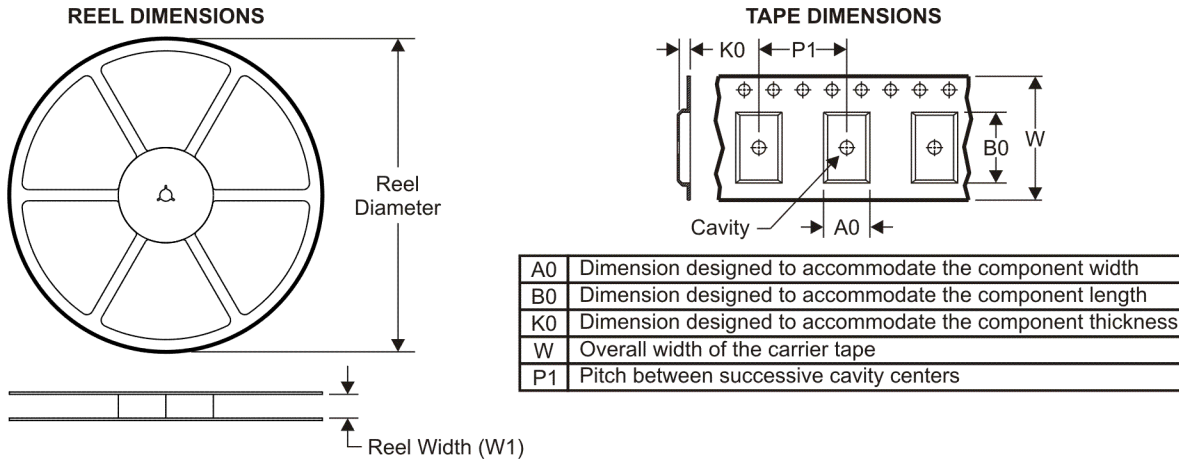
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

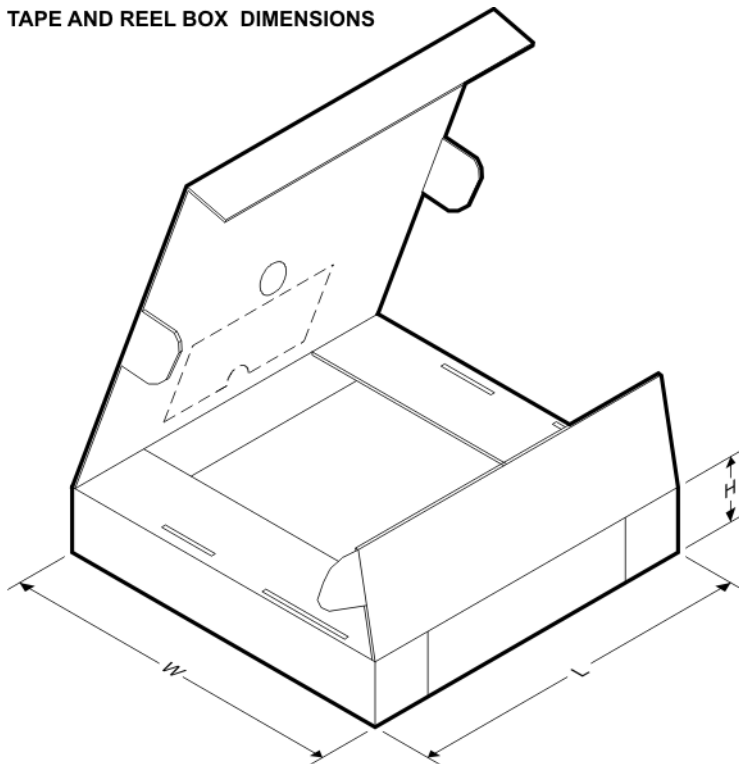


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79301DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79301DBVR	SOT-23	DBV	6	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS79318DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79318DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79318YEQR	DSBGA	YEQ	5	3000	178.0	8.4	0.96	1.46	0.69	4.0	8.0	Q1
TPS79318YZQR	DSBGA	YZQ	5	3000	178.0	8.4	0.98	1.46	0.69	4.0	8.0	Q1
TPS79318YZQT	DSBGA	YZQ	5	250	178.0	8.4	0.98	1.46	0.69	4.0	8.0	Q1
TPS79325DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79325DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS79325YEQR	DSBGA	YEQ	5	3000	178.0	8.4	0.96	1.46	0.69	4.0	8.0	Q1
TPS79325YZQR	DSBGA	YZQ	5	3000	178.0	8.4	0.98	1.46	0.69	4.0	8.0	Q1
TPS79325YZQT	DSBGA	YZQ	5	250	178.0	8.4	0.98	1.46	0.69	4.0	8.0	Q1
TPS793285DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS793285DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS793285YEQR	DSBGA	YEQ	5	3000	178.0	8.4	0.96	1.46	0.69	4.0	8.0	Q1
TPS793285YZQR	DSBGA	YZQ	5	3000	178.0	8.4	0.98	1.46	0.69	4.0	8.0	Q1
TPS793285YZQT	DSBGA	YZQ	5	250	178.0	8.4	0.98	1.46	0.69	4.0	8.0	Q1
TPS793285YZQT	DSBGA	YZQ	5	250	178.0	8.4	0.96	1.46	0.69	4.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79328DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79328YEQR	DSBGA	YEQ	5	3000	178.0	8.4	0.96	1.46	0.69	4.0	8.0	Q1
TPS79328YEQT	DSBGA	YEQ	5	250	178.0	8.4	0.96	1.46	0.69	4.0	8.0	Q1
TPS79328YZQR	DSBGA	YZQ	5	3000	178.0	8.4	0.98	1.46	0.69	4.0	8.0	Q1
TPS79328YZQT	DSBGA	YZQ	5	250	178.0	8.4	0.98	1.46	0.69	4.0	8.0	Q1
TPS79330DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79330YEQR	DSBGA	YEQ	5	3000	178.0	8.4	0.96	1.46	0.69	4.0	8.0	Q1
TPS79330YEQT	DSBGA	YEQ	5	250	178.0	8.4	0.96	1.46	0.69	4.0	8.0	Q1
TPS79330YZQR	DSBGA	YZQ	5	3000	178.0	8.4	0.98	1.46	0.69	4.0	8.0	Q1
TPS79330YZQT	DSBGA	YZQ	5	250	178.0	8.4	0.98	1.46	0.69	4.0	8.0	Q1
TPS79330YZQT	DSBGA	YZQ	5	250	178.0	8.4	0.96	1.46	0.69	4.0	8.0	Q1
TPS79333DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS79333DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS793475DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79301DBVR	SOT-23	DBV	6	3000	195.0	200.0	45.0
TPS79301DBVR	SOT-23	DBV	6	3000	182.0	182.0	20.0
TPS79318DBVR	SOT-23	DBV	5	3000	195.0	200.0	45.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79318DBVT	SOT-23	DBV	5	250	195.0	200.0	45.0
TPS79318YEQR	DSBGA	YEQ	5	3000	195.2	193.7	34.9
TPS79318YZQR	DSBGA	YZQ	5	3000	217.0	193.0	35.0
TPS79318YZQT	DSBGA	YZQ	5	250	217.0	193.0	35.0
TPS79325DBVR	SOT-23	DBV	5	3000	195.0	200.0	45.0
TPS79325DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS79325YEQR	DSBGA	YEQ	5	3000	195.2	193.7	34.9
TPS79325YZQR	DSBGA	YZQ	5	3000	217.0	193.0	35.0
TPS79325YZQT	DSBGA	YZQ	5	250	217.0	193.0	35.0
TPS793285DBVR	SOT-23	DBV	5	3000	195.0	200.0	45.0
TPS793285DBVT	SOT-23	DBV	5	250	195.0	200.0	45.0
TPS793285YEQR	DSBGA	YEQ	5	3000	195.2	193.7	34.9
TPS793285YZQR	DSBGA	YZQ	5	3000	217.0	193.0	35.0
TPS793285YZQT	DSBGA	YZQ	5	250	217.0	193.0	35.0
TPS793285YZQT	DSBGA	YZQ	5	250	195.2	193.7	34.9
TPS79328DBVR	SOT-23	DBV	5	3000	195.0	200.0	45.0
TPS79328YEQR	DSBGA	YEQ	5	3000	195.2	193.7	34.9
TPS79328YEQT	DSBGA	YEQ	5	250	195.2	193.7	34.9
TPS79328YZQR	DSBGA	YZQ	5	3000	217.0	193.0	35.0
TPS79328YZQT	DSBGA	YZQ	5	250	217.0	193.0	35.0
TPS79330DBVR	SOT-23	DBV	5	3000	195.0	200.0	45.0
TPS79330YEQR	DSBGA	YEQ	5	3000	195.2	193.7	34.9
TPS79330YEQT	DSBGA	YEQ	5	250	195.2	193.7	34.9
TPS79330YZQR	DSBGA	YZQ	5	3000	217.0	193.0	35.0
TPS79330YZQT	DSBGA	YZQ	5	250	217.0	193.0	35.0
TPS79330YZQT	DSBGA	YZQ	5	250	195.2	193.7	34.9
TPS79333DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS79333DBVR	SOT-23	DBV	5	3000	195.0	200.0	45.0
TPS793475DBVR	SOT-23	DBV	5	3000	195.0	200.0	45.0

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