ULTRALOW-NOISE, HIGH PSRR, FAST RF 200-mA LOW-DROPOUT LINEAR REGULATORS IN NANOSTAR™ WAFER CHIP SCALE AND SOT23

FEATURES

- **200-mA RF Low-Dropout Regulator With Enable**
- **Available in 1.8-V, 2.5-V, 2.8-V, 2.85-V, 3-V, 3.3-V, 4.75-V, and Adj (1.22 V to 5.5 V)**
- **High PSRR (70 dB at 10 kHz)**
- **Ultralow Noise (32 µV)**
- **Fast Start-Up Time (50 µs)**
- **Stable With a 2.2-µF Ceramic Capacitor**
- **Excellent Load/Line Transient Response**
- **Very Low Dropout Voltage (112 mV at Full Load, TPS79330)**
- **5-Pin SOT23 (DBV) and NanoStar Wafer Chip Scale (YEQ) Packages**

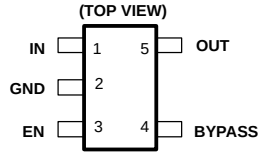
APPLICATIONS

- **Cellular and Cordless Telephones**
- **Bluetooth™, Wireless LAN**
- **RF**
- **VCOs**
- **Handheld Organizers, PDA**

DESCRIPTION

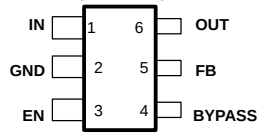
The TPS793xx family of low-dropout (LDO) low-power linear voltage regulators features high power supply rejection ratio (PSRR), ultralow noise, fast start-up, and excellent line and load transient responses in NanoStar wafer chip scale and SOT23 packages. NanoStar packaging gives an ultrasmall footprint as well as an ultralow profile and package weight, making it ideal for portable applications such as handsets and PDAs. Each device in the family is stable, with a small 2.2-µF ceramic capacitor on the output. The TPS793xx family uses an advanced, proprietary BiCMOS fabrication process to yield extremely low dropout voltages (e.g., 112 mV at 200 mA, TPS79330). Each device achieves fast start-up times (approximately 50 µs with a 0.001-µF bypass capacitor) while consuming very low quiescent current (170 µA typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than 1 µA. The TPS79328 exhibits approximately 32 μV_{RMS} of output voltage noise with a 0.1-µF bypass capacitor. Applications with analog components that are noise sensitive, such as portable RF electronics, benefit from the high PSRR and low-noise features as well as the fast response time.

DBV PACKAGE
(TOP VIEW)



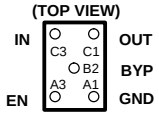
Fixed Option

DBV PACKAGE
(TOP VIEW)

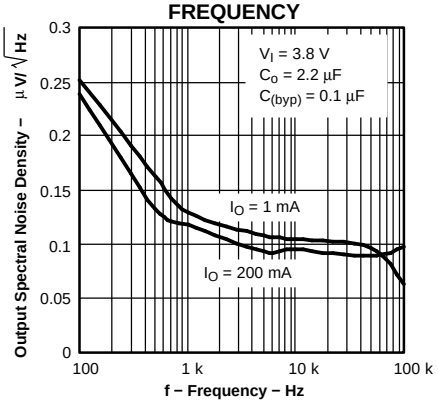


Adjustable Option

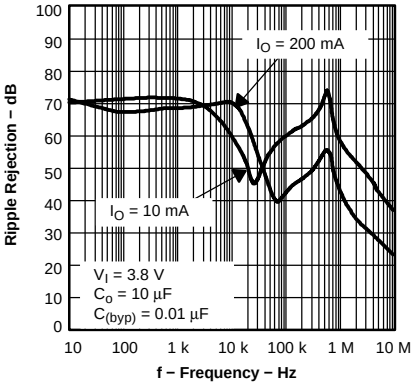
YEQ
PACKAGE
(TOP VIEW)



TPS79328
OUTPUT SPECTRAL NOISE DENSITY
VS
FREQUENCY



TPS79328
RIPPLE REJECTION
VS
FREQUENCY



AVAILABLE OPTIONS

T_J	VOLTAGE	PACKAGE	PART NUMBER	SYMBOL
-40°C to 125°C	1.22 to 5.5 V	SOT23 (DBV)	TPS79301DBVR(1)	PGVI
	1.8 V		TPS79318DBVR(1)	PHHI
	1.8 V	CSP (YEQ)	TPS79318YEQ (2)(3)	79318
	2.5 V	SOT23 (DBV)	TPS79325DBVR(1)	PGWI
	2.5 V	CSP (YEQ)	TPS79325YEQ (2)(3)	79325
	2.8 V	SOT23 (DBV)	TPS79328DBVR(1)	PGXI
	2.8 V	CSP (YEQ)	TPS79328YEQ (2)(3)	79328
	2.85 V	SOT23 (DBV)	TPS793285DBVR(1)	PHII
	2.85 V	CSP (YEQ)	TPS793285YEQ (2)	793285
	3 V	SOT23 (DBV)	TPS79330DBVR(1)	PGYI
	3 V	CSP (YEQ)	TPS79330YEQ (2)(3)	79330
	3.3 V	SOT23 (DBV)	TPS79333DBVR(1)	PHUI
	4.75 V		TPS793475DBVR(1)	PHJI

(1) The DBVR indicates tape and reel of 3000 parts.
(2) The YEQR indicates tape and reel of 3000 parts. YEQT indicates tape and reel of 250 parts.
(3) Product preview stage of development.

ABSOLUTE MAXIMUM RATINGS

over operating temperature range (unless otherwise noted)(1)

	UNIT
Input voltage range	-0.3 V to 6 V
Voltage range at EN	-0.3 V to V_I + 0.3 V
Voltage range at OUT	-0.3 V to 6 V
Peak output current	Internally limited
ESD rating, HBM	2 kV
ESD rating, CDM	500 V
Continuous total power dissipation	See Dissipation Rating Table
Operating junction temperature range, DBV package	-40°C to 150°C
Operating junction temperature range, YEQ package	-40°C to 125°C
Operating ambient temperature range, T_A	-40°C to 85°C
Storage temperature range, T_{stg}	-65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

BOARD	PACKAGE	$R_{\Theta JC}$	$R_{\Theta JA}$	DERATING FACTOR ABOVE T_A = 25°C	$T_A \leq$ 25°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
Low K(1)	DBV	65°C/W	255°C/W	3.9 mW/°C	390 mW	215 mW	155 mW
High K(2)	DBV	65°C/W	180°C/W	5.6 mW/°C	560 mW	310 mW	225 mW
Low K(1)	YEQ	27°C/W	255°C/W	3.9 mW/°C	390 mW	215 mW	155 mW
High K(2)	YEQ	27°C/W	190°C/W	5.3 mW/°C	530 mW	296 mW	216 mW

(1) The JEDEC low K (1s) board design used to derive this data was a 3-inch x 3-inch, two layer board with 2 ounce copper traces on top of the board.
(2) The JEDEC high K (2s2p) board design used to derive this data was a 3-inch x 3-inch, multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.

ELECTRICAL CHARACTERISTICS

over recommended operating temperature range EN = V_I, T_J = -40 to 125 °C, $V_I = V_{O(typ)}$ + 1 V, I_O= 1 mA, C_o = 10 µF, $C_{(byp)}$ = 0.01 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_I Input voltage (1)				2.7		5.5	V
I_O Continuous output current				0		200	mA
T_J Operating junction temperature				-40		125	°C
Output voltage	TPS79301	0 µA< I_O < 200 mA, (see Note 4)	1.22 V ≤ V_O≤ 5.2 V,	0.98 V_O		1.02 V_O	V
	TPS79318	T_J = 25°C			1.8		V
		0 µA< I_O < 200 mA,	2.8 V < V_I < 5.5 V	1.764		1.836	
	TPS79325	T_J = 25°C			2.5		V
		0 µA< I_O < 200 mA,	3.5 V < V_I < 5.5 V	2.45		2.55	
	TPS79328	T_J = 25°C			2.8		V
		0 µA< I_O < 200 mA,	3.8 V < V_I < 5.5 V	2.744		2.856	
	TPS793285	T_J = 25°C			2.85		V
		0 µA< I_O < 200 mA,	3.85 V < V_I < 5.5 V	2.793		2.907	
	TPS79330	T_J = 25°C			3		V
		0 µA< I_O < 200 mA,	4 V < V_I < 5.5 V	2.94		3.06	
	TPS79333	T_J = 25°C			3.3		V
		0 µA ≤ I_O < 200 mA,	4.3 V < V_I < 5.5 V	3.234		3.366	
	TPS793475	T_J = 25°C			4.75		V
		0 µA< I_O < 200 mA,	5.25 V < V_I < 5.5 V	4.655		4.845	
Quiescent current (GND current)		0 µA< I_O < 200 mA,	T_J = 25°C		170		µA
		0 µA< I_O < 200 mA				220	µA
Load regulation		0 µA< I_O < 200 mA,	T_J = 25°C		5		mV
Output voltage line regulation ($\Delta V_O/V_O$) (2)		V_O + 1 V < V_I≤ 5.5 V,	T_J = 25°C		0.05		%/V
		V_O + 1 V < V_I≤ 5.5 V				0.12	
Output noise voltage (TPS79328)		BW = 200 Hz to 100 kHz,I_O = 200 mA, T_J = 25°C	$C_{(byp)}$ = 0.001 µF		55		μV_{RMS}
			$C_{(byp)}$ = 0.0047 µF		36		
			$C_{(byp)}$ = 0.01 µF		33		
			$C_{(byp)}$ = 0.1 µF		32		
Time, start-up (TPS79328)		R_L = 14 Ω, C_o=1 µF, T_J = 25°C	$C_{(byp)}$ = 0.001 µF		50		µs
			$C_{(byp)}$ = 0.0047 µF		70		
			$C_{(byp)}$ = 0.01 µF		100		
Output current limit		V_O = 0 V,		285		600	mA

(1) Minimum $V_{(IN)}$ is 2.7 V or $V_{(OUT)}$ + $V_{(DO)}$, whichever is greater.
(2) If $V_O \leq$ 2.5 V then $V_{(IN),min}$ = 2.7 V, $V_{(IN),max}$ = 5.5 V.

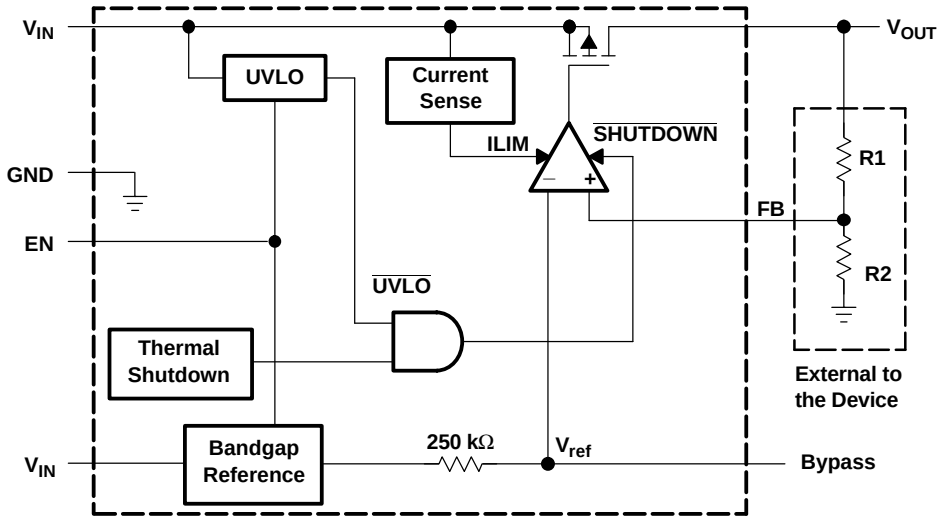
ELECTRICAL CHARACTERISTICS (continued)

over recommended operating temperature range EN = V_I, T_J = -40 to 125 °C, V_I = $V_{O(typ)}$ + 1 V, I_O= 1 mA, C_o = 10 µF, $C_{(byp)}$ = 0.01 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Standby current		EN = 0 V, 2.7 V < V_I < 5.5 V			0.07	1	µA
High level enable input voltage		2.7 V < V_I < 5.5 V		2			V
Low level enable input voltage		2.7 V < V_I < 5.5 V				0.7	V
Input current (EN)		EN = 0		-1		1	µA
Input current (FB) (TPS79301)		FB = 1.8 V				1	µA
Power supply ripple rejection	TPS79328	f = 100 Hz, T_J = 25°C,	I_O = 10 mA		70		dB
		f = 100 Hz, T_J = 25°C,	I_O = 200 mA		68		
		f = 10 kHz, T_J = 25°C,	I_O = 200 mA		70		
		f = 100 kHz, T_J = 25°C,	I_O = 200 mA		43		
Dropout voltage (3)	TPS79328	I_O = 200 mA,	T_J = 25°C		120		mV
		I_O = 200 mA				200	
	TPS793285	I_O = 200 mA,	T_J = 25°C		120		
		I_O = 200 mA				200	
	TPS79330	I_O = 200 mA,	T_J = 25°C		112		
		I_O = 200 mA				200	
	TPS79333	I_O = 200 mA,	T_J = 25°C		102		mV
		I_O = 200 mA				180	
	TPS793475	I_O = 200 mA,	T_J = 25°C		77		mV
		I_O = 200 mA				125	
UVLO threshold		V_{CC} rising		2.25		2.65	V
UVLO hysteresis		T_J = 25°C	V_{CC} rising		100		mV

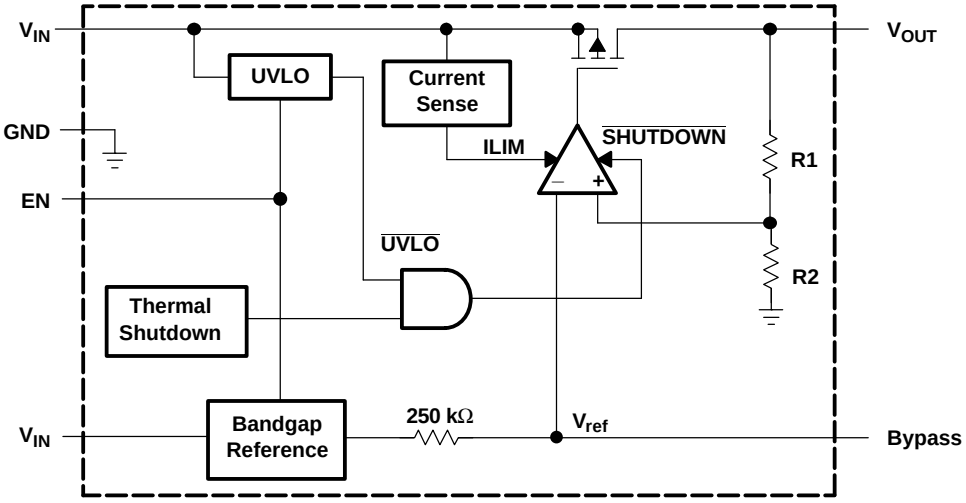
(3) $V_{(IN)}$ = $V_{(OUT),\ typ}$ - 100 mV. The TPS79325 dropout voltage is limited by the input voltage range.

FUNCTIONAL BLOCK DIAGRAM-ADJUSTABLE VERSION



Functional Block Diagram-Adjustable Version (continued)

Functional Block Diagram-Fixed Version



Terminal Functions

TERMINAL				DESCRIPTION
NAME	SOT23 ADJ	SOT23 FIXED	CSP FIXED	
BYPASS	4	4	B2	An external bypass capacitor, connected to this terminal, in conjunction with an internal resistor, creates a low-pass filter to further reduce regulator noise.
EN	3	3	A3	The EN terminal is an input which enables or shuts down the device. When EN goes to a logic high, the device will be enabled. When the device goes to a logic low, the device is in shutdown mode.
FB	5	N/A	N/A	This terminal is the feedback input voltage for the adjustable device.
GND	2	2	A1	Regulator ground
IN	1	1	C3	Unregulated input to the device.
OUT	6	5	C1	Output of the regulator.

TYPICAL CHARACTERISTICS (SOT23 PACKAGE)

TPS79328
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

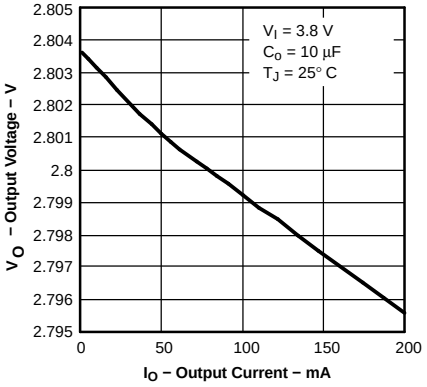


Figure 1.

TPS79328
OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

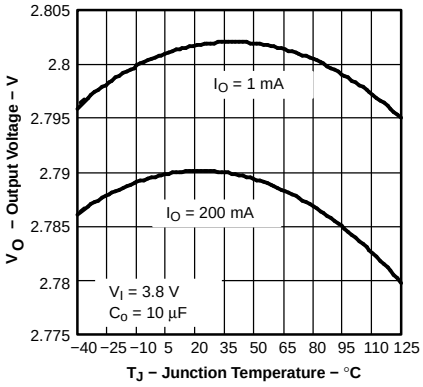


Figure 2.

TPS79328
GROUND CURRENT
vs
JUNCTION TEMPERATURE

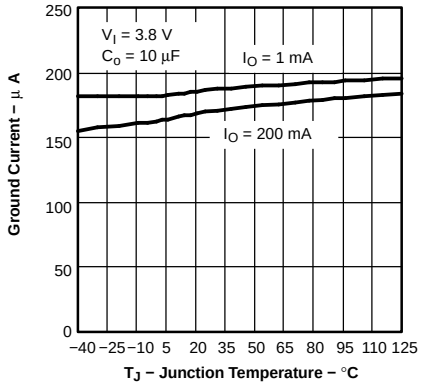


Figure 3.

TPS79328
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

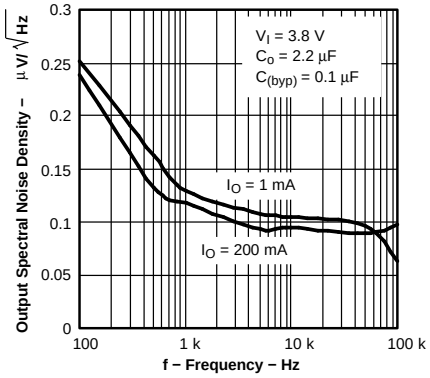


Figure 4.

TPS79328
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

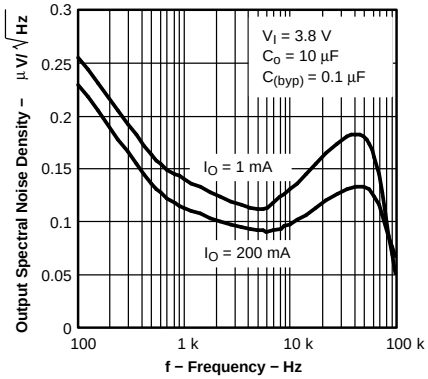


Figure 5.

TPS79328
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

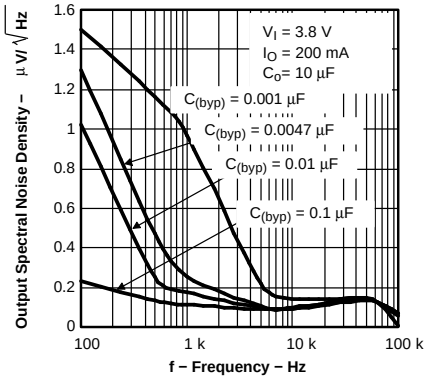


Figure 6.

TYPICAL CHARACTERISTICS (SOT23 PACKAGE) (continued)

ROOT MEAN SQUARE OUTPUT NOISE vs BYPASS CAPACITANCE

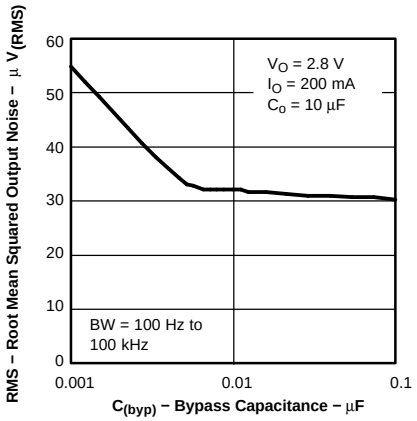


Figure 7.

OUTPUT IMPEDANCE vs FREQUENCY

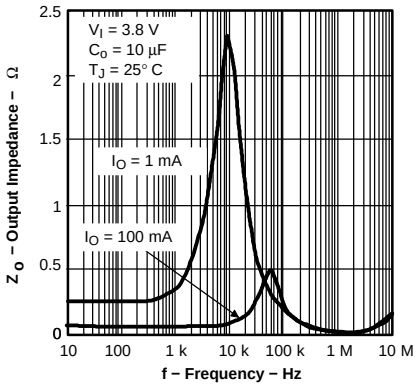


Figure 8.

TPS79328 DROPOUT VOLTAGE vs JUNCTION TEMPERATURE

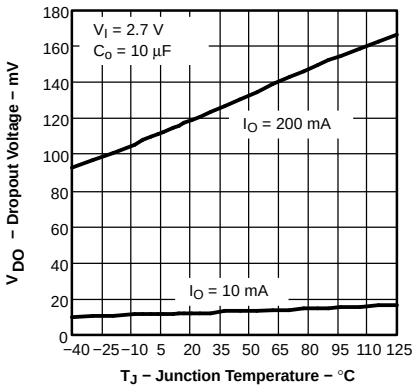


Figure 9.

TPS79328 RIPPLE REJECTION vs FREQUENCY

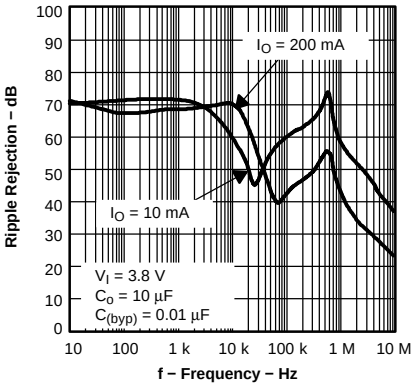


Figure 10.

TPS79328 RIPPLE REJECTION vs FREQUENCY

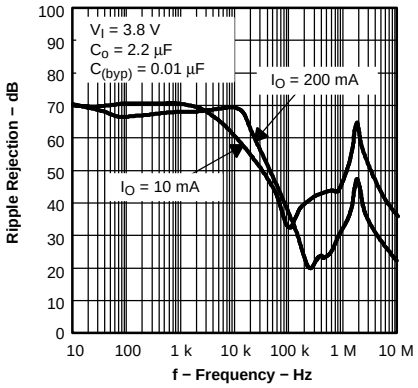


Figure 11.

TPS79328 RIPPLE REJECTION vs FREQUENCY

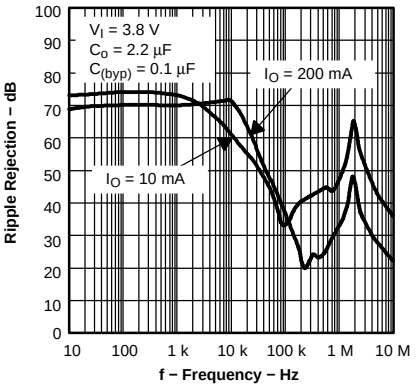


Figure 12.

TYPICAL CHARACTERISTICS (SOT23 PACKAGE) (continued)

TPS79328
OUTPUT VOLTAGE,
ENABLE VOLTAGE
vs
TIME (START-UP)

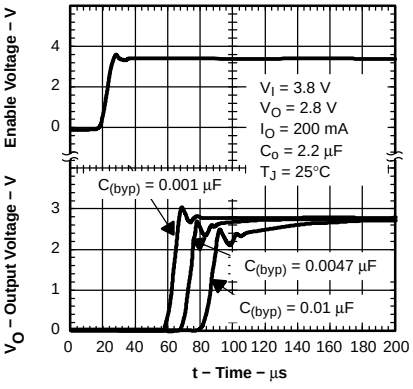


Figure 13.

TPD79328
LINE TRANSIENT RESPONSE

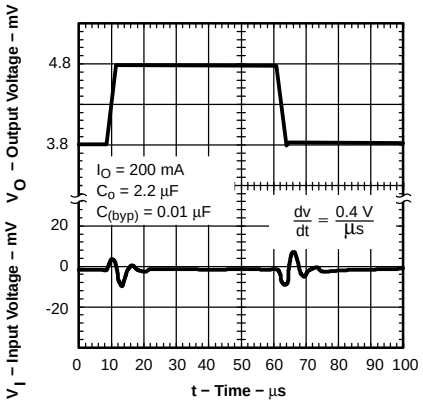


Figure 14.

TPD79328
LOAD TRANSIENT RESPONSE

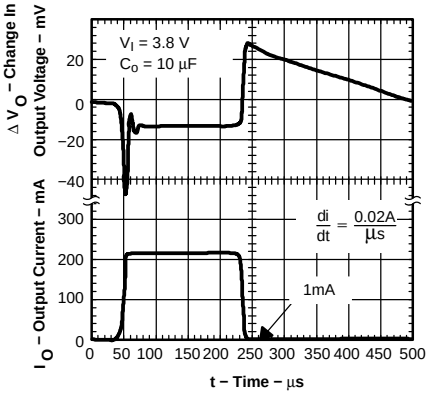


Figure 15.

POWER UP / POWER DOWN

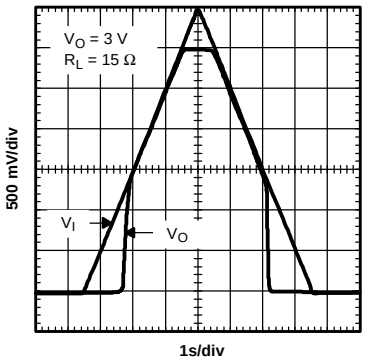


Figure 16.

DC DROPOUT VOLTAGE
vs
OUTPUT CURRENT

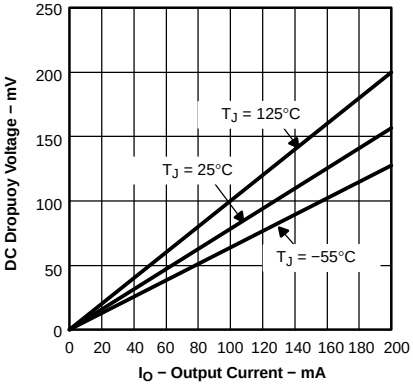


Figure 17.

TPS79301
DROPOUT VOLTAGE
vs
INPUT VOLTAGE

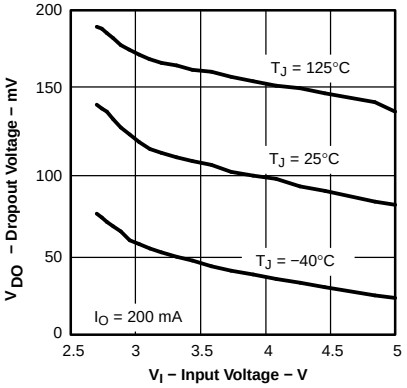


Figure 18.

TYPICAL CHARACTERISTICS (SOT23 PACKAGE) (continued)

MINIMUM REQUIRED INPUT VOLTAGE vs OUTPUT VOLTAGE

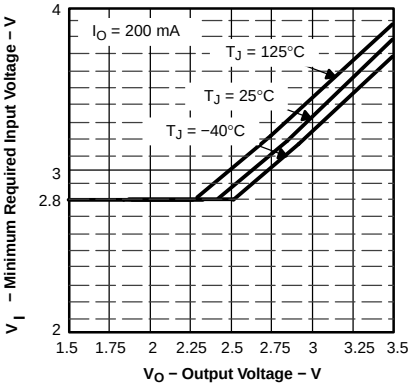


Figure 19.

TYPICAL REGIONS OF STABILITY EQUIVALENT SERIES RESISTANCE (ESR) vs OUTPUT CURRENT

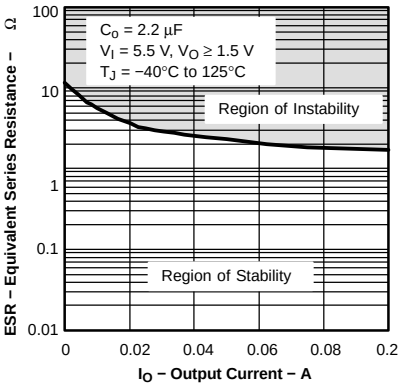


Figure 20.

TYPICAL REGIONS OF STABILITY EQUIVALENT SERIES RESISTANCE (ESR) vs OUTPUT CURRENT

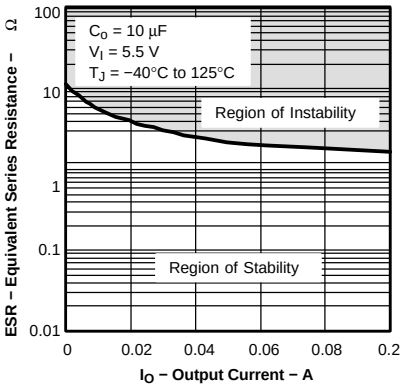


Figure 21.

APPLICATION INFORMATION

The TPS793xx family of low-dropout (LDO) regulators has been optimized for use in noise-sensitive battery-operated equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current (170 µA typically), and enable-input to reduce supply currents to less than 1 µA when the regulator is turned off.

A typical application circuit is shown in Figure 22.

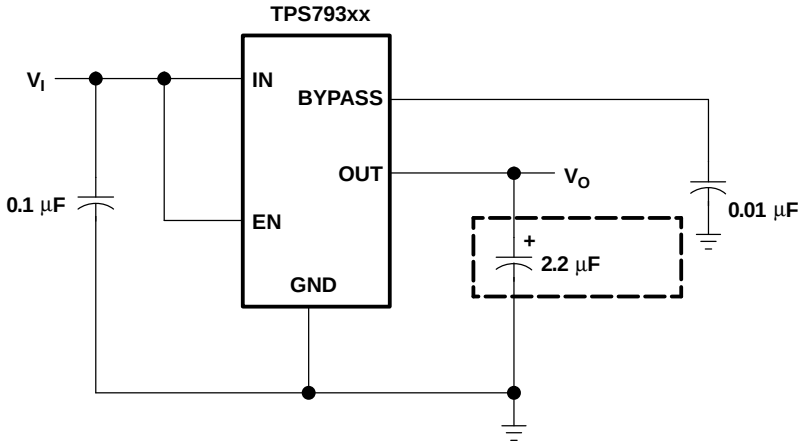


Figure 22. Typical Application Circuit

External Capacitor Requirements

A 0.1-µF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS793xx, is required for stability and improves transient response, noise rejection, and ripple rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like all low dropout regulators, the TPS793xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 2.2 µF. Any 2.2 µF or larger ceramic capacitor is suitable, provided the capacitance does not vary significantly over temperature.

The internal voltage reference is a key source of noise in an LDO regulator. The TPS793xx has a BYPASS pin which is connected to the voltage reference through a 250-kΩ internal resistor. The 250-kΩ internal resistor, in conjunction with an external bypass capacitor connected to the BYPASS pin, creates a low pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. In order for the regulator to operate properly, the current flow out of the BYPASS pin must be at a minimum, because any leakage current creates an IR drop across the internal resistor thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current.

For example, the TPS79328 exhibits only 32 μV_{RMS} of output voltage noise using a 0.1-µF ceramic bypass capacitor and a 2.2-µF ceramic output capacitor. Note that the output starts up slower as the bypass capacitance increases due to the RC time constant at the BYPASS pin that is created by the internal 250-kΩ resistor and external capacitor.

Board Layout Recommendation to Improve PSRR and Noise Performance

To improve ac measurements like PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

APPLICATION INFORMATION (continued)

Power Dissipation and Junction Temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}} \quad (1)$$

Where:

$T_J max$ is the maximum allowable junction temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, see the dissipation rating table.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = \left(V_I - V_O\right) \times I_O \quad (2)$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

Programming the TPS79301 Adjustable LDO Regulator

The output voltage of the TPS79301 adjustable regulator is programmed using an external resistor divider as shown in Figure 23. The output voltage is calculated using:

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \quad (3)$$

Where:

V_{ref} = 1.2246 V typ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 50-µA divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Higher resistor values should be avoided as leakage current into/out of FB across R1/R2 creates an offset voltage that artificially increases/decreases the feedback voltage and thus erroneously decreases/increases V_O. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at 50 µA, C1 = 15 pF for stability, and then calculate R1 using:

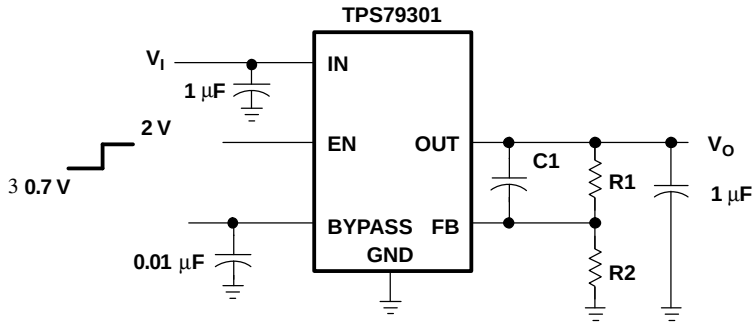
$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \quad (4)$$

In order to improve the stability of the adjustable version, it is suggested that a small compensation capacitor be placed between OUT and FB. For voltages <1.8 V, the value of this capacitor should be 100 pF. For voltages >1.8 V, the approximate value of this capacitor can be calculated as:

$$C1 = \frac{(3 \times 10^{-7}) \times (R1 + R2)}{(R1 \times R2)} \quad (5)$$

The suggested value of this capacitor for several resistor ratios is shown in the table below. If this capacitor is not used (such as in a unity-gain configuration) or if an output voltage <1.8 V is chosen, then the minimum recommended output capacitor is 4.7 µF instead of 2.2 µF.

APPLICATION INFORMATION (continued)



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	C1
1.22 V	short	open	0 pF
2.5 V	31.6 kΩ	30.1 kΩ	22 pF
3.3 V	51 kΩ	30.1 kΩ	15 pF
3.6 V	59 kΩ	30.1 kΩ	15 pF

Figure 23. TPS79301 Adjustable LDO Regulator Programming

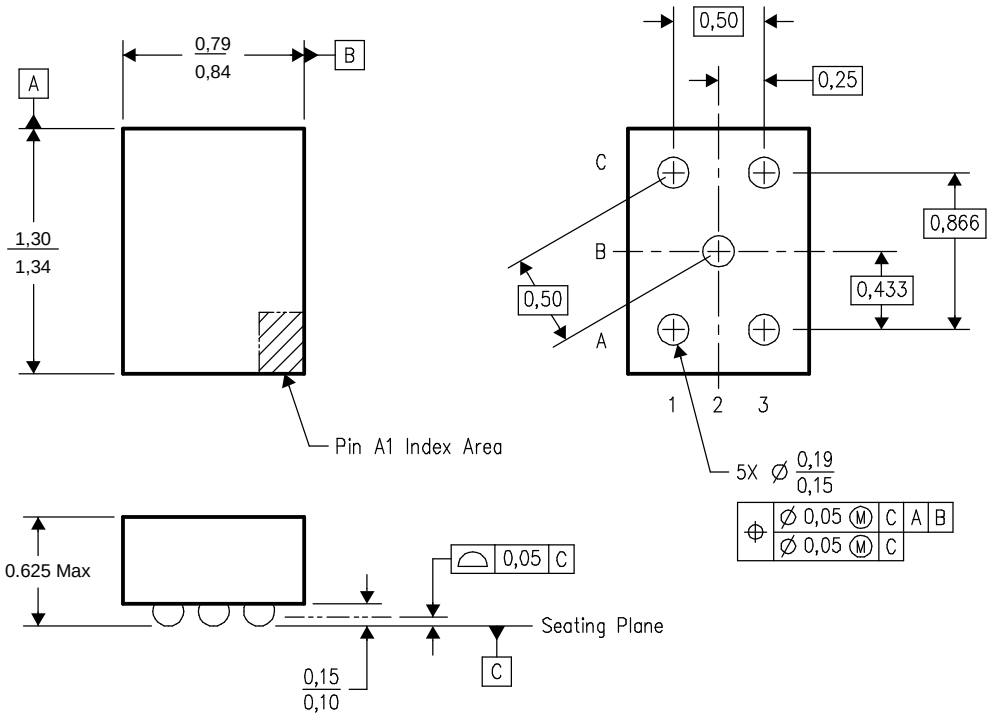
Regulator Protection

The TPS793xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS793xx features internal current limiting and thermal protection. During normal operation, the TPS793xx limits output current to approximately 400 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package or the absolute maximum voltage ratings of the device. If the temperature of the device exceeds approximately 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately 140°C, regulator operation resumes.

APPLICATION INFORMATION (continued)

TPS793xxYEQ NanoStar™ Wafer Chip Scale Information



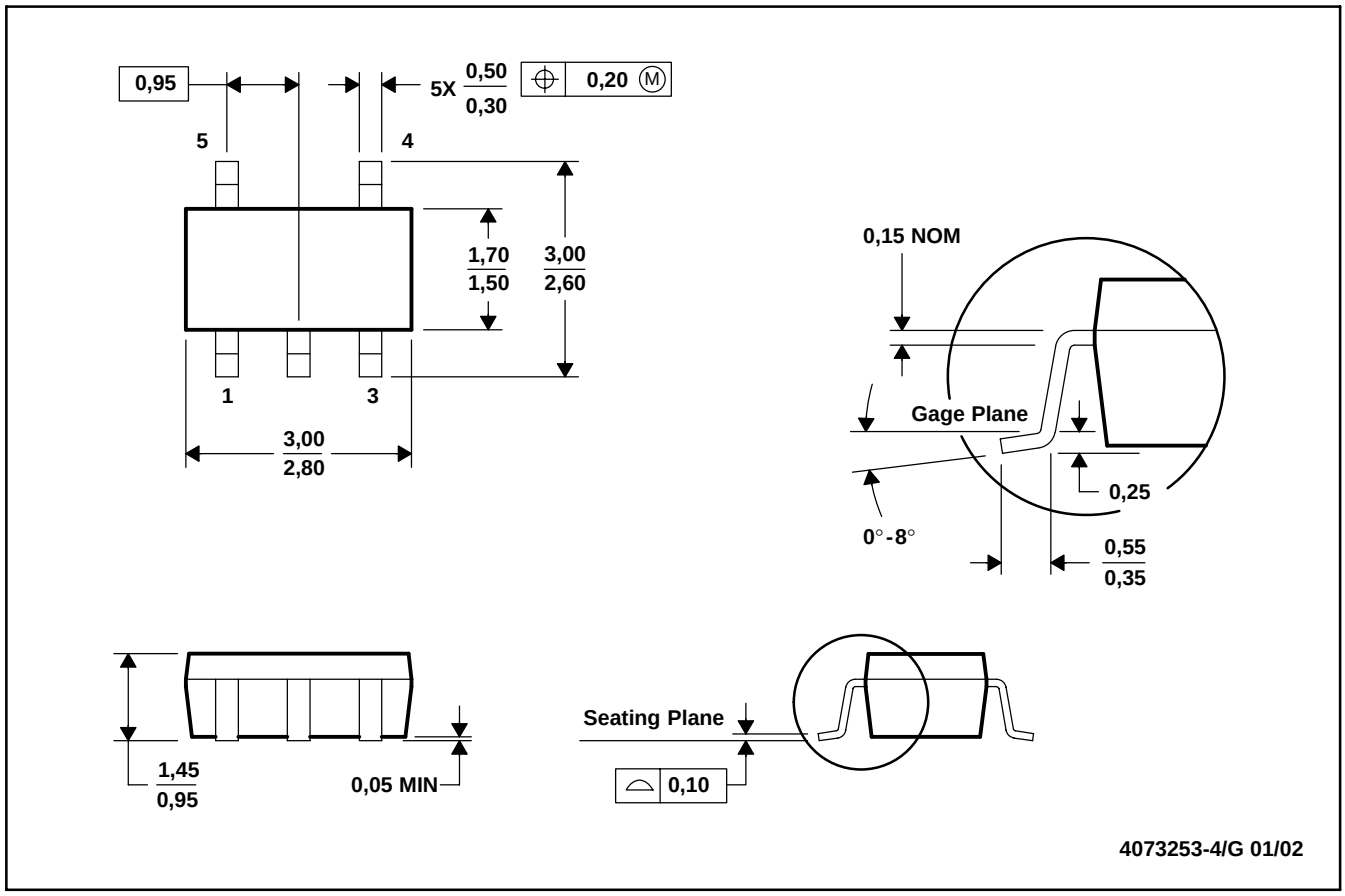
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoStar™ package configuration.
D. This package is tin-lead (SnPb), consult the factory for availability of lead-free material.

NanoStar is a trademark of Texas Instruments.

Figure 24. NanoStar™ Wafer Chip Scale Package

MPDS018E - FEBRUARY 1996 - REVISED FEBRUARY 2002

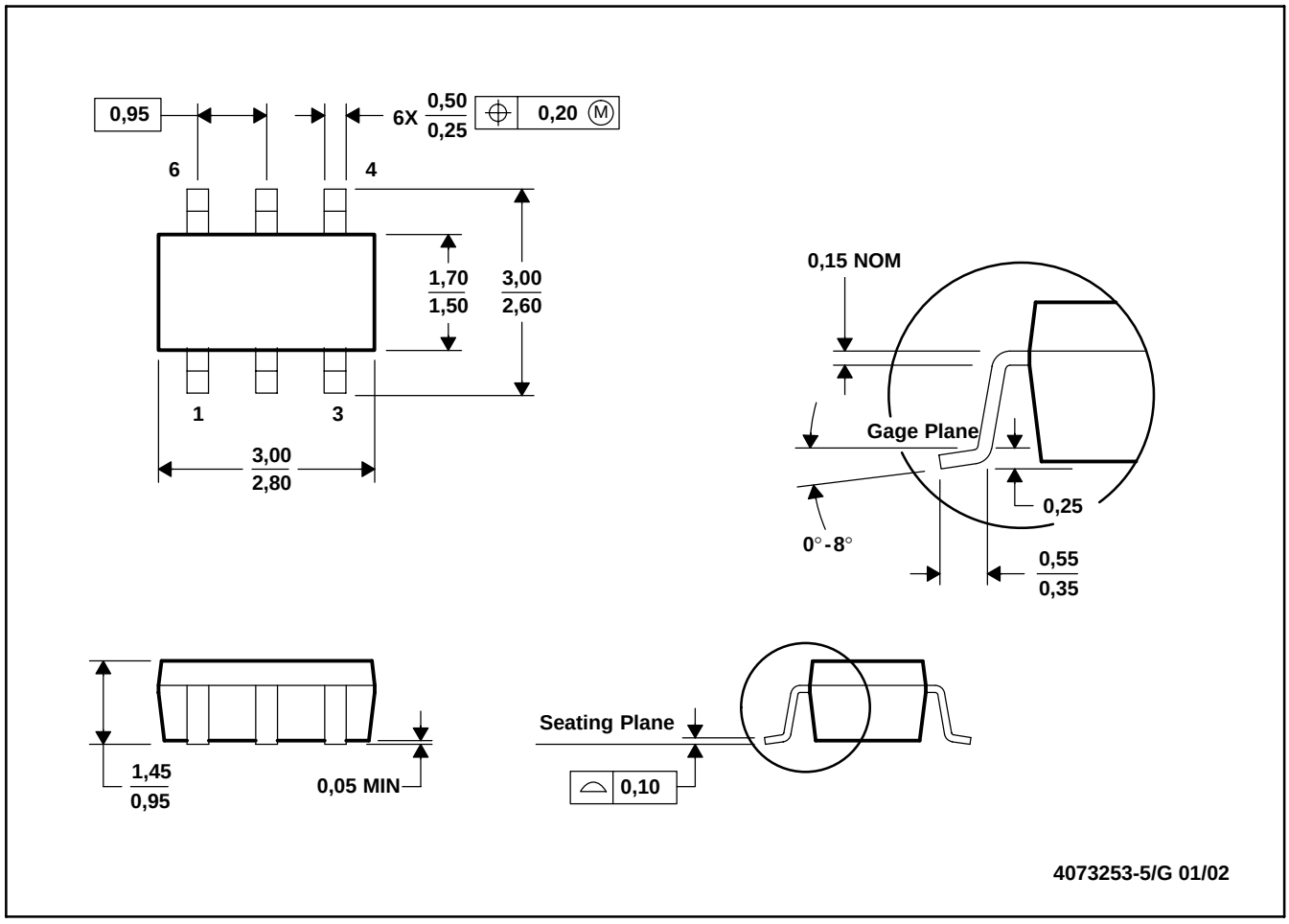
DBV (R-PDSO-G5) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-178

MPDS026D - FEBRUARY 1997 - REVISED FEBRUARY 2002

DBV (R-PDSO-G6) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Leads 1, 2, 3 may be wider than leads 4, 5, 6 for package orientation.

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