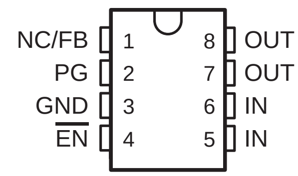
- **250-mA Low-Dropout Voltage Regulator**
- **Available in 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3.0-V, 3.3-V, 5.0-V Fixed Output and Adjustable Versions**
- **Dropout Voltage to 140 mV (Typ) at 250 mA (TPS76650)**
- **Ultra-Low 35-μA Typical Quiescent Current**
- **3% Tolerance Over Specified Conditions for Fixed-Output Versions**
- **Open Drain Power Good**
- **8-Pin SOIC Package**
- **Thermal Shutdown Protection**

D PACKAGE
(TOP VIEW)

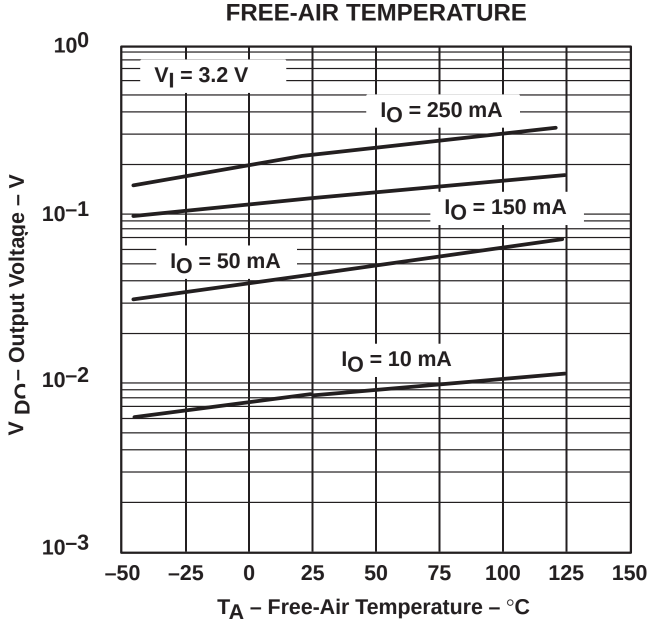


description

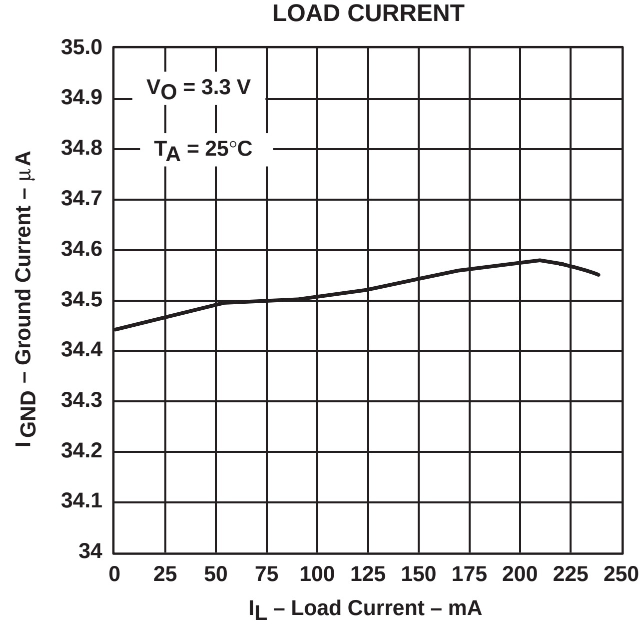
This device is designed to have an ultra-low quiescent current and be stable with a 4.7-μF capacitor. This combination provides high performance at a reasonable cost.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 230 mV at an output current of 250 mA for the TPS76650) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 35 μA over the full range of output current, 0 mA to 250 mA). These two key specifications yield a significant improvement in operating life for battery-powered systems. This LDO family also features a sleep mode; applying a TTL high signal to EN (enable) shuts down the regulator, reducing the quiescent current to less than 1 μA (typ).

TPS76633
DROPOUT VOLTAGE
vs
FREE-AIR TEMPERATURE



TPS76633
GROUND CURRENT
vs
LOAD CURRENT



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

description (continued)

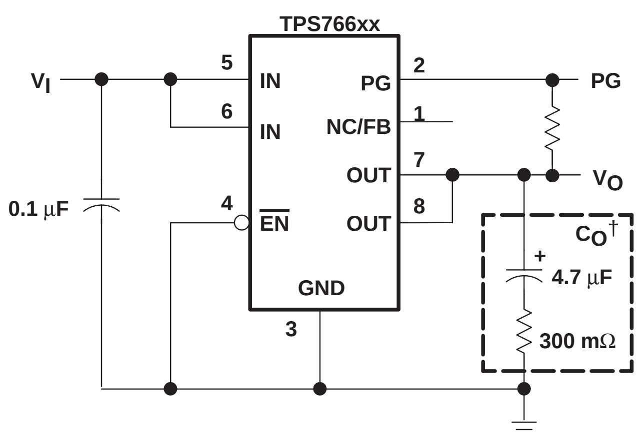
Power good (PG) is an active high output, which can be used to implement a power-on reset or a low-battery indicator.

The TPS766xx is offered in 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3.0-V, 3.3-V and 5.0-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.25 V to 5.5 V). Output voltage tolerance is specified as a maximum of 3% over line, load, and temperature ranges. The TPS766xx family is available in 8 pin SOIC package.

AVAILABLE OPTIONS

T_J	OUTPUT VOLTAGE (V)	PACKAGED DEVICES
	TYP	SOIC (D)
–40°C to 125°C	5.0	TPS76650D
	3.3	TPS76633D
	3.0	TPS76630D
	2.8	TPS76628D
	2.7	TPS76627D
	2.5	TPS76625D
	1.8	TPS76618D
	1.5	TPS76615D
	Adjustable 1.25 V to 5.5 V	TPS76601D

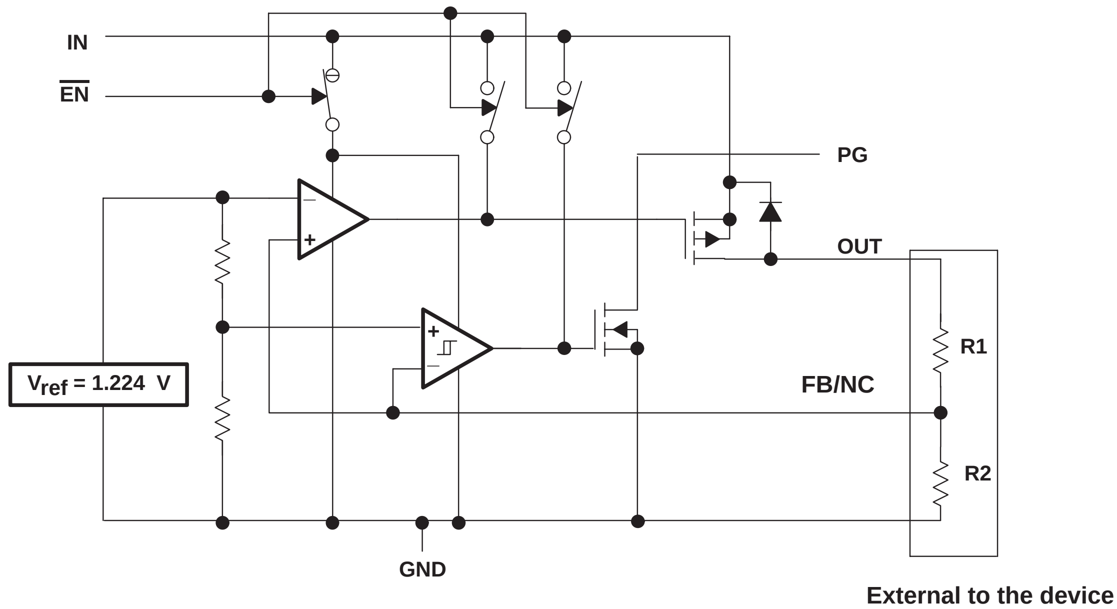
The TPS76601 is programmable using an external resistor divider (see application information). The D package is available taped and reeled. Add an R suffix to the device type (e.g., TPS76601DR).



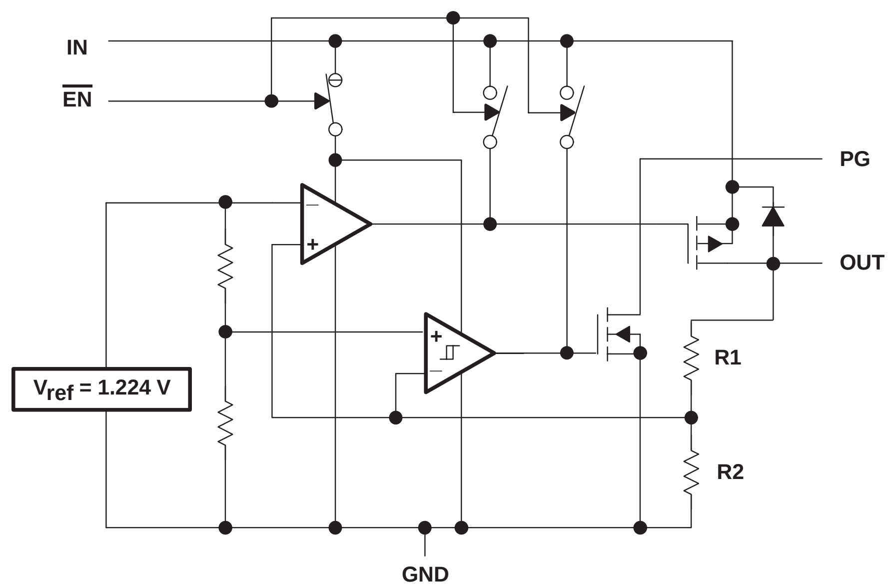
† See application information section for capacitor selection details.

Figure 1. Typical Application Configuration for Fixed Output Options

functional block diagram—adjustable version



functional block diagram—fixed-voltage version



Terminal Functions – SOIC Package

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{EN}$	4	I	Enable input
FB/NC	1	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	3		Regulator ground
IN	5	I	Input voltage
IN	6	I	Input voltage
OUT	7	O	Regulated output voltage
OUT	8	O	Regulated output voltage
PG	2	O	PG output

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range‡, V_I . . . . –0.3 V to 13.5 V
Voltage range at $\overline{EN}$ . . . . –0.3 V to 16.5 V
Maximum PG voltage . . . . 16.5 V
Peak output current . . . . Internally limited
Continuous total power dissipation . . . . See dissipation rating tables
Output voltage, V_O (OUT, FB) . . . . 7 V
Operating virtual junction temperature range, T_J . . . . –40°C to 125°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
ESD rating, HBM . . . . 2 kV

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURES

PACKAGE	AIR FLOW (CFM)	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
D	0	568 mW	5.68 mW/°C	312 mW	227 mW
	250	904 mW	9.04 mW/°C	497 mW	361 mW

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I☆	2.7	10	V
Output voltage range, V_O	1.2	5.5	V
Output current, I_O (Note 1)	0	250	mA
Operating virtual junction temperature, T_J (Note 1)	–40	125	°C

☆ To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$.
NOTE 1: Continuous current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

electrical characteristics over recommended operating free-air temperature range, $V_i = V_{O(typ)} + 1$ V, $I_O = 10$ µA, $\overline{EN} = 0$ V, $C_O = 4.7$ µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output voltage (10 µA to 250 mA load) (see Note 2)	TPS76601	5.5 V ≥ V_O ≥ 1.25 V,	T_J = 25°C		V_O		V
	TPS76601	5.5 V ≥ V_O ≥ 1.25 V,	T_J = –40°C to 125°C	0.97V_O		1.03V_O	
	TPS76615	T_J = 25°C,	2.7 V < V_{IN} < 10 V		1.5		
	TPS76615	T_J = –40°C to 125°C,	2.7 V < V_{IN} < 10 V	1.455		1.545	
	TPS76618	T_J = 25°C,	2.8 V < V_{IN} < 10 V		1.8		
	TPS76618	T_J = –40°C to 125°C,	2.8 V < V_{IN} < 10 V	1.746		1.854	
	TPS76625	T_J = 25°C,	3.5 V < V_{IN} < 10 V		2.5		
	TPS76625	T_J = –40°C to 125°C,	3.5 V < V_{IN} < 10 V	2.425		2.575	
	TPS76627	T_J = 25°C,	3.7 V < V_{IN} < 10 V		2.7		
	TPS76627	T_J = –40°C to 125°C,	3.7 V < V_{IN} < 10 V	2.619		2.781	
	TPS76628	T_J = 25°C,	3.8 V < V_{IN} < 10 V		2.8		
	TPS76628	T_J = –40°C to 125°C,	3.8 V < V_{IN} < 10 V	2.716		2.884	
	TPS76630	T_J = 25°C,	4.0 V < V_{IN} < 10 V		3.0		
	TPS76630	T_J = –40°C to 125°C,	4.0 V < V_{IN} < 10 V	2.910		3.090	
	TPS76633	T_J = 25°C,	4.3 V < V_{IN} < 10 V		3.3		
	TPS76633	T_J = –40°C to 125°C,	4.3 V < V_{IN} < 10 V	3.201		3.399	
	TPS76650	T_J = 25°C,	6.0 V < V_{IN} < 10 V		5.0		
	TPS76650	T_J = –40°C to 125°C,	6.0 V < V_{IN} < 10 V	4.850		5.150	
Quiescent current (GND current) $\overline{EN}$ = 0V, (see Note 2)		10 µA < I_O < 250 mA,	T_J = 25°C		35		µA
		I_O = 250 mA,	T_J = –40°C to 125°C			50	
Output voltage line regulation ($\Delta V_O/V_O$) (see Notes 2 and 3)		V_O + 1 V < V_I ≤ 10 V,	T_J = 25°C		0.01		%/V
Load regulation		I_O = 10 µA to 250 mA			0.5%		
Output noise voltage		BW = 300 Hz to 50 kHz, C_O = 4.7 µF,	T_J = 25°C		200		µVrms
Output current Limit		V_O = 0 V			0.8	1.2	A
Thermal shutdown junction temperature					150		°C
Standby current		$\overline{EN}$ = V_I,	T_J = 25°C, 2.7 V < V_I < 10 V		1		µA
		$\overline{EN}$ = V_I,	T_J = –40°C to 125°C 2.7 V < V_I < 10 V			10	µA
FB input current	TPS76601	FB = 1.5 V			2		nA
High level enable input voltage				2.0			V
Low level enable input voltage						0.8	V
Power supply ripple rejection (see Note 2)		f = 1 kHz, I_O = 10 µA,	C_O = 4.7 µF, T_J = 25°C		63		dB
PG	Minimum input voltage for valid PG	$I_{O(PG)}$ = 300µA			1.1		V
PG	Trip threshold voltage	V_O decreasing		92		98	%V_O
PG	Hysteresis voltage	Measured at V_O			0.5		%V_O
PG	Output low voltage	V_I = 2.7 V,	$I_{O(PG)}$ = 1mA		0.15	0.4	V
PG	Leakage current	$V_{(PG)}$ = 5 V				1	µA
Input current (EN)		$\overline{EN}$ = 0 V		–1	0	1	µA
		$\overline{EN}$ = V_I		–1		1	

NOTE: 2. Minimum IN operating voltage is 2.7 V or $V_{O(typ)}$ + 1 V, whichever is greater. Maximum IN voltage 10 V.

electrical characteristics over recommended operating free-air temperature range, $V_i = V_{O(typ)} + 1$ V, $I_O = 10$ µA, $\overline{EN} = 0$ V, $C_O = 4.7$ µF (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Dropout voltage (See Note 4)	TPS76628	$I_O = 250$ mA,	$T_J = 25°C$		310		mV
		$I_O = 250$ mA,	$T_J = –40°C$ to 125°C			540	
	TPS76630	$I_O = 250$ mA,	$T_J = 25°C$		270		
		$I_O = 250$ mA,	$T_J = –40°C$ to 125°C			470	
	TPS76633	$I_O = 250$ mA,	$T_J = 25°C$		230		
		$I_O = 250$ mA,	$T_J = –40°C$ to 125°C			400	
	TPS76650	$I_O = 250$ mA,	$T_J = 25°C$		140		
		$I_O = 250$ mA,	$T_J = –40°C$ to 125°C			250	

NOTES: 3. If $V_O \le 1.8$ V then $V_{imin} = 2.7$ V, $V_{imax} = 10$ V:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O\left(V_{imax} - 2.7\ V\right)}{100} \times 1000$$

If $V_O \ge 2.5$ V then $V_{imin} = V_O + 1$ V, $V_{imax} = 10$ V:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O\left(V_{imax} - \left(V_O + 1\ V\right)\right)}{100} \times 1000$$

4. IN voltage equals V_O(Typ) – 100 mV; TPS76601 output voltage set to 3.3 V nominal with external resistor divider. TPS76615, TPS76618, TPS76625, and TPS76627 dropout voltage limited by input voltage range limitations (i.e., TPS76630 input voltage needs to drop to 2.9 V for purpose of this test).

Table of Graphs

		FIGURE
Output voltage	vs Load current	2, 3
	vs Free-air temperature	4, 5
Ground current	vs Load current	6, 7
	vs Free-air temperature	8, 9
Power supply ripple rejection	vs Frequency	10
Output spectral noise density	vs Frequency	11
Output impedance	vs Frequency	12
Dropout voltage	vs Free-air temperature	13, 14
Line transient response		15, 17
Load transient response		16, 18
Output voltage	vs Time	19
Dropout voltage	vs Input voltage	20
Equivalent series resistance (ESR)	vs Output current	21 – 24
Equivalent series resistance (ESR)	vs Added ceramic capacitance	25, 26

TYPICAL CHARACTERISTICS

TPS76633
OUTPUT VOLTAGE
vs
LOAD CURRENT

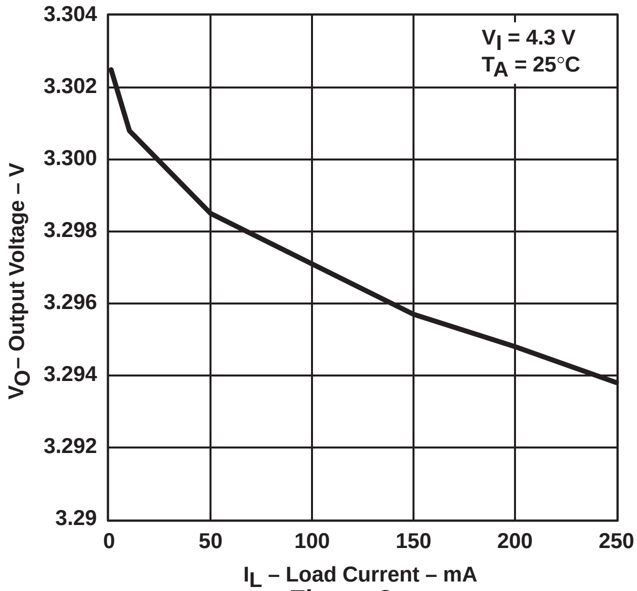


Figure 2

TPS76615
OUTPUT VOLTAGE
vs
LOAD CURRENT

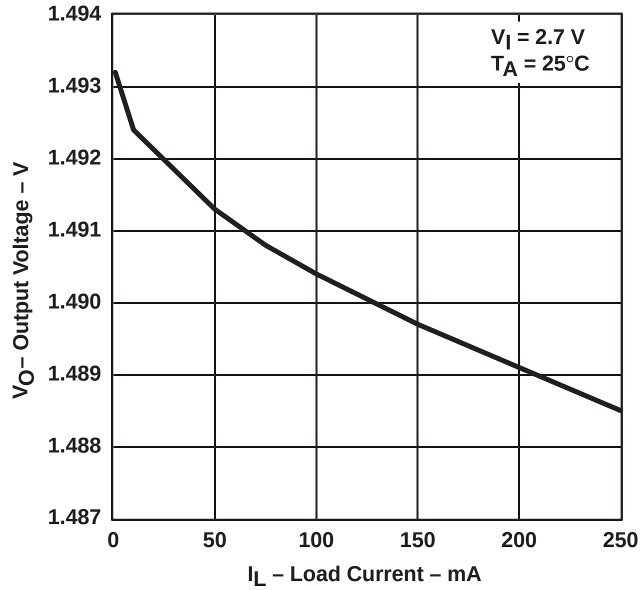


Figure 3

TPS76633
OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

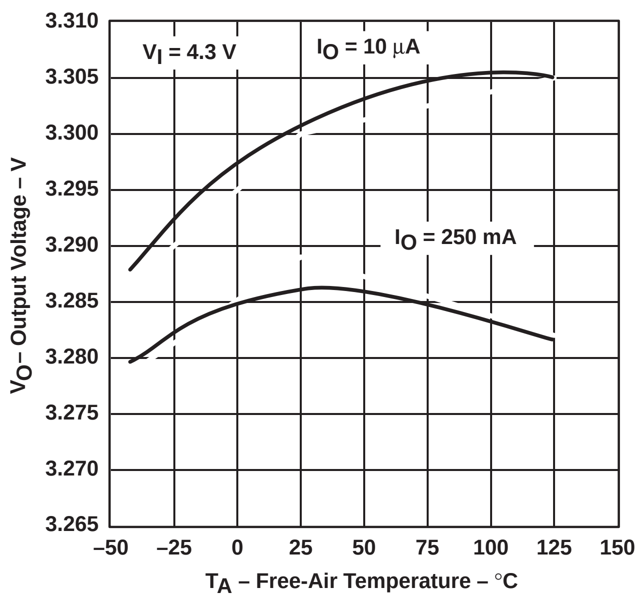


Figure 4

TPS76615
OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

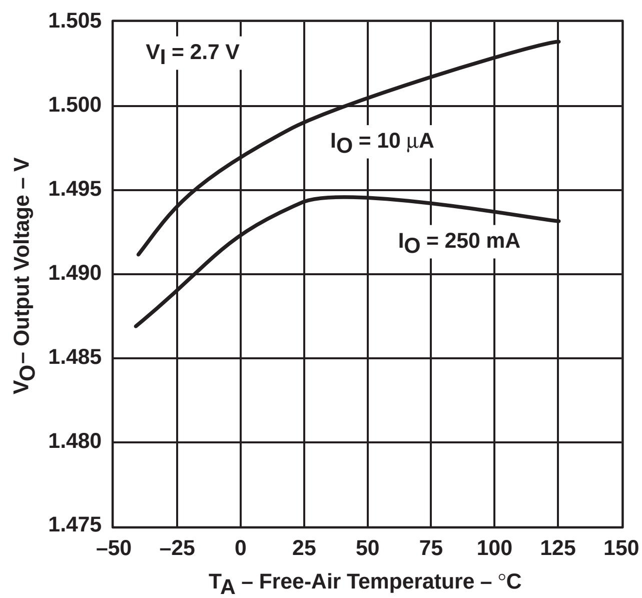


Figure 5

TYPICAL CHARACTERISTICS

TPS76633
GROUND CURRENT
vs
LOAD CURRENT

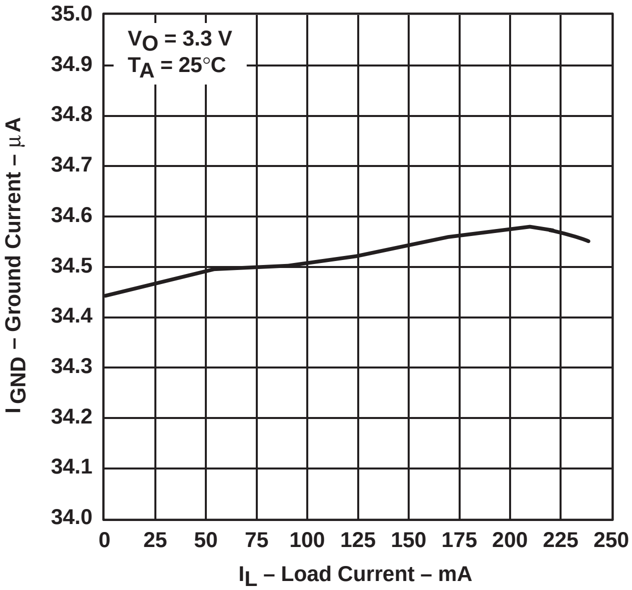


Figure 6

TPS76615
GROUND CURRENT
vs
LOAD CURRENT

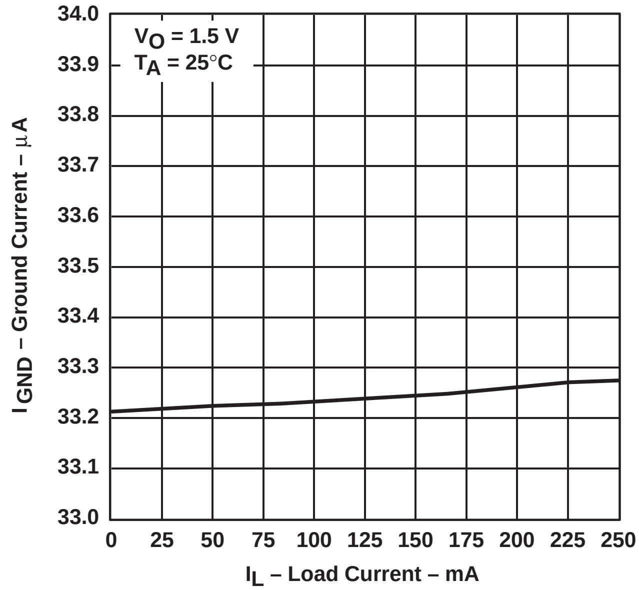


Figure 7

TPS76633
GROUND CURRENT
vs
FREE-AIR TEMPERATURE

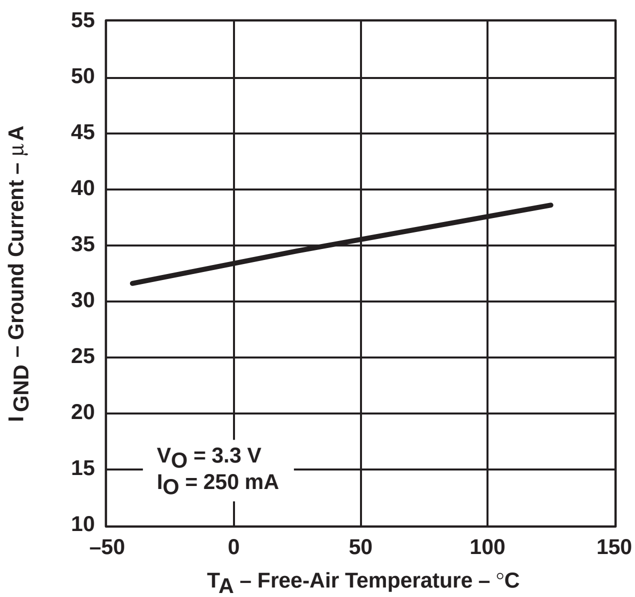


Figure 8

TPS76615
GROUND CURRENT
vs
FREE-AIR TEMPERATURE

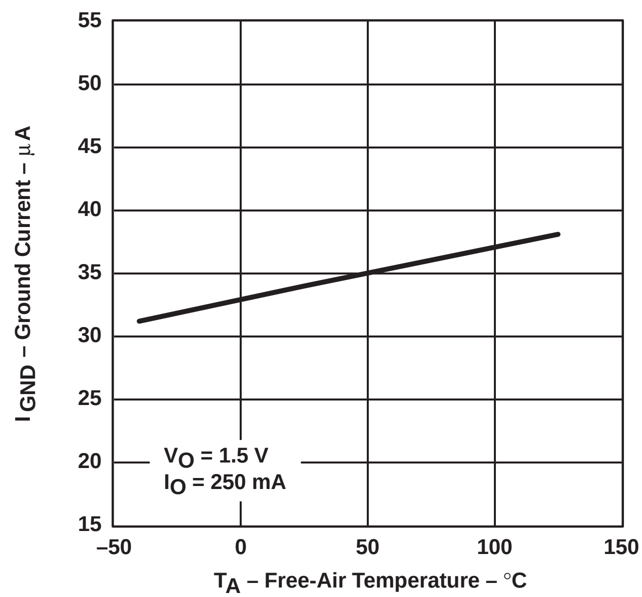


Figure 9

TYPICAL CHARACTERISTICS

TPS76633
POWER SUPPLY RIPPLE REJECTION
vs
FREQUENCY

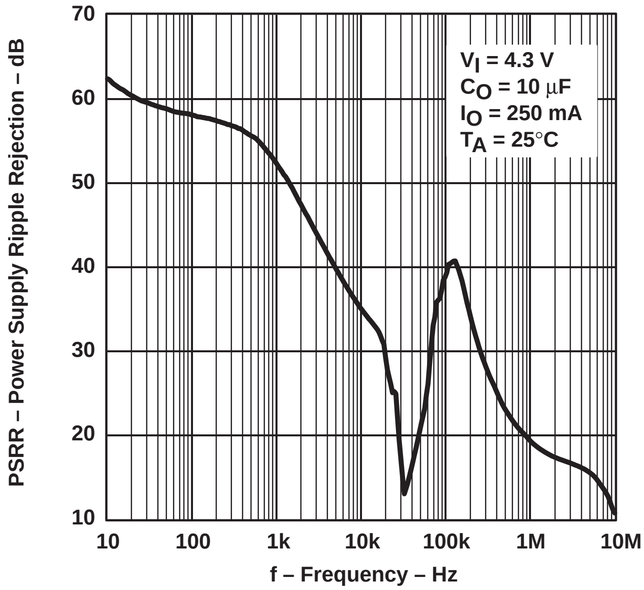


Figure 10

TPS76633
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

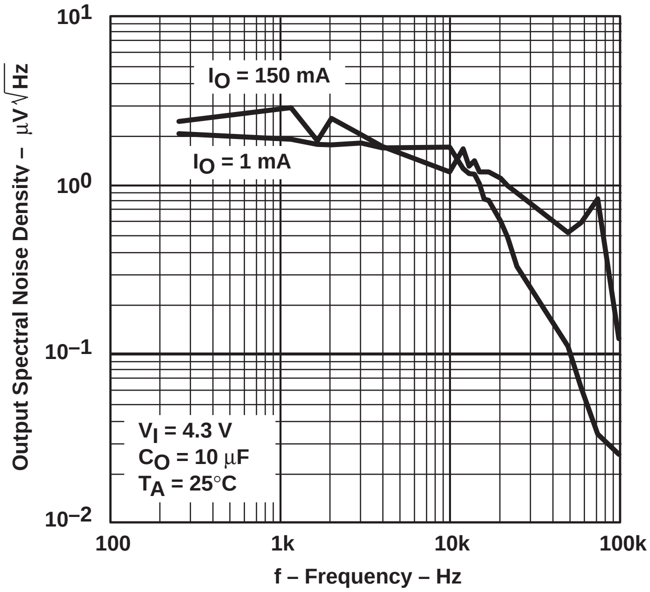


Figure 11

TPS76633
OUTPUT IMPEDANCE
vs
FREQUENCY

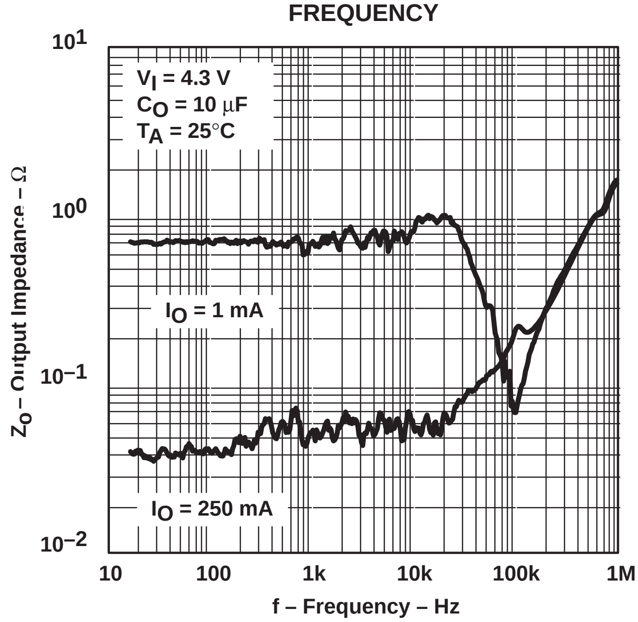


Figure 12

TYPICAL CHARACTERISTICS

TPS76650
DROPOUT VOLTAGE
vs
FREE-AIR TEMPERATURE

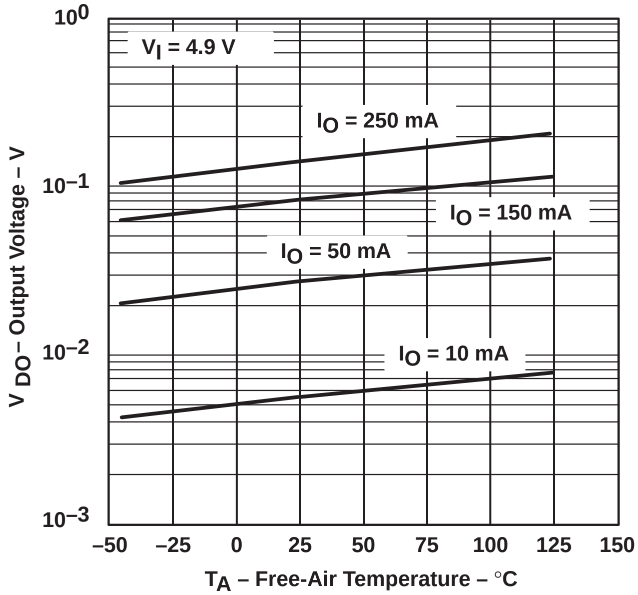


Figure 13

TPS76633
DROPOUT VOLTAGE
vs
FREE-AIR TEMPERATURE

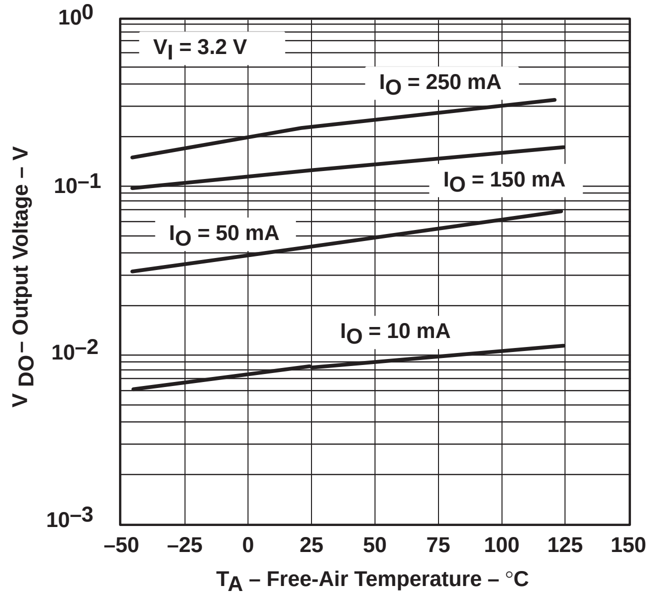


Figure 14

TPS76615
LINE TRANSIENT RESPONSE

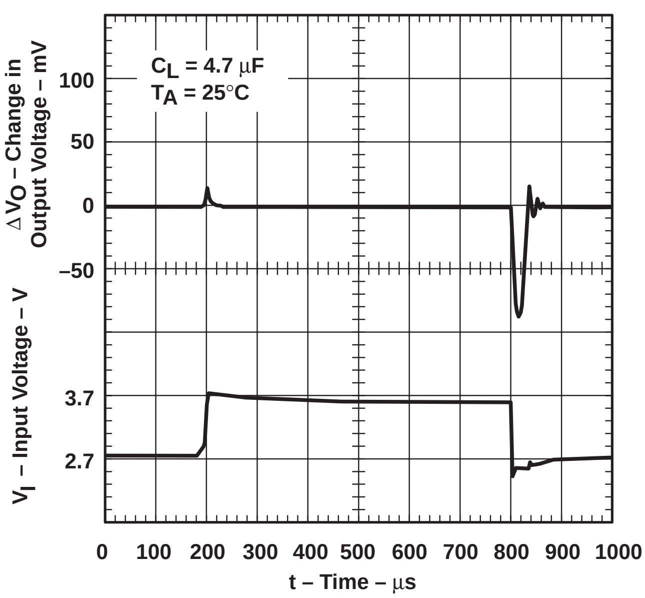


Figure 15

TPS76615
LOAD TRANSIENT RESPONSE

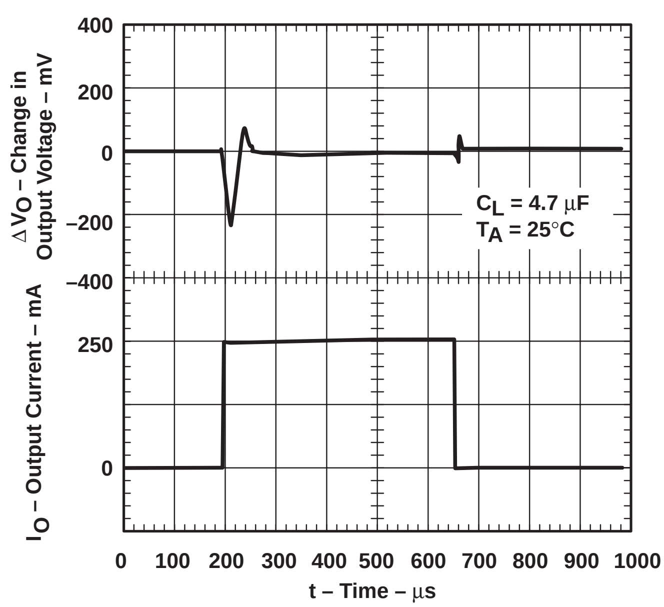


Figure 16

TYPICAL CHARACTERISTICS

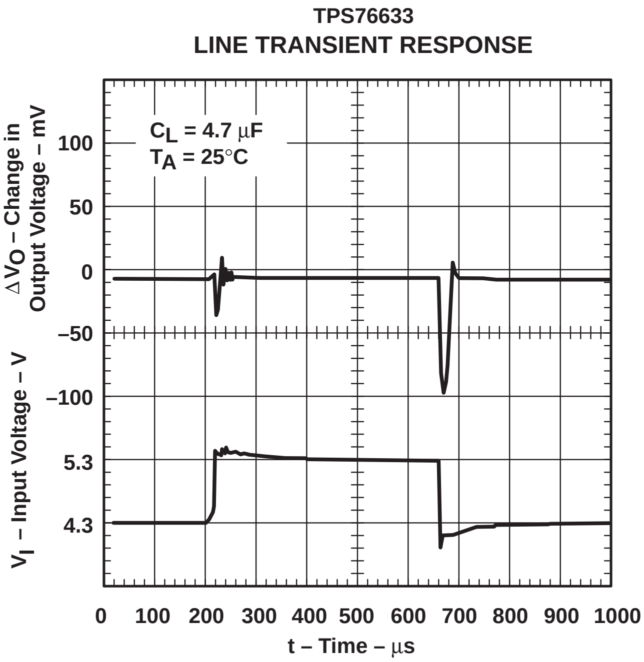


Figure 17

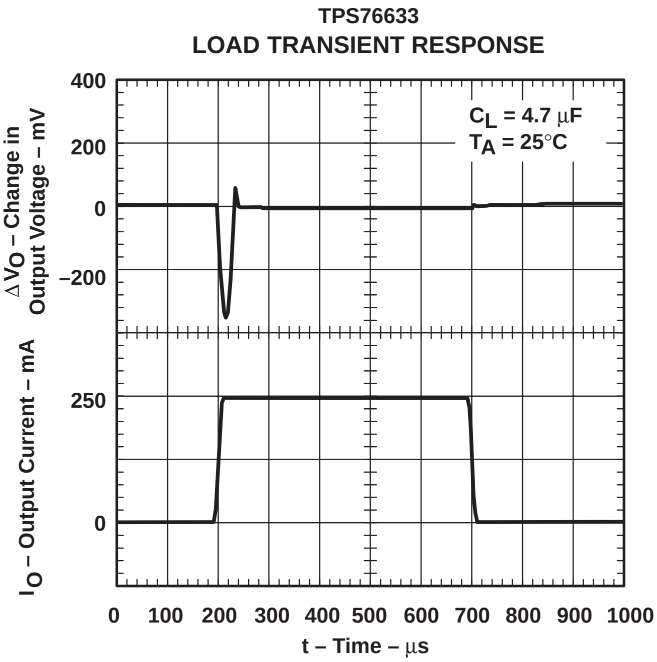


Figure 18

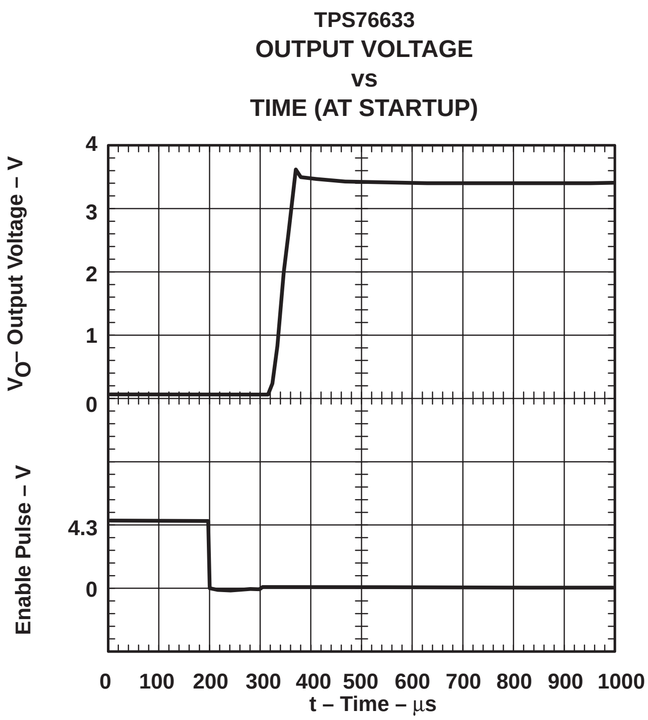


Figure 19

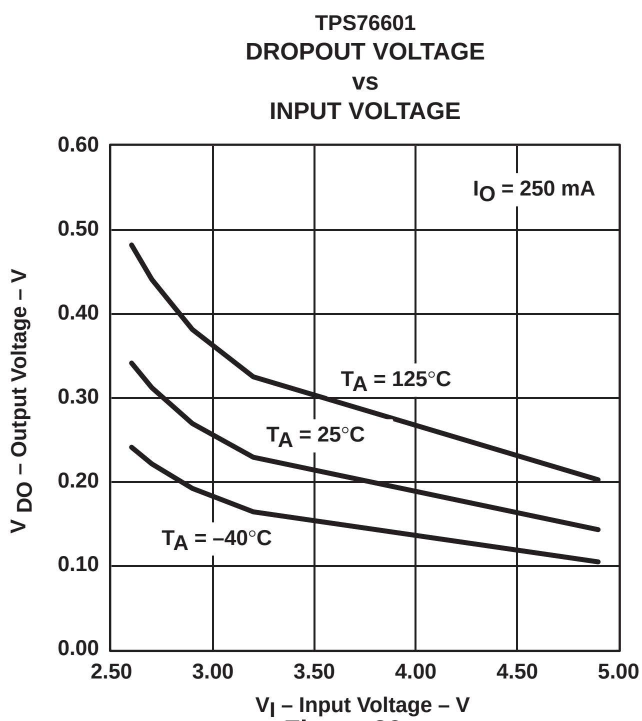


Figure 20

TYPICAL CHARACTERISTICS

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†
vs
OUTPUT CURRENT

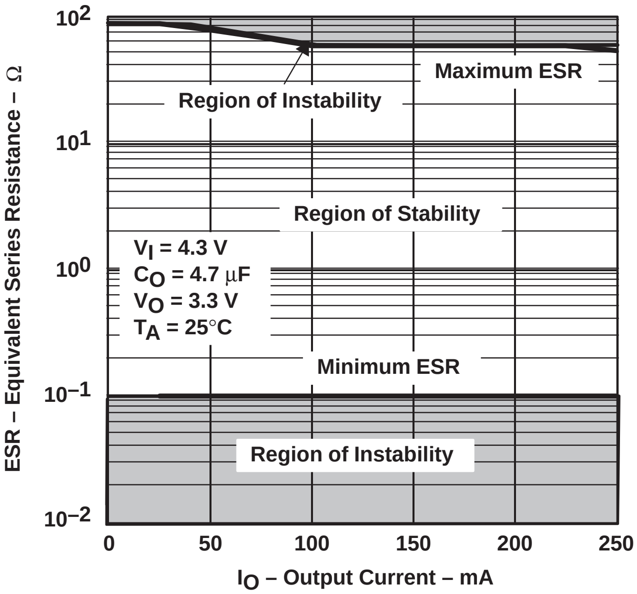


Figure 21

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†
vs
OUTPUT CURRENT

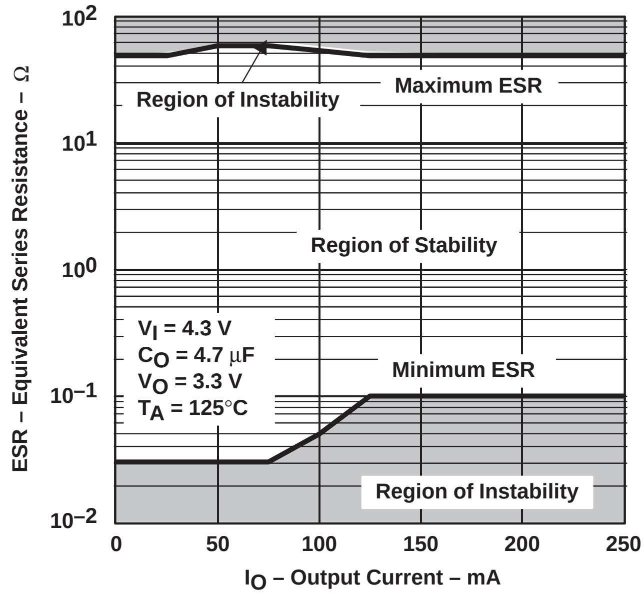


Figure 22

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†
vs
OUTPUT CURRENT

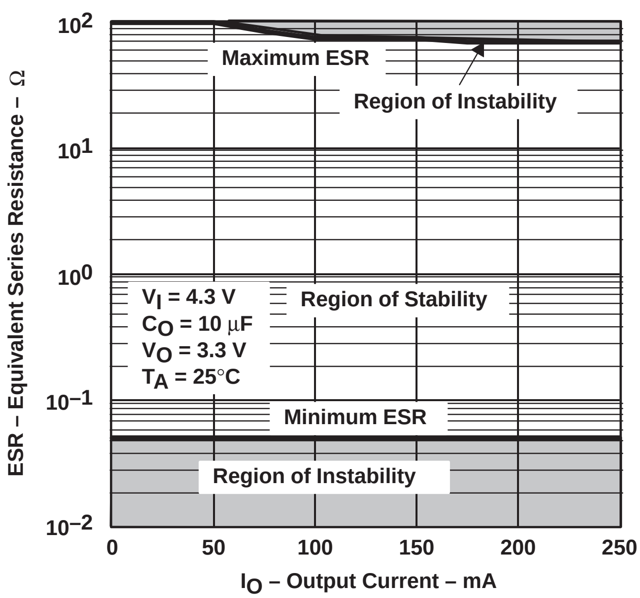


Figure 23

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE†
vs
OUTPUT CURRENT

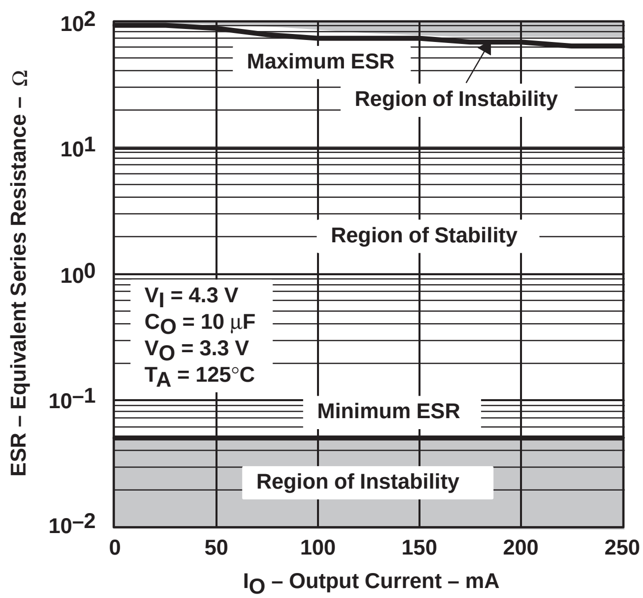


Figure 24

† Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

TYPICAL CHARACTERISTICS

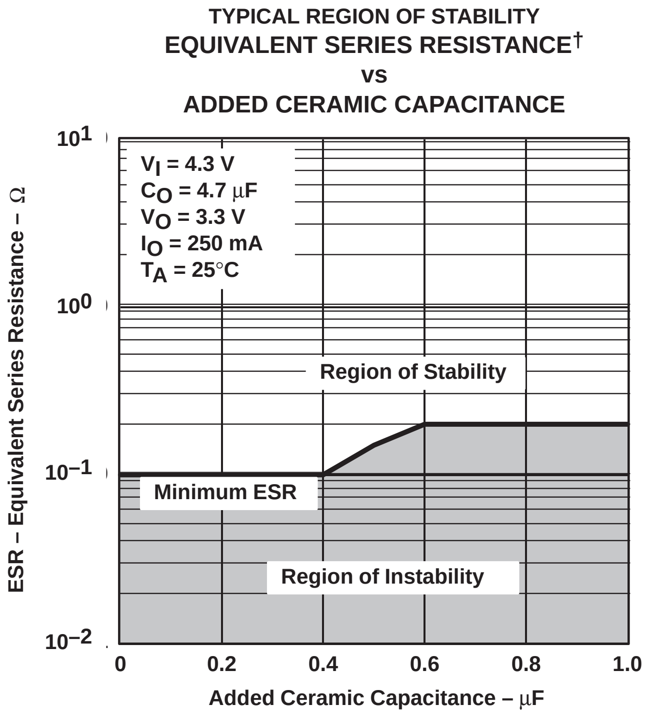


Figure 25

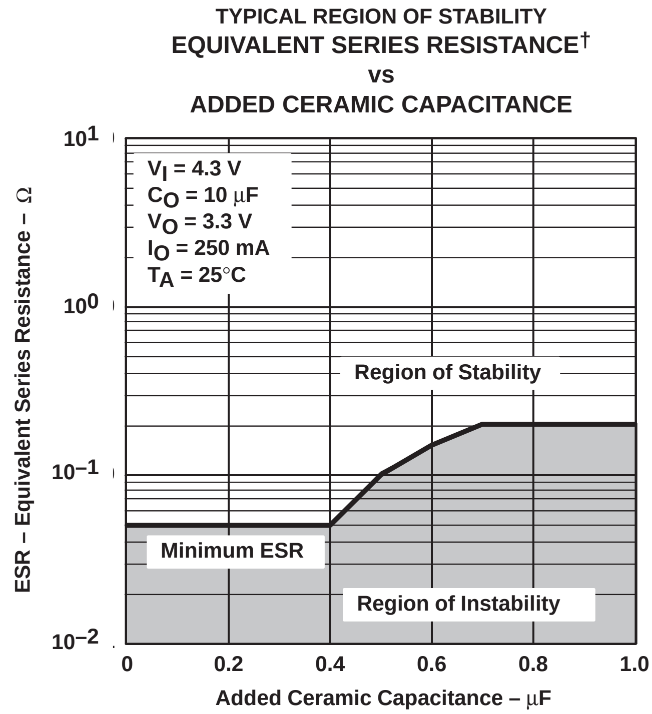


Figure 26

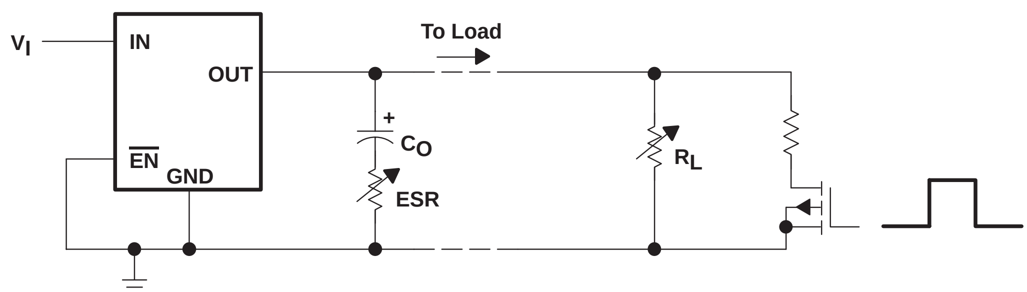


Figure 27. Test Circuit for Typical Regions of Stability (Figures 21 through 24) (Fixed Output Options)

† Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

APPLICATION INFORMATION

The TPS766xx family includes eight fixed-output voltage regulators (1.5 V, 1.8 V, 2.5 V, 2.7 V, 2.8 V, 3.0 V, 3.3 V, and 5.0 V), and an adjustable regulator, the TPS76601 (adjustable from 1.25 V to 5.5 V).

device operation

The TPS766xx features very low quiescent current, which remains virtually constant even with varying loads. Conventional LDO regulators use a pnp pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). The TPS766xx uses a PMOS transistor to pass current; because the gate of the PMOS is voltage driven, operating current is low and invariable over the full load range.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS766xx quiescent current remains low even when the regulator drops out, eliminating both problems.

The TPS766xx family also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to 1 µA (typ). If the shutdown feature is not used, $\overline{EN}$ should be tied to ground. Response to an enable transition is quick; regulated output voltage is reestablished in typically 160 µs.

minimum load requirements

The TPS766xx family is stable even at zero load; no minimum load is required for operation.

FB - pin connection (adjustable version only)

The FB pin is an input pin to sense the output voltage and close the loop for the adjustable option . The output voltage is sensed through a resistor divider network to close the loop as it is shown in Figure 29. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit to improve performance at that point. Internally, FB connects to a high-impedance wide-bandwidth amplifier and noise pickup feeds through to the regulator output. Routing the FB connection to minimize/avoid noise pickup is essential.

external capacitor requirements

An input capacitor is not usually required; however, a ceramic bypass capacitor (0.047 µF or larger) improves load transient response and noise rejection if the TPS766xx is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Like all low dropout regulators, the TPS766xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 4.7 µF and the ESR (equivalent series resistance) must be between 300-mΩ and 20-Ω. Capacitor values 4.7 µF or larger are acceptable, provided the ESR is less than 20 Ω. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described previously.

APPLICATION INFORMATION

external capacitor requirements (continued)

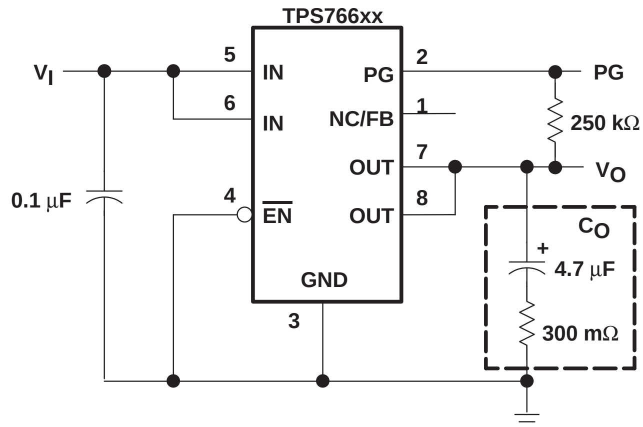


Figure 28. Typical Application Circuit (Fixed Versions)

programming the TPS76601 adjustable LDO regulator

The output voltage of the TPS76601 adjustable regulator is programmed using an external resistor divider as shown in Figure 29. The output voltage is calculated using:

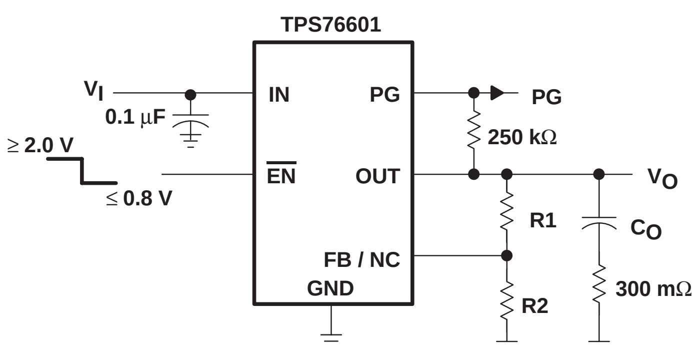
$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \tag{1}$$

Where

V_{ref} = 1.224 V typ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 7-µA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 169 kΩ to set the divider current at 7 µA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \tag{2}$$



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	UNIT
2.5 V	174	169	kΩ
3.3 V	287	169	kΩ
3.6 V	324	169	kΩ
4.0 V	383	169	kΩ
5.0 V	523	169	kΩ

Figure 29. TPS76601 Adjustable LDO Regulator Programming

APPLICATION INFORMATION

power-good indicator

The TPS766xx features a power-good (PG) output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the PG output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. PG can be used to drive power-on reset circuitry or used as a low-battery indicator.

regulator protection

The TPS766xx PMOS-pass transistor has a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS766xx also features internal current limiting and thermal protection. During normal operation, the TPS766xx limits output current to approximately 0.8 µA (typ). When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C(typ), regulator operation resumes.

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}}$$

Where

$T_J max$ is the maximum allowable junction temperature

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 176°C/W for the 8-terminal SOIC.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

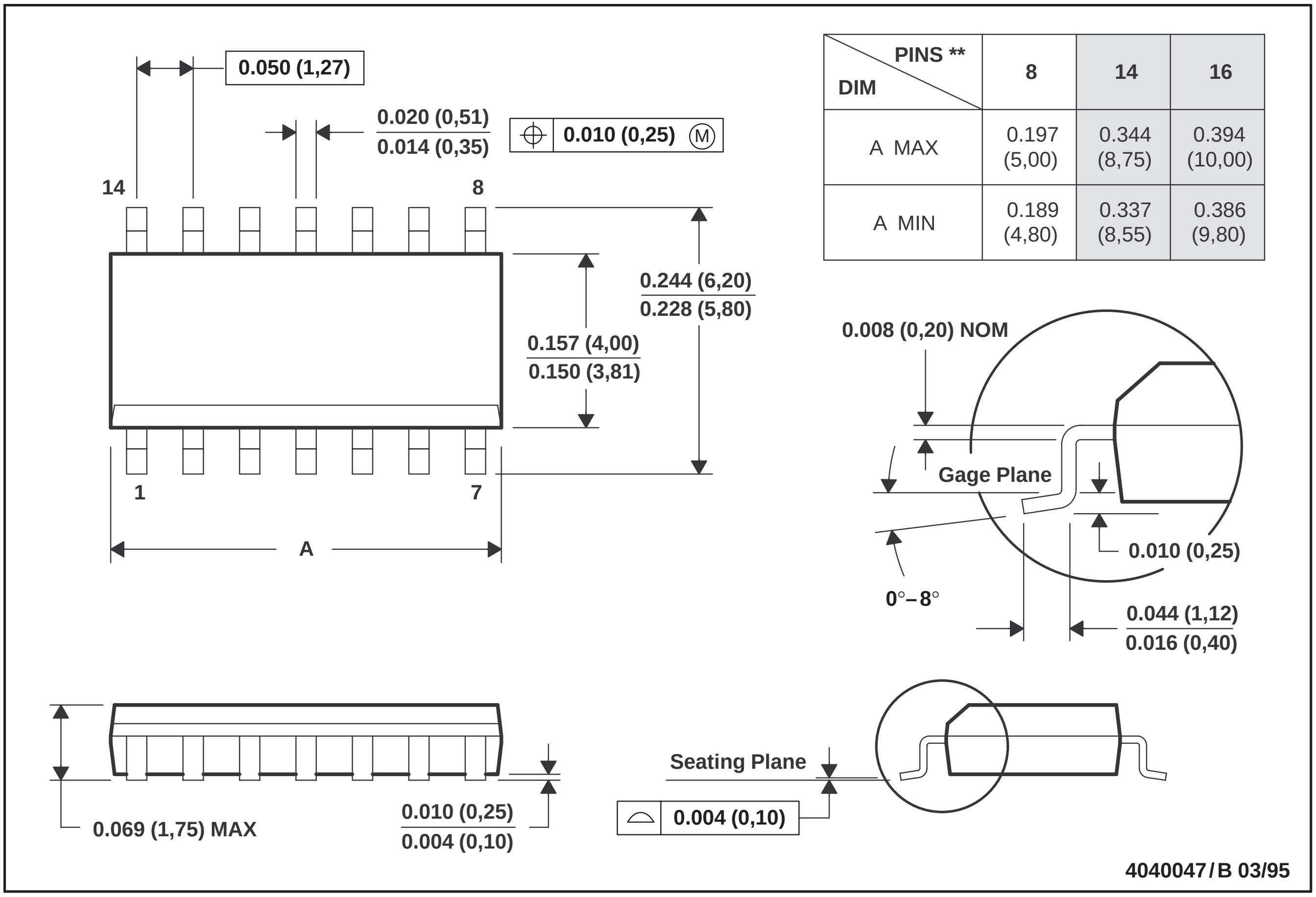
$$P_D = \left(V_I - V_O\right) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Four center pins are connected to die mount pad.
E. Falls within JEDEC MS-012

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TPS76601D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76601DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76601DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76601DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76615D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76615DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76615DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76615DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76618D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76618DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76618DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76618DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76625D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76625DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76625DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76625DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76627D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76627DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76627DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76627DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76628D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76628DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76628DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76628DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76630D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TPS76630DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76630DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76630DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76633D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76633DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76633DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76633DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76650D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76650DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76650DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76650DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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