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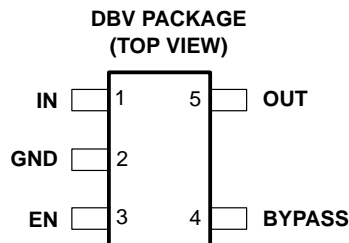
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Jameco Part Number 829329

# TPS76425, TPS76427, TPS76428, TPS76430, TPS76433 LOW-POWER LOW-NOISE 150-mA LOW-DROPOUT LINEAR REGULATORS

SLVS180B – MARCH 1999 – REVISED MAY 2001

- 150-mA Low Noise, Low-Dropout Regulator
- Output Voltage: 2.5 V, 2.7 V, 2.8 V, 3.0 V, 3.3 V
- Output Noise Typically 50  $\mu$ V
- Quiescent Current Typically 85  $\mu$ A
- Dropout Voltage, Typically 300 mV at 150 mA
- Thermal Protection
- Over Current Limitation
- Less Than 2- $\mu$ A Quiescent Current in Shutdown Mode
- -40°C to 125°C Operating Junction Temperature Range
- 5-Pin SOT-23 (DBV) Package



## description

The TPS764xx family of low-dropout (LDO) voltage regulators offers the benefits of a low noise, low-dropout voltage, low-power operation, and miniaturized package. Additionally, they feature low quiescent current when compared to conventional LDO regulators. Offered in 5-terminal small outline integrated-circuit SOT-23 package, the TPS764xx series devices are ideal for low-noise applications, cost-sensitive designs and applications where board space is at a premium.

A combination of new circuit design and process innovation has enabled the usual pnp pass transistor to be replaced by a PMOS pass element. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage is very low—typically 300 mV at 150 mA of load current (TPS76433)—and is directly proportional to the load current. Since the PMOS pass element is a voltage-driven device, the quiescent current is very low (140  $\mu$ A maximum) and is stable over the entire range of output load current (0 mA to 150 mA). Intended for use in portable systems such as laptops and cellular phones, the low-dropout voltage feature and low-power operation result in a significant increase in system battery operating life.

The TPS764xx also features a logic-enabled sleep mode to shut down the regulator, reducing quiescent current to 1  $\mu$ A maximum at  $T_J = 25^\circ\text{C}$ . The TPS764xx is offered in 2.5-V, 2.7-V, 2.8-V, 3.0-V, and 3.3-V fixed-voltages.

## AVAILABLE OPTIONS

$T_J$	VOLTAGE	PACKAGE	PART NUMBER		SYMBOL
-40°C to 125°C	2.5 V	SOT-23 (DBV)	TPS76425DBVT†	TPS76425DBVR‡	PBJI
	2.7 V		TPS76427DBVT†	TPS76427DBVR‡	PBKI
	2.8 V		TPS76428DBVT†	TPS76428DBVR‡	PCEI
	3.0 V		TPS76430DBVT†	TPS76430DBVR‡	PBLI
	3.3 V		TPS76433DBVT†	TPS76433DBVR‡	PBMI

† The DBVT passive indicates tape and reel of 250 parts.

‡ The DBVR passive indicates tape and reel of 3000 parts.



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 **TEXAS  
INSTRUMENTS**

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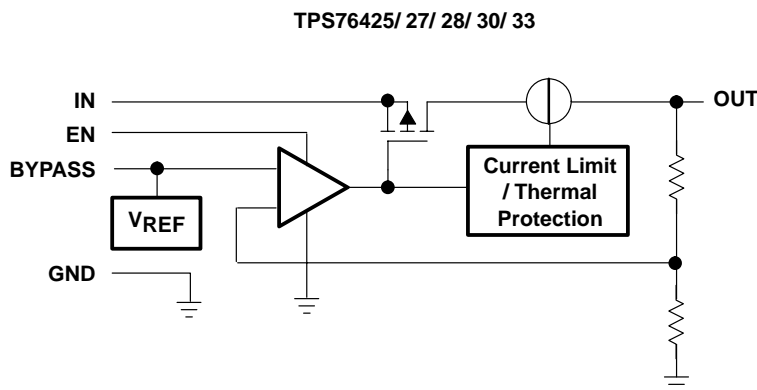
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# TPS76425, TPS76427, TPS76428, TPS76430, TPS76433

## LOW-POWER LOW-NOISE 150-mA LOW-DROPOUT LINEAR REGULATORS

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### functional block diagram



### Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
GND		Ground
EN	I	Enable input
BYPASS		Output bypass capacitor
IN	I	Input supply voltage
OUT	O	Regulated output voltage

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Input voltage range (see Note 1)	–0.3 V to 10 V
Voltage range at EN	–0.3 V to $V_I + 0.3$ V
Voltage on OUT,	7 V
Peak output current	Internally limited
ESD rating, HBM	2 kV
Continuous total power dissipation	See dissipation rating tables
Operating virtual junction temperature range, $T_J$	–40°C to 150°C
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A \leq 25^\circ\text{C}$ POWER RATING	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
Low K <sup>‡</sup>	DBV	65.8 °C/W	259 °C/W	3.9 mW/°C	386 mW	212 mW	154 mW
High K <sup>§</sup>	DBV	65.8 °C/W	180 °C/W	5.6 mW/°C	555 mW	305 mW	222 mW

<sup>‡</sup> The JEDEC Low K (1s) board design used to derive this data was a 3 inch x 3 inch, two layer board with 2 ounce copper traces on top of the board.

<sup>§</sup> The JEDEC High K (2s2p) board design used to derive this data was a 3 inch x 3 inch, multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.



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## recommended operating conditions

	MIN	NOM	MAX	UNIT
Input voltage, $V_I$ †	2.7		10	V
Continuous output current, $I_O$	0		150	mA
Operating junction temperature, $T_J$	-40		125	°C

† To calculate the minimum input voltage for your maximum output current, use the following equation:  $V_{I(\min)} = V_{O(\max)} + V_{DO(\max \text{ load})}$

## electrical characteristics over recommended operating free-air temperature range, $V_I = V_{O(\text{typ})} + 1 \text{ V}$ , $I_O = 1 \text{ mA}$ , $EN = IN$ , $C_O = 4.7 \mu\text{F}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$V_O$	Output voltage	TPS76425	$I_O = 1 \text{ mA to } 100 \text{ mA}$ , $T_J = 25^\circ\text{C}$	2.45	2.5	2.55	V
			$I_O = 1 \text{ mA to } 100 \text{ mA}$	2.425	2.5	2.575	
			$I_O = 1 \text{ mA to } 150 \text{ mA}$ , $T_J = 25^\circ\text{C}$	2.438	2.5	2.562	
			$I_O = 1 \text{ mA to } 150 \text{ mA}$	2.407	2.5	2.593	
		TPS76427	$I_O = 1 \text{ mA to } 100 \text{ mA}$ , $T_J = 25^\circ\text{C}$	2.646	2.7	2.754	V
			$I_O = 1 \text{ mA to } 100 \text{ mA}$	2.619	2.7	2.781	
			$I_O = 1 \text{ mA to } 150 \text{ mA}$ , $T_J = 25^\circ\text{C}$	2.632	2.7	2.768	
			$I_O = 1 \text{ mA to } 150 \text{ mA}$	2.598	2.7	2.8013	
		TPS76428	$I_O = 1 \text{ mA to } 100 \text{ mA}$ , $T_J = 25^\circ\text{C}$	2.744	2.8	2.856	V
			$I_O = 1 \text{ mA to } 150 \text{ mA}$ ,	2.73	2.8	2.870	
			$I_O = 1 \text{ mA to } 150 \text{ mA}$ , $T_J = 25^\circ\text{C}$	2.716	2.8	2.884	
			$I_O = 1 \text{ mA to } 150 \text{ mA}$	2.695	2.8	2.905	
		TPS76430	$I_O = 1 \text{ mA to } 100 \text{ mA}$ , $T_J = 25^\circ\text{C}$	2.94	3.0	3.06	V
			$I_O = 1 \text{ mA to } 100 \text{ mA}$	2.925	3.0	3.075	
			$I_O = 1 \text{ mA to } 150 \text{ mA}$ , $T_J = 25^\circ\text{C}$	2.91	3.0	3.090	
			$I_O = 1 \text{ mA to } 150 \text{ mA}$	2.887	3.0	3.112	
		TPS76433	$I_O = 1 \text{ mA to } 100 \text{ mA}$ , $T_J = 25^\circ\text{C}$	3.234	3.3	3.366	V
			$I_O = 1 \text{ mA to } 100 \text{ mA}$	3.201	3.3	3.399	
			$I_O = 1 \text{ mA to } 150 \text{ mA}$ , $T_J = 25^\circ\text{C}$	3.218	3.3	3.382	
			$I_O = 1 \text{ mA to } 150 \text{ mA}$	3.177	3.3	3.423	
$I_{(Q)}$	Quiescent current (GND terminal current)	$I_O = 0 \text{ to } 150 \text{ mA}$ , $T_J = 25^\circ\text{C}$ , See Note 2		85	100	$\mu\text{A}$	
		$I_O = 0 \text{ to } 150 \text{ mA}$ , See Note 2			140		
		Standby current	$EN < 0.5 \text{ V}$ , $T_J = 25^\circ\text{C}$		0.5		1
		$EN < 0.5 \text{ V}$			2		
$V_n$	Output noise voltage	$BW = 300 \text{ Hz to } 50 \text{ kHz}$ , $C_O = 10 \mu\text{F}$ , $T_J = 25^\circ\text{C}$ , See Note 2		50		$\mu\text{V}$	
	Bypass voltage	$T_J = 25^\circ\text{C}$		1.192		V	
PSRR	Ripple rejection	$f = 1 \text{ kHz}$ , $C_O = 10 \mu\text{F}$ , $T_J = 25^\circ\text{C}$ , See Note 2		60		dB	
	Current limit	$T_J = 25^\circ\text{C}$ See Note 3		0.8	1.5	A	

NOTES: 2. Minimum  $I_N$  operating voltage is 2.7 V or  $V_{O(\text{typ})} + 1 \text{ V}$ , whichever is greater.  
3. Test condition includes, output voltage  $V_O = 0 \text{ V}$  and pulse duration = 10 mS.



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## LOW-POWER LOW-NOISE 150-mA LOW-DROPOUT LINEAR REGULATORS

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electrical characteristics over recommended operating free-air temperature range,  
 $V_I = V_{O(\text{typ})} + 1 \text{ V}$ ,  $I_O = 1 \text{ mA}$ ,  $EN = IN$ ,  $C_O = 4.7 \mu\text{F}$  (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Output voltage line regulation ( $\Delta V_O/V_O$ ) (see Note 4)		$V_O + 1 \text{ V} < V_I \leq 10 \text{ V}$ , $V_I \geq 3.5 \text{ V}$ , $T_J = 25^\circ\text{C}$		0.04	0.07	%V	
		$V_O + 1 \text{ V} < V_I \leq 10 \text{ V}$ , $V_I \geq 3.5 \text{ V}$			0.1		
$V_{IH}$	EN high level input	See Note 2		1.4	2	V	
$V_{IL}$	EN low level input	See Note 2	0.5	1.2			
$I_I$	EN input current	EN = 0 V		-0.01	-0.5	$\mu\text{A}$	
		EN = IN		-0.01	-0.5		
$V_{DO}$	Dropout voltage (see Note 5)	TPS76425	$I_O = 0 \text{ mA}$ , $T_J = 25^\circ\text{C}$		0.2	mV	
			$I_O = 1 \text{ mA}$ , $T_J = 25^\circ\text{C}$		3		
			$I_O = 50 \text{ mA}$ , $T_J = 25^\circ\text{C}$		120		150
			$I_O = 50 \text{ mA}$				200
			$I_O = 75 \text{ mA}$ , $T_J = 25^\circ\text{C}$		180		225
			$I_O = 75 \text{ mA}$				300
			$I_O = 100 \text{ mA}$ , $T_J = 25^\circ\text{C}$		240		300
			$I_O = 100 \text{ mA}$				400
			$I_O = 150 \text{ mA}$ , $T_J = 25^\circ\text{C}$		360		450
			$I_O = 150 \text{ mA}$				600
		TPS76433	$I_O = 0 \text{ mA}$ , $T_J = 25^\circ\text{C}$		0.2		
			$I_O = 1 \text{ mA}$ , $T_J = 25^\circ\text{C}$		3		
			$I_O = 50 \text{ mA}$ , $T_J = 25^\circ\text{C}$		100		125
			$I_O = 50 \text{ mA}$				166
			$I_O = 75 \text{ mA}$ , $T_J = 25^\circ\text{C}$		150		188
			$I_O = 75 \text{ mA}$				250
			$I_O = 100 \text{ mA}$ , $T_J = 25^\circ\text{C}$		200		250
			$I_O = 100 \text{ mA}$				333
			$I_O = 150 \text{ mA}$ , $T_J = 25^\circ\text{C}$		300		375
			$I_O = 150 \text{ mA}$				500

NOTES: 2. Minimum IN operating voltage is 2.7 V or  $V_{O(\text{typ})} + 1 \text{ V}$ , whichever is greater.

4. If  $V_O < 2.5 \text{ V}$  and  $V_{I\text{max}} = 10 \text{ V}$ ,  $V_{I\text{min}} = 3.5 \text{ V}$ :

$$\text{Line Reg. (mV)} = (\%/\text{V}) \times \frac{V_O(V_{I\text{max}} - 3.5 \text{ V})}{100} \times 1000$$

If  $V_O > 2.5 \text{ V}$  and  $V_{I\text{max}} = 10 \text{ V}$ ,  $V_{I\text{min}} = V_O + 1 \text{ V}$ :

$$\text{Line Reg. (mV)} = (\%/\text{V}) \times \frac{V_O(V_{I\text{max}} - (V_O + 1))}{100} \times 1000$$

5. Dropout voltage is defined as the differential voltage between  $V_O$  and  $V_I$  when  $V_O$  drops 100 mV below the value measured with  $V_I = V_O + 1.0 \text{ V}$ .



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## TYPICAL CHARACTERISTICS

### Table of Graphs

			FIGURE
$V_O$	Output voltage	vs Output current	1
		vs Free-air temperature	2, 3, 4
$V_n$	Output noise	vs Frequency	5
$V_n$	Output noise voltage	vs Bypass capacitance	6
		vs Load current	7
$Z_O$	Output impedance	vs Frequency	8
$V_{DO}$	Dropout voltage	vs Free-air temperature	9
	Ripple rejection	vs Frequency	10
		Line transient response	11, 13
		Load transient response	12, 14
	Compensation series resistance (CSR)	vs Output current	15, 17
		vs Added ceramic capacitance	16, 18

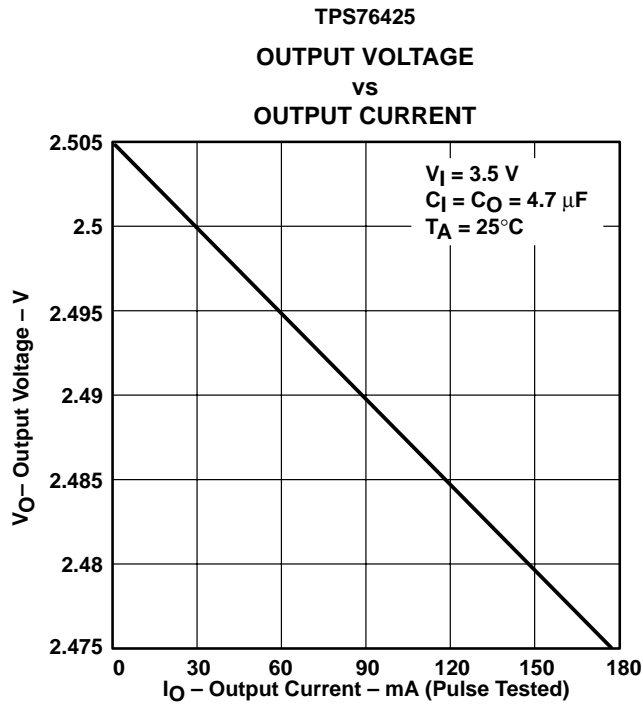


Figure 1

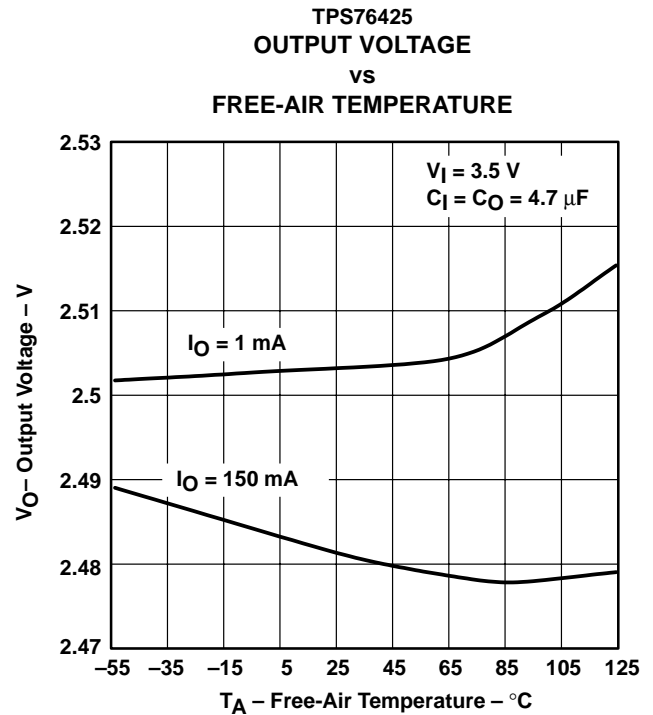


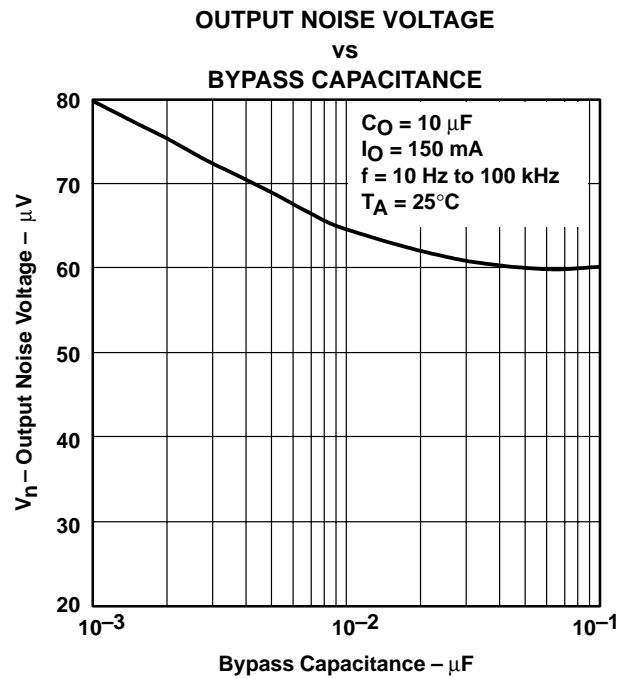
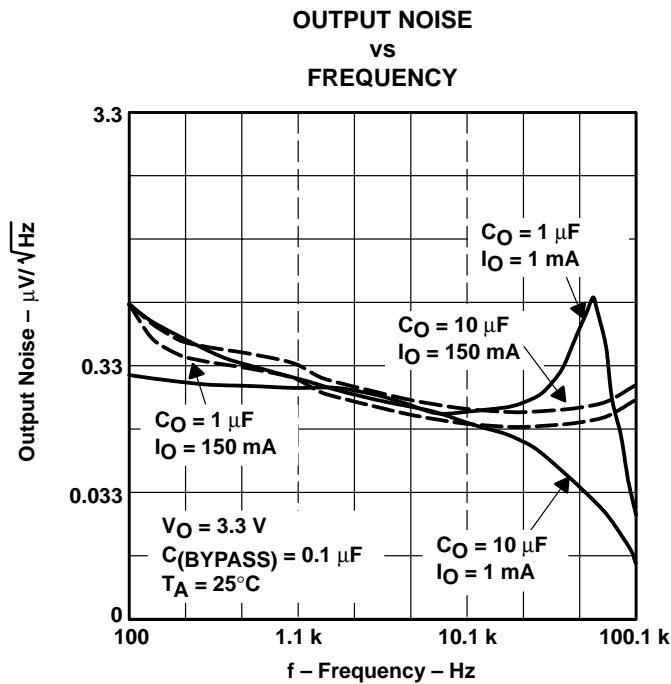
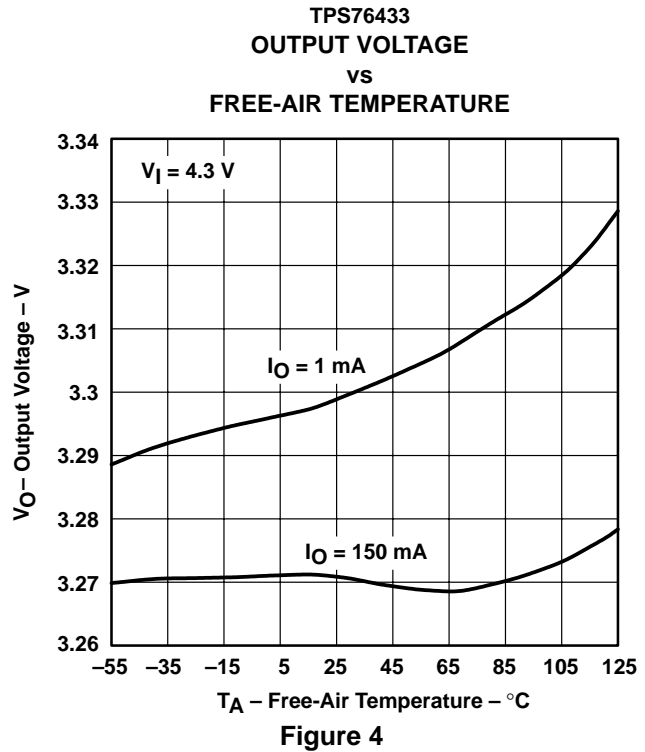
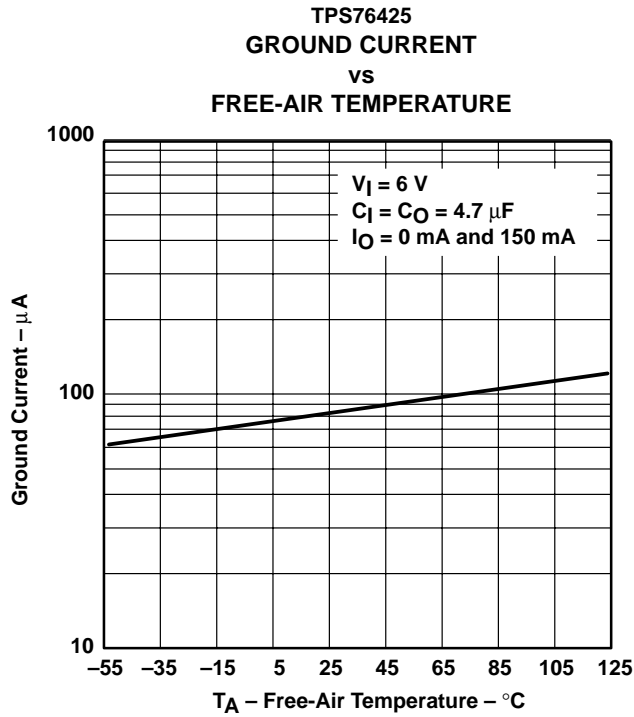
Figure 2

# TPS76425, TPS76427, TPS76428, TPS76430, TPS76433

## LOW-POWER LOW-NOISE 150-mA LOW-DROPOUT LINEAR REGULATORS

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### TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

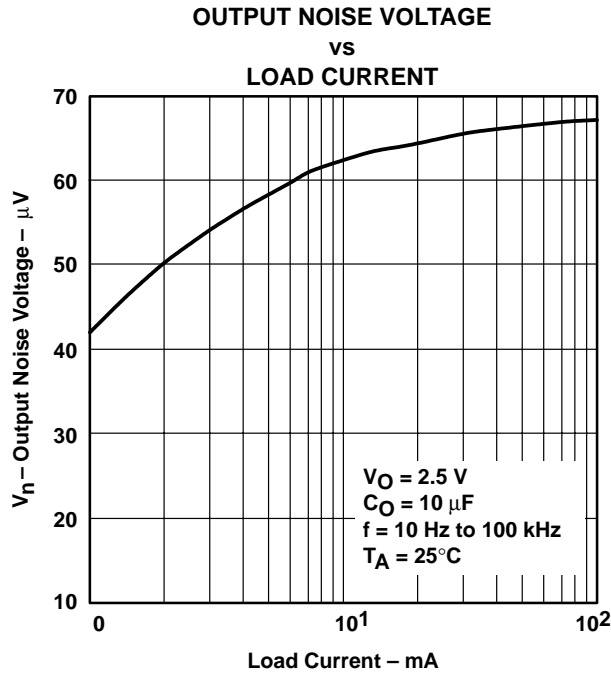


Figure 7

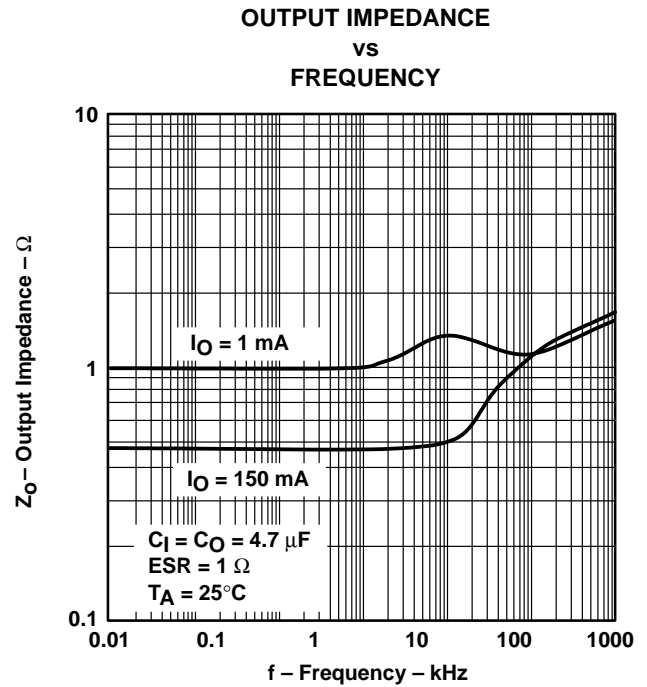


Figure 8

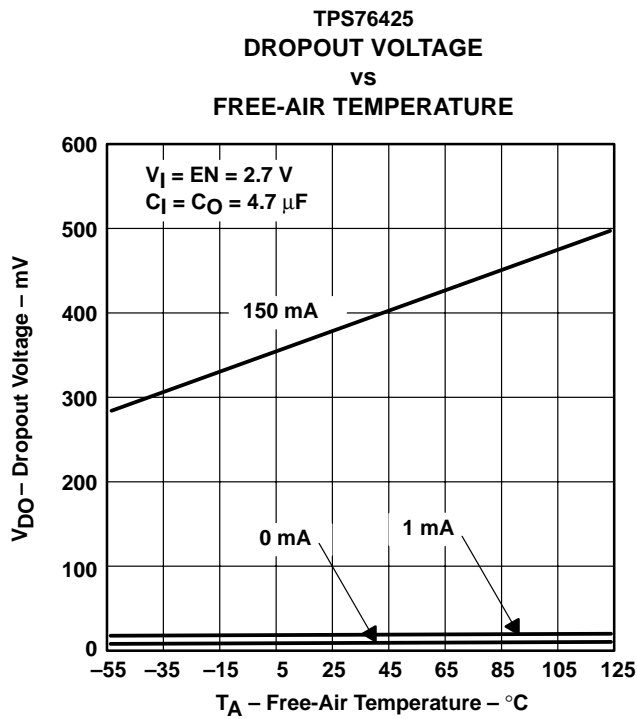


Figure 9

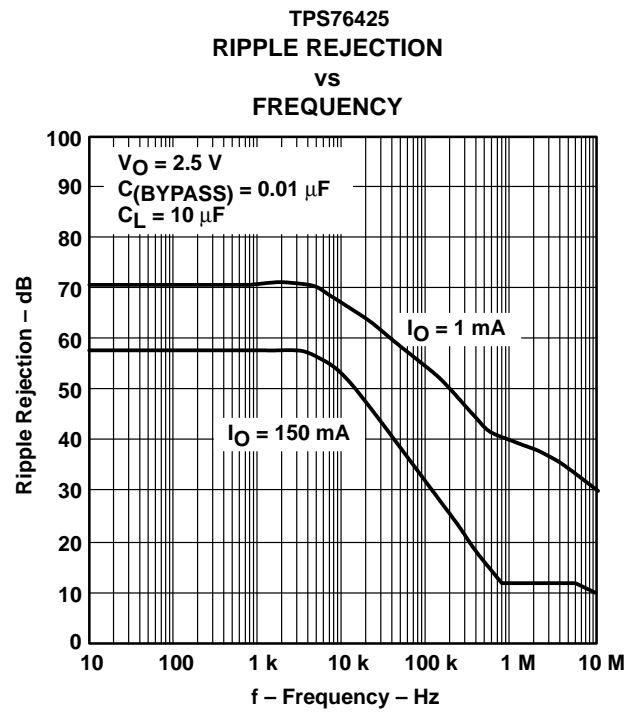


Figure 10

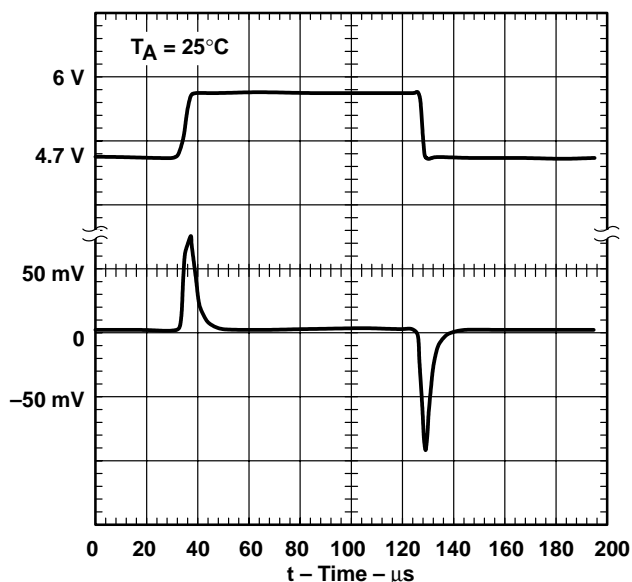
# TPS76425, TPS76427, TPS76428, TPS76430, TPS76433

## LOW-POWER LOW-NOISE 150-mA LOW-DROPOUT LINEAR REGULATORS

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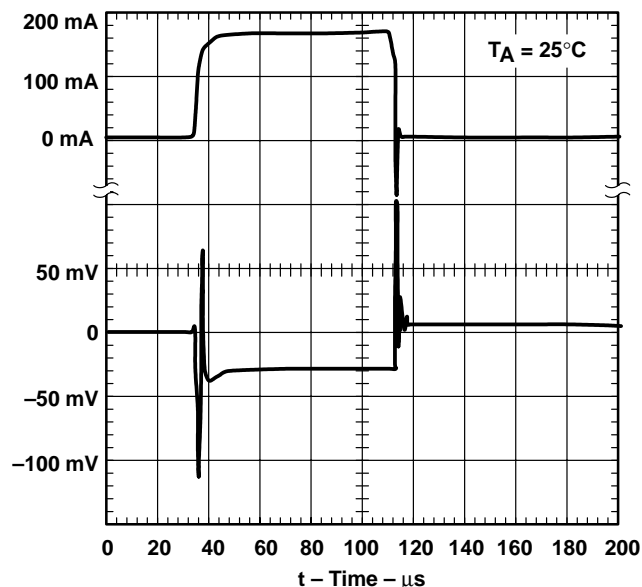
### TYPICAL CHARACTERISTICS

**TPS76425**  
**LINE TRANSIENT RESPONSE**



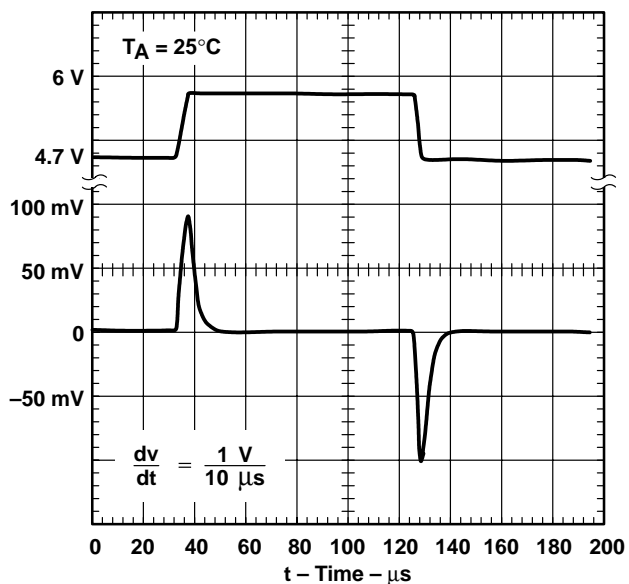
**Figure 11**

**TPS76425**  
**LOAD TRANSIENT RESPONSE**



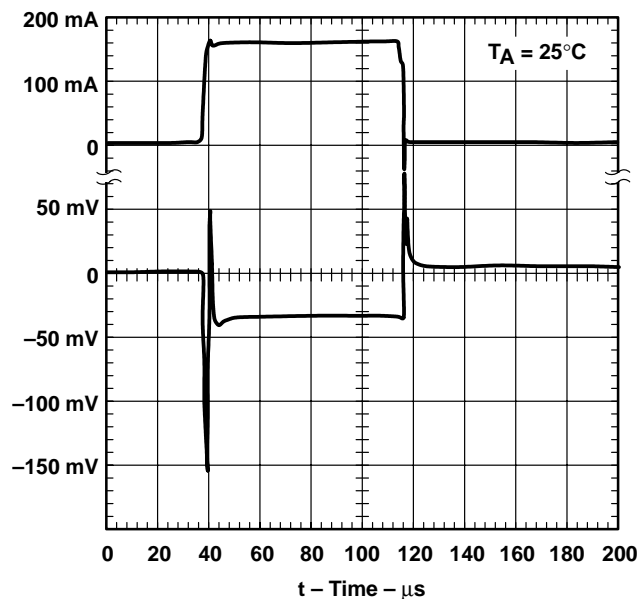
**Figure 12**

**TPS76433**  
**LINE TRANSIENT RESPONSE**



**Figure 13**

**TPS76433**  
**LOAD TRANSIENT RESPONSE**



**Figure 14**

TYPICAL CHARACTERISTICS

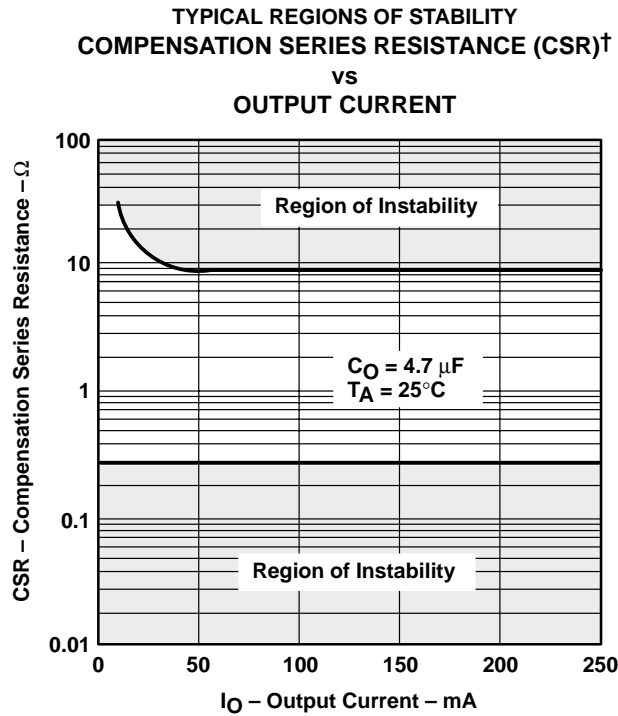


Figure 15

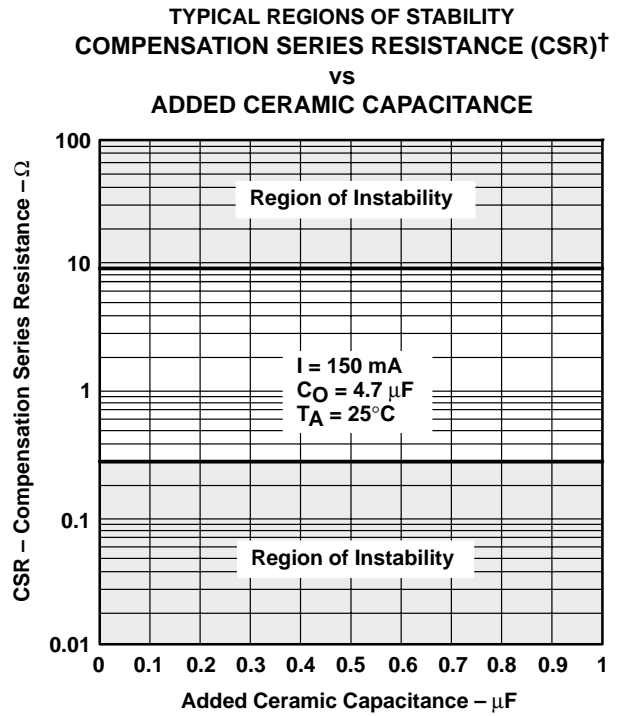


Figure 16

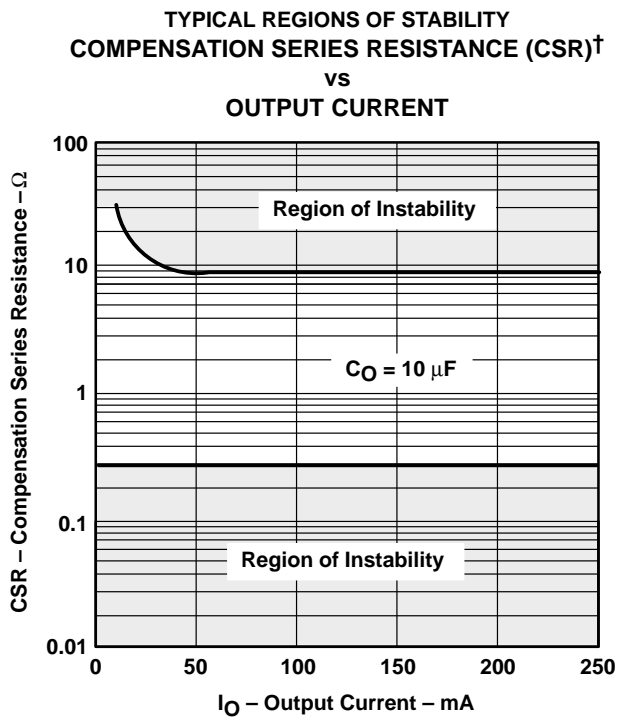


Figure 17

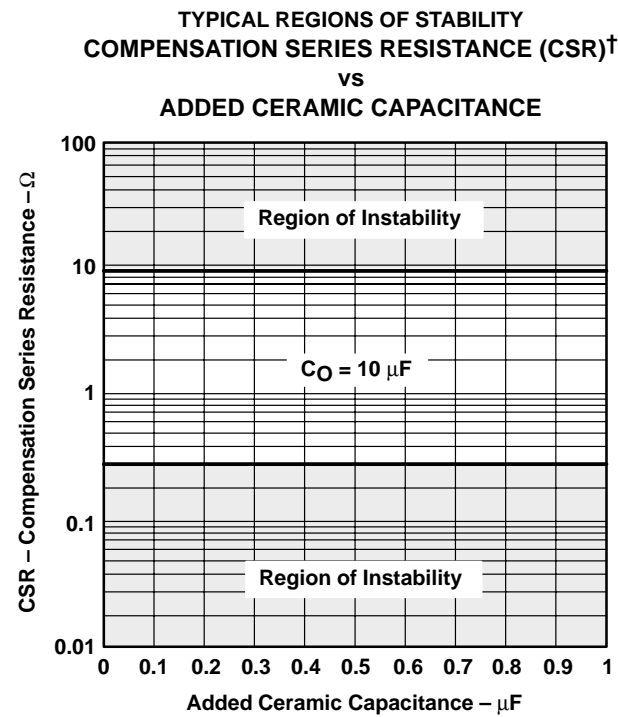


Figure 18

<sup>†</sup> CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to  $C_O$ .

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## APPLICATION INFORMATION

The TPS764xx family of low-noise and low-dropout (LDO) regulators are optimized for use in battery-operated equipment. They feature extremely low noise (50  $\mu\text{V}$ ), low dropout voltages, low quiescent current (140  $\mu\text{A}$ ), and an enable input to reduce supply current to less than 2  $\mu\text{A}$  when the regulator is turned off.

### device operation

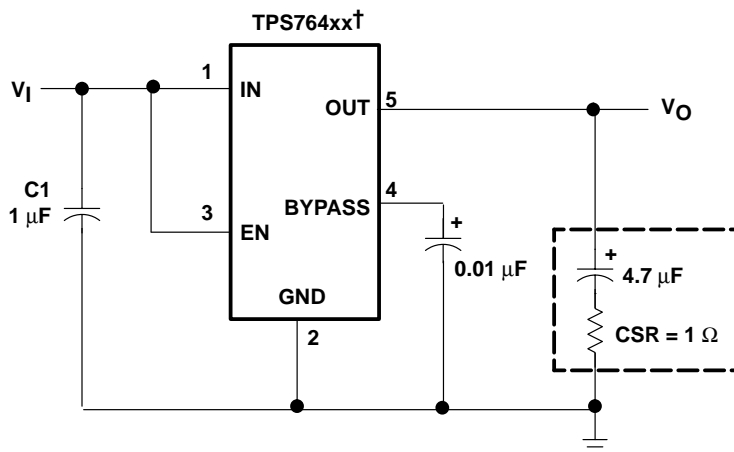
The TPS764xx uses a PMOS pass element to dramatically reduce both dropout voltage and supply current over more conventional PNP-pass-element LDO designs. The PMOS pass element is a voltage-controlled device which, unlike a PNP transistor, does not require increased drive current as output current increases. Supply current in the TPS764xx is essentially constant from no-load to maximum load.

Current limiting and thermal protection prevent damage by excessive output current and/or power dissipation. The device switches into a constant-current mode at approximately 1 A; further load reduces the output voltage instead of increasing the output current. The thermal protection shuts the regulator off if the junction temperature rises above 165°C. Recovery is automatic when the junction temperature drops approximately 25°C below the high temperature trip point. The PMOS pass element includes a back diode that safely conducts reverse current when the input voltage level drops below the output voltage level.

An internal resistor, in conjunction with external 0.01- $\mu\text{F}$  bypass capacitor, creates a low-pass filter to further reduce the noise. The TPS764xx exhibits only 50  $\mu\text{V}$  of output voltage noise using 0.01  $\mu\text{F}$  bypass and 4.7- $\mu\text{F}$  output capacitors.

A logic low on the enable input, EN, shuts off the output and reduces the supply current to less than 2  $\mu\text{A}$ . EN should be tied high in applications where the shutdown feature is not used.

A typical application circuit is shown in Figure 19.



† TPS76425, TPS76427, TPS76430, TPS76433.

Figure 19. Typical Application Circuit

# TPS76425, TPS76427, TPS76428, TPS76430, TPS76433 LOW-POWER LOW-NOISE 150-mA LOW-DROPOUT LINEAR REGULATORS

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## APPLICATION INFORMATION

### external capacitor requirements

Although not required, a 0.047- $\mu\text{F}$  or larger ceramic bypass input capacitor, connected between IN and GND and located close to the TPS764xx, is recommended to improve transient response and noise rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like all low dropout regulators, the TPS764xx requires an output capacitor connected between OUT and GND to stabilize the internal loop control. The minimum recommended capacitance value is 4.7  $\mu\text{F}$  and the ESR (equivalent series resistance) must be between 0.2  $\Omega$  and 10  $\Omega$ . Capacitor values 4.7  $\mu\text{F}$  or larger are acceptable, provided the ESR is less than 10  $\Omega$ . Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Most of the commercially available 4.7  $\mu\text{F}$  surface-mount solid tantalum capacitors, including devices from Sprague, Kemet, and Nichico, meet the ESR requirements previously stated. Multilayer ceramic capacitors should have minimum values of 1  $\mu\text{F}$  over the full operating temperature range of the equipment.

### CAPACITOR SELECTION

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
T494B475K016AS	KEMET	4.7 $\mu\text{F}$	1.5 $\Omega$	1.9 × 3.5 × 2.8
195D106x0016x2T	SPRAGUE	10 $\mu\text{F}$	1.5 $\Omega$	1.3 × 7.0 × 2.7
695D106x003562T	SPRAGUE	10 $\mu\text{F}$	1.3 $\Omega$	2.5 × 7.6 × 2.5
TPSC475K035R0600	AVX	4.7 $\mu\text{F}$	0.6 $\Omega$	2.6 × 6.0 × 3.2

† Size is in mm. ESR is maximum resistance in ohms at 100 kHz and  $T_A = 25^\circ\text{C}$ . Listings are sorted by height.

# TPS76425, TPS76427, TPS76428, TPS76430, TPS76433 LOW-POWER LOW-NOISE 150-mA LOW-DROPOUT LINEAR REGULATORS

SLVS180B – MARCH 1999 – REVISED MAY 2001

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## APPLICATION INFORMATION

### power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature allowable without damaging the device is 150°C. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation,  $P_{D(max)}$ , and the actual dissipation,  $P_D$ , which must be less than or equal to  $P_{D(max)}$ .

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

Where:

$T_{Jmax}$  is the maximum allowable junction temperature

$R_{\theta JA}$  is the thermal resistance junction-to-ambient for the package, see the dissipation rating table.

$T_A$  is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \times I_O$$

Power dissipation resulting from quiescent current is negligible.

### regulator protection

The TPS764xx pass element has a built-in back diode that safely conducts reverse current when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage is anticipated, external limiting might be appropriate.

The TPS764xx also features internal current limiting and thermal protection. During normal operation, the TPS764xx limits output current to approximately 800 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below 140°C, regulator operation resumes.



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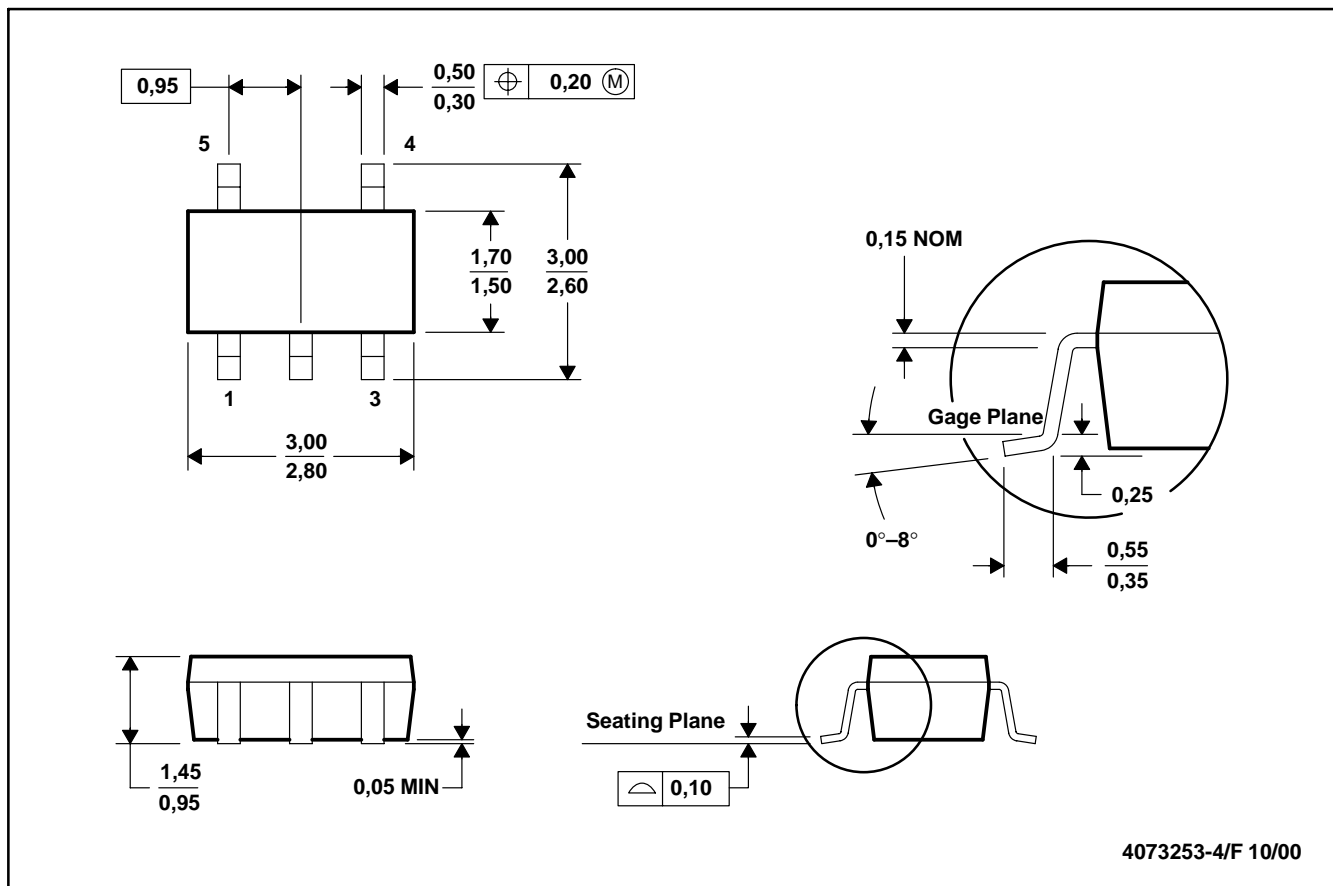
TPS76425, TPS76427, TPS76428, TPS76430, TPS76433  
 LOW-POWER LOW-NOISE 150-mA LOW-DROPOUT LINEAR REGULATORS

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MECHANICAL DATA

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion.  
 D. Falls within JEDEC MO-178

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TPS76425DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76425DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76425DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76425DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76427DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76427DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76427DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76427DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76428DBV	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI
TPS76428DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76428DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76428DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76428DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76430DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76430DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76430DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76430DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76433DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76433DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76433DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS76433DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check

<http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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