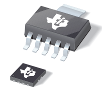


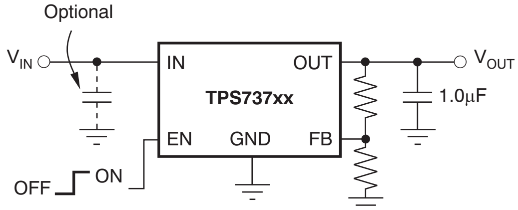
1A Low-Dropout Regulator with Reverse Current Protection

FEATURES

- **Stable with 1.0µF or Larger Ceramic Output Capacitor**
- **Input Voltage Range: 2.2V to 5.5V**
- **Ultra-Low Dropout Voltage: 130mV typ at 1A**
- **Excellent Load Transient Response—Even With Only 1.0µF Output Capacitor**
- **NMOS Topology Delivers Low Reverse Leakage Current**
- **1.0% Initial Accuracy**
- **3% Overall Accuracy Over Line, Load, and Temperature**
- **Less Than 20nA typical I_Q in Shutdown Mode**
- **Thermal Shutdown and Current Limit for Fault Protection**
- **Available in Multiple Output Voltage Versions**
  - **Adjustable Output: 1.20V to 5.5V**
  - **Custom Outputs Available Using Factory Package-Level Programming**

APPLICATIONS

- **Point of Load Regulation for DSPs, FPGAs, ASICs, and Microprocessors**
- **Post-Regulation for Switching Supplies**
- **Portable/Battery-Powered Equipment**



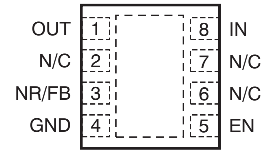
Typical Application Circuit

DESCRIPTION

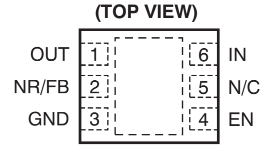
The TPS737xx family of linear low-dropout (LDO) voltage regulators uses an NMOS pass element in a voltage-follower configuration. This topology is relatively insensitive to output capacitor value and ESR, allowing a wide variety of load configurations. Load transient response is excellent, even with a small 1.0µF ceramic output capacitor. The NMOS topology also allows very low dropout.

The TPS737xx family uses an advanced BiCMOS process to yield high precision while delivering very low dropout voltages and low ground pin current. Current consumption, when not enabled, is under 20nA and ideal for portable applications. These devices are protected by thermal shutdown and foldback current limit.

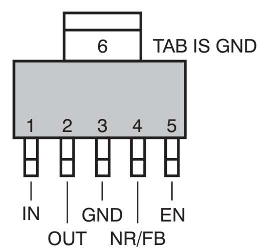
DRB PACKAGE
3mm x 3mm SON
(TOP VIEW)



DRV PACKAGE(1)
2mm x 2mm SON
(TOP VIEW)



DCQ PACKAGE
SOT223
(TOP VIEW)



(1) Power dissipation may limit operating range. Check Thermal Information table.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT} (2)
TPS737**xx** ***yy yz***	**XX** is nominal output voltage (for example, 25 = 2.5V, 01 = Adjustable(3)). **YYY** is package designator. **Z** is package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
(2) Most output voltages of 1.25V and 1.3V to 5.0V in 100mV increments are available on a quick-turn basis using innovative factory package-level programming. Minimum order quantities apply; contact factory for details and availability.
(3) For fixed 1.20V operation, tie FB to OUT.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range unless otherwise noted.

PARAMETER	TPS737xx	UNIT
V_{IN} range	–0.3 to +6.0	V
V_{EN} range	–0.3 to +6.0	V
V_{OUT} range	–0.3 to +5.5	V
V_{NR}, V_{FB} range	–0.3 to +6.0	V
Peak output current	Internally limited	
Output short-circuit duration	Indefinite	
Continuous total power dissipation	See *Thermal Information* table	
Junction temperature range, T_J	–55 to +150	°C
Storage temperature range	–65 to +150	°C
ESD rating, HBM	2	kV
ESD rating, CDM	500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the *Electrical Characteristics* is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC[1]		TPS737xx[2]			UNITS
		DRB	DCQ	DRV	
		8 PINS	6 PINS	6 PINS	
θ_{JA}	Junction-to-ambient thermal resistance[3]	47.8	70.4	50.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[4]	83	70	59	
θ_{JB}	Junction-to-board thermal resistance[5]	N/A	N/A	N/A	
ψ_{JT}	Junction-to-top characterization parameter[6]	2.1	6.8	0.1	
ψ_{JB}	Junction-to-board characterization parameter[7]	17.8	30.1	30.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[8]	12.1	6.3	8.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953A.

(2) Thermal data for the DRB, DCQ, and DRV packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:

(a) i. DRB: The exposed pad is connected to the PCB ground layer through a 2x2 thermal via array.
ii. DCQ: The exposed pad is connected to the PCB ground layer through a 3x2 thermal via array.
iii. DRV: The exposed pad is connected to the PCB ground layer through a 2x2 thermal via array. Due to size limitation of thermal pad, 0.8-mm pitch array is used which is off the JEDEC standard.

(b) i. DRB: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.
ii. DCQ: Each of top and bottom copper layers has a dedicated pattern for 20% copper coverage.
iii DRV: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.

(c) These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3in × 3in copper area. To understand the effects of the copper area on thermal performance, see the *Power Dissipation* and *Estimating Junction Temperature* sections of this data sheet.

(3) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

(4) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the top of the package. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

(5) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

(6) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).

(7) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).

(8) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

Over operating temperature range (T_J = –40°C to +125°C), $V_{IN} = V_{OUT(nom)}$ + 1.0V[1], I_{OUT} = 10mA, V_{EN} = 2.2V, and C_{OUT} = 2.2μF, unless otherwise noted. Typical values are at T_J = +25°C.

PARAMETER			TEST CONDITIONS	TPS737xx MIN	TPS737xx TYP	TPS737xx MAX	UNIT
V_{IN}	Input voltage range[1], [2]			2.2		5.5	V
V_{FB}	Internal reference (TPS73701-DCQ)		T_J = +25°C	1.198	1.2	1.210	V
	Internal reference (TPS73701-DRB)		T_J = +25°C	1.192	1.2	1.216	
V_{OUT}	Output voltage range (TPS73701)[3]			V_{FB}		5.5 – V_{DO}	V
	Accuracy[1], [4]	Nominal	T_J = +25°C	–1.0		+1.0	%
			5.36V < V_{IN} < 5.5V, V_{OUT} = 5.08V, 10mA < I_{OUT} < 800mA, –40C < T_J < +85°C, TPS73701DCQ	–2.0		+2.0	
		over V_{IN}, I_{OUT}, and T	V_{OUT} + 0.5V ≤ V_{IN} ≤ 5.5V; 10mA ≤ I_{OUT} ≤ 1A	–3.0	±0.5	+3.0	
$\Delta V_{OUT}\%/\Delta V_{IN}$	Line regulation[1]		$V_{OUT(nom)}$ + 0.5V ≤ V_{IN} ≤ 5.5V		0.01		%/V
$\Delta V_{OUT}\%/\Delta I_{OUT}$	Load regulation		1mA ≤ I_{OUT} ≤ 1A		0.002		%/mA
			10mA ≤ I_{OUT} ≤ 1A		0.0005		
V_{DO}	Dropout voltage[5] ($V_{IN} = V_{OUT(nom)}$ – 0.1V)		I_{OUT} = 1A		130	500	mV
Z_O(DO)	Output impedance in dropout		2.2V ≤ V_{IN} ≤ V_{OUT} + V_{DO}		0.25		Ω
I_{CL}	Output current limit		V_{OUT} = 0.9 × $V_{OUT(nom)}$	1.05	1.6	2.2	A
I_{SC}	Short-circuit current		V_{OUT} = 0V		450		mA
I_{REV}	Reverse leakage current[6] (–I_{IN})		V_{EN} ≤ 0.5V, 0V ≤ V_{IN} ≤ V_{OUT}		0.1		μA
I_{GND}	GND pin current		I_{OUT} = 10mA (I_Q)		400		μA
			I_{OUT} = 1A		1300		
I_{SHDN}	Shutdown current (I_{GND})		V_{EN} ≤ 0.5V, V_{OUT} ≤ V_{IN} ≤ 5.5		20		nA
I_{FB}	FB pin current (TPS73701)				0.1	0.6	μA
PSRR	Power-supply rejection ratio (ripple rejection)		f = 100Hz, I_{OUT} = 1A		58		dB
			f = 10kHz, I_{OUT} = 1A		37		
V_N	Output noise voltage BW = 10Hz to 100kHz		C_{OUT} = 10μF		27 × V_{OUT}		μV_{RMS}
t_{STR}	Startup time		V_{OUT} = 3V, R_L = 30Ω, C_{OUT} = 1μF		600		μs
$V_{EN(HI)}$	EN pin high (enabled)			1.7		V_{IN}	V
$V_{EN(LO)}$	EN pin low (shutdown)			0		0.5	V
$I_{EN(HI)}$	EN pin current (enabled)		V_{EN} = 5.5V		20		nA
T_{SD}	Thermal shutdown temperature		Shutdown, temperature increasing		+160		°C
			Reset, temperature decreasing		+140		
T_J	Operating junction temperature			–40		+125	°C

(1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or 2.2V, whichever is greater.
(2) For $V_{OUT(nom)}$ < 1.6V, when V_{IN} ≤ 1.6V, the output will lock to V_{IN} and may result in an over-voltage condition on the output. To avoid this situation, disable the device before powering down V_{IN}.
(3) TPS73701 is tested at V_{OUT} = 1.2V.
(4) Tolerance of external resistors not included in this specification.
(5) V_{DO} is not measured for fixed output versions with $V_{OUT(nom)}$ < 2.3V since minimum V_{IN} = 2.2V.
(6) Fixed-voltage versions only; refer to the *Applications* section for more information.

FUNCTIONAL BLOCK DIAGRAMS

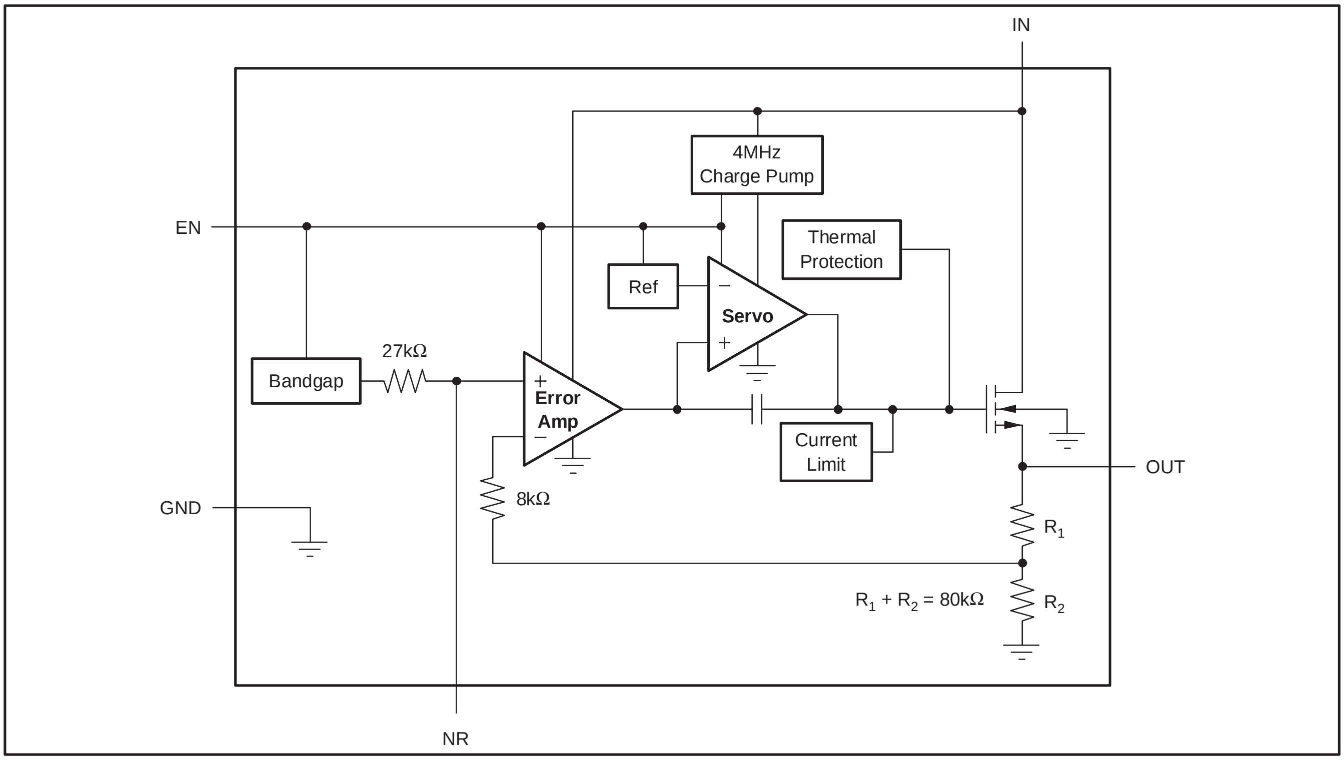


Figure 1. Fixed Voltage Version

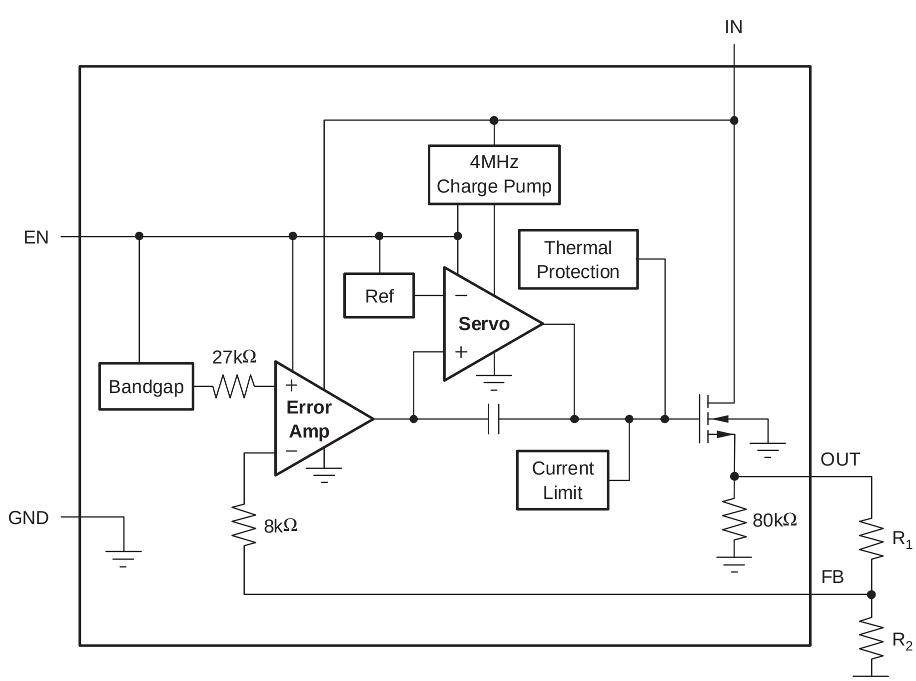


Table 1. Standard 1% Resistor Values for Common Output Voltages

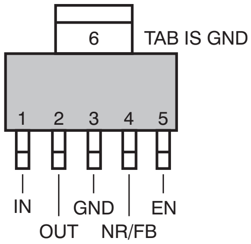
V_O	R_1	R_2
1.2V	Short	Open
1.5V	23.2kΩ	95.3kΩ
1.8V	28.0kΩ	56.2kΩ
2.5V	39.2kΩ	36.5kΩ
2.8V	44.2kΩ	33.2kΩ
3.0V	46.4kΩ	30.9kΩ
3.3V	52.3kΩ	30.1kΩ

NOTE: $V_{OUT} = (R_1 + R_2)/R_2 \times 1.204$; $R_1 || R_2 \cong 19k\Omega$ for best accuracy.

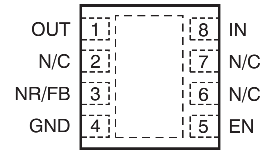
Figure 2. Adjustable Voltage Version

PIN CONFIGURATIONS

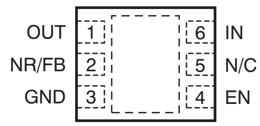
DCQ PACKAGE
SOT223-6
(TOP VIEW)



DRB PACKAGE
3mm x 3mm SON
(TOP VIEW)



DRV PACKAGE(1)
2mm x 2mm SON
(TOP VIEW)



(1) Power dissipation may limit operating range. Check Thermal Information table.

Table 1. Pin Descriptions

PIN NAME	SOT223 (DCQ) PIN NO.	3×3 SON (DRB) PIN NO.	2×2 SON (DRV) PIN NO.	DESCRIPTION
IN	1	8	6	Unregulated input supply
GND	3, 6	4, Pad	3, Pad	Ground
EN	5	5	4	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. Refer to the *Shutdown* section under *Applications Information* for more details. EN must not be left floating and can be connected to IN if not used.
NR	4	3	2	Fixed voltage versions only—connecting an external capacitor to this pin bypasses noise generated by the internal bandgap, reducing output noise to very low levels.
FB	4	3	2	Adjustable voltage version only—this is the input to the control loop error amplifier, and is used to set the output voltage of the device.
OUT	2	1	1	Regulator output. A 1.0μF or larger capacitor of any type is required for stability.
NC	—	2, 6, 7	5	Not connected

TYPICAL CHARACTERISTICS

For all voltage versions at T_J = +25°C, V_{IN} = $V_{OUT(nom)}$ + 1.0V, I_{OUT} = 10mA, V_{EN} = 2.2V, and C_{OUT} = 2.2µF, unless otherwise noted.

LOAD REGULATION

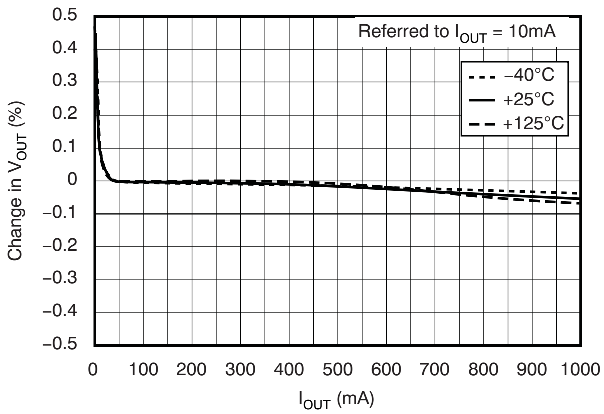


Figure 3.

LINE REGULATION

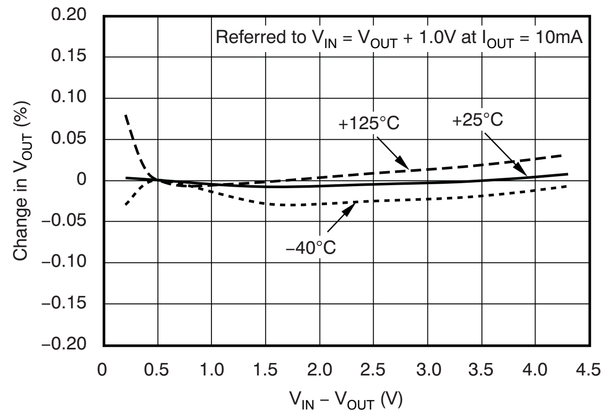


Figure 4.

DROPOUT VOLTAGE vs OUTPUT CURRENT

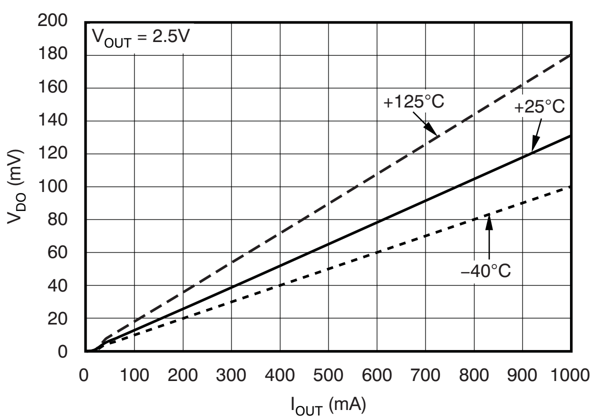


Figure 5.

DROPOUT VOLTAGE vs TEMPERATURE

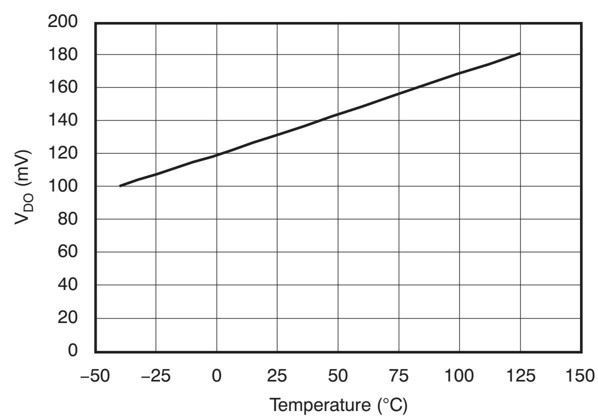


Figure 6.

OUTPUT VOLTAGE HISTOGRAM

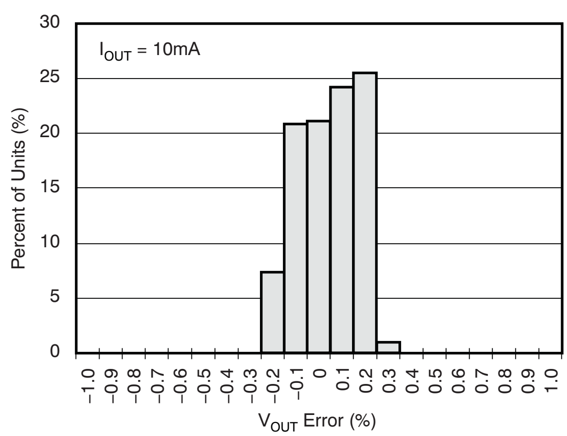


Figure 7.

DROPOUT VOLTAGE DRIFT HISTOGRAM

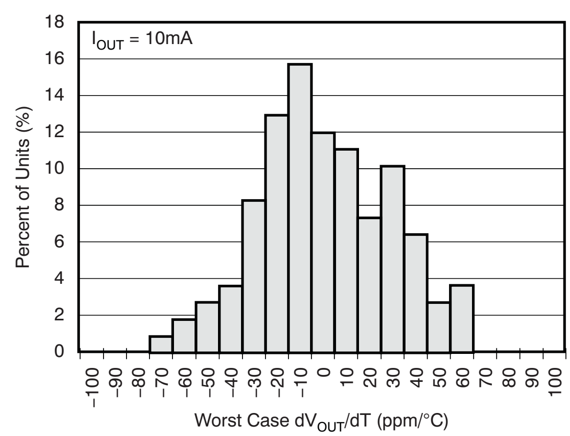


Figure 8.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions at T_J = +25°C, V_{IN} = $V_{OUT(nom)}$ + 1.0V, I_{OUT} = 10mA, V_{EN} = 2.2V, and C_{OUT} = 2.2μF, unless otherwise noted.

GROUND PIN CURRENT vs OUTPUT CURRENT

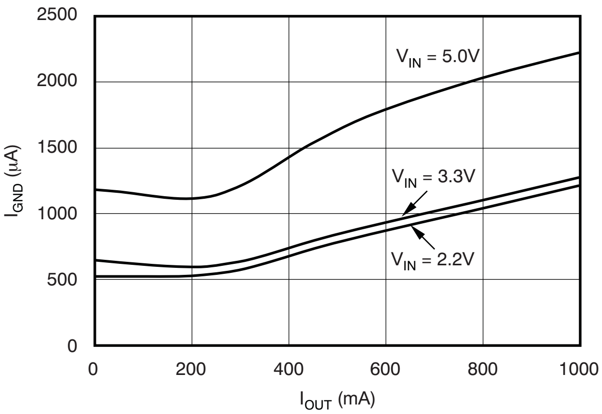


Figure 9.

GROUND PIN CURRENT vs TEMPERATURE

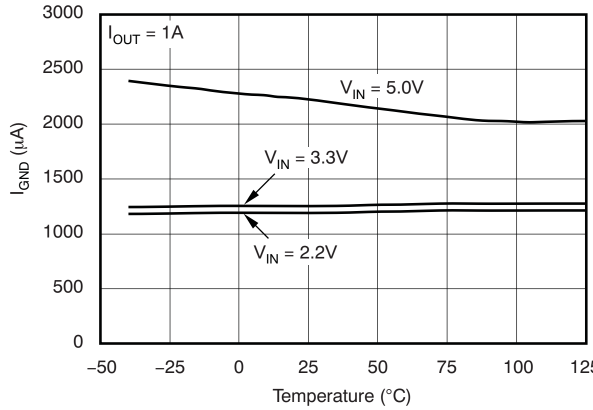


Figure 10.

GROUND PIN CURRENT IN SHUTDOWN vs TEMPERATURE

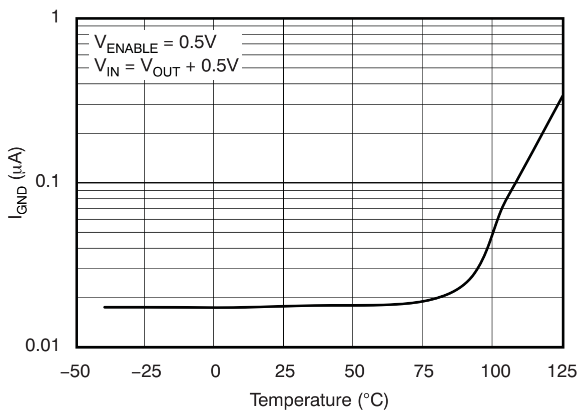


Figure 11.

CURRENT LIMIT vs V_{OUT} (FOLDBACK)

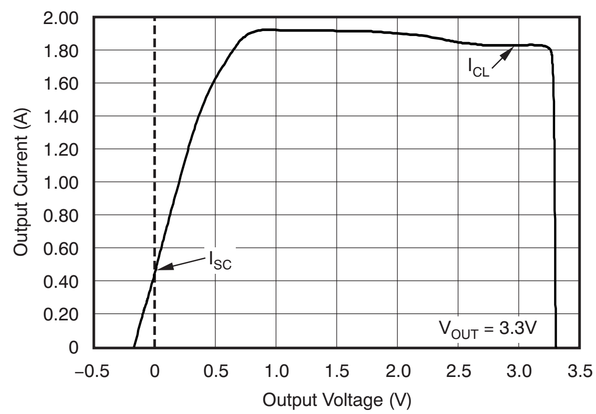


Figure 12.

CURRENT LIMIT vs V_{IN}

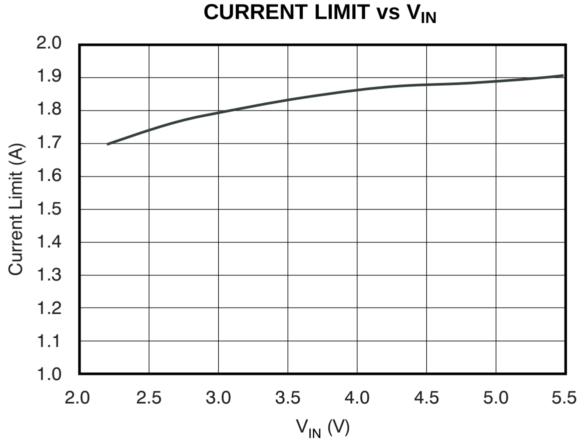


Figure 13.

CURRENT LIMIT vs TEMPERATURE

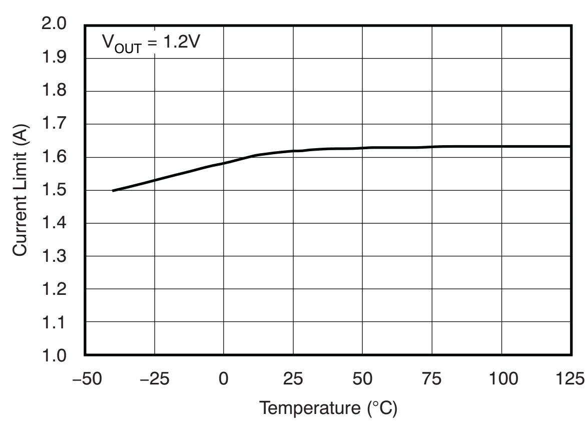


Figure 14.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions at T_J = +25°C, V_{IN} = $V_{OUT(nom)}$ + 1.0V, I_{OUT} = 10mA, V_{EN} = 2.2V, and C_{OUT} = 2.2μF, unless otherwise noted.

PSRR (RIPPLE REJECTION) vs FREQUENCY

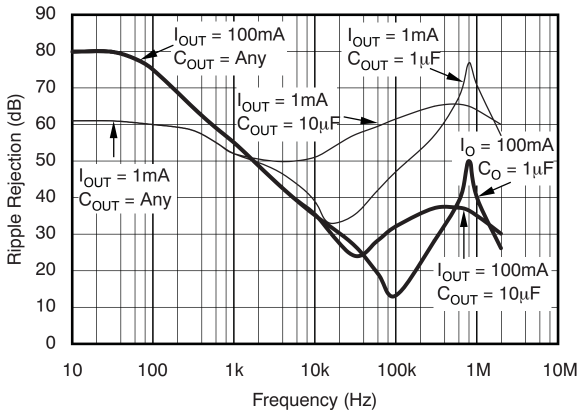


Figure 15.

PSRR (RIPPLE REJECTION) vs V_{IN} – V_{OUT}

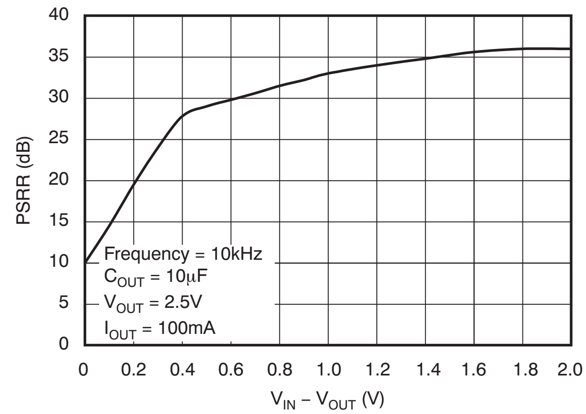


Figure 16.

NOISE SPECTRAL DENSITY

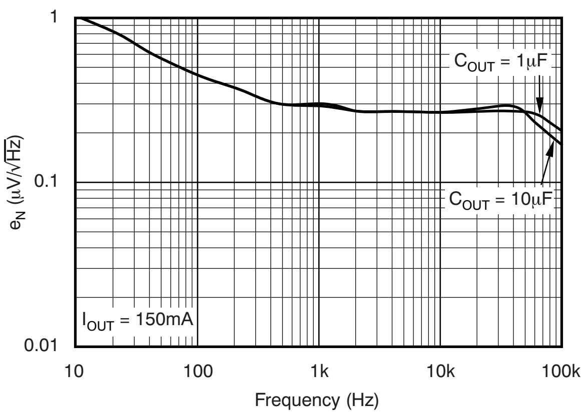


Figure 17.

TPS73701
RMS NOISE VOLTAGE vs C_{FB}

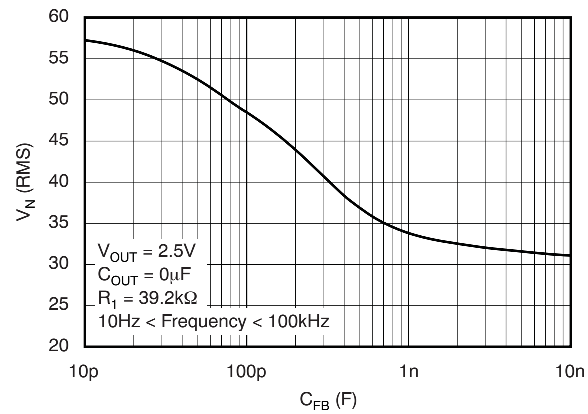


Figure 18.

RMS NOISE VOLTAGE vs C_{OUT}

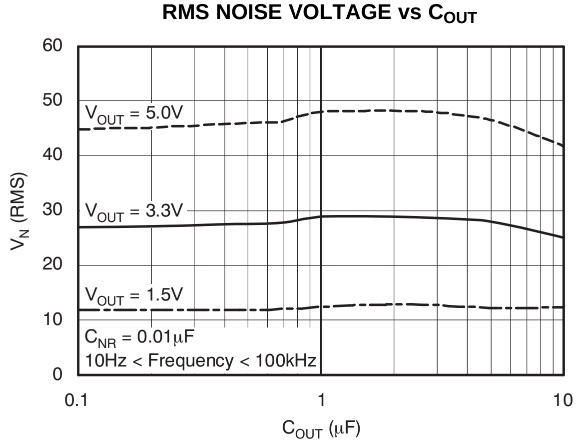


Figure 19.

RMS NOISE VOLTAGE vs C_{NR}

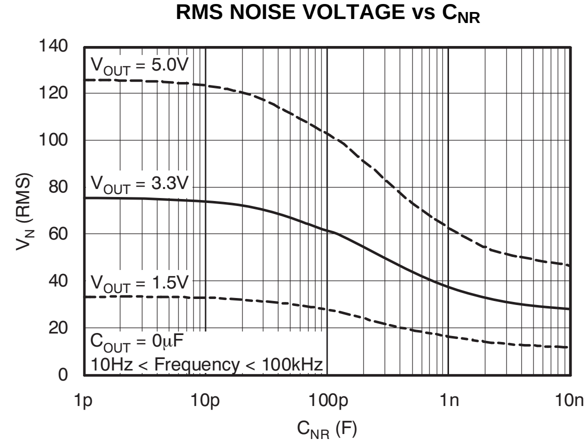


Figure 20.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions at T_J = +25°C, V_{IN} = $V_{OUT(nom)}$ + 1.0V, I_{OUT} = 10mA, V_{EN} = 2.2V, and C_{OUT} = 2.2μF, unless otherwise noted.

TPS73733
LOAD TRANSIENT RESPONSE

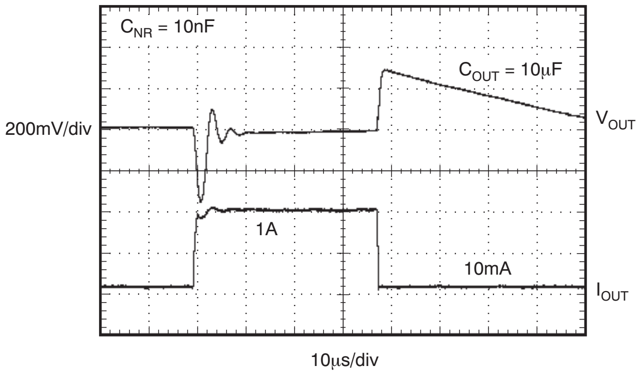


Figure 21.

TPS73733
LINE TRANSIENT RESPONSE

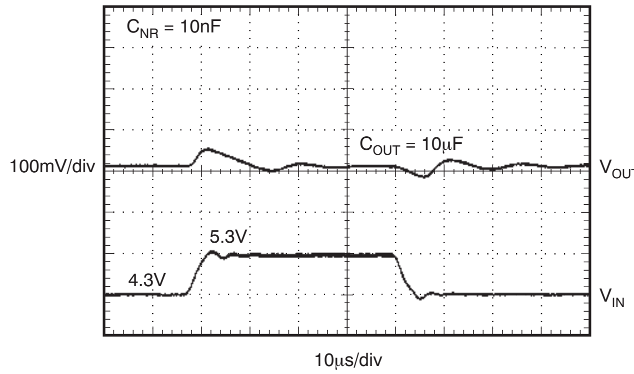


Figure 22.

TPS73701
TURN-ON RESPONSE

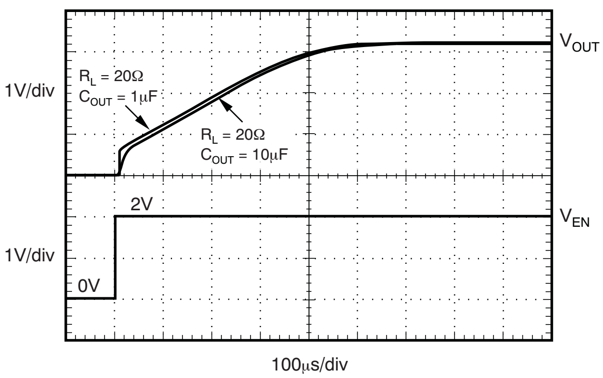


Figure 23.

TPS73701
TURN-OFF RESPONSE

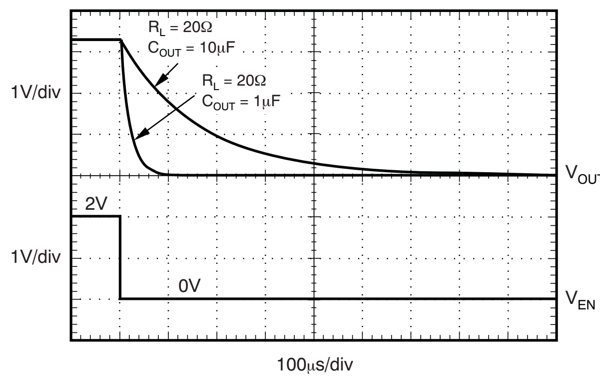


Figure 24.

TPS73701, V_{OUT} = 3.3V
POWER-UP/POWER-DOWN

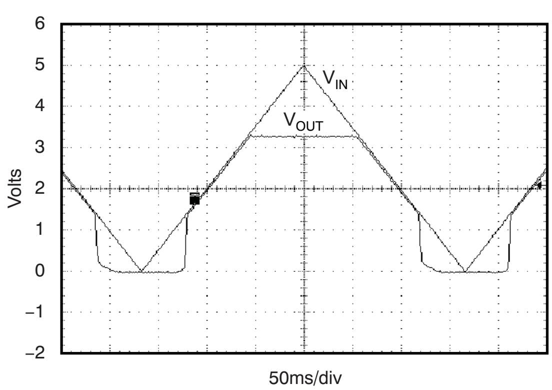


Figure 25.

I_{ENABLE} vs TEMPERATURE

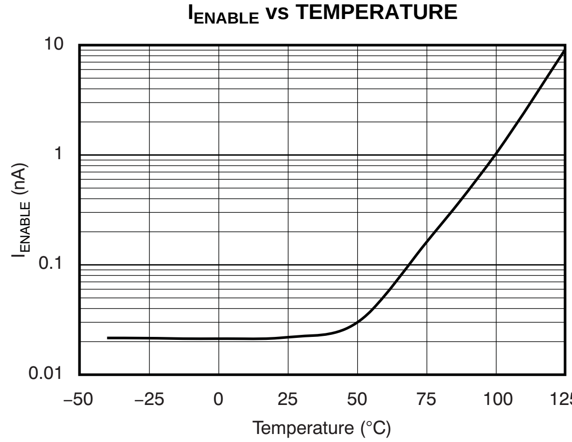


Figure 26.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions at T_J = +25°C, V_{IN} = $V_{OUT(nom)}$ + 1.0V, I_{OUT} = 10mA, V_{EN} = 2.2V, and C_{OUT} = 2.2µF, unless otherwise noted.

TPS73701
RMS NOISE VOLTAGE vs C_{FB}

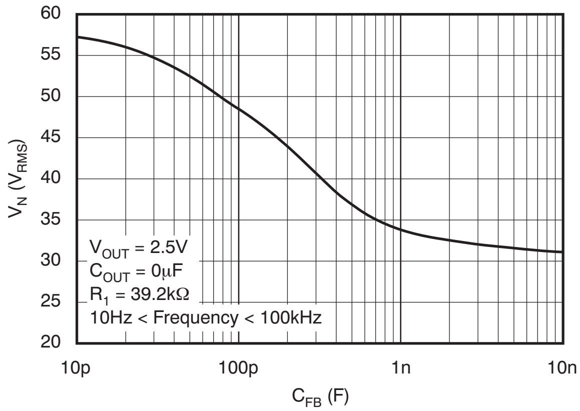


Figure 27.

TPS73701
I_{FB} vs TEMPERATURE

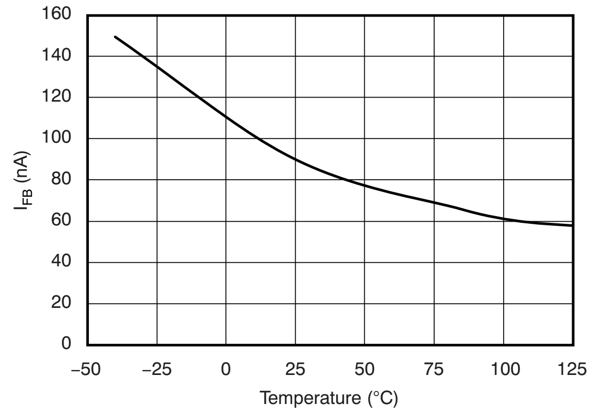


Figure 28.

TPS73701
LOAD TRANSIENT, ADJUSTABLE VERSION

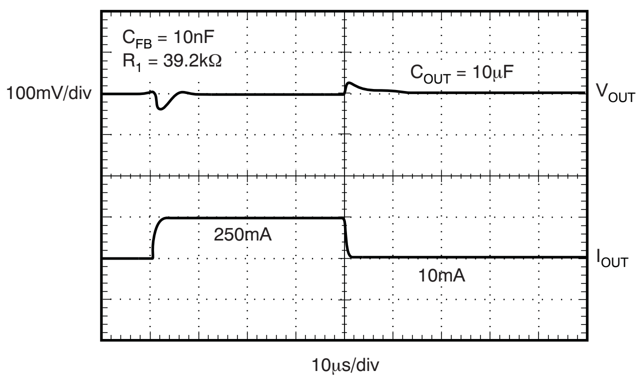


Figure 29.

TPS73701
LINE TRANSIENT, ADJUSTABLE VERSION

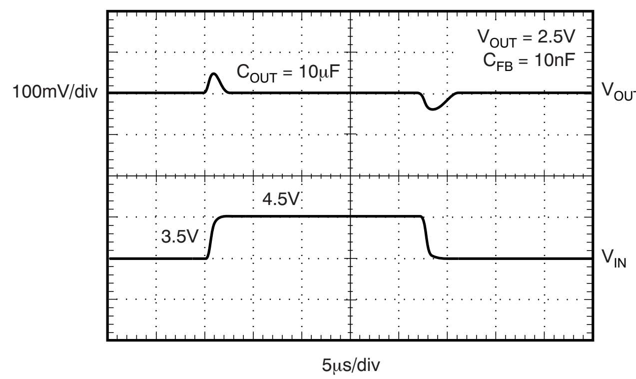


Figure 30.

APPLICATION INFORMATION

The TPS737xx belongs to a family of new generation LDO regulators that use an NMOS pass transistor to achieve ultra-low-dropout performance, reverse current blockage, and freedom from output capacitor constraints. These features combined with an enable input make the TPS737xx ideal for portable applications. This regulator family offers a wide selection of fixed output voltage versions and an adjustable output version. All versions have thermal and over-current protection, including foldback current limit.

Figure 31 shows the basic circuit connections for the fixed voltage models. Figure 32 gives the connections for the adjustable output version (TPS73701).

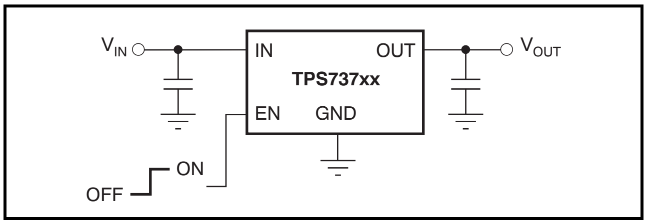


Figure 31. Typical Application Circuit for Fixed-Voltage Versions

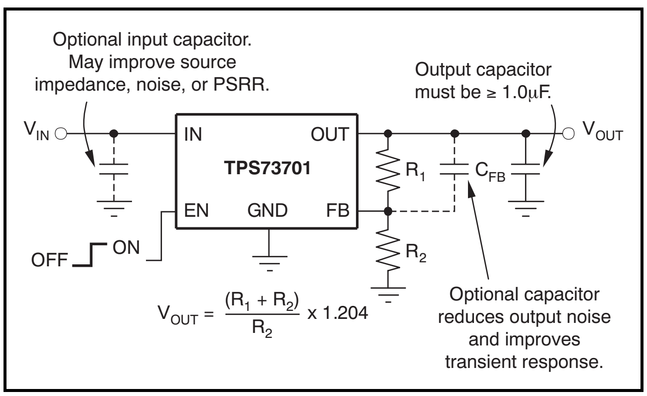


Figure 32. Typical Application Circuit for Adjustable-Voltage Version

R_1 and R_2 can be calculated for any output voltage using the formula shown in Figure 32. Sample resistor values for common output voltages are shown in Figure 2.

For best accuracy, make the parallel combination of R_1 and R_2 approximately equal to 19kΩ. This 19kΩ, in addition to the internal 8kΩ resistor, presents the same impedance to the error amp as the 27kΩ bandgap reference output. This impedance helps compensate for leakages into the error amp terminals.

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

Although an input capacitor is not required for stability if input impedance is very low, it is good analog design practice to connect a 0.1µF to 1µF low equivalent series resistance (ESR) capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source.

The TPS737xx requires a 1.0µF output capacitor for stability. It is designed to be stable for all available types and values of capacitors. In applications where multiple low ESR capacitors are in parallel, ringing may occur when the product of C_{OUT} and total ESR drops below 50nΩF. Total ESR includes all parasitic resistances, including capacitor ESR and board, socket, and solder joint resistance. In most applications, the sum of capacitor ESR and trace resistance will meet this requirement.

OUTPUT NOISE

A precision bandgap reference is used to generate the internal reference voltage, V_{REF}. This reference is the dominant noise source within the TPS737xx and it generates approximately $32\mu V_{RMS}$ (10Hz to 100kHz) at the reference output (NR). The regulator control loop gains up the reference noise with the same gain as the reference voltage, so that the noise voltage of the regulator is approximately given by:

$$V_N = 32\mu V_{RMS} \times \frac{(R_1 + R_2)}{R_2} = 32\mu V_{RMS} \times \frac{V_{OUT}}{V_{REF}} \quad (1)$$

Since the value of V_{REF} is 1.2V, this relationship reduces to:

$$V_N(\mu V_{RMS}) = 27\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}\,(V) \quad (2)$$

for the case of no C_{NR}.

An internal 27kΩ resistor in series with the noise reduction pin (NR) forms a low-pass filter for the voltage reference when an external noise reduction capacitor, C_{NR}, is connected from NR to ground. For C_{NR} = 10nF, the total noise in the 10Hz to 100kHz bandwidth is reduced by a factor of ~3.2, giving the approximate relationship:

$$V_N(\mu V_{RMS}) = 8.5 \left(\frac{\mu V_{RMS}}{V}\right) x\ V_{OUT}(V) \quad (3)$$

for C_{NR} = 10nF.

This noise reduction effect is shown as RMS Noise Voltage vs C_{NR} in the Typical Characteristics section.

The TPS73701 adjustable version does not have the NR pin available. However, connecting a feedback capacitor, C_{FB}, from the output to the feedback pin (FB) reduces output noise and improve load transient performance. This capacitor should be limited to 0.1µF.

The TPS737xx uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the NMOS pass element above V_{OUT}. The charge pump generates ~250µV of switching noise at ~4MHz; however, charge-pump noise contribution is negligible at the output of the regulator for most values of I_{OUT} and C_{OUT}.

BOARD LAYOUT RECOMMENDATION TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the printed circuit board (PCB) be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

INTERNAL CURRENT LIMIT

The TPS737xx internal current limit helps protect the regulator during fault conditions. Foldback current limit helps to protect the regulator from damage during output short-circuit conditions by reducing current limit when V_{OUT} drops below 0.5V. See Figure 12 in the Typical Characteristics section.

Note from Figure 12 that approximately –0.2V of V_{OUT} results in a current limit of 0mA. Therefore, if OUT is forced below –0.2V before EN goes high, the device may not start up. In applications that work with both a positive and negative voltage supply, the TPS737xx should be enabled first.

ENABLE PIN AND SHUTDOWN

The enable pin (EN) is active high and is compatible with standard TTL-CMOS levels. A V_{EN} below 0.5V (max) turns the regulator off and drops the GND pin current to approximately 10nA. When EN is used to shutdown the regulator, all charge is removed from the pass transistor gate, and the output ramps back up to a regulated V_{OUT} (see Figure 23).

When shutdown capability is not required, EN can be connected to V_{IN}. However, the pass gate may not be discharged using this configuration, and the pass transistor may be left on (enhanced) for a significant time after V_{IN} has been removed. This scenario can result in reverse current flow (if the IN pin is low impedance) and faster ramp times upon power-up. In addition, for V_{IN} ramp times slower than a few milliseconds, the output may overshoot upon power-up.

Note that current limit foldback can prevent device start-up under some conditions. See the *Internal Current Limit* section for more information.

DROPOUT VOLTAGE

The TPS737xx uses an NMOS pass transistor to achieve extremely low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the NMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DS,\ ON}$ of the NMOS pass element.

For large step changes in load current, the TPS737xx requires a larger voltage drop from V_{IN} to V_{OUT} to avoid degraded transient response. The boundary of this transient dropout region is approximately twice the dc dropout. Values of V_{IN} – V_{OUT} above this line ensure normal transient response.

Operating in the transient dropout region can cause an increase in recovery time. The time required to recover from a load transient is a function of the magnitude of the change in load current rate, the rate of change in load current, and the available headroom (V_{IN} to V_{OUT} voltage drop). Under worst-case conditions [full-scale instantaneous load change with (V_{IN} – V_{OUT}) close to dc dropout levels], the TPS737xx can take a couple of hundred microseconds to return to the specified regulation accuracy.

TRANSIENT RESPONSE

The low open-loop output impedance provided by the NMOS pass element in a voltage follower configuration allows operation without a 1.0μF output capacitor. As with any regulator, the addition of additional capacitance from the OUT pin to ground reduces undershoot magnitude but increases its duration. In the adjustable version, the addition of a capacitor, C_{FB}, from the OUT pin to the FB pin will also improve the transient response.

The TPS737xx does not have active pull-down when the output is over-voltage. This architecture allows applications that connect higher voltage sources, such as alternate power supplies, to the output. This architecture also results in an output overshoot of several percent if the load current quickly drops to zero when a capacitor is connected to the output. The duration of overshoot can be reduced by adding a load resistor. The overshoot decays at a rate determined by output capacitor C_{OUT} and the internal/external load resistance. The rate of decay is given by:

(Fixed voltage version)

$$\frac{dV}{dT} = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \parallel R_{LOAD}} \quad (4)$$

(Adjustable voltage version)

$$\frac{dV}{dT} = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \parallel (R_1 + R_2) \parallel R_{LOAD}} \quad (5)$$

REVERSE CURRENT

The NMOS pass element of the TPS737xx provides inherent protection against current flow from the output of the regulator to the input when the gate of the pass device is pulled low. To ensure that all charge is removed from the gate of the pass element, the EN pin must be driven low before the input voltage is removed. If this is not done, the pass element may be left on because of stored charge on the gate.

After the EN pin is driven low, no bias voltage is needed on any pin for reverse current blocking. Note that reverse current is specified as the current flowing out of the IN pin because of voltage applied on the OUT pin. There will be additional current flowing into the OUT pin as a result of the 80kΩ internal resistor divider to ground (see Figure 1 and Figure 2).

For the TPS73701, reverse current may flow when V_{FB} is more than 1.0V above V_{IN}.

THERMAL PROTECTION

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your application. This produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS737xx has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS737xx into thermal shutdown degrades device reliability.

POWER DISSIPATION

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the tab or pad is critical to avoiding thermal shutdown and ensuring reliable operation.

Power dissipation of the device depends on input voltage and load conditions and can be calculated using Equation 6:

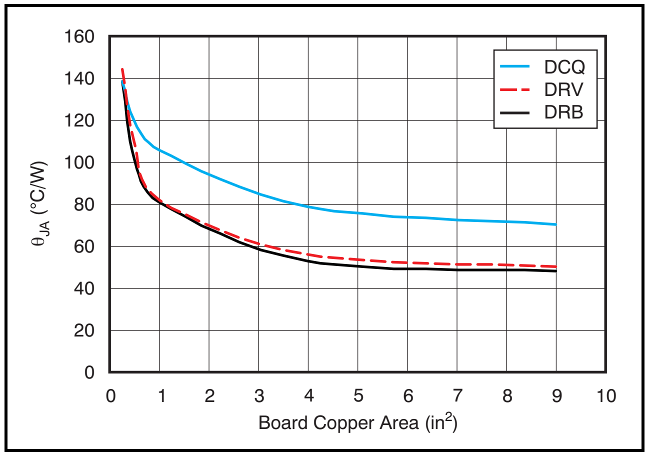
$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (6)$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On both SON (DRB) and SON (DRV) packages, the primary conduction path for heat is through the exposed pad to the printed circuit board (PCB). The pad can be connected to ground or be left floating; however, it should be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. On the SOT-223 (DCQ) package, the primary conduction path for heat is through the tab to the PCB. That tab should be connected to ground. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using Equation 7:

$$R_{\theta JA} = \frac{(+125^{o}C - T_A)}{P_D} \quad (7)$$

Knowing the maximum $R_{\theta JA}$, the minimum amount of PCB copper area needed for appropriate heatsinking can be estimated using Figure 33.



Note: θ_{JA} value at board size of 9in^2 (that is, 3in × 3in) is a JEDEC standard.

Figure 33. θ_{JA} vs Board Size

Figure 33 shows the variation of θ_{JA} as a function of ground plane copper area in the board. It is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and should not be used to estimate actual thermal performance in real application environments.

NOTE: When the device is mounted on an application PCB, it is strongly recommended to use Ψ_{JT} and Ψ_{JB}, as explained in the *Estimating Junction Temperature* section.

ESTIMATING JUNCTION TEMPERATURE

Using the thermal metrics Ψ_{JT} and Ψ_{JB}, as shown in the *Thermal Information* table, the junction temperature can be estimated with corresponding formulas (given in Equation 8). For backwards compatibility, an older θ_{JC},*Top* parameter is listed as well.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$

$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \qquad (8)$$

Where P_D is the power dissipation shown by Equation 6, T_T is the temperature at the center-top of the IC package, and T_B is the PCB temperature measured 1mm away from the IC package *on the PCB surface* (as Figure 35 shows).

NOTE: Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the application note SBVA025, *Using New Thermal Metrics*, available for download at www.ti.com.

By looking at Figure 34, the new thermal metrics (Ψ_{JT} and Ψ_{JB}) have very little dependency on board size. That is, using Ψ_{JT} or Ψ_{JB} with Equation 8 is a good way to estimate T_J by simply measuring T_T or T_B, regardless of the application board size.

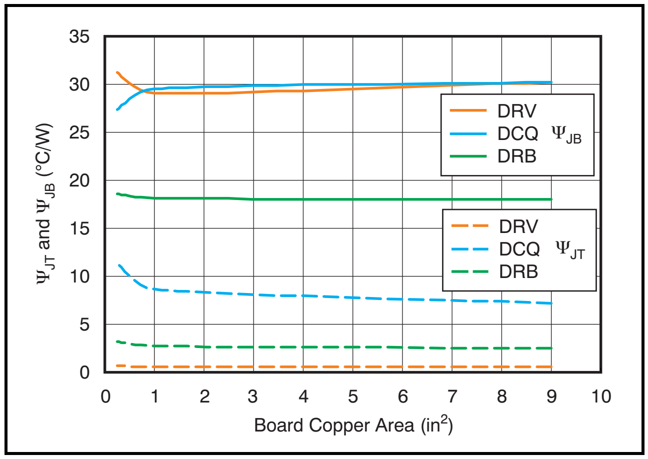
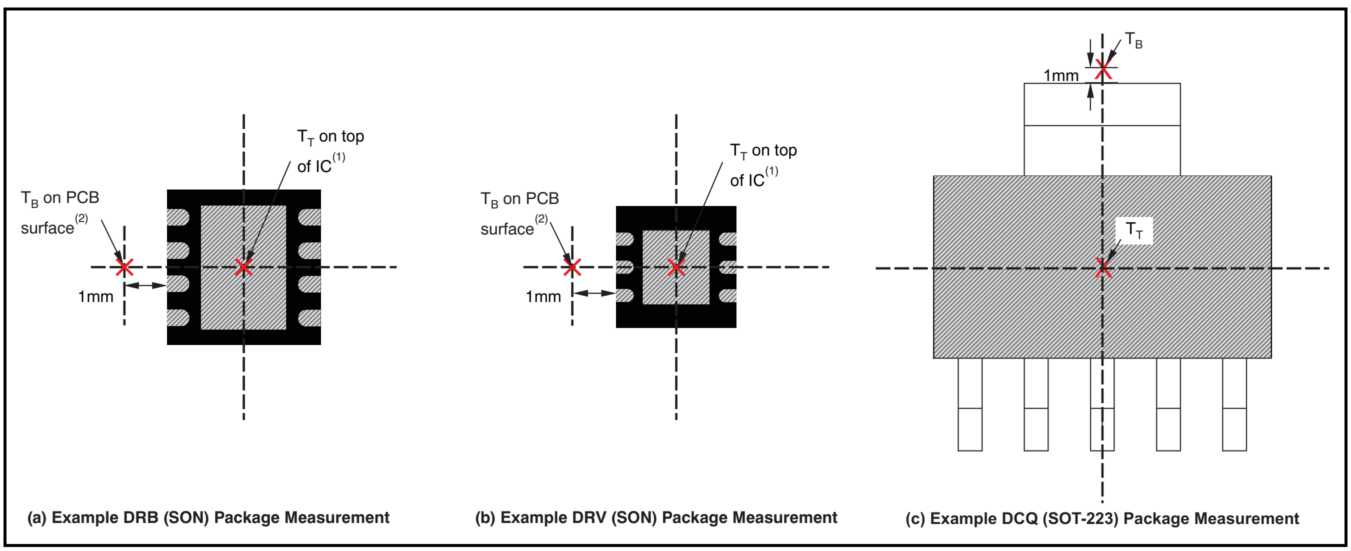


Figure 34. Ψ_{JT} and Ψ_{JB} vs Board Size

For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, refer to application report SBVA025, *Using New Thermal Metrics*, available for download at www.ti.com. For further information, refer to application report SPRA953, *IC Package Thermal Metrics*, also available on the TI website.



(1) T_T is measured at the center of both the X- and Y-dimensional axes.

(2) T_B is measured ***below*** the package lead on the PCB surface.

Figure 35. Measuring Points for T_T and T_B

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision K (April, 2010) to Revision L	Page
• Replaced the *Dissipation Ratings* table with the *Thermal Information* table	4
• Corrected y-axis value in Figure 12	8
• Revised *Power Dissipation* section; deleted *Package Mounting* section	15
• Added *Estimating Junction Temperature* section	16

Changes from Revision J (August, 2009) to Revision K	Page
• Added DRV package option and footnote (1) to front-page drawing	1
• Added DRV package pinout drawing and pin information to Pin Configurations	6

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS73701DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS73701DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS73701DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS73701DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS73701DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS73701DRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS73701DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS73701DRBTG4	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS73701DRVR	PREVIEW	SON	DRV	6	3000	TBD	Call TI	Call TI	
TPS73701DRVT	PREVIEW	SON	DRV	6	250	TBD	Call TI	Call TI	
TPS73718DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS73718DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS73718DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS73718DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS73725DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS73725DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS73725DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS73725DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS73730DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS73730DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS73733DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS73733DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS73733DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS73733DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS73734DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS73734DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS73733 :

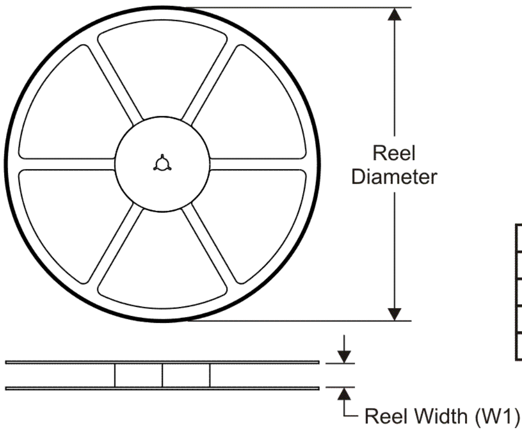
- Automotive: TPS73733-Q1

NOTE: Qualified Version Definitions:

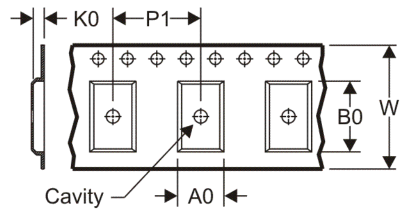
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

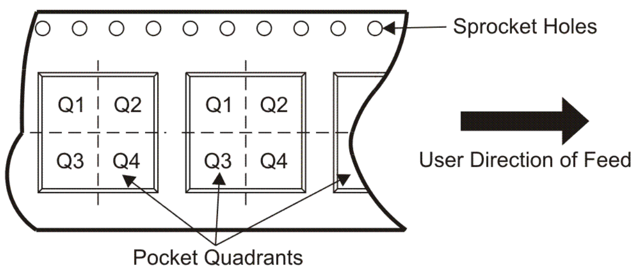


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

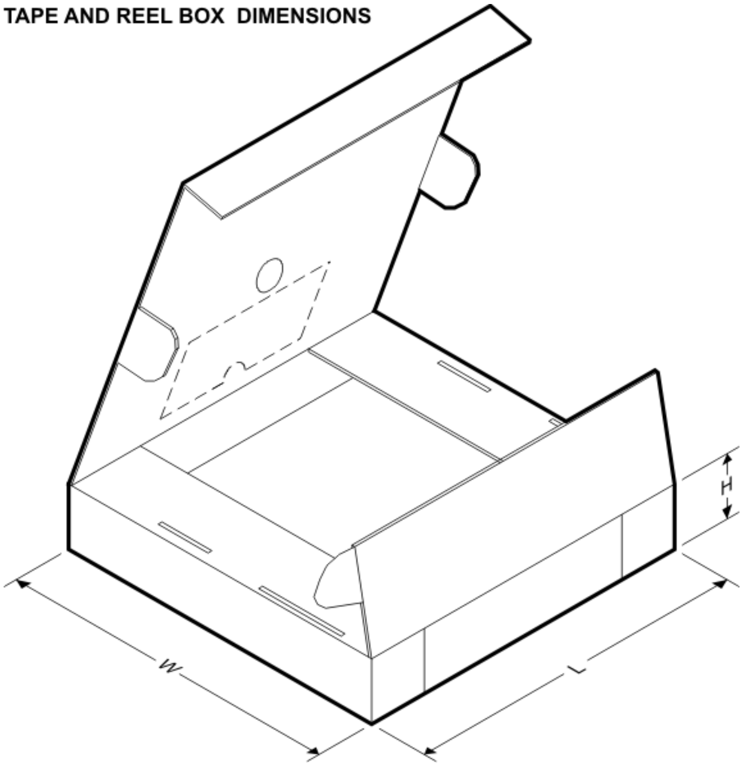
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73701DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.8	7.3	1.88	8.0	12.0	Q3
TPS73701DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73701DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73718DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.8	7.3	1.88	8.0	12.0	Q3
TPS73725DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.8	7.3	1.88	8.0	12.0	Q3
TPS73730DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73730DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73733DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.8	7.3	1.88	8.0	12.0	Q3
TPS73734DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.8	7.3	1.88	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73701DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS73701DRBR	SON	DRB	8	3000	346.0	346.0	29.0
TPS73701DRBT	SON	DRB	8	250	190.5	212.7	31.8
TPS73718DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS73725DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS73730DRBR	SON	DRB	8	3000	346.0	346.0	29.0
TPS73730DRBT	SON	DRB	8	250	190.5	212.7	31.8
TPS73733DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS73734DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0