



Cap-Free, NMOS, 400mA Low-Dropout Regulator with Reverse Current Protection

FEATURES

- Stable with No Output Capacitor or Any Value or Type of Capacitor
- Input Voltage Range of 1.7V to 5.5V
- Ultra-Low Dropout Voltage: 75mV typ
- Excellent Load Transient Response—with or without Optional Output Capacitor
- New NMOS Topology Delivers Low Reverse Leakage Current
- Low Noise: 30 μ V_{RMS} typ (10Hz to 100kHz)
- 0.5% Initial Accuracy
- 1% Overall Accuracy Over Line, Load, and Temperature
- Less Than 1 μ A max I_Q in Shutdown Mode
- Thermal Shutdown and Specified Min/Max Current Limit Protection
- Available in Multiple Output Voltage Versions
 - Fixed Outputs of 1.2V, 1.5V, 1.8V, 2.5V, 3.0V, 3.2V, 3.3V and 4.3V
 - Adjustable Output from 1.20V to 5.5V
 - Custom Outputs Available

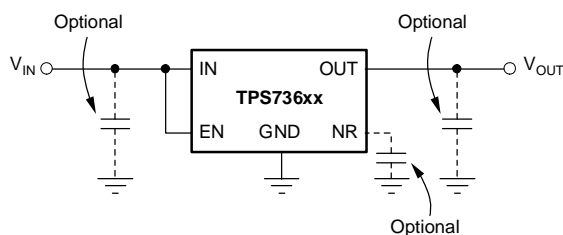
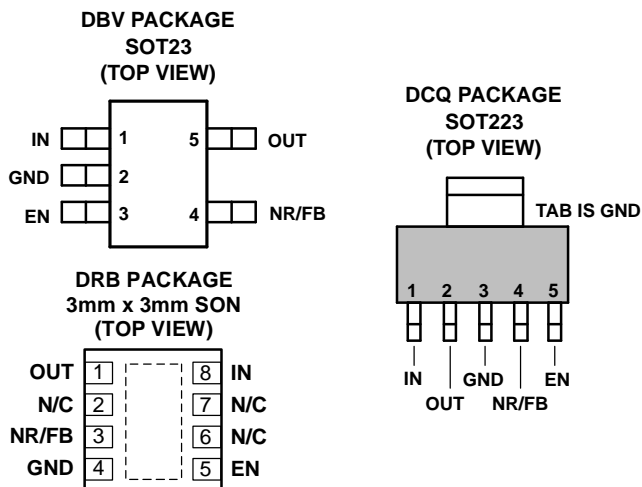
APPLICATIONS

- Portable/Battery-Powered Equipment
- Post-Regulation for Switching Supplies
- Noise-Sensitive Circuitry such as VCOs
- Point of Load Regulation for DSPs, FPGAs, ASICs, and Microprocessors

DESCRIPTION

The TPS736xx family of low-dropout (LDO) linear voltage regulators uses a new topology: an NMOS pass element in a voltage-follower configuration. This topology is stable using output capacitors with low ESR, and even allows operation without a capacitor. It also provides high reverse blockage (low reverse current) and ground pin current that is nearly constant over all values of output current.

The TPS736xx uses an advanced BiCMOS process to yield high precision while delivering very low dropout voltages and low ground pin current. Current consumption, when not enabled, is under 1 μ A and ideal for portable applications. The extremely low output noise (30 μ V_{RMS} with 0.1 μ F C_{NR}) is ideal for powering VCOs. These devices are protected by thermal shutdown and foldback current limit.



Typical Application Circuit for Fixed Voltage Versions



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION⁽¹⁾

PRODUCT	V _{OUT} ⁽²⁾	PACKAGE-LEAD (DESIGNATOR) ⁽³⁾	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TPS73601	Adjustable or 1.2V ⁽⁴⁾	SOT23-5 (DBV)	-40°C to +125°C	PJFQ	TPS73601DBVT	Tape and Reel, 250
					TPS73601DBVR	Tape and Reel, 3000
		SOT223-5 (DCQ)	-40°C to +125°C	PS73601	TPS73601DCQ	Tube, 78
					TPS73601DCQR	Tape and Reel, 2500
		3mm x 3mm SON (DRB) ⁽⁵⁾	-40°C to +125°C	PJFQ	TPS73601DRBT	Tape and Reel, 250
					TPS73601DRBR	Tape and Reel, 3000
TPS73615	1.5V	SOT23-5 (DBV)	-40°C to +125°C	T44	TPS73615DBVT	Tape and Reel, 250
					TPS73615DBVR	Tape and Reel, 3000
		SOT223-5 (DCQ)	-40°C to +125°C	PS73615	TPS73615DCQ	Tube, 78
					TPS73615DCQR	Tape and Reel, 2500
TPS73618	1.8V	SOT23-5 (DBV)	-40°C to +125°C	T43	TPS73618DBVT	Tape and Reel, 250
					TPS73618DBVR	Tape and Reel, 3000
		SOT223-5 (DCQ)	-40°C to +125°C	PS73618	TPS73618DCQ	Tube, 78
					TPS73618DCQR	Tape and Reel, 2500
TPS73625	2.5V	SOT23-5 (DBV)	-40°C to +125°C	T42	TPS73625DBVT	Tape and Reel, 250
					TPS73625DBVR	Tape and Reel, 3000
		SOT223-5 (DCQ)	-40°C to +125°C	PS73625	TPS73625DCQ	Tube, 78
					TPS73625DCQR	Tape and Reel, 2500
TPS73630	3.0V	SOT23-5 (DBV)	-40°C to +125°C	T45	TPS73630DBVT	Tape and Reel, 250
					TPS73630DBVR	Tape and Reel, 3000
		SOT223-5 (DCQ)	-40°C to +125°C	PS73630	TPS73630DCQ	Tube, 78
					TPS73630DCQR	Tape and Reel, 2500
TPS73632 ⁽⁶⁾	3.2V	SOT23-5 (DBV)	-40°C to +125°C	T53	TPS73632DBVT	Tape and Reel, 250
					TPS73632DBVR	Tape and Reel, 3000
TPS73633	3.3V	SOT23-5 (DBV)	-40°C to +125°C	T46	TPS73633DBVT	Tape and Reel, 250
					TPS73633DBVR	Tape and Reel, 3000
		SOT223-5 (DCQ)	-40°C to +125°C	PS73633	TPS73633DCQ	Tube, 78
					TPS73633DCQR	Tape and Reel, 2500
		3mm x 3mm SON (DRB) ⁽⁵⁾	-40°C to +125°C	T46	TPS73633DRBT	Tape and Reel, 250
TPS73633DRBR	Tape and Reel, 2500					
TPS73643 ⁽⁶⁾	4.3V	SOT23-5 (DBV)	-40°C to +125°C	T51	TPS73643DBVT	Tape and Reel, 250
					TPS73643DBVR	Tape and Reel, 3000

- (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.
- (2) Custom output voltages from 1.3V to 4V in 100mV increments are available on a quick-turn basis for prototyping. Minimum order quantities apply; contact factory for details and availability.
- (3) For the most current specification and package information, refer to our web site at www.ti.com.
- (4) For fixed 1.2V operation, tie FB to OUT.
- (5) Available August 2004.
- (6) Available Q3 2004



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾

	TPS736xx	UNIT
V _{IN} range	-0.3 to 6.0	V
V _{EN} range	-0.3 to 6.0	V
V _{OUT} range	-0.3 to 5.5	V
Peak output current	Internally limited	
Output short-circuit duration	Indefinite	
Continuous total power dissipation	See Dissipation Ratings Table	
Junction temperature range, T _J	-55 to +150	°C
Storage temperature range	-65 to +150	°C
ESD rating, HBM	2	kV
ESD rating, CDM	500	V

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the Electrical Characteristics is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

POWER DISSIPATION RATINGS⁽¹⁾

BOARD	PACKAGE	R _{θJC}	R _{θJA}	DERATING FACTOR ABOVE T _A = 25°C	T _A ≤ 25°C POWER RATING	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
Low-K ⁽²⁾	DBV	64°C/W	255°C/W	3.9mW/°C	390mW	215mW	155mW
High-K ⁽³⁾	DBV	64°C/W	180°C/W	5.6mW/°C	560mW	310mW	225mW
Low-K ⁽²⁾	DCQ	15°C/W	53°C/W	18.9mW/°C	1.89W	1.04W	0.76W
High-K ⁽³⁾⁽⁴⁾	DRB	1.2°C/W	40°C/W	25.0mW/°C	2.50W	1.38W	1.0W

- (1) See *Power Dissipation* in the **Applications** section for more information related to thermal design.
 (2) The JEDEC Low-K (1s) board design used to derive this data was a 3inch x 3inch, 2-layer board with 2-ounce copper traces on top of the board.
 (3) The JEDEC High-K (2s2p) board design used to derive this data was a 3inch x 3inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on the top and bottom of the board.
 (4) Based on preliminary thermal simulations.

ELECTRICAL CHARACTERISTICS

Over operating temperature range ($T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$), $V_{IN} = V_{OUT(nom)} + 0.5\text{V}^{(1)}$, $I_{OUT} = 10\text{mA}$, $V_{EN} = 1.7\text{V}$, and $C_{OUT} = 0.1\mu\text{F}$, unless otherwise noted. Typical values are at $T_J = 25^{\circ}\text{C}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range ⁽¹⁾		1.7		5.5	V
V_{FB}	Internal reference (TPS73601)	$T_J = 25^{\circ}\text{C}$	1.198	1.20	1.210	V
V_{OUT}	Output voltage range (TPS73601)		V_{FB}		$5.5 - V_{DO}$	V
	Accuracy ⁽¹⁾	Nominal	$T_J = 25^{\circ}\text{C}$	-0.5		+0.5
over V_{IN} , I_{OUT} , and T		$V_{OUT} + 0.5\text{V} \leq V_{IN} \leq 5.5\text{V}$; $10\text{mA} \leq I_{OUT} \leq 400\text{mA}$	-1.0	± 0.5	+1.0	
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation ⁽¹⁾	$V_{O(nom)} + 0.5\text{V} \leq V_{IN} \leq 5.5\text{V}$		0.01		%/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	$1\text{mA} \leq I_{OUT} \leq 400\text{mA}$		0.002		%/mA
		$10\text{mA} \leq I_{OUT} \leq 400\text{mA}$		0.0005		
V_{DO}	Dropout voltage ⁽²⁾ ($V_{IN} = V_{OUT(nom)} - 0.1\text{V}$)	$I_{OUT} = 400\text{mA}$		75	200	mV
$Z_O(\text{DO})$	Output impedance in dropout	$1.7\text{V} \leq V_{IN} \leq V_{OUT} + V_{DO}$		0.25		Ω
I_{CL}	Output current limit	$V_{OUT} = 0.9 \times V_{OUT(nom)}$	400	650	800	mA
		$3.6\text{V} \leq V_{IN} \leq 4.2\text{V}$, $0^{\circ}\text{C} \leq T_J \leq 70^{\circ}\text{C}$	500		800	
I_{SC}	Short-circuit current	$V_{OUT} = 0\text{V}$		450		mA
I_{REV}	Reverse leakage current ⁽³⁾ ($-I_{IN}$)	$V_{EN} \leq 0.5\text{V}$, $0\text{V} \leq V_{IN} \leq V_{OUT}$		0.1	10	μA
I_{GND}	Ground pin current	$I_{OUT} = 10\text{mA}$ (I_Q)		300	550	μA
		$I_{OUT} = 400\text{mA}$		750	1000	
I_{SHDN}	Shutdown current (I_{GND})	$V_{EN} \leq 0.5\text{V}$, $V_{OUT} \leq V_{IN} \leq 5.5$		0.02	1	μA
I_{FB}	FB pin current (TPS73601)			0.1	0.3	μA
PSRR	Power-supply rejection ratio (ripple rejection)	$f = 100\text{Hz}$, $I_{OUT} = 400\text{mA}$		58		dB
		$f = 10\text{KHz}$, $I_{OUT} = 400\text{mA}$		37		
V_N	Output noise voltage BW = 10Hz - 100KHz	$C_{OUT} = 10\mu\text{F}$, No C_{NR}		$27 \times V_{OUT}$		μV_{RMS}
		$C_{OUT} = 10\mu\text{F}$, $C_{NR} = 0.01\mu\text{F}$		$8.5 \times V_{OUT}$		
t_{STR}	Startup time	$V_{OUT} = 3\text{V}$, $R_L = 30\Omega$, $C_{OUT} = 1\mu\text{F}$, $C_{NR} = 0.01\mu\text{F}$		600		μs
$V_{EN}(\text{HI})$	Enable high (enabled)		1.7		V_{IN}	V
$V_{EN}(\text{LO})$	Enable low (shutdown)		0		0.5	V
$I_{EN}(\text{HI})$	Enable pin current (enabled)	$V_{EN} = 5.5\text{V}$		0.02	0.1	μA
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		160		$^{\circ}\text{C}$
		Reset, temperature decreasing		140		
T_J	Operating junction temperature		-40		125	$^{\circ}\text{C}$

(1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or 1.7V, whichever is greater.

(2) V_{DO} is not measured for the TPS73615 ($V_{OUT(nom)} = 1.5\text{V}$) since minimum $V_{IN} = 1.7\text{V}$.

(3) Refer to **Applications** section for more information.

FUNCTIONAL BLOCK DIAGRAMS

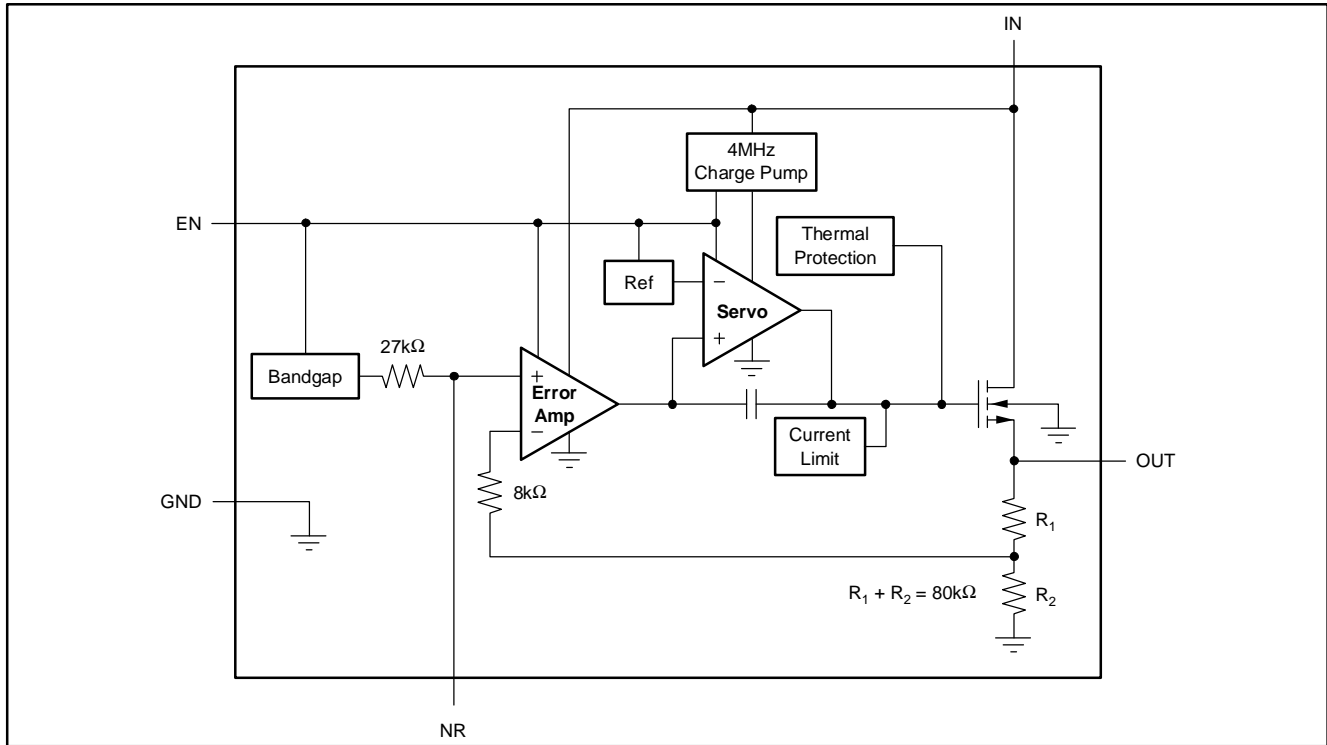


Figure 1. Fixed Voltage Version

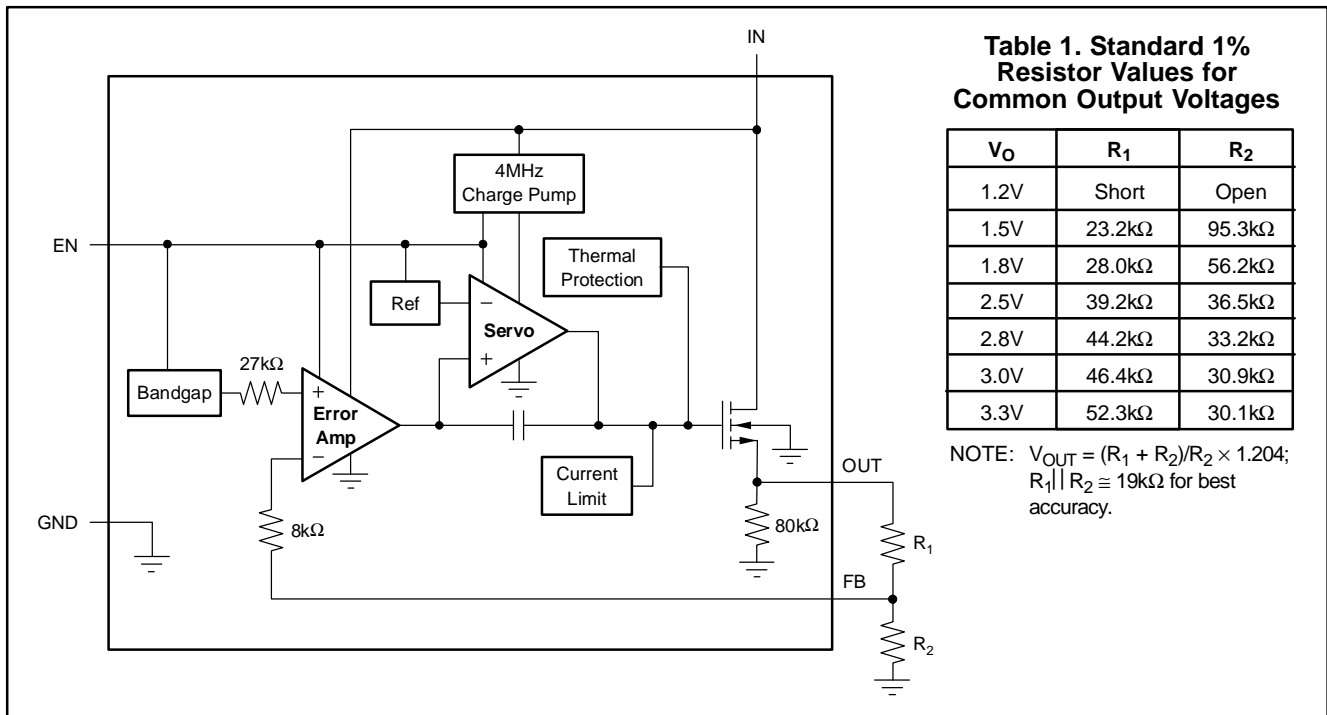


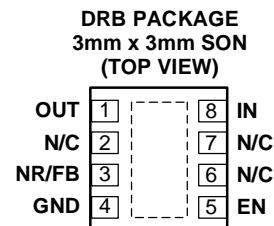
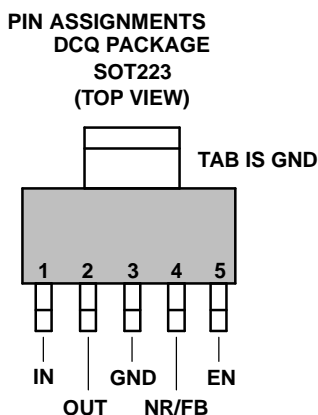
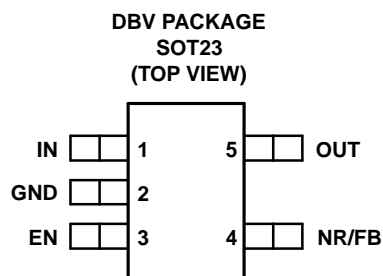
Table 1. Standard 1% Resistor Values for Common Output Voltages

V _O	R ₁	R ₂
1.2V	Short	Open
1.5V	23.2kΩ	95.3kΩ
1.8V	28.0kΩ	56.2kΩ
2.5V	39.2kΩ	36.5kΩ
2.8V	44.2kΩ	33.2kΩ
3.0V	46.4kΩ	30.9kΩ
3.3V	52.3kΩ	30.1kΩ

NOTE: $V_{OUT} = (R_1 + R_2)/R_2 \times 1.204$;
 $R_1 || R_2 \cong 19k\Omega$ for best accuracy.

Figure 2. Adjustable Voltage Version

FUNCTIONAL BLOCK DIAGRAMS (continued)



Terminal Functions

NAME	SOT23 (DBV) PIN NO.	SOT223 (DCQ) PIN NO.	3x3 SON (DRB) PIN NO.	DESCRIPTION
IN	1	1	8	Unregulated input supply
GND	2	3	4, Pad	Ground
EN	3	5	5	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. Refer to the Shutdown section under Applications Information for more details. EN can be connected to IN if not used.
NR	4	4	3	Fixed voltage versions only—connecting an external capacitor to this pin bypasses noise generated by the internal bandgap. This allows output noise to be reduced to very low levels.
FB	4	4	3	Adjustable voltage version only—this is the input to the control loop error amplifier, and is used to set the output voltage of the device.
OUT	5	2	1	Output of the Regulator. There are no output capacitor requirements for stability.

TYPICAL CHARACTERISTICS

For all voltage versions, at $T_J = +25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{V}$, $I_{OUT} = 10\text{mA}$, $V_{EN} = 1.7\text{V}$, and $C_{OUT} = 0.1\mu\text{F}$, unless otherwise noted.

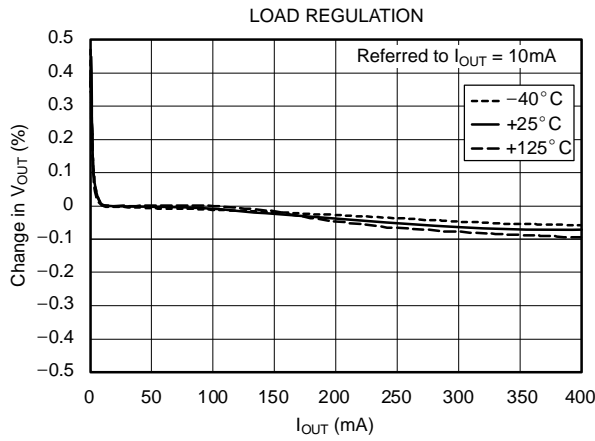


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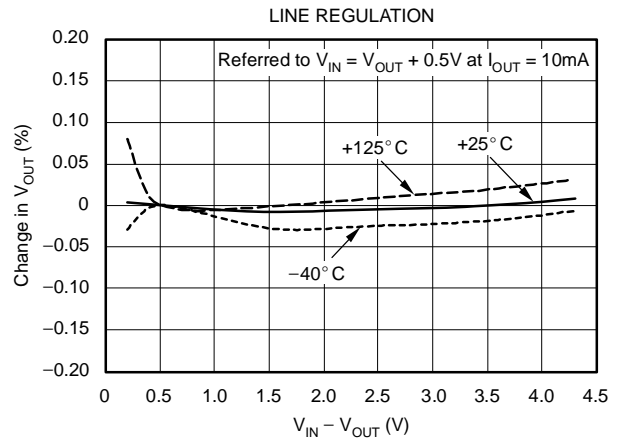


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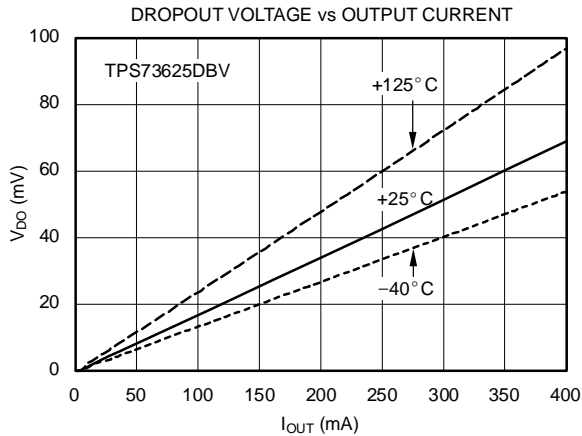


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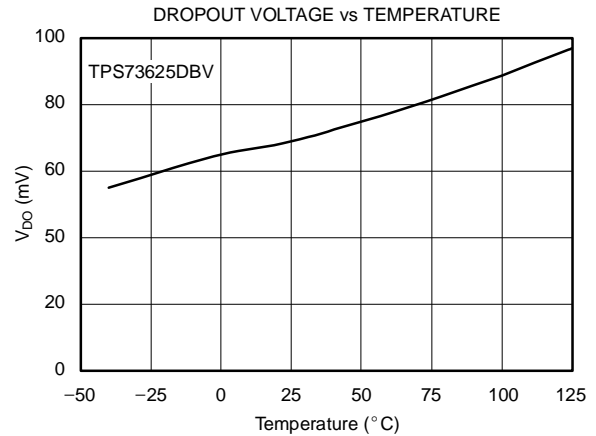


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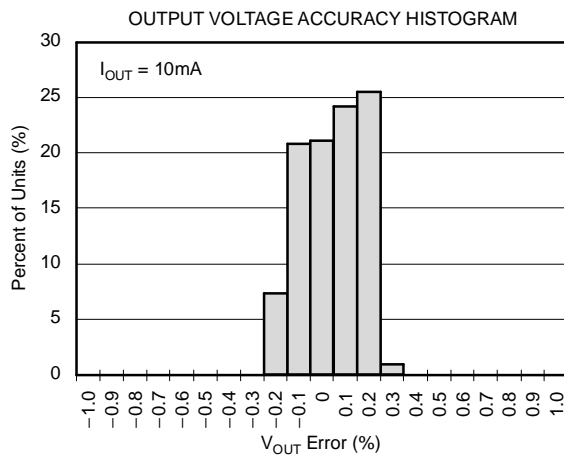


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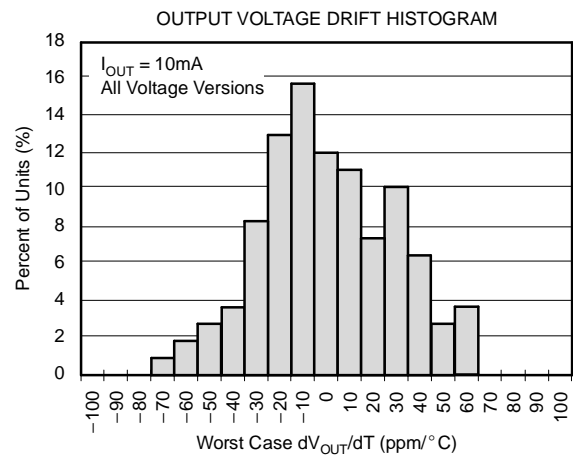


Figure 8.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions, at $T_J = +25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{V}$, $I_{OUT} = 10\text{mA}$, $V_{EN} = 1.7\text{V}$, and $C_{OUT} = 0.1\mu\text{F}$, unless otherwise noted.

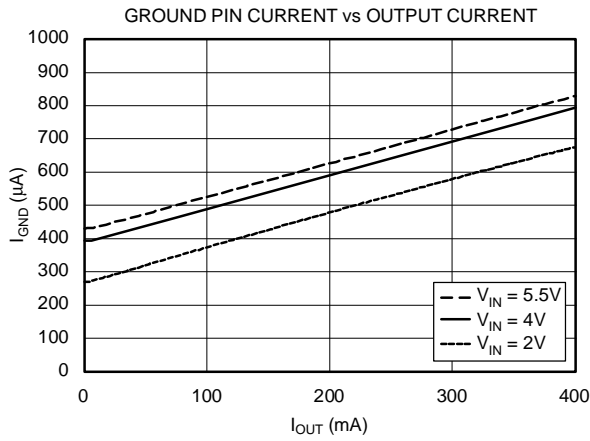


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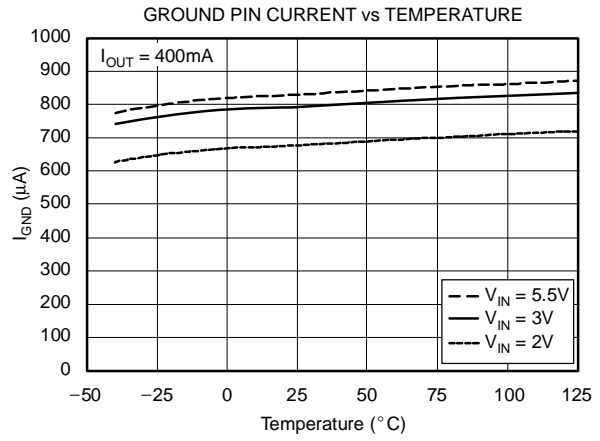


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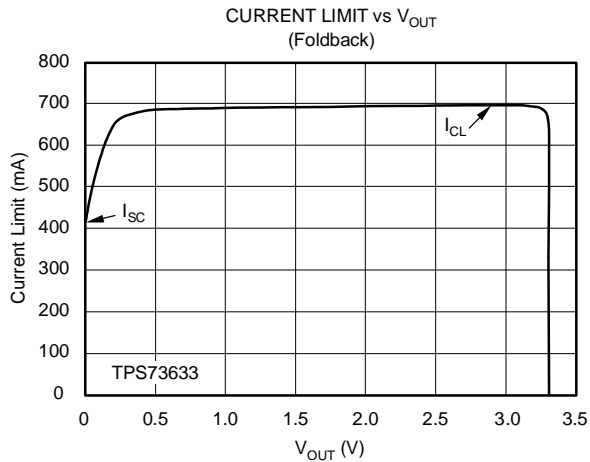


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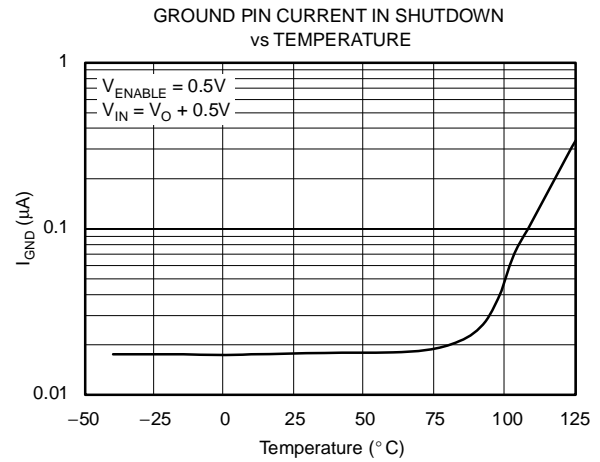


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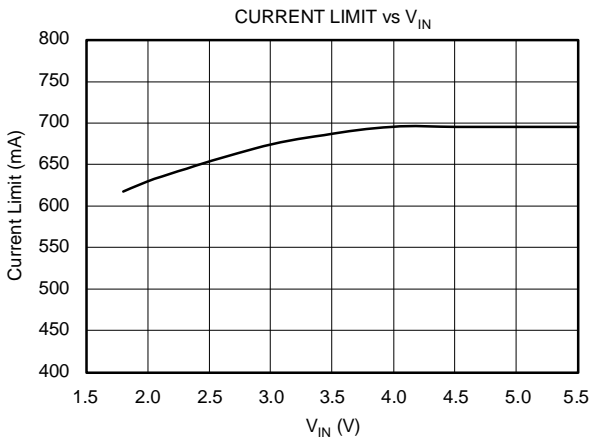


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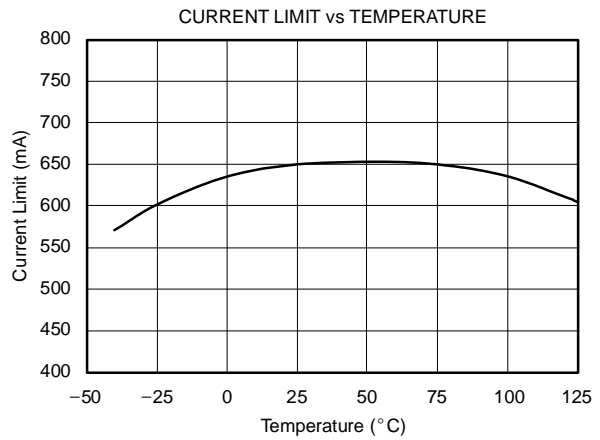


Figure 14.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions, at $T_J = +25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{V}$, $I_{OUT} = 10\text{mA}$, $V_{EN} = 1.7\text{V}$, and $C_{OUT} = 0.1\mu\text{F}$, unless otherwise noted.

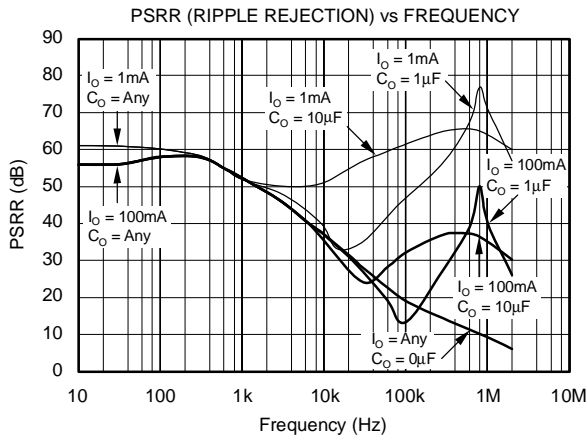


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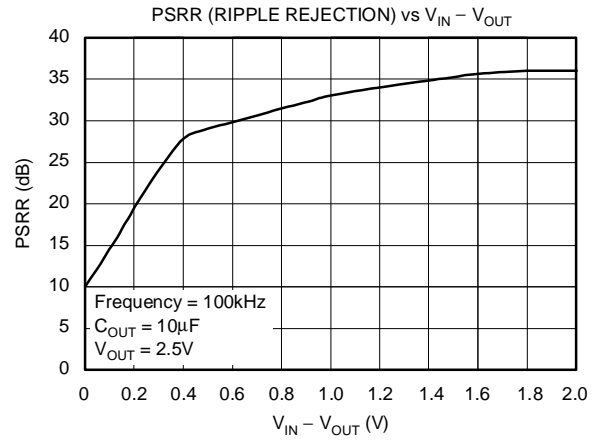


Figure 16.

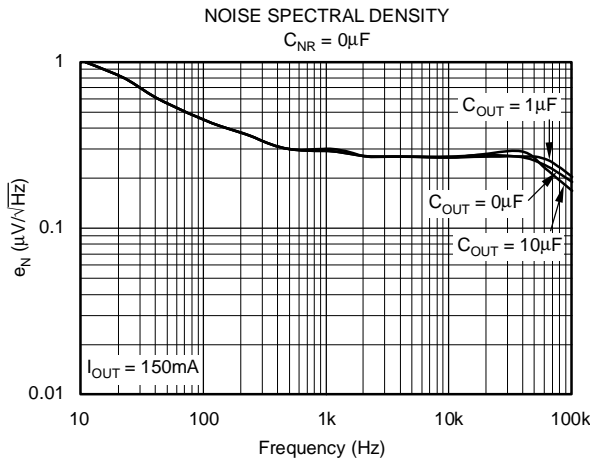


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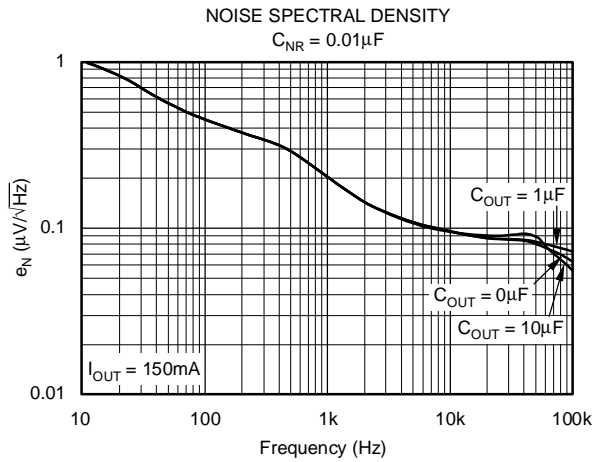


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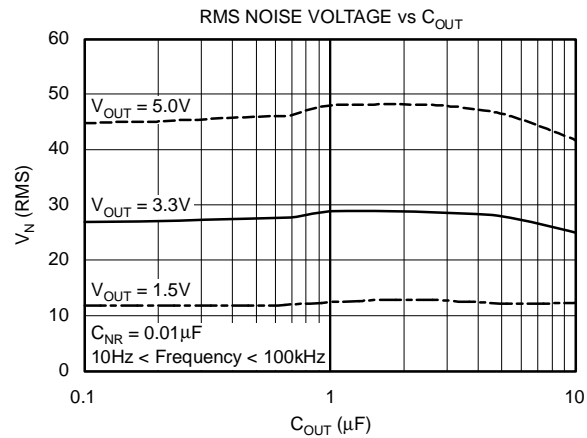


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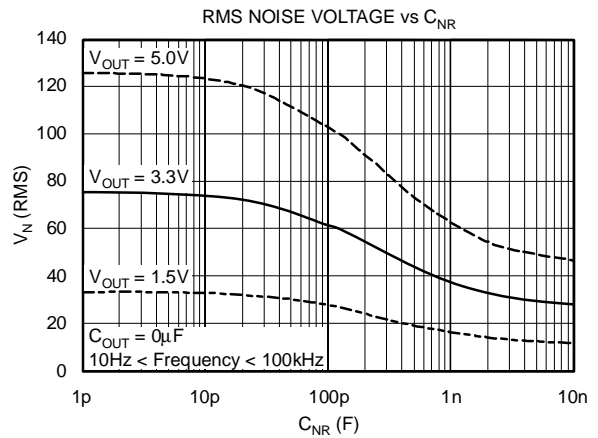


Figure 20.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions, at $T_J = +25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{V}$, $I_{OUT} = 10\text{mA}$, $V_{EN} = 1.7\text{V}$, and $C_{OUT} = 0.1\mu\text{F}$, unless otherwise noted.

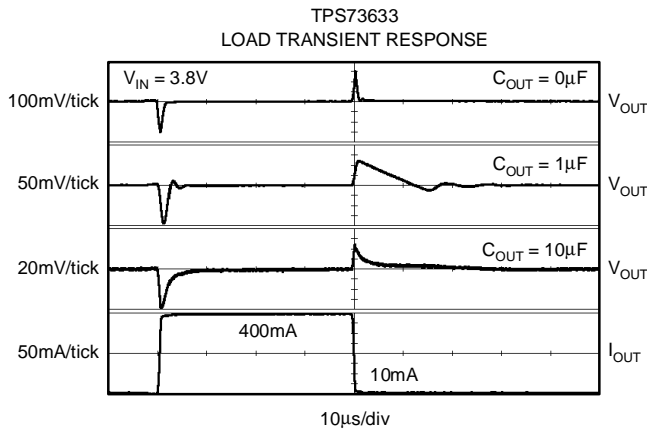


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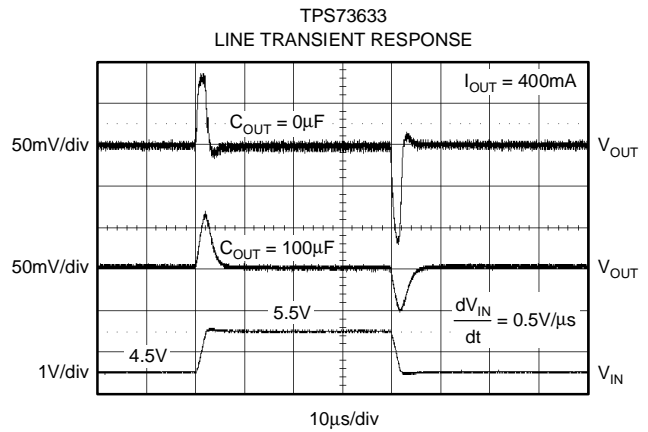


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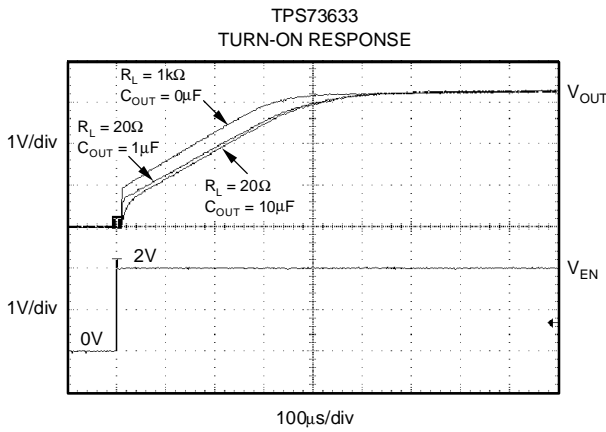


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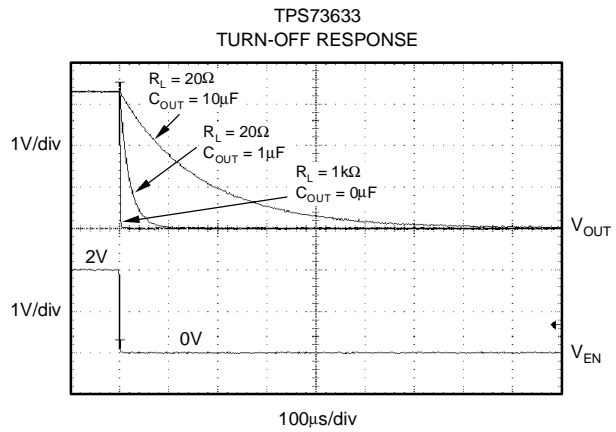


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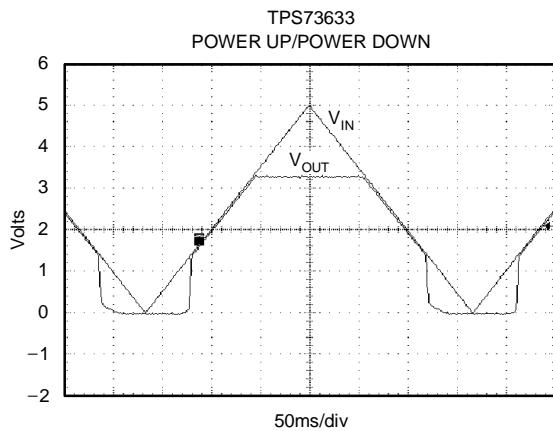


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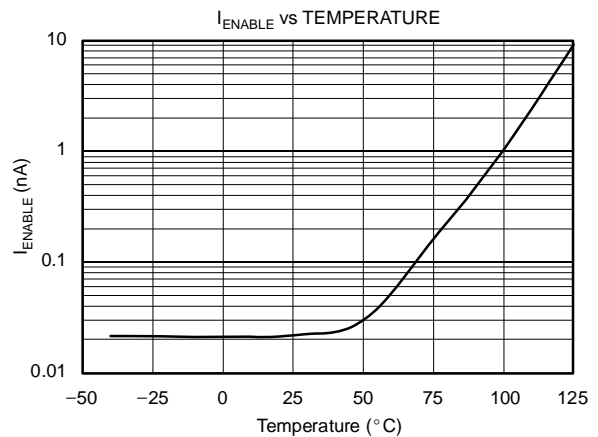


Figure 26.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions, at $T_J = +25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{V}$, $I_{OUT} = 10\text{mA}$, $V_{EN} = 1.7\text{V}$, and $C_{OUT} = 0.1\mu\text{F}$, unless otherwise noted.

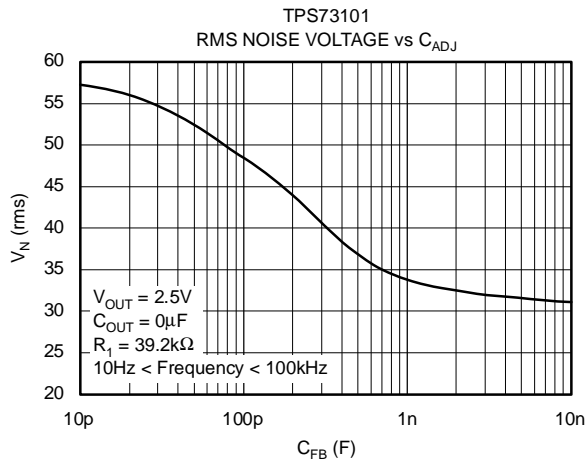


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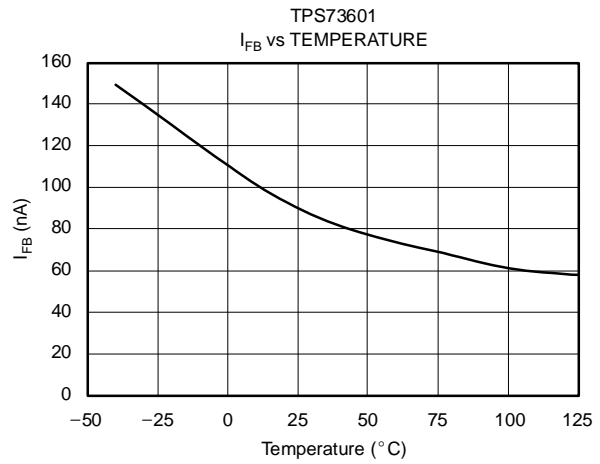


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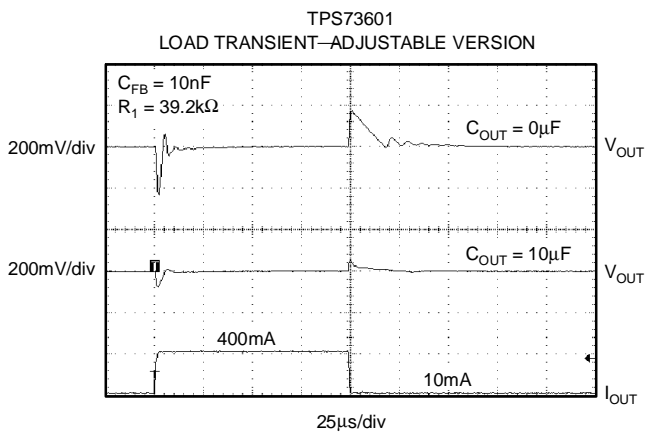


Figure 29.

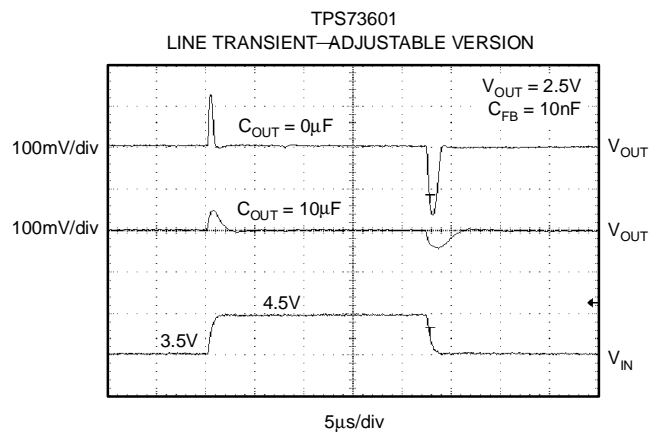


Figure 30.

APPLICATION INFORMATION

The TPS736xx belongs to a family of new generation LDO regulators that use an NMOS pass transistor to achieve ultra-low-dropout performance, reverse current blockage, and freedom from output capacitor constraints. These features, combined with low noise and an enable input, make the TPS736xx ideal for portable applications. This regulator family offers a wide selection of fixed output voltage versions and an adjustable output version. All versions have thermal and over-current protection, including foldback current limit.

Figure 31 shows the basic circuit connections for the fixed voltage models. Figure 32 gives the connections for the adjustable output version (TPS73601). R_1 and R_2 can be calculated for any output voltage using the formula in Figure 32. Sample resistor values for common output voltages are shown in Figure 2. For best accuracy, make the parallel combination of R_1 and R_2 approximately $19k\Omega$.

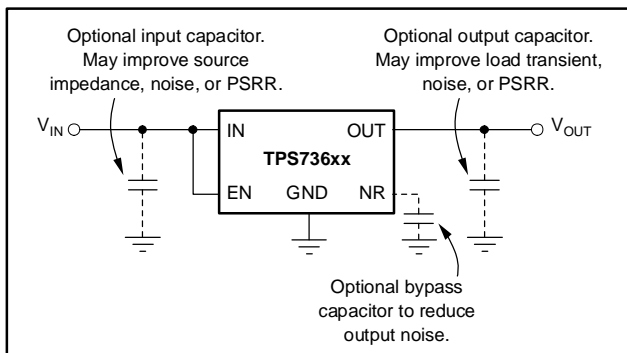


Figure 31. Typical Application Circuit for Fixed-Voltage Versions

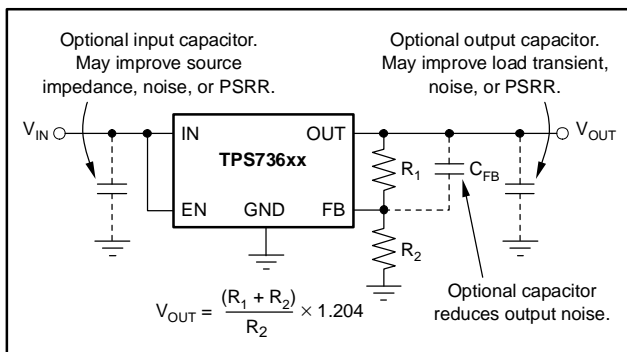


Figure 32. Typical Application Circuit for Fixed-Voltage Versions

Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, it is good analog design practice to connect a $0.1\mu\text{F}$ to $1\mu\text{F}$ low ESR capacitor across the input supply near the regulator. This will counteract reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source.

The TPS736xx does not require an output capacitor for stability and has maximum phase margin with no capacitor. It is designed to be stable for all available types and values of capacitors. In applications where $V_{\text{IN}} - V_{\text{OUT}} < 0.5\text{V}$ and multiple low ESR capacitors are in parallel, ringing may occur when the product of C_{OUT} and total ESR drops below $50\text{n}\Omega\text{F}$. Total ESR includes all parasitic resistances, including capacitor ESR and board, socket, and solder joint resistance. In most applications, the sum of capacitor ESR and trace resistance will meet this requirement.

Output Noise

A precision band-gap reference is used to generate the internal reference voltage, V_{REF} . This reference is the dominant noise source within the TPS736xx and it generates approximately $32\mu\text{V}_{\text{RMS}}$ (10Hz to 100kHz) at the reference output (NR). The regulator control loop gains up the reference noise with the same gain as the reference voltage, so that the noise voltage of the regulator is approximately given by:

$$V_{\text{N}} = 32\mu\text{V}_{\text{RMS}} \times \frac{(R_1 + R_2)}{R_2} = 32\mu\text{V}_{\text{RMS}} \times \frac{V_{\text{OUT}}}{V_{\text{REF}}} \quad (1)$$

Since the value of V_{REF} is 1.2V , this relationship reduces to:

$$V_{\text{N}}(\mu\text{V}_{\text{RMS}}) = 27 \left(\frac{\mu\text{V}_{\text{RMS}}}{\text{V}} \right) \times V_{\text{OUT}}(\text{V}) \quad (2)$$

for the case of no C_{NR} .

An internal $27k\Omega$ resistor in series with the noise reduction pin (NR) forms a low-pass filter for the voltage reference when an external noise reduction capacitor, C_{NR} , is connected from NR to ground. For $C_{\text{NR}} = 10\text{nF}$, the total noise in the 10Hz to 100kHz bandwidth is reduced by a factor of ~ 3.2 , giving the approximate relationship:

$$V_{\text{N}}(\mu\text{V}_{\text{RMS}}) = 8.5 \left(\frac{\mu\text{V}_{\text{RMS}}}{\text{V}} \right) \times V_{\text{OUT}}(\text{V}) \quad (3)$$

for $C_{\text{NR}} = 10\text{nF}$.

This noise reduction effect is shown as RMS Noise Voltage vs C_{NR} in the Typical Characteristics section.

The TPS73601 adjustable version does not have the noise-reduction pin available. However, connecting a feedback capacitor, C_{FB} , from the output to the FB pin will reduce output noise and improve load transient performance.

The TPS736xx uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the NMOS pass element above V_{OUT} . The charge pump generates $\sim 250\mu V$ of switching noise at $\sim 4\text{MHz}$; however, charge-pump noise contribution is negligible at the output of the regulator for most values of I_{OUT} and C_{OUT} .

Board Layout Recommendation to Improve PSRR and Noise Performance

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT} , with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

Internal Current Limit

The TPS736xx internal current limit helps protect the regulator during fault conditions. Foldback helps to protect the regulator from damage during output short-circuit conditions by reducing current limit when V_{OUT} drops below 0.5V. See Figure 11 in the Typical Characteristics section for a graph of I_{OUT} vs V_{OUT} .

Shutdown

The Enable pin is active high and is compatible with standard TTL-CMOS levels. V_{EN} below 0.5V (max) turns the regulator off and drops the ground pin current to approximately 10nA. When shutdown capability is not required, the Enable pin can be connected to V_{IN} . When a pull-up resistor is used, and operation down to 1.8V is required, use pull-up resistor values below 50k Ω .

Dropout Voltage

The TPS736xx uses an NMOS pass transistor to achieve extremely low dropout. When $(V_{IN} - V_{OUT})$ is less than the dropout voltage (V_{DO}), the NMOS pass device is in its linear region of operation and the input-to-output resistance is the R_{DS-ON} of the NMOS pass element.

For large step changes in load current, the TPS736xx requires a larger voltage drop from V_{IN} to V_{OUT} to avoid degraded transient response. The boundary of this transient dropout region is approximately twice the dc dropout. Values of $V_{IN} - V_{OUT}$ above this line insure normal transient response.

Operating in the transient dropout region can cause an increase in recovery time. The time required to recover from a load transient is a function of the magnitude of the change in load current rate, the rate of change in load current, and the available headroom (V_{IN} to V_{OUT} voltage drop). Under worst-case conditions [full-scale instantaneous load change with $(V_{IN} - V_{OUT})$ close to dc dropout levels], the TPS736xx can take a couple of hundred microseconds to return to the specified regulation accuracy.

Transient Response

The low open-loop output impedance provided by the NMOS pass element in a voltage follower configuration allows operation without an output capacitor for many applications. As with any regulator, the addition of a capacitor (nominal value 1 μF) from the output pin to ground will reduce undershoot magnitude but increase duration. In the adjustable version, the addition of a capacitor, C_{FB} , from the output to the adjust pin will also improve the transient response.

The TPS736xx does not have active pull-down when the output is over-voltage. This allows applications that connect higher voltage sources, such as alternate power supplies, to the output. This also results in an output overshoot of several percent if load current quickly drops to zero when a capacitor is connected to the output. The duration of overshoot can be reduced by adding a load resistor. The overshoot decays at a rate determined by output capacitor C_{OUT} and the internal/external load resistance. The rate of decay is given by:

(Fixed Voltage Version)

$$dV/dt = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega} \quad (4)$$

(Adjustable Voltage Version)

$$dV/dt = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \parallel (R_1 + R_2)} \quad (5)$$

Reverse Current

The NMOS pass element of the TPS736xx provides inherent protection against current flow from the output of the regulator to the input when the gate of the pass device is pulled low. To ensure that all charge is removed from the gate of the pass element, the enable pin must be driven low before the input voltage is removed. If this is not done, the pass element may be left on due to stored charge on the gate.

After the enable pin is driven low, no bias voltage is needed on any pin for reverse current blocking. Note that reverse current is specified as the current flowing out of the IN pin due to voltage applied on the OUT pin. There will be additional current flowing into the OUT pin due to the 80k Ω internal resistor divider to ground (see Figure 1 and Figure 2).

For the TPS73601, reverse current may flow when V_{FB} is more than 1.0V above V_{IN} .

Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This limits the dissipation of the regulator, protecting it from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of your application. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS736xx has been designed to protect against overload conditions. It was not intended to replace proper heat sinking. Continuously running the TPS736xx into thermal shutdown will degrade reliability.

Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low and high K boards are shown in the Power Dissipation Ratings table. Using heavier copper will increase the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers will also improve the heat-sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (6)$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to assure the required output voltage.

Package Mounting

Solder pad footprint recommendations for the TPS736xx are presented in Application Bulletin *Solder Pad Recommendations for Surface-Mount Devices* (AB-132), available from the Texas Instruments web site at www.ti.com.

PACKAGING INFORMATION

ORDERABLE DEVICE	STATUS(1)	PACKAGE TYPE	PACKAGE DRAWING	PINS	PACKAGE QTY
TPS73601DBVR	ACTIVE	SOP	DBV	5	3000
TPS73601DBVT	ACTIVE	SOP	DBV	5	250
TPS73601DCQ	ACTIVE	SOP	DCQ	6	78
TPS73601DCQR	ACTIVE	SOP	DCQ	6	2500
TPS73615DBVR	ACTIVE	SOP	DBV	5	3000
TPS73615DBVT	ACTIVE	SOP	DBV	5	250
TPS73615DCQ	ACTIVE	SOP	DCQ	6	78
TPS73615DCQR	ACTIVE	SOP	DCQ	6	2500
TPS73618DBVR	ACTIVE	SOP	DBV	5	3000
TPS73618DBVT	ACTIVE	SOP	DBV	5	250
TPS73618DCQ	ACTIVE	SOP	DCQ	6	78
TPS73618DCQR	ACTIVE	SOP	DCQ	6	3000
TPS73625DBVR	ACTIVE	SOP	DBV	5	3000
TPS73625DBVT	ACTIVE	SOP	DBV	5	250
TPS73625DCQ	ACTIVE	SOP	DCQ	6	78
TPS73625DCQR	ACTIVE	SOP	DCQ	6	2500
TPS73630DBVR	ACTIVE	SOP	DBV	5	3000
TPS73630DBVT	ACTIVE	SOP	DBV	5	250
TPS73630DCQ	ACTIVE	SOP	DCQ	6	78
TPS73630DCQR	ACTIVE	SOP	DCQ	6	2500
TPS73633DBVR	ACTIVE	SOP	DBV	5	3000
TPS73633DBVT	ACTIVE	SOP	DBV	5	250
TPS73633DCQ	ACTIVE	SOP	DCQ	6	78
TPS73633DCQR	ACTIVE	SOP	DCQ	6	2500
TPS73633DRBR	PREVIEW	SON	DRB	8	3000
TPS73633DRBT	PREVIEW	SON	DRB	8	1000

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

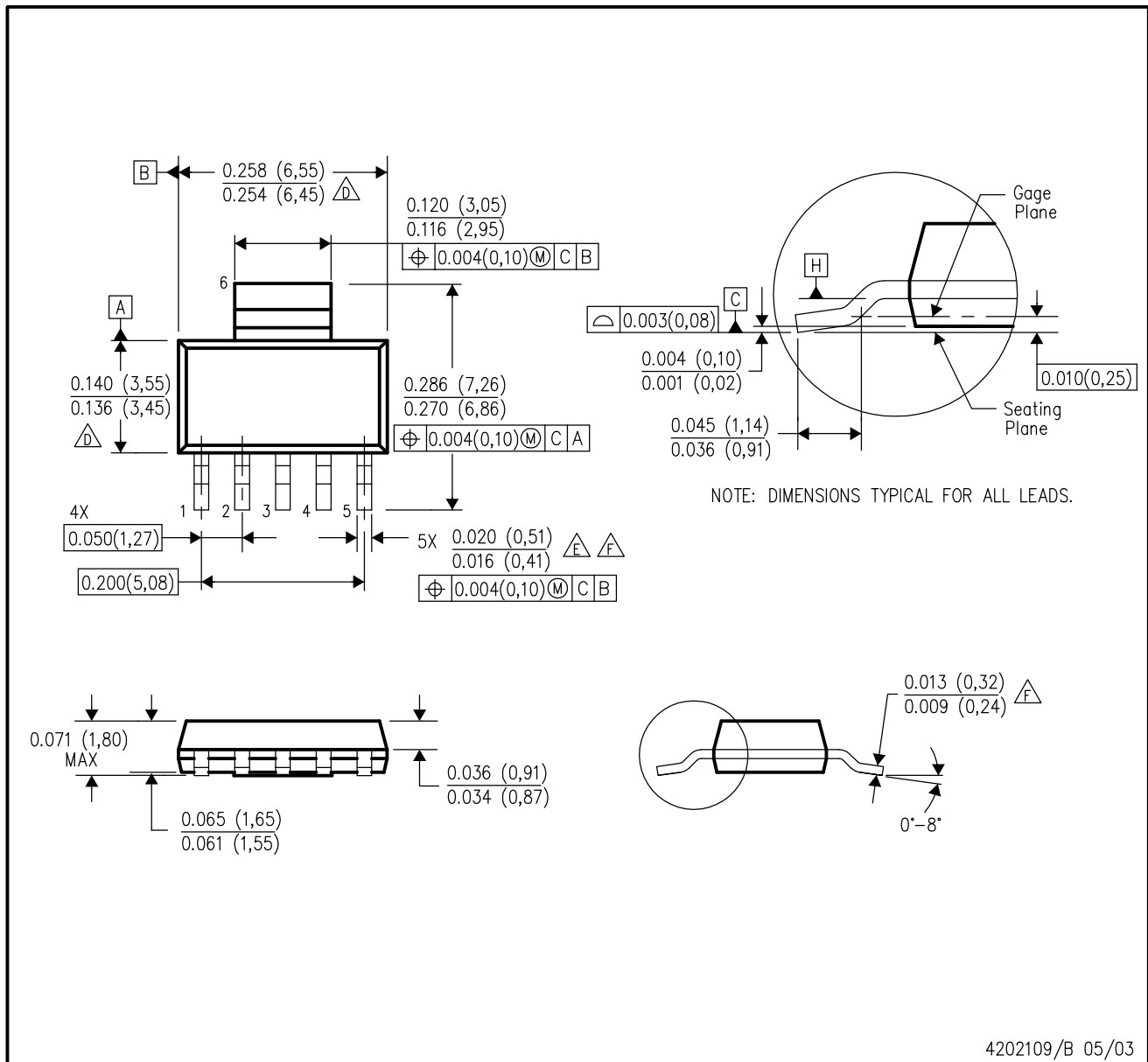
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

DCQ (R-PDSO-G6)

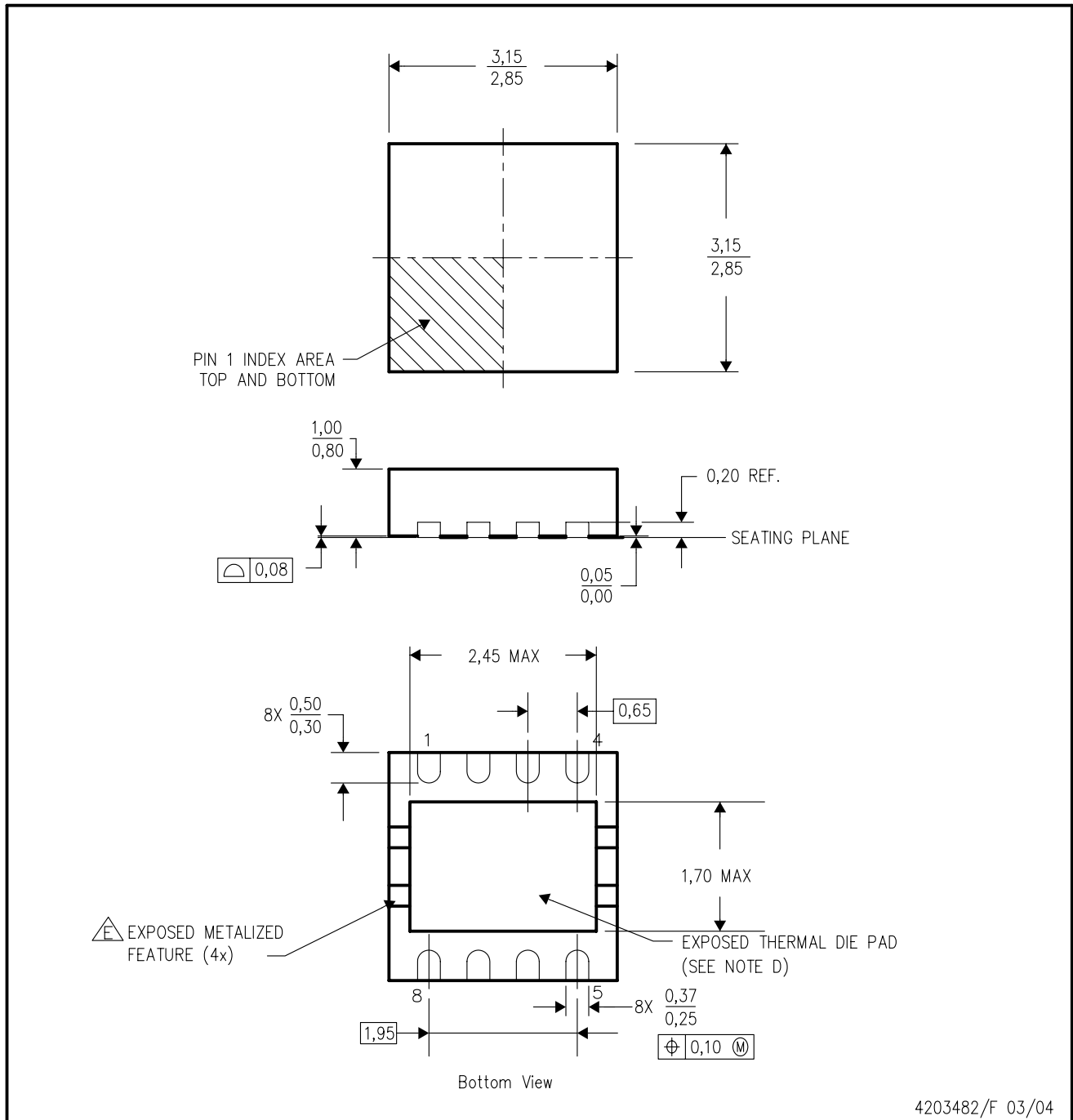
PLASTIC SMALL-OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Controlling dimension in inches.
 - $\triangle D$ Body length and width dimensions are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and the bottom of the plastic body.
 - $\triangle E$ Lead width dimension does not include dambar protrusion.
 - $\triangle F$ Lead width and thickness dimensions apply to solder plated leads.
 - G. Interlead flash allow 0.008 inch max.
 - H. Gate burr/protrusion max. 0.006 inch.
 - I. Datums A and B are to be determined at Datum H.
 - J. Package dimensions per JEDEC outline drawing TO-261, issue B, dated Feb. 1999. This variation is not yet included.

DRB (S-PDSO-N8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Small Outline No-Lead (SON) package configuration.
 - D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane.
 - E. Metalized features are supplier options and may not be on the package.

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