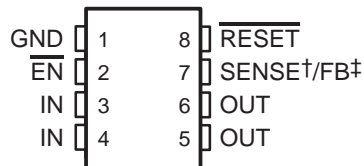


# TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q LOW-DROPOUT VOLTAGE REGULATORS WITH INTEGRATED DELAYED RESET FUNCTION

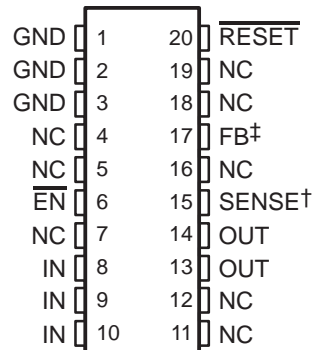
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- Available in 2.5-V, 3-V, 3.3-V, 4.85-V, and 5-V Fixed-Output and Adjustable Versions
- Integrated Precision Supply-Voltage Supervisor Monitoring Regulator Output Voltage
- Active-Low Reset Signal with 200-ms Pulse Width
- Very Low Dropout Voltage . . . Maximum of 35 mV at  $I_O = 100$  mA (TPS7350)
- Low Quiescent Current – Independent of Load . . . 340  $\mu$ A Typ
- Extremely Low Sleep-State Current, 0.5  $\mu$ A Max
- 2% Tolerance Over Full Range of Load, Line, and Temperature for Fixed-Output Versions<sup>§</sup>
- Output Current Range of 0 mA to 500 mA
- TSSOP Package Option Offers Reduced Component Height For Critical Applications

**D OR P PACKAGE  
(TOP VIEW)**



**PW PACKAGE  
(TOP VIEW)**



## description

The TPS73xx devices are members of a family of micropower low-dropout (LDO) voltage regulators.

They are differentiated from the TPS71xx and TPS72xx LDOs by their integrated delayed microprocessor-reset function. If the precision delayed reset is not required, the TPS71xx and TPS72xx should be considered.<sup>¶</sup>

NC – No internal connection

† SENSE – Fixed voltage options only  
(TPS7325, TPS7330, TPS7333, TPS7348, and TPS7350)

‡ FB – Adjustable version only (TPS7301)

## AVAILABLE OPTIONS

T <sub>J</sub>	OUTPUT VOLTAGE (V)			NEGATIVE-GOING RESET THRESHOLD VOLTAGE (V)			PACKAGED DEVICES			CHIP FORM (Y)
	MIN	TYP	MAX	MIN	TYP	MAX	SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
–40°C to 125°C	4.9	5	5.1	4.55	4.65	4.75	TPS7350QD	TPS7350QP	TPS7350QPW	TPS7350Y
	4.75	4.85	4.95	4.5	4.6	4.7	TPS7348QD	TPS7348QP	TPS7348QPW	TPS7348Y
	3.23	3.3	3.37	2.868	2.934	3	TPS7333QD	TPS7333QP	TPS7333QPW	TPS7333Y
	2.94	3	3.06	2.58	2.64	2.7	TPS7330QD	TPS7330QP	TPS7330QPW	TPS7330Y
	2.425	2.5	2.575	2.23	2.32	2.39	TPS7325QD	TPS7325QP	TPS7325QPW	TPS7325Y
	Adjustable 1.2 V to 9.75 V			1.101	1.123	1.145	TPS7301QD	TPS7301QP	TPS7301QPW	TPS7301Y

The D and PW packages are available taped and reeled. Add an R suffix to device type (e.g., TPS7350QDR). The TPS7301Q is programmable using an external resistor divider (see application information). The chip form is tested at 25°C.

<sup>§</sup> The TPS7325 has a tolerance of  $\pm 3\%$  over the full temperature range.

<sup>¶</sup> The TPS71xx and the TPS72xx are 500-mA and 250-mA output regulators respectively, offering performance similar to that of the TPS73xx but without the delayed-reset function. The TPS72xx devices are further differentiated by availability in 8-pin thin-shrink small-outline packages (TSSOP) for applications requiring minimum package size.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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# TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q LOW-DROPOUT VOLTAGE REGULATORS WITH INTEGRATED DELAYED RESET FUNCTION

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## description (continued)

The  $\overline{\text{RESET}}$  output of the TPS73xx initiates a reset in microcomputer and microprocessor systems in the event of an undervoltage condition. An internal comparator in the TPS73xx monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage.

If that occurs, the  $\overline{\text{RESET}}$  output (open-drain NMOS) turns on, taking the  $\overline{\text{RESET}}$  signal low.  $\overline{\text{RESET}}$  stays low for the duration of the undervoltage condition. Once the undervoltage condition ceases, a 200-ms (typ) time-out begins. At the completion of the 200-ms delay,  $\overline{\text{RESET}}$  goes high.

An order of magnitude reduction in dropout voltage and quiescent current over conventional LDO performance is achieved by replacing the typical pnp pass transistor with a PMOS device.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (maximum of 35 mV at an output current of 100 mA for the TPS7350) and is directly proportional to the output current (see Figure 1). Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is low and remains constant, independent of output loading (typically 340  $\mu\text{A}$  over the full range of output current, 0 mA to 500 mA). These two key specifications yield a significant improvement in operating life for battery-powered systems.

The LDO family also features a sleep mode; applying a logic high signal to  $\overline{\text{EN}}$  (enable) shuts down the regulator, reducing the quiescent current to 0.5  $\mu\text{A}$  maximum at  $T_J = 25^\circ\text{C}$ .

The TPS73xx is offered in 2.5-V, 3-V, 3.3-V, 4.85-V, and 5-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.2 V to 9.75 V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges (3% for the 2.5 V and the adjustable version). The TPS73xx family is available in PDIP (8 pin), SO (8 pin) and TSSOP (20 pin) packages. The TSSOP has a maximum height of 1.2 mm.

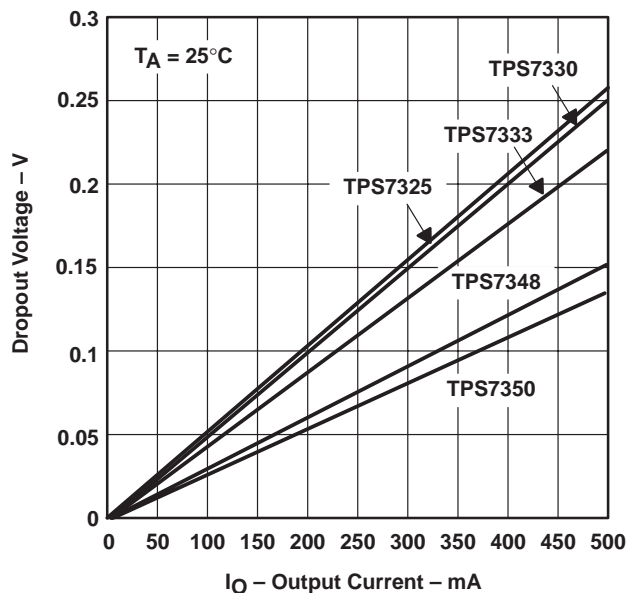
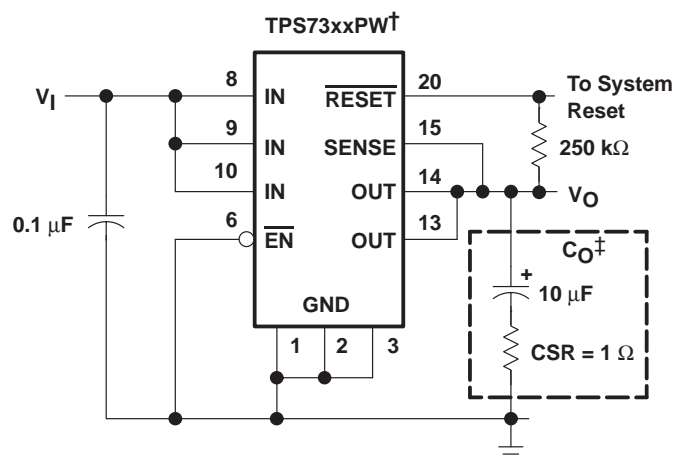


Figure 1. Dropout Voltage Versus Output Current



† TPS7325, TPS7330, TPS7333, TPS7348, TPS7350 (fixed-voltage options)

‡ Capacitor selection is nontrivial. See application information section for details.

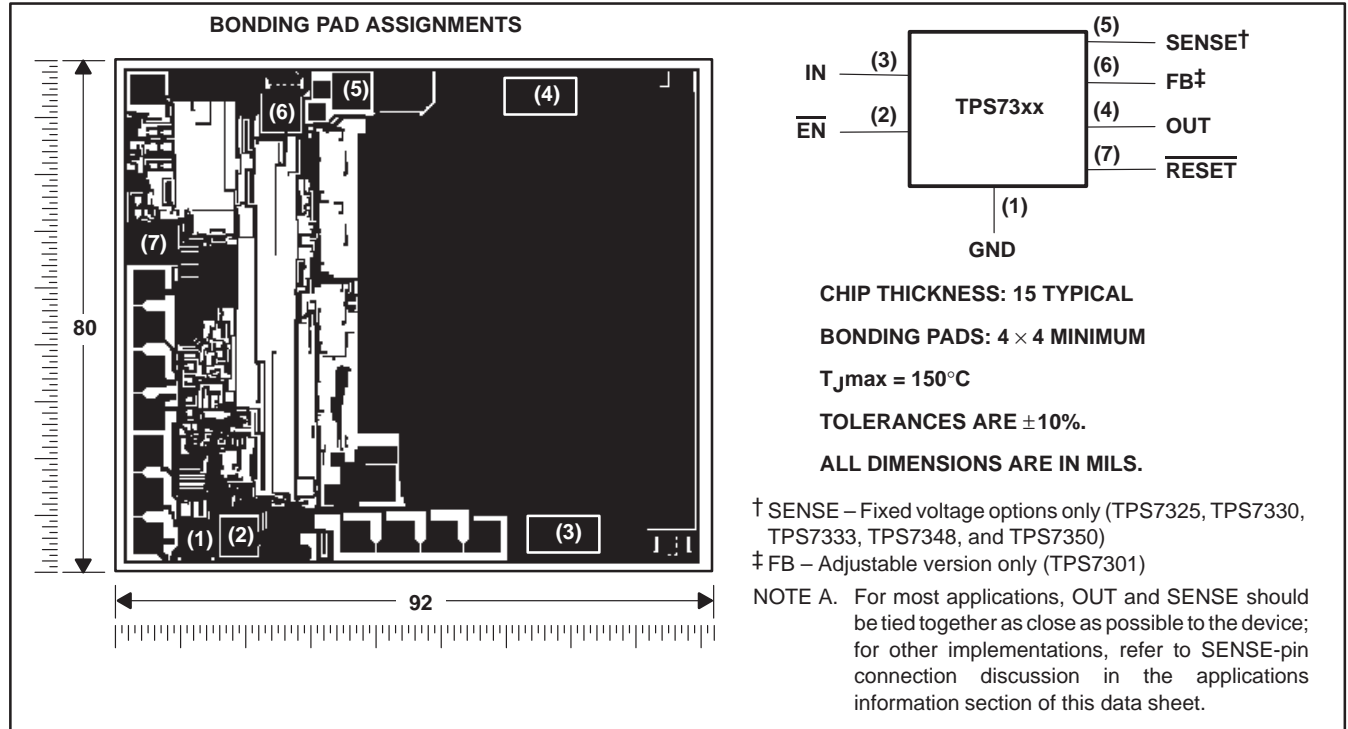
Figure 2. Typical Application Configuration

# TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q LOW-DROPOUT VOLTAGE REGULATORS WITH INTEGRATED DELAYED RESET FUNCTION

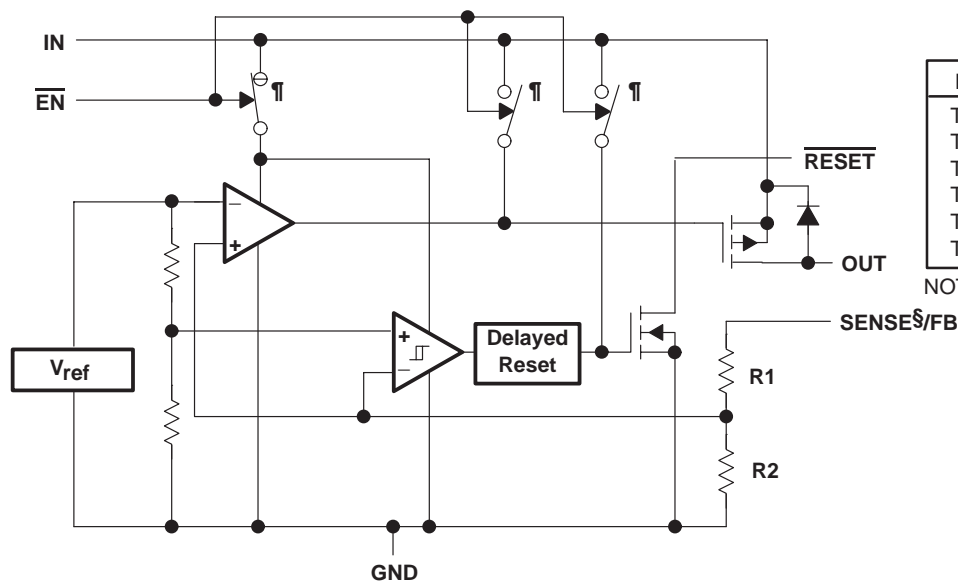
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## TPS73xxY chip information

These chips, when properly assembled, display characteristics similar to those of the TPS73xxQ. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



## functional block diagram



**RESISTOR DIVIDER OPTIONS**

DEVICE	R1	R2	UNIT
TPS7301	0	∞	Ω
TPS7325	260	233	kΩ
TPS7330	358	233	kΩ
TPS7333	420	233	kΩ
TPS7348	726	233	kΩ
TPS7350	756	233	kΩ

NOTE A. Resistors are nominal values only.

**COMPONENT COUNT**

COMPONENT	COUNT
MOS transistors	464
Bipolar transistors	41
Diodes	4
Capacitors	17
Resistors	76

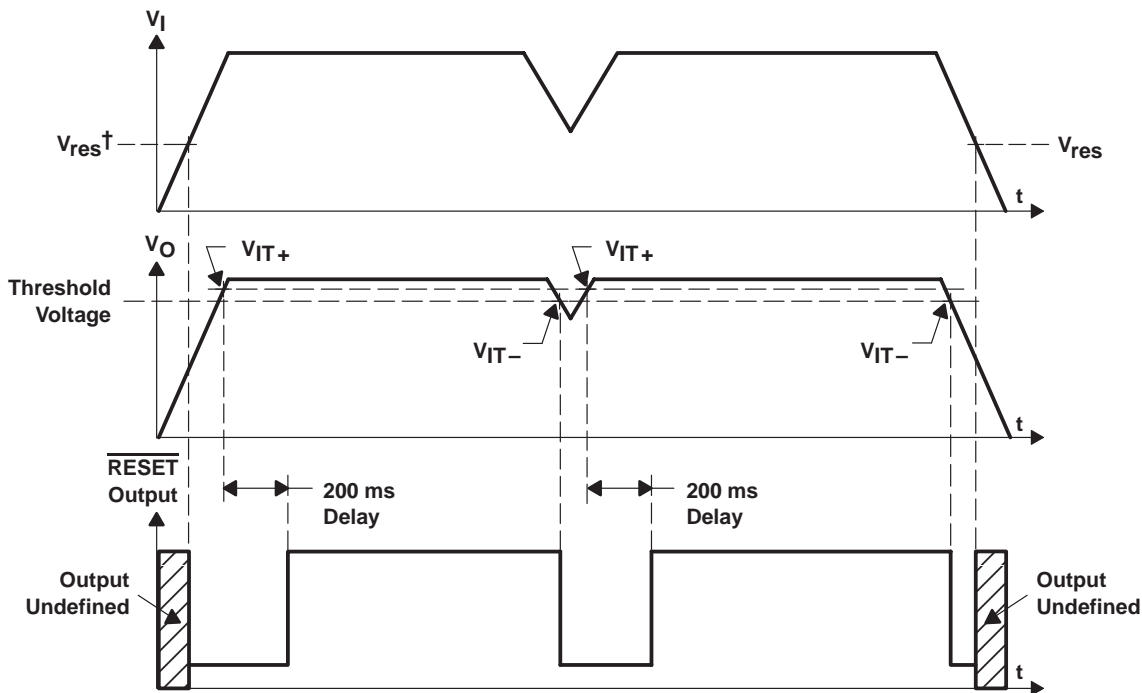
§ For most applications, SENSE should be externally connected to OUT as close as possible to the device. For other implementations, refer to SENSE-pin connection discussion in applications information section.

¶ Switch positions are shown with EN low (active).

**TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q**  
**LOW-DROPOUT VOLTAGE REGULATORS**  
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**timing diagram**



†  $V_{res}$  is the minimum input voltage for a valid  $\overline{RESET}$ . The symbol  $V_{res}$  is not currently listed within EIA or JEDEC standards for semiconductor symbology.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡**

Input voltage range§, $V_I$ , $\overline{RESET}$ , SENSE, $\overline{EN}$ .....	-0.3 V to 11 V
Output current, $I_O$ .....	2 A
Continuous total power dissipation .....	See Dissipation Rating Tables 1 and 2
Operating virtual junction temperature range, $T_J$ .....	-55°C to 150°C
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .....	260°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

§ All voltage values are with respect to network terminal ground.



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DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE (SEE FIGURE 3)

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	145 mW
P	1175 mW	9.4 mW/°C	752 mW	235 mW
PW†	700 mW	5.6 mW/°C	448 mW	140 mW

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE (SEE FIGURE 4)

PACKAGE	$T_C \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_C = 25^\circ\text{C}$	$T_C = 70^\circ\text{C}$ POWER RATING	$T_C = 125^\circ\text{C}$ POWER RATING
D	2188 mW	9.4 mW/°C	1765 mW	1248 mW
P	2738 mW	21.9 mW/°C	1752 mW	548 mW
PW†	4025 mW	32.2 mW/°C	2576 mW	805 mW

† Refer to Thermal Information section for detailed power dissipation considerations when using the TSSOP package.

MAXIMUM CONTINUOUS DISSIPATION  
 vs  
 FREE-AIR TEMPERATURE

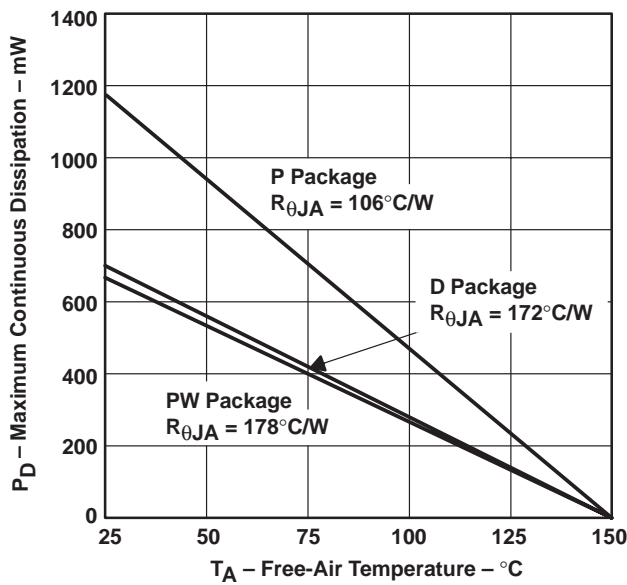


Figure 3

MAXIMUM CONTINUOUS DISSIPATION  
 vs  
 CASE TEMPERATURE

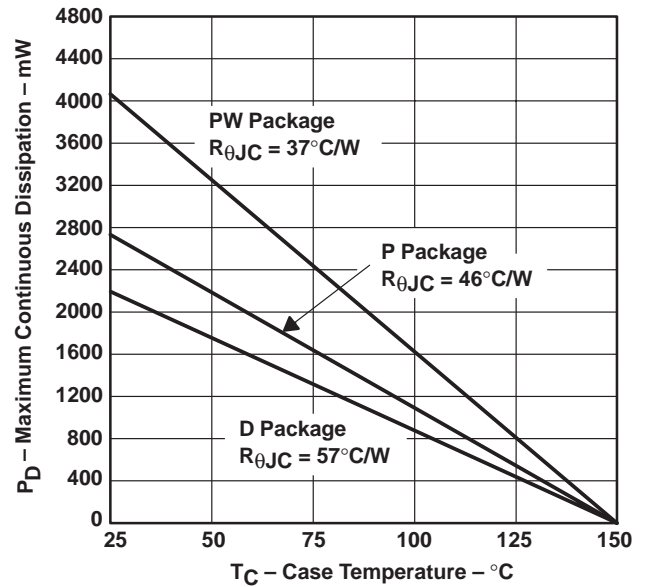


Figure 4

**TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q**  
**LOW-DROPOUT VOLTAGE REGULATORS**  
**WITH INTEGRATED DELAYED RESET FUNCTION**

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**recommended operating conditions**

		MIN	MAX	UNIT
Input voltage, $V_I$ †	TPS7301Q	2.47	10	V
	TPS7325Q	3.1	10	
	TPS7330Q	3.5	10	V
	TPS7333Q	3.77	10	V
	TPS7348Q	5.2	10	
	TPS7350Q	5.33	10	
High-level input voltage at $\overline{EN}$ , $V_{IH}$		2		V
Low-level input voltage at $\overline{EN}$ , $V_{IL}$			0.5	V
Output current range, $I_O$		0	500	mA
Operating virtual junction temperature range, $T_J$		-40	125	°C

† Minimum input voltage defined in the recommended operating conditions is the maximum specified output voltage plus dropout voltage,  $V_{DO}$ , at the maximum specified load range. Since dropout voltage is a function of output current, the usable range can be extended for lighter loads. To calculate the minimum input voltage for the maximum load current used in a given application, use the following equation:

$$V_{I(\min)} = V_{O(\max)} + V_{DO(\max \text{ load})}$$

Because the TPS7301 is programmable,  $r_{DS(on)}$  should be used to calculate  $V_{DO}$  before applying the above equation. The equation for calculating  $V_{DO}$  from  $r_{DS(on)}$  is given in Note 2 in the TPS7301 electrical characteristics table. The minimum value of 2.97 V is the absolute lower limit for the recommended input voltage range for the TPS7301.



**TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q**  
**LOW-DROPOUT VOLTAGE REGULATORS**  
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**electrical characteristics at  $I_O = 10\text{ mA}$ ,  $\overline{EN} = 0\text{ V}$ ,  $C_O = 4.7\text{ }\mu\text{F}$  ( $CSR^\ddagger = 1\text{ }\Omega$ ), SENSE/FB shorted to OUT (unless otherwise noted)**

PARAMETER	TEST CONDITIONS <sup>§</sup>	T <sub>J</sub>	MIN	TYP	MAX	UNIT
Ground current (active mode)	$\overline{EN} \leq 0.5\text{ V}$ , $0\text{ mA} \leq I_O \leq 500\text{ mA}$	$V_I = V_O + 1\text{ V}$ , 25°C		340	400	$\mu\text{A}$
		-40°C to 125°C			550	
Input current (standby mode)	$EN = V_I$ , $2.7\text{ V} \leq V_I \leq 10\text{ V}$	25°C		0.01	0.5	$\mu\text{A}$
		-40°C to 125°C			2	
Output current limit	$V_O = 0\text{ V}$ , $V_I = 10\text{ V}$	25°C		1.2	2	A
		-40°C to 125°C			2	
Pass-element leakage current in standby mode	$\overline{EN} = V_I$ , $2.7\text{ V} \leq V_I \leq 10\text{ V}$	25°C		0.01	0.5	$\mu\text{A}$
		-40°C to 125°C			1	
$\overline{RESET}$ leakage current	Normal operation, V at $\overline{RESET} = 10\text{ V}$	25°C		0.02	0.5	$\mu\text{A}$
		-40°C to 125°C			0.5	
Output voltage temperature coefficient		-40°C to 125°C		61	75	ppm/°C
Thermal shutdown junction temperature				165		°C
$\overline{EN}$ logic high (standby mode)	$2.5\text{ V} \leq V_I \leq 6\text{ V}$	-40°C to 125°C		2		V
	$6\text{ V} \leq V_I \leq 10\text{ V}$			2.7		
EN logic low (active mode)	$2.7\text{ V} \leq V_I \leq 10\text{ V}$	25°C			0.5	V
		-40°C to 125°C			0.5	
$\overline{EN}$ hysteresis voltage		25°C		50		mV
$\overline{EN}$ input current	$0\text{ V} \leq V_I \leq 10\text{ V}$	25°C	-0.5	0.001	0.5	$\mu\text{A}$
		-40°C to 125°C	-0.5		0.5	
Minimum $V_I$ for active pass element		25°C		2.05	2.5	V
		-40°C to 125°C			2.5	
Minimum $V_I$ for valid $\overline{RESET}$	$I_O(\overline{RESET}) = -300\text{ }\mu\text{A}$	25°C		1	1.5	V
		-40°C to 125°C			1.9	

<sup>‡</sup> CSR (compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to  $C_O$ .

<sup>§</sup> Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

**TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q**  
**LOW-DROPOUT VOLTAGE REGULATORS**  
**WITH INTEGRATED DELAYED RESET FUNCTION**

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**TPS7301Q electrical characteristics at  $I_O = 10\text{ mA}$ ,  $V_I = 3.5\text{ V}$ ,  $\overline{\text{EN}} = 0\text{ V}$ ,  $C_O = 4.7\text{ }\mu\text{F}$  ( $\text{CSR}^\dagger = 1\text{ }\Omega$ ), FB shorted to OUT at device leads (unless otherwise noted)**

PARAMETER	TEST CONDITIONS <sup>‡</sup>		T <sub>J</sub>	MIN	TYP	MAX	UNIT
Reference voltage (measured at FB)			25°C	1.182			V
	$2.5\text{ V} \leq V_I \leq 10\text{ V}$ , See Note 1	$5\text{ mA} \leq I_O \leq 500\text{ mA}$	-40°C to 125°C	1.147		1.217	V
Reference voltage temperature coefficient			-40°C to 125°C		61	75	ppm/°C
Pass-element series resistance (See Note 2)	$V_I = 2.4\text{ V}$ ,	$50\text{ }\mu\text{A} \leq I_O \leq 150\text{ mA}$	25°C	0.7		1	$\Omega$
			-40°C to 125°C			1	
	$V_I = 2.4\text{ V}$ ,	$150\text{ mA} \leq I_O \leq 500\text{ mA}$	25°C	0.83		1.3	
			-40°C to 125°C			1.3	
	$V_I = 2.9\text{ V}$ ,	$50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$	25°C	0.52		0.85	
-40°C to 125°C					0.85		
Input regulation	$V_I = 2.5\text{ V}$ to 10 V, See Note 1	$50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$	25°C	3		18	mV
			-40°C to 125°C			25	
Output regulation	$2.5\text{ V} \leq V_I \leq 10\text{ V}$ , See Note 1	$I_O = 5\text{ mA}$ to 500 mA,	25°C	5		14	mV
			-40°C to 125°C			25	
	$2.5\text{ V} \leq V_I \leq 10\text{ V}$ , See Note 1	$I_O = 50\text{ }\mu\text{A}$ to 500 mA,	25°C	7		22	mV
			-40°C to 125°C			54	
Ripple rejection	$f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$	25°C	48	59		dB
			-40°C to 125°C			44	
		$I_O = 500\text{ mA}$ , See Note 1	25°C	45	54		
			-40°C to 125°C			44	
Output noise-spectral density	$f = 120\text{ Hz}$		25°C	2		$\mu\text{V}/\sqrt{\text{Hz}}$	
Output noise voltage	$10\text{ Hz} \leq f \leq 100\text{ kHz}$	$C_O = 4.7\text{ }\mu\text{F}$	25°C	95		$\mu\text{V}_{\text{rms}}$	
		$C_O = 10\text{ }\mu\text{F}$	25°C	89			
		$C_O = 100\text{ }\mu\text{F}$	25°C	74			
$\overline{\text{RESET}}$ trip-threshold voltage <sup>§</sup>	$V_{O(\text{FB})}$ decreasing		-40°C to 125°C	1.101	1.145		V
$\overline{\text{RESET}}$ hysteresis voltage <sup>§</sup>	Measured at $V_{O(\text{FB})}$		25°C	12			mV
$\overline{\text{RESET}}$ output low voltage <sup>§</sup>	$V_I = 2.13\text{ V}$ ,	$I_{O(\text{RESET})} = 400\text{ }\mu\text{A}$	25°C	0.1		0.4	V
			-40°C to 125°C			0.4	
FB input current			25°C	-10	0.1	10	nA
			-40°C to 125°C			20	

<sup>†</sup> CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to  $C_O$ .

<sup>‡</sup> Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

<sup>§</sup> Output voltage programmed to 2.5 V with closed-loop configuration (see application information).

- NOTES: 1. When  $V_I < 2.9\text{ V}$  and  $I_O > 150\text{ mA}$  simultaneously, pass element  $r_{\text{DS(on)}}$  increases (see Figure 33) to a point where the resulting dropout voltage prevents the regulator from maintaining the specified tolerance range.
2. To calculate dropout voltage, use equation:  $V_{\text{DO}} = I_O \cdot r_{\text{DS(on)}}$   
 $r_{\text{DS(on)}}$  is a function of both output current and input voltage. This parametric table lists  $r_{\text{DS(on)}}$  for  $V_I = 2.4\text{ V}$ , 2.9 V, 3.9 V, and 5.9 V, which corresponds to dropout conditions for programmed output voltages of 2.5 V, 3 V, 4 V, and 6 V respectively. For other programmed values, refer to Figure 33.



**TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q**  
**LOW-DROPOUT VOLTAGE REGULATORS**  
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**TPS7325Q electrical characteristics at  $I_O = 10\text{ mA}$ ,  $V_I = 3.5\text{ V}$ ,  $\overline{\text{EN}} = 0\text{ V}$ ,  $C_O = 10\text{ }\mu\text{F}$  ( $\text{CSR}^\dagger = 1\text{ }\Omega$ ), SENSE shorted to OUT (unless otherwise noted)**

PARAMETER	TEST CONDITIONS‡		T <sub>J</sub>	MIN	TYP	MAX	UNIT
Output voltage			25°C	2.45	2.5	2.55	V
	$3.5\text{ V} \leq V_I \leq 10\text{ V}$ ,	$5\text{ mA} \leq I_O \leq 500\text{ mA}$	-40°C to 125°C	2.425		2.575	
Dropout voltage§	$I_O = 10\text{ mA}$ ,	$V_I = 2.97\text{ V}$	25°C	5			mV
			-40°C to 125°C			14	
	$I_O = 100\text{ mA}$ ,	$V_I = 2.97\text{ V}$	25°C	50		80	
			-40°C to 125°C			150	
	$I_O = 500\text{ mA}$ ,	$V_I = 2.97\text{ V}$	25°C	270		400	
			-40°C to 125°C			600	
Pass-element series resistance§	$(2.97\text{ V} - V_O)/I_O$ , $I_O = 500\text{ mA}$	$V_I = 2.97\text{ V}$ ,	25°C	0.5		0.7	$\Omega$
			-40°C to 125°C			1.4	
Input regulation	$V_I = 3.5\text{ V to }10\text{ V}$ ,	$50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$	25°C	6		20	mV
			-40°C to 125°C			25	
Output regulation	$I_O = 5\text{ mA to }500\text{ mA}$ ,	$3.5\text{ V} \leq V_I \leq 10\text{ V}$	25°C	20		32	mV
			-40°C to 125°C			50	
	$I_O = 50\text{ }\mu\text{A to }500\text{ mA}$ ,	$3.5\text{ V} \leq V_I \leq 10\text{ V}$	25°C	28		60	mV
			-40°C to 125°C			100	
Ripple rejection	$f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$	25°C	50	53		dB
			-40°C to 125°C	49			
		$I_O = 500\text{ mA}$	25°C	49	53		
			-40°C to 125°C	32			
Output noise-spectral density	$f = 120\text{ Hz}$		25°C	2		$\mu\text{V}/\sqrt{\text{Hz}}$	
Output noise voltage	$10\text{ Hz} \leq f \leq 100\text{ kHz}$	$C_O = 4.7\text{ }\mu\text{F}$	25°C	274		$\mu\text{Vrms}$	
		$C_O = 10\text{ }\mu\text{F}$	25°C	228			
		$C_O = 100\text{ }\mu\text{F}$	25°C	159			
$\overline{\text{RESET}}$ trip-threshold voltage	$V_O$ decreasing		-40°C to 125°C	2.23	2.32	2.39	V
$\overline{\text{RESET}}$ output low voltage	$V_I = 2.1\text{ V}$ ,	$I_O(\text{RESET}) = -0.8\text{ mA}$	25°C	0.14		0.4	V
			-40°C to 125°C			0.4	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to  $C_O$ .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

§ Dropout test and pass-element series resistance test are not production tested. Test method requires SENSE terminal to be disconnected from output voltage.

**TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q**  
**LOW-DROPOUT VOLTAGE REGULATORS**  
**WITH INTEGRATED DELAYED RESET FUNCTION**

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**TPS7330Q electrical characteristics at  $I_O = 10\text{ mA}$ ,  $V_I = 4\text{ V}$ ,  $\overline{\text{EN}} = 0\text{ V}$ ,  $C_O = 4.7\text{ }\mu\text{F}$  ( $\text{CSRT}^\dagger = 1\text{ }\Omega$ ), SENSE shorted to OUT (unless otherwise noted)**

PARAMETER	TEST CONDITIONS‡		T <sub>J</sub>	MIN	TYP	MAX	UNIT
Output voltage			25°C	3			V
	$4\text{ V} \leq V_I \leq 10\text{ V}$ ,	$5\text{ mA} \leq I_O \leq 500\text{ mA}$	-40°C to 125°C	2.94	3.06		
Dropout voltage	$I_O = 10\text{ mA}$ ,	$V_I = 2.94\text{ V}$	25°C	5.2	7		mV
			-40°C to 125°C	10			
	$I_O = 100\text{ mA}$ ,	$V_I = 2.94\text{ V}$	25°C	52	75		
			-40°C to 125°C	100			
	$I_O = 500\text{ mA}$ ,	$V_I = 2.94\text{ V}$	25°C	267	450		
			-40°C to 125°C	500			
Pass-element series resistance	$(2.94\text{ V} - V_O)/I_O$ , $I_O = 500\text{ mA}$	$V_I = 2.94\text{ V}$ ,	25°C	0.5	0.7		$\Omega$
			-40°C to 125°C	1			
Input regulation	$V_I = 4\text{ V}$ to 10 V,	$50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$	25°C	6	23		mV
			-40°C to 125°C	29			
Output regulation	$I_O = 5\text{ mA}$ to 500 mA,	$4\text{ V} \leq V_I \leq 10\text{ V}$	25°C	20	32		mV
			-40°C to 125°C	60			
	$I_O = 50\text{ }\mu\text{A}$ to 500 mA,	$4\text{ V} \leq V_I \leq 10\text{ V}$	25°C	28	60		mV
			-40°C to 125°C	120			
Ripple rejection	f = 120 Hz	$I_O = 50\text{ }\mu\text{A}$	25°C	43	53		dB
			-40°C to 125°C	40			
		$I_O = 500\text{ mA}$	25°C	39	53		
			-40°C to 125°C	36			
Output noise-spectral density	f = 120 Hz		25°C	2		$\mu\text{V}/\sqrt{\text{Hz}}$	
Output noise voltage	10 Hz $\leq$ f $\leq$ 100 kHz	$C_O = 4.7\text{ }\mu\text{F}$	25°C	274		$\mu\text{V}_{\text{rms}}$	
		$C_O = 10\text{ }\mu\text{F}$	25°C	228			
		$C_O = 100\text{ }\mu\text{F}$	25°C	159			
$\overline{\text{RESET}}$ trip-threshold voltage	$V_O$ decreasing		-40°C to 125°C	2.58	2.64	2.7	V
$\overline{\text{RESET}}$ output low voltage	$V_I = 2.6\text{ V}$ ,	$I_O(\overline{\text{RESET}}) = -0.8\text{ mA}$	25°C	0.14	0.4		V
			-40°C to 125°C	0.4			

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to  $C_O$ .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.



**TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q**  
**LOW-DROPOUT VOLTAGE REGULATORS**  
**WITH INTEGRATED DELAYED RESET FUNCTION**

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**TPS7333Q electrical characteristics at  $I_O = 10\text{ mA}$ ,  $V_I = 4.3\text{ V}$ ,  $\overline{\text{EN}} = 0\text{ V}$ ,  $C_O = 4.7\text{ }\mu\text{F}$  ( $\text{CSR}^\dagger = 1\text{ }\Omega$ ), SENSE shorted to OUT (unless otherwise noted)**

PARAMETER	TEST CONDITIONS <sup>‡</sup>		T <sub>J</sub>	MIN	TYP	MAX	UNIT		
Output voltage			25°C	3.3			V		
	4.3 V ≤ V <sub>I</sub> ≤ 10 V, 5 mA ≤ I <sub>O</sub> ≤ 500 mA		–40°C to 125°C	3.23	3.37				
Dropout voltage	I <sub>O</sub> = 10 mA, V <sub>I</sub> = 3.23 V	25°C		4.5 7			mV		
		–40°C to 125°C		8					
	I <sub>O</sub> = 100 mA, V <sub>I</sub> = 3.23 V	25°C		44 60					
		–40°C to 125°C		80					
	I <sub>O</sub> = 500 mA, V <sub>I</sub> = 3.23 V	25°C		235 300					
		–40°C to 125°C		400					
Pass-element series resistance	(3.23 V – V <sub>O</sub> )/I <sub>O</sub> , I <sub>O</sub> = 500 mA	25°C		0.44 0.6			Ω		
		–40°C to 125°C		0.8					
Input regulation	V <sub>I</sub> = 4.3 V to 10 V, 50 μA ≤ I <sub>O</sub> ≤ 500 mA	25°C		6 23			mV		
		–40°C to 125°C		29					
Output regulation	I <sub>O</sub> = 5 mA to 500 mA, 4.3 V ≤ V <sub>I</sub> ≤ 10 V	25°C		21 38			mV		
		–40°C to 125°C		75					
	I <sub>O</sub> = 50 μA to 500 mA, 4.3 V ≤ V <sub>I</sub> ≤ 10 V	25°C		31 60			mV		
		–40°C to 125°C		120					
Ripple rejection	f = 120 Hz	I <sub>O</sub> = 50 μA	25°C		43 51		dB		
			–40°C to 125°C		40				
		I <sub>O</sub> = 500 mA	25°C		39 49				
			–40°C to 125°C		36				
Output noise-spectral density	f = 120 Hz		25°C	2			μV/√Hz		
Output noise voltage	10 Hz ≤ f ≤ 100 kHz	C <sub>O</sub> = 4.7 μF		25°C			274		μVrms
		C <sub>O</sub> = 10 μF		25°C			228		
		C <sub>O</sub> = 100 μF		25°C			159		
$\overline{\text{RESET}}$ trip-threshold voltage	V <sub>O</sub> decreasing		–40°C to 125°C	2.868			V		
$\overline{\text{RESET}}$ hysteresis voltage			25°C	18			mV		
$\overline{\text{RESET}}$ output low voltage	V <sub>I</sub> = 2.8 V, I <sub>O</sub> (RESET) = –1 mA	25°C		0.17 0.4			V		
		–40°C to 125°C		0.4					

<sup>†</sup> CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C<sub>O</sub>.

<sup>‡</sup> Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

**TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q**  
**LOW-DROPOUT VOLTAGE REGULATORS**  
**WITH INTEGRATED DELAYED RESET FUNCTION**

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**TPS7348Q electrical characteristics at  $I_O = 10\text{ mA}$ ,  $V_I = 5.85\text{ V}$ ,  $\overline{\text{EN}} = 0\text{ V}$ ,  $C_O = 4.7\text{ }\mu\text{F}$  ( $\text{CSRT}^\dagger = 1\text{ }\Omega$ ), SENSE shorted to OUT (unless otherwise noted)**

PARAMETER	TEST CONDITIONS‡	T <sub>J</sub>	MIN	TYP	MAX	UNIT
Output voltage		25°C		4.85		V
	$5.85\text{ V} \leq V_I \leq 10\text{ V}$ , $5\text{ mA} \leq I_O \leq 500\text{ mA}$	-40°C to 125°C	4.75		4.95	
Dropout voltage	$I_O = 10\text{ mA}$ , $V_I = 4.75\text{ V}$	25°C		2.9	6	mV
		-40°C to 125°C			8	
	$I_O = 100\text{ mA}$ , $V_I = 4.75\text{ V}$	25°C		28	37	
		-40°C to 125°C			54	
	$I_O = 500\text{ mA}$ , $V_I = 4.75\text{ V}$	25°C		150	180	
		-40°C to 125°C			250	
Pass-element series resistance	$(4.75\text{ V} - V_O)/I_O$ , $V_I = 4.75\text{ V}$ , $I_O = 500\text{ mA}$	25°C		0.28	0.37	$\Omega$
		-40°C to 125°C			0.52	
Input regulation	$V_I = 5.85\text{ V}$ to 10 V, $50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$	25°C		9	35	mV
		-40°C to 125°C			37	
Output regulation	$I_O = 5\text{ mA}$ to 500 mA, $5.85\text{ V} \leq V_I \leq 10\text{ V}$	25°C		28	42	mV
		-40°C to 125°C			80	
	$I_O = 50\text{ }\mu\text{A}$ to 500 mA, $5.85\text{ V} \leq V_I \leq 10\text{ V}$	25°C		42	65	mV
		-40°C to 125°C			130	
Ripple rejection	$f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$	25°C	42	53	dB
			-40°C to 125°C	39		
		$I_O = 500\text{ mA}$	25°C	39	50	
			-40°C to 125°C	35		
Output noise-spectral density	$f = 120\text{ Hz}$	25°C		2	$\mu\text{V}/\sqrt{\text{Hz}}$	
Output noise voltage	$10\text{ Hz} \leq f \leq 100\text{ kHz}$	$C_O = 4.7\text{ }\mu\text{F}$	25°C	410	$\mu\text{V}_{\text{rms}}$	
		$C_O = 10\text{ }\mu\text{F}$	25°C	328		
		$C_O = 100\text{ }\mu\text{F}$	25°C	212		
$\overline{\text{RESET}}$ trip-threshold voltage	$V_O$ decreasing	-40°C to 125°C	4.5		4.7	V
$\overline{\text{RESET}}$ hysteresis voltage		25°C		26		mV
$\overline{\text{RESET}}$ output low voltage	$I_O(\overline{\text{RESET}}) = -1.2\text{ mA}$ , $V_I = 4.12\text{ V}$	25°C		0.2	0.4	V
		-40°C to 125°C			0.4	

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to  $C_O$ .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.



**TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q**  
**LOW-DROPOUT VOLTAGE REGULATORS**  
**WITH INTEGRATED DELAYED RESET FUNCTION**

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**TPS7350Q electrical characteristics at  $I_O = 10\text{ mA}$ ,  $V_I = 6\text{ V}$ ,  $\overline{\text{EN}} = 0\text{ V}$ ,  $C_O = 4.7\text{ }\mu\text{F}$  ( $\text{CSR}^\dagger = 1\text{ }\Omega$ ), SENSE shorted to OUT (unless otherwise noted)**

PARAMETER	TEST CONDITIONS <sup>‡</sup>		T <sub>J</sub>	MIN	TYP	MAX	UNIT
Output voltage			25°C	5			V
	$6\text{ V} \leq V_I \leq 10\text{ V}$ ,	$5\text{ mA} \leq I_O \leq 500\text{ mA}$	-40°C to 125°C	4.9	5.1		
Dropout voltage	$I_O = 10\text{ mA}$ ,	$V_I = 4.88\text{ V}$	25°C	2.9		6	mV
			-40°C to 125°C	8			
	$I_O = 100\text{ mA}$ ,	$V_I = 4.88\text{ V}$	25°C	27		35	
			-40°C to 125°C	50			
	$I_O = 500\text{ mA}$ ,	$V_I = 4.88\text{ V}$	25°C	146		170	
			-40°C to 125°C	230			
Pass-element series resistance	$(4.88\text{ V} - V_O)/I_O$ , $I_O = 500\text{ mA}$	$V_I = 4.88\text{ V}$ ,	25°C	0.27	0.35		$\Omega$
			-40°C to 125°C	0.5			
Input regulation	$V_I = 6\text{ V to } 10\text{ V}$ ,	$50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$	25°C	4		25	mV
			-40°C to 125°C	45			
Output regulation	$I_O = 5\text{ mA to } 500\text{ mA}$ ,	$6\text{ V} \leq V_I \leq 10\text{ V}$	25°C	30		45	mV
			-40°C to 125°C	86			
	$I_O = 50\text{ }\mu\text{A to } 500\text{ mA}$ ,	$6\text{ V} \leq V_I \leq 10\text{ V}$	25°C	45		65	mV
			-40°C to 125°C	140			
Ripple rejection	$f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$	25°C	43	53		dB
			-40°C to 125°C	38			
		$I_O = 500\text{ mA}$	25°C	41	51		
			-40°C to 125°C	36			
Output noise-spectral density	$f = 120\text{ Hz}$		25°C	2		$\mu\text{V}/\sqrt{\text{Hz}}$	
Output noise voltage	$10\text{ Hz} \leq f \leq 100\text{ kHz}$	$C_O = 4.7\text{ }\mu\text{F}$	25°C	430		$\mu\text{Vrms}$	
		$C_O = 10\text{ }\mu\text{F}$	25°C	345			
		$C_O = 100\text{ }\mu\text{F}$	25°C	220			
$\overline{\text{RESET}}$ trip-threshold voltage	$V_O$ decreasing		-40°C to 125°C	4.55	4.75		V
$\overline{\text{RESET}}$ hysteresis voltage			25°C	28		mV	
$\overline{\text{RESET}}$ output low voltage	$I_O(\text{RESET}) = -1.2\text{ mA}$ , $V_I = 4.25\text{ V}$		25°C	0.15	0.4		V
			-40°C to 125°C	0.4			

<sup>†</sup> CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to  $C_O$ .

<sup>‡</sup> Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

**TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q**  
**LOW-DROPOUT VOLTAGE REGULATORS**  
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**switching characteristics**

PARAMETER	TEST CONDITIONS	T <sub>J</sub>	TPS7301Q, TPS7333Q TPS7348Q, TPS7350Q			UNIT
			MIN	TYP	MAX	
RESET time-out delay	See Figure 5	25°C	140	200	260	ms
		-40°C to 125°C	100		300	

**electrical characteristics at I<sub>O</sub> = 10 mA, EN = 0 V, C<sub>O</sub> = 4.7 μF (CSR† = 1 Ω), T<sub>J</sub> = 25°C, SENSE/FB shorted to OUT (unless otherwise noted)**

PARAMETER	TEST CONDITIONS‡	TPS7301Y, TPS7333Y TPS7348Y, TPS7350Y			UNIT
		MIN	TYP	MAX	
Ground current (active mode)	EN ≤ 0.5 V, V <sub>I</sub> = V <sub>O</sub> + 1 V, 0 mA ≤ I <sub>O</sub> ≤ 500 mA		340		μA
Input current (standby mode)	EN = V <sub>I</sub> , 2.7 V ≤ V <sub>I</sub> ≤ 10 V		0.01		μA
Output current limit	V <sub>O</sub> = 0 V, V <sub>I</sub> = 10 V		1.2		A
Pass-element leakage current in standby mode	EN = V <sub>I</sub> , 2.7 V ≤ V <sub>I</sub> ≤ 10 V		0.01		μA
RESET leakage current	Normal operation, V at RESET = 10 V		0.02		μA
Thermal shutdown junction temperature			165		°C
EN logic low (active mode)	2.7 V ≤ V <sub>I</sub> ≤ 10 V			0.5	V
EN hysteresis voltage			50		mV
EN input current	0 V ≤ V <sub>I</sub> ≤ 10 V		0.001		μA
Minimum V <sub>I</sub> for active pass element			2.05		V
Minimum V <sub>I</sub> for valid RESET	I <sub>O</sub> (RESET) = -300 μA		1		V

† CSR (compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C<sub>O</sub>.

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.



**TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q**  
**LOW-DROPOUT VOLTAGE REGULATORS**  
**WITH INTEGRATED DELAYED RESET FUNCTION**

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**TPS7301Y electrical characteristics at  $I_O = 10\text{ mA}$ ,  $V_I = 3.5\text{ V}$ ,  $\overline{\text{EN}} = 0\text{ V}$ ,  $C_O = 4.7\text{ }\mu\text{F}$  ( $\text{CSR}^\dagger = 1\text{ }\Omega$ ),  $T_J = 25^\circ\text{C}$ , FB shorted to OUT at device leads (unless otherwise noted)**

PARAMETER	TEST CONDITIONS <sup>‡</sup>	MIN	TYP	MAX	UNIT
Reference voltage (measured at FB)			1.182		V
Pass-element series resistance (See Note 2)	$V_I = 2.4\text{ V}$ , $50\text{ }\mu\text{A} \leq I_O \leq 150\text{ mA}$		0.7		$\Omega$
	$V_I = 2.4\text{ V}$ , $150\text{ mA} \leq I_O \leq 500\text{ mA}$		0.83		
	$V_I = 2.9\text{ V}$ , $50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$		0.52		
	$V_I = 3.9\text{ V}$ , $50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$		0.32		
	$V_I = 5.9\text{ V}$ , $50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$		0.23		
Input regulation	$V_I = 2.5\text{ V to } 10\text{ V}$ , $50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$ , See Note 1		3		mV
Output regulation	$2.5\text{ V} \leq V_I \leq 10\text{ V}$ , $I_O = 5\text{ mA to } 500\text{ mA}$ , See Note 1		5		mV
	$2.5\text{ V} \leq V_I \leq 10\text{ V}$ , $I_O = 50\text{ }\mu\text{A to } 500\text{ mA}$ , See Note 1		7		mV
Ripple rejection	$f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$		59	dB
		$I_O = 500\text{ mA}$ , See Note 1		54	
Output noise-spectral density	$f = 120\text{ Hz}$		2		$\mu\text{V}/\sqrt{\text{Hz}}$
Output noise voltage	$10\text{ Hz} \leq f \leq 100\text{ kHz}$	$C_O = 4.7\text{ }\mu\text{F}$		95	$\mu\text{V}_{\text{rms}}$
		$C_O = 10\text{ }\mu\text{F}$		89	
		$C_O = 100\text{ }\mu\text{F}$		74	
$\overline{\text{RESET}}$ hysteresis voltage <sup>§</sup>	Measured at $V_O(\text{FB})$		12		mV
$\overline{\text{RESET}}$ output low voltage <sup>§</sup>	$V_I = 2.13\text{ V}$ , $I_O(\overline{\text{RESET}}) = 400\text{ }\mu\text{A}$		0.1		V
FB input current			0.1		nA

<sup>†</sup> CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to  $C_O$ .

<sup>‡</sup> Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

<sup>§</sup> Output voltage programmed to 2.5 V with closed-loop configuration (see application information).

- NOTES:
- When  $V_I < 2.9\text{ V}$  and  $I_O > 150\text{ mA}$  simultaneously, pass element  $r_{\text{DS(on)}}$  increases (see Figure 33) to a point where the resulting dropout voltage prevents the regulator from maintaining the specified tolerance range.
  - To calculate dropout voltage, use equation:  $V_{\text{DO}} = I_O \cdot r_{\text{DS(on)}}$   
 $r_{\text{DS(on)}}$  is a function of both output current and input voltage. The parametric table lists  $r_{\text{DS(on)}}$  for  $V_I = 2.4\text{ V}$ ,  $2.9\text{ V}$ ,  $3.9\text{ V}$ , and  $5.9\text{ V}$ , which corresponds to dropout conditions for programmed output voltages of 2.5 V, 3 V, 4 V, and 6 V respectively. For other programmed values, refer to Figure 33.

**TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q**  
**LOW-DROPOUT VOLTAGE REGULATORS**  
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**TPS7325Y electrical characteristics at  $I_O = 10\text{ mA}$ ,  $V_I = 3.5\text{ V}$ ,  $\overline{EN} = 0\text{ V}$ ,  $C_O = 10\text{ }\mu\text{F}$  ( $CSR^\dagger = 1\text{ }\Omega$ ),  $T_J = 25^\circ\text{C}$ , SENSE shorted to OUT (unless otherwise noted)**

PARAMETER	TEST CONDITIONS‡	MIN	TYP	MAX	UNIT
Output voltage			2.5		V
Dropout voltage§	$I_O = 10\text{ mA}$ , $V_I = 2.97\text{ V}$		5		mV
	$I_O = 100\text{ mA}$ , $V_I = 2.97\text{ V}$		50		
	$I_O = 500\text{ mA}$ , $V_I = 2.97\text{ V}$		270		
Pass-element series resistance§	$(2.97\text{ V} - V_O)/I_O$ , $V_I = 2.97\text{ V}$ , $I_O = 500\text{ mA}$		0.5		$\Omega$
Input regulation	$V_I = 3.5\text{ V to }10\text{ V}$ , $50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$		6		mV
Output regulation	$I_O = 5\text{ mA to }500\text{ mA}$ , $3.5\text{ V} \leq V_I \leq 10\text{ V}$		20		mV
	$I_O = 50\text{ }\mu\text{A to }500\text{ mA}$ , $3.5\text{ V} \leq V_I \leq 10\text{ V}$		28		mV
Ripple rejection	$f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$		53	dB
		$I_O = 500\text{ mA}$		53	
Output noise-spectral density	$f = 120\text{ Hz}$		2		$\mu\text{V}/\sqrt{\text{Hz}}$
Output noise voltage	$10\text{ Hz} \leq f \leq 100\text{ kHz}$	$C_O = 4.7\text{ }\mu\text{F}$		274	$\mu\text{Vrms}$
		$C_O = 10\text{ }\mu\text{F}$		228	
		$C_O = 100\text{ }\mu\text{F}$		159	
$\overline{\text{RESET}}$ output low voltage	$V_I = 2.1\text{ V}$ , $I_O(\overline{\text{RESET}}) = -0.8\text{ mA}$		0.14		V

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to  $C_O$ .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

§ Dropout test and pass-element series resistance test are not production tested. Test method requires SENSE terminal to be disconnected from output voltage.



**TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q**  
**LOW-DROPOUT VOLTAGE REGULATORS**  
**WITH INTEGRATED DELAYED RESET FUNCTION**

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**TPS7330Y electrical characteristics at  $I_O = 10\text{ mA}$ ,  $V_I = 4\text{ V}$ ,  $\overline{EN} = 0\text{ V}$ ,  $C_O = 4.7\text{ }\mu\text{F}$  ( $\text{CSR}^\dagger = 1\text{ }\Omega$ ),  $T_J = 25^\circ\text{C}$ , SENSE shorted to OUT (unless otherwise noted)**

PARAMETER	TEST CONDITIONS <sup>‡</sup>	MIN	TYP	MAX	UNIT
Output voltage			3		V
Dropout voltage	$I_O = 10\text{ mA}$ , $V_I = 2.94\text{ V}$		5.2		mV
	$I_O = 100\text{ mA}$ , $V_I = 2.94\text{ V}$		52		
	$I_O = 500\text{ mA}$ , $V_I = 2.94\text{ V}$		267		
Pass-element series resistance	$(2.94\text{ V} - V_O)/I_O$ , $V_I = 2.94\text{ V}$ , $I_O = 500\text{ mA}$		0.5		$\Omega$
Input regulation	$V_I = 4\text{ V to }10\text{ V}$ , $50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$		6		mV
Output regulation	$I_O = 5\text{ mA to }500\text{ mA}$ , $4\text{ V} \leq V_I \leq 10\text{ V}$		20		mV
	$I_O = 50\text{ }\mu\text{A to }500\text{ mA}$ , $4\text{ V} \leq V_I \leq 10\text{ V}$		28		mV
Ripple rejection	$f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$	53		dB
		$I_O = 500\text{ mA}$	53		
Output noise-spectral density	$f = 120\text{ Hz}$		2		$\mu\text{V}/\sqrt{\text{Hz}}$
Output noise voltage	$10\text{ Hz} \leq f \leq 100\text{ kHz}$	$C_O = 4.7\text{ }\mu\text{F}$	274		$\mu\text{V}_{\text{rms}}$
		$C_O = 10\text{ }\mu\text{F}$	228		
		$C_O = 100\text{ }\mu\text{F}$	159		
$\overline{\text{RESET}}$ output low voltage	$V_I = 2.6\text{ V}$ , $I_O(\overline{\text{RESET}}) = -0.8\text{ mA}$		0.14		V

<sup>†</sup> CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to  $C_O$ .

<sup>‡</sup> Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

**TPS7333Y electrical characteristics at  $I_O = 10\text{ mA}$ ,  $V_I = 4.3\text{ V}$ ,  $\overline{EN} = 0\text{ V}$ ,  $C_O = 4.7\text{ }\mu\text{F}$  ( $\text{CSR}^\dagger = 1\text{ }\Omega$ ),  $T_J = 25^\circ\text{C}$ , SENSE shorted to OUT (unless otherwise noted)**

PARAMETER	TEST CONDITIONS <sup>‡</sup>	MIN	TYP	MAX	UNIT
Output voltage			3.3		V
Dropout voltage	$I_O = 10\text{ mA}$ , $V_I = 3.23\text{ V}$		4.5		mV
	$I_O = 100\text{ mA}$ , $V_I = 3.23\text{ V}$		44		
	$I_O = 500\text{ mA}$ , $V_I = 3.23\text{ V}$		235		
Pass-element series resistance	$(3.23\text{ V} - V_O)/I_O$ , $V_I = 3.23\text{ V}$ , $I_O = 500\text{ mA}$		0.44		$\Omega$
Input regulation	$V_I = 4.3\text{ V to }10\text{ V}$ , $50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$		6		mV
Output regulation	$I_O = 5\text{ mA to }500\text{ mA}$ , $4.3\text{ V} \leq V_I \leq 10\text{ V}$		21		mV
	$I_O = 50\text{ }\mu\text{A to }500\text{ mA}$ , $4.3\text{ V} \leq V_I \leq 10\text{ V}$		31		mV
Ripple rejection	$f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$	51		dB
		$I_O = 500\text{ mA}$	49		
Output noise-spectral density	$f = 120\text{ Hz}$		2		$\mu\text{V}/\sqrt{\text{Hz}}$
Output noise voltage	$10\text{ Hz} \leq f \leq 100\text{ kHz}$	$C_O = 4.7\text{ }\mu\text{F}$	274		$\mu\text{V}_{\text{rms}}$
		$C_O = 10\text{ }\mu\text{F}$	228		
		$C_O = 100\text{ }\mu\text{F}$	159		
$\overline{\text{RESET}}$ hysteresis voltage			18		mV
$\overline{\text{RESET}}$ output low voltage	$V_I = 2.8\text{ V}$ , $I_O(\overline{\text{RESET}}) = -1\text{ mA}$		0.17		V

<sup>†</sup> CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to  $C_O$ .

<sup>‡</sup> Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.



**TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q**  
**LOW-DROPOUT VOLTAGE REGULATORS**  
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**TPS7348Y electrical characteristics at  $I_O = 10\text{ mA}$ ,  $V_I = 5.85\text{ V}$ ,  $\overline{EN} = 0\text{ V}$ ,  $C_O = 4.7\text{ }\mu\text{F}$  ( $CSRT = 1\text{ }\Omega$ ),  $T_J = 25^\circ\text{C}$ , SENSE shorted to OUT (unless otherwise noted)**

PARAMETER	TEST CONDITIONS‡	MIN	TYP	MAX	UNIT
Output voltage			4.85		V
Dropout voltage	$I_O = 10\text{ mA}$ , $V_I = 4.75\text{ V}$		2.9		mV
	$I_O = 100\text{ mA}$ , $V_I = 4.75\text{ V}$		28		
	$I_O = 500\text{ mA}$ , $V_I = 4.75\text{ V}$		150		
Pass-element series resistance	$(4.75\text{ V} - V_O)/I_O$ , $V_I = 4.75\text{ V}$ , $I_O = 500\text{ mA}$		0.28		$\Omega$
Input regulation	$V_I = 5.85\text{ V to }10\text{ V}$ , $50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$		9		mV
Output regulation	$I_O = 5\text{ mA to }500\text{ mA}$ , $5.85\text{ V} \leq V_I \leq 10\text{ V}$		28		mV
	$I_O = 50\text{ }\mu\text{A to }500\text{ mA}$ , $5.85\text{ V} \leq V_I \leq 10\text{ V}$		42		mV
Ripple rejection	$f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$		53	dB
		$I_O = 500\text{ mA}$		50	
Output noise-spectral density	$f = 120\text{ Hz}$		2		$\mu\text{V}/\sqrt{\text{Hz}}$
Output noise voltage	$10\text{ Hz} \leq f \leq 100\text{ kHz}$	$C_O = 4.7\text{ }\mu\text{F}$		410	$\mu\text{Vrms}$
		$C_O = 10\text{ }\mu\text{F}$		328	
		$C_O = 100\text{ }\mu\text{F}$		212	
$\overline{\text{RESET}}$ hysteresis voltage			26		mV
$\overline{\text{RESET}}$ output low voltage	$I_O(\overline{\text{RESET}}) = -1.2\text{ mA}$ , $V_I = 4.12\text{ V}$		0.2		V

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to  $C_O$ .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.



**TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q**  
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**TPS7350Y electrical characteristics at  $I_O = 10\text{ mA}$ ,  $V_I = 6\text{ V}$ ,  $\overline{EN} = 0\text{ V}$ ,  $C_O = 4.7\text{ }\mu\text{F}$  ( $CSR^\dagger = 1\text{ }\Omega$ ),  $T_J = 25^\circ\text{C}$ , SENSE shorted to OUT (unless otherwise noted)**

PARAMETER	TEST CONDITIONS‡	MIN	TYP	MAX	UNIT
Output voltage			5		V
Dropout voltage	$I_O = 10\text{ mA}$ , $V_I = 4.88\text{ V}$		2.9	6	mV
	$I_O = 100\text{ mA}$ , $V_I = 4.88\text{ V}$		27	35	
	$I_O = 500\text{ mA}$ , $V_I = 4.88\text{ V}$		146	170	
Pass-element series resistance	$(4.88\text{ V} - V_O)/I_O$ , $V_I = 4.88\text{ V}$ , $I_O = 500\text{ mA}$		0.27	0.35	$\Omega$
Input regulation	$V_I = 6\text{ V to }10\text{ V}$ , $50\text{ }\mu\text{A} \leq I_O \leq 500\text{ mA}$		4	25	mV
Output regulation	$I_O = 5\text{ mA to }500\text{ mA}$ , $6\text{ V} \leq V_I \leq 10\text{ V}$		28	75	mV
	$I_O = 50\text{ }\mu\text{A to }500\text{ mA}$ , $6\text{ V} \leq V_I \leq 10\text{ V}$		41		mV
Ripple rejection	$f = 120\text{ Hz}$	$I_O = 50\text{ }\mu\text{A}$		53	dB
		$I_O = 500\text{ mA}$		51	
Output noise-spectral density	$f = 120\text{ Hz}$		2		$\mu\text{V}/\sqrt{\text{Hz}}$
Output noise voltage	$10\text{ Hz} \leq f \leq 100\text{ kHz}$	$C_O = 4.7\text{ }\mu\text{F}$		430	$\mu\text{Vrms}$
		$C_O = 10\text{ }\mu\text{F}$		345	
		$C_O = 100\text{ }\mu\text{F}$		220	
$\overline{\text{RESET}}$ hysteresis voltage			28		mV
$\overline{\text{RESET}}$ output low voltage	$I_O(\overline{\text{RESET}}) = -1.2\text{ mA}$ , $V_I = 4.25\text{ V}$		0.15	0.4	V

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to  $C_O$ .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

PARAMETER MEASUREMENT INFORMATION

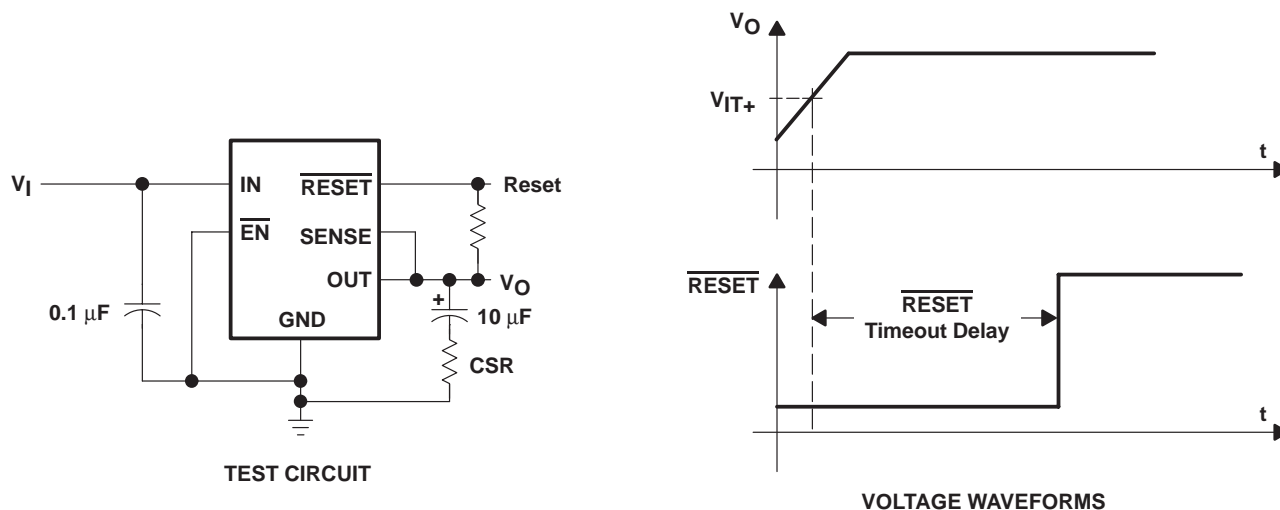
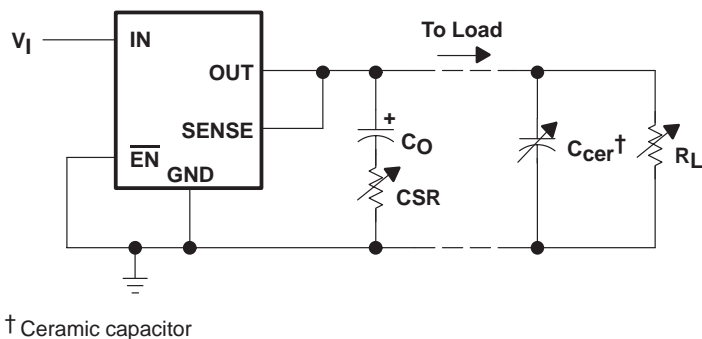


Figure 5. Test Circuit and Voltage Waveforms



† Ceramic capacitor

Figure 6. Test Circuit for Typical Regions of Stability (Refer to Figures 29 through 32)

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**TYPICAL CHARACTERISTICS**

**Table of Graphs**

$I_Q$	Quiescent current		vs Output current	7
			vs Input voltage	8
$I_Q$	Quiescent current	TPS7348	vs Free-air temperature	9
$I_Q$	Quiescent current	TPS7325	vs Input voltage	10
			vs Free-air temperature	11
$V_{DO}$	Dropout voltage		vs Output current	12
$\Delta V_{DO}$	Change in dropout voltage		vs Free-air temperature	13
$V_{DO}$	Dropout voltage	TPS7301	vs Output current	14
$\Delta V_O$	Change in output voltage		vs Free-air temperature	15
$V_O$	Output voltage		vs Input voltage	16
$V_O$	Output voltage	TPS7325	vs Input voltage	17
	Line regulation			18
$V_O$	Output voltage	TPS7301	vs Output current	19
		TPS7325	vs Output current	20
		TPS7330	vs Output current	21
		TPS7333	vs Output current	22
		TPS7348	vs Output current	23
		TPS7350	vs Output current	24
	Output voltage response from enable ( $\overline{EN}$ )			25
	Load transient response	TPS7301 or TPS7333		26
		TPS7325		27
		TPS7348 or TPS7350		28
		TPS7301		29
		TPS7333		30
		TPS7348 or TPS7350		31
	Ripple rejection		vs Frequency	32
	Output spectral noise density		vs Frequency	33
	Compensation series resistance (CSR)	$C_O = 4.7 \mu\text{F}$	vs Output current	34
			vs Added ceramic capacitance	35
		$C_O = 10 \mu\text{F}$	vs Output current	36
			vs Added ceramic capacitance	37
$r_{DS(on)}$	Pass-element resistance		vs Input voltage	38
$V_I$	Minimum input voltage for valid $\overline{\text{RESET}}$		vs Free-air temperature	39
$V_{IT-}$	Negative-going reset threshold		vs Free-air temperature	40
$I_{OL(\text{RESET})}$	$\overline{\text{RESET}}$ output current		vs Input voltage	41
$t_d$	Reset time delay		vs Free-air temperature	42
$t_d$	Distribution for reset delay			43

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**APPLICATION INFORMATION**

**external capacitor requirements (continued)**

As with most LDO regulators, the TPS73xx family requires an output capacitor for stability. A low-ESR 10- $\mu$ F solid-tantalum capacitor connected from the regulator output to ground is sufficient to ensure stability over the full load range (see Figure 42). Adding high-frequency ceramic or film capacitors (such as power-supply bypass capacitors for digital or analog ICs) can cause the regulator to become unstable unless the ESR of the tantalum capacitor is less than 1.2  $\Omega$  over temperature. Capacitors with published ESR specifications such as the AVX TPSD106M035R0300 and the Sprague 593D106X0035D2W work well because the maximum ESR at 25°C is 300 m $\Omega$  (typically, the ESR in solid-tantalum capacitors increases by a factor of 2 or less when the temperature drops from 25°C to -40°C). Where component height and/or mounting area is a problem, physically smaller, 10- $\mu$ F devices can be screened for ESR. Figures 29 through 32 show the stable regions of operation using different values of output capacitance with various values of ceramic load capacitance.

In applications with little or no high-frequency bypass capacitance (< 0.2  $\mu$ F), the output capacitance can be reduced to 4.7  $\mu$ F, provided ESR is maintained between 0.7 and 2.5  $\Omega$ . Because capacitor minimum ESR is seldom if ever specified, it may be necessary to add a 0.5- $\Omega$  to 1- $\Omega$  resistor in series with the capacitor and limit ESR to 1.5  $\Omega$  maximum. As shown in the CSR graphs (Figures 29 through 32), minimum ESR is not a problem when using 10- $\mu$ F or larger output capacitors.

Below is a partial listing of surface-mount capacitors usable with the TPS73xx family. This information, along with the CSR graphs, is included to assist in selection of suitable capacitance for the user's application. When necessary to achieve low height requirements along with high output current and/or high ceramic load capacitance, several higher ESR capacitors can be used in parallel to meet the guidelines above.

All load and temperature conditions with up to 1  $\mu$ F of added ceramic load capacitance:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
T421C226M010AS	Kemet	22 $\mu$ F, 10 V	0.5	2.8 × 6 × 3.2
593D156X0025D2W	Sprague	15 $\mu$ F, 25 V	0.3	2.8 × 7.3 × 4.3
593D106X0035D2W	Sprague	10 $\mu$ F, 35 V	0.3	2.8 × 7.3 × 4.3
TPSD106M035R0300	AVX	10 $\mu$ F, 35 V	0.3	2.8 × 7.3 × 4.3

Load < 200 mA, ceramic load capacitance < 0.2  $\mu$ F, full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
592D156X0020R2T	Sprague	15 $\mu$ F, 20 V	1.1	1.2 × 7.2 × 6
595D156X0025C2T	Sprague	15 $\mu$ F, 25 V	1	2.5 × 7.1 × 3.2
595D106X0025C2T	Sprague	10 $\mu$ F, 25 V	1.2	2.5 × 7.1 × 3.2
293D226X0016D2W	Sprague	22 $\mu$ F, 16 V	1.1	2.8 × 7.3 × 4.3

Load < 100 mA, ceramic load capacitance < 0.2  $\mu$ F, full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
195D106X06R3V2T	Sprague	10 $\mu$ F, 6.3 V	1.5	1.3 × 3.5 × 2.7
195D106X0016X2T	Sprague	10 $\mu$ F, 16 V	1.5	1.3 × 7 × 2.7
595D156X0016B2T	Sprague	15 $\mu$ F, 16 V	1.8	1.6 × 3.8 × 2.6
695D226X0015F2T	Sprague	22 $\mu$ F, 15 V	1.4	1.8 × 6.5 × 3.4
695D156X0020F2T	Sprague	15 $\mu$ F, 20 V	1.5	1.8 × 6.5 × 3.4
695D106X0035G2T	Sprague	10 $\mu$ F, 35 V	1.3	2.5 × 7.6 × 2.5

† Size is in mm. ESR is maximum resistance at 100 kHz and T<sub>A</sub> = 25°C. Listings are sorted by height.



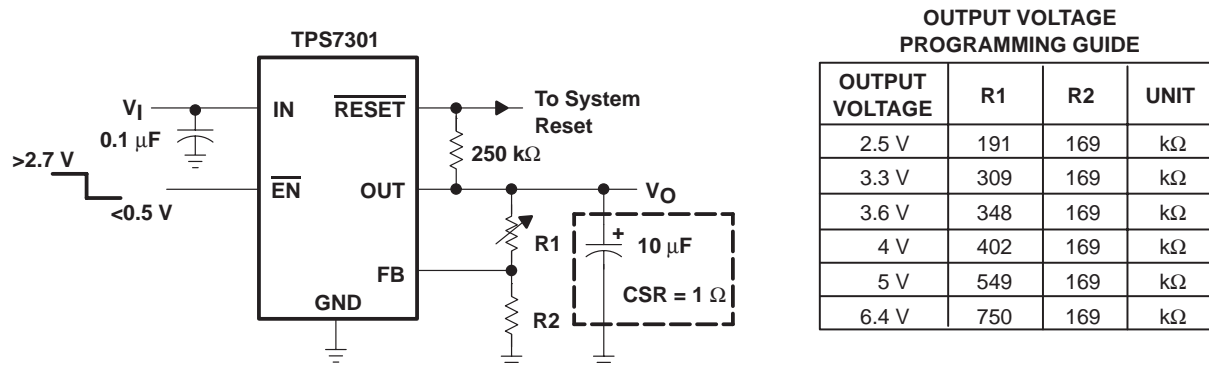
**TPS7301Q, TPS7325Q, TPS7330Q, TPS7333Q, TPS7348Q, TPS7350Q**  
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Resistors R1 and R2 should be chosen for approximately 7- $\mu$ A divider current. A recommended value for R2 is 169 k $\Omega$  with R1 adjusted for the desired output voltage. Smaller resistors can be used, but offer no inherent advantage and consume more power. Larger values of R1 and R2 should be avoided as leakage currents at FB will introduce an error. Solving for R1 yields a more useful equation for choosing the appropriate resistance:

$$R1 = \left( \frac{V_O}{V_{ref}} - 1 \right) \times R2$$



**Figure 48. TPS7301 Adjustable LDO Regulator Programming**

**undervoltage supervisor function**

The  $\overline{\text{RESET}}$  output of the TPS73xx initiates a reset in microcomputer and microprocessor systems in the event of an undervoltage condition. An internal comparator in the TPS73xx monitors the output voltage of the regulator to detect the undervoltage condition. When that occurs, the  $\overline{\text{RESET}}$  output transistor turns on taking the  $\overline{\text{RESET}}$  signal low.

On power up, the output voltage tracks the input voltage. The  $\overline{\text{RESET}}$  output becomes active (low) as  $V_{I1}$  approaches the minimum required for a valid  $\overline{\text{RESET}}$  signal (specified at 1.5 V for 25°C and 1.9 V over full recommended operating temperature range). When the output voltage reaches the appropriate positive-going input threshold ( $V_{IT+}$ ), a 200-ms (typical) timeout period begins during which the  $\overline{\text{RESET}}$  output remains low. Once the timeout has expired, the  $\overline{\text{RESET}}$  output becomes inactive. Since the  $\overline{\text{RESET}}$  output is an open-drain NMOS, a pullup resistor should be used to ensure that a logic-high signal is indicated.

The supply-voltage-supervisor function is also activated during power-down. As the input voltage decays and after the dropout voltage is reached, the output voltage tracks linearly with the decaying input voltage. When the output voltage drops below the specified negative-going input threshold ( $V_{IT-}$  — see electrical characteristics tables), the  $\overline{\text{RESET}}$  output becomes active (low). It is important to note that if the input voltage decays below the minimum required for a valid  $\overline{\text{RESET}}$ , the  $\overline{\text{RESET}}$  is undefined.

Since the circuit is monitoring the regulator output voltage, the  $\overline{\text{RESET}}$  output can also be triggered by disabling the regulator or by any fault condition that causes the output to drop below  $V_{IT-}$ . Examples of fault conditions include a short circuit on the output and a low input voltage. Once the output voltage is reestablished, either by reenabling the regulator or removing the fault condition, then the internal timer is initiated, which holds the  $\overline{\text{RESET}}$  signal active during the 200-ms (typical) timeout period.



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TPS7301QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS7301QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS7301QP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TPS7301QPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TPS7301QPW	ACTIVE	TSSOP	PW	20	70	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPS7301QPWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI
TPS7301QPWR	ACTIVE	TSSOP	PW	20	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPS7325QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS7325QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS7325QDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS7325QP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TPS7325QPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TPS7325QPW	ACTIVE	TSSOP	PW	20	70	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPS7325QPWR	ACTIVE	TSSOP	PW	20	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPS7330QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS7330QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS7330QP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TPS7330QPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TPS7330QPW	ACTIVE	TSSOP	PW	20	70	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPS7330QPWR	ACTIVE	TSSOP	PW	20	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPS7333QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS7333QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS7333QDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS7333QP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TPS7333QPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TPS7333QPW	ACTIVE	TSSOP	PW	20	70	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPS7333QPWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI
TPS7333QPWR	ACTIVE	TSSOP	PW	20	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPS7348QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TPS7348QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS7348QDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS7348QP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TPS7348QPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TPS7348QPW	ACTIVE	TSSOP	PW	20	70	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPS7348QPWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI
TPS7348QPWR	ACTIVE	TSSOP	PW	20	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPS7350QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS7350QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS7350QP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TPS7350QPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TPS7350QPW	ACTIVE	TSSOP	PW	20	70	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPS7350QPWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI
TPS7350QPWR	ACTIVE	TSSOP	PW	20	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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