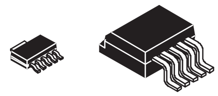


LOW INPUT VOLTAGE, 1-A LOW-DROPOUT LINEAR REGULATORS WITH SUPERVISOR

FEATURES

- **1-A Low-Dropout Regulator Supports Input Voltages Down to 1.8-V**
- **Available in 1.26-V, 1.5-V, 1.6-V, 1.8-V, 2.5-V**
- **Stable With Any Type/Value Output Capacitor**
- **±2% Output Voltage Tolerance Over Line, Load, and Temperature (–40°C to +125°C)**
- **Integrated Supervisor (SVS) With 200-ms $\overline{\text{RESET}}$ Delay Time**
- **Low 170-mV Dropout Voltage at 1 A (TPS72625)**
- **Low 210-µA Ground Current at Full Load**
- **Less than 1-µA Standby Current**
- **Integrated UVLO with Thermal and Overcurrent Protection**
- **5-Lead SOT223 or DDPAK Surface-Mount Package**

APPLICATIONS

- **PCI Cards**
- **Modem Banks and Telecom Boards**
- **DSP, FPGA, and Microprocessor Power Supplies**
- **Portable, Battery-Powered Applications**
- **1.26-V Core Voltage for the Following DSPs:**
  - **TMS320vC5501**
  - **TMS320vC5502**

DESCRIPTION

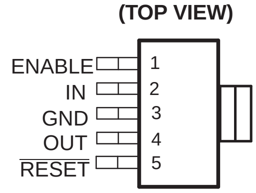
The TPS726xx family of 1-A low-dropout (LDO) linear regulators has fixed voltage options available that are commonly used to power the latest DSPs, FPGAs, and microcontrollers. The integrated supervisory circuitry provides an active low $\overline{\text{RESET}}$ signal when the output falls out of regulation. The no capacitor/any capacitor feature allows the customer to tailor output transient performance as needed. Therefore, compared to other regulators capable of providing the same output current, this family of regulators can provide a stand alone power supply solution or a post regulator for a switch mode power supply.

These regulators operate over a wide range of input voltages (1.8 V to 6 V) and have very low dropout (170 mV at 1-A). Ground current is typically 210 µA at full load and drops to less than 80 µA at no load. Standby current is less than 1 µA.

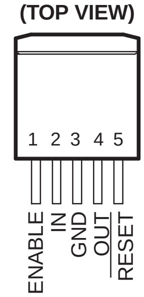
Unlike some regulators that have a minimum current requirement, the TPS726xx family is stable with no output load current. The low noise capability of this family, coupled with its high current operation and ease of power dissipation, make it ideal for telecom boards, modem banks, and other noise sensitive applications.

The TPS726xx is available in either a SOT223 or DDPAK package. The TPS726126 is available in a SOT223 package only.

DCQ PACKAGE
SOT223-5
(TOP VIEW)



KTT PACKAGE
DDPAK
(TOP VIEW)



Note: Tab is GND for both packages

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT}
TPS726***xxxyyyz***	**XXX** is nominal output voltage (for example, 126 = 1.26V, 15 = 1.5V). **YYY** is package designator. **Z** is package quantity.

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		UNIT
Input voltage, V_I (2)	–0.3 to 7	V
Voltage range at EN	–0.3 to V_I + 0.3	V
Voltage on $\overline{RESET}$	V_{IN} + 0.3	V
Voltage on OUT	6	V
ESD rating, HBM	2	kV
Continuous total power dissipation	See Dissipation Rating Table	
Operating junction temperature range, T_J	–50 to 150	°C
Maximum junction temperature range, T_J	150	°C
Storage temperature, T_{stg}	–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

PACKAGE DISSIPATION RATINGS

PACKAGE	BOARD	$R_{\theta JC}$	$R_{\theta JA}$
DDPAK	High K(1)	2 °C/W	23 °C/W
SOT223	Low K(2)	15 °C/W	53 °C/W

(1) The JEDEC high K (2s2p) board design used to derive this data was a 3-inch x 3-inch (7,5-cm x 7,5-cm), multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.
(2) The JEDEC low K (1s) board design used to derive this data was a 3-inch x 3-inch (7,5-cm x 7,5-cm), two-layer board with 2 ounce copper traces on top of the board.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range $V_I = V_{O(typ)} + 1$ V, I_O= 1 mA, EN = IN, C_O = 1 µF, C_I = 1 µF (unless otherwise noted). Typical values are at +25°C.

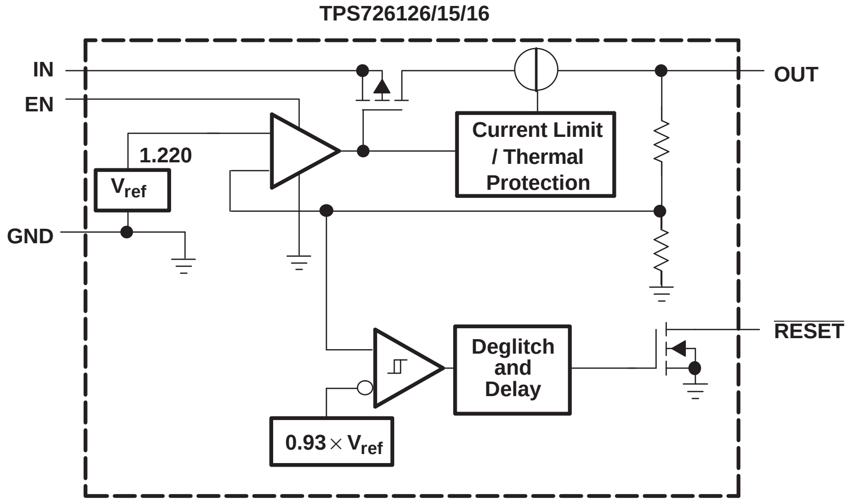
PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_I (1)	Input voltage				1.8		6	V
I_O	Continuous output current				0		1	A
	Bandgap voltage reference				1.177	1.220	1.263	V
V_O	Output voltage	TPS726126	0 µA < I_O < 1 A	1.8 V ≤ V_I ≤ 5.5 V	1.222	1.26	1.298	V
		TPS72615	0 µA < I_O < 1 A	1.8 V ≤ V_I ≤ 5.5 V	1.47	1.5	1.53	
		TPS72616	0 µA < I_O < 1 A	2.6 V ≤ V_I ≤ 5.5 V	1.568	1.6	1.632	
		TPS72618	0 µA < I_O < 1 A	2.8 V ≤ V_I ≤ 5.5 V	1.764	1.8	1.836	
		TPS72625	0 µA < I_O < 1 A	3.5 V ≤ V_I ≤ 5.5 V	2.45	2.5	2.55	
I	Ground current		I_O = 0 µA			75	120	µA
			I_O = 1 A			210	300	
	Standby current		EN < 0.4 V			0.2	1	µA
V_n	Output noise voltage		BW = 200 Hz to 100 kHz	C_O = 10 µF		150		µV
PSRR	Ripple rejection		f = 1 kHz, C_o = 10 µF			60		dB
	Current limit (2)				1.1	1.6	2.3	A
	Output voltage line regulation ($\Delta V_O/V_O$) (3)		V_O + 1 V < V_I ≤ 5.5 V		–0.15	0.02	0.15	%/V
	Output voltage load regulation		0 µA < I_O < 1 A		–0.25	0.05	0.25	%/A
V_{IH}	EN high level input				1.3			V
V_{IL}	EN low level input				–0.2		0.4	
I_I	EN input current		EN = 0 V or V_I			0.01	100	nA
	UVLO threshold		V_{CC} rising		1.45	1.57	1.70	V
	UVLO hysteresis		V_{CC} rising			50		mV
	UVLO deglitch		V_{CC} rising			10		µs
	UVLO delay		V_{CC} rising			100		µs
V_{DO}	Dropout voltage (4)	TPS72625	I_O = 1 A			170	280	mV
		TPS72618	I_O = 1 A			210	320	
$\overline{RESET}$	Minimum input voltage for valid $\overline{RESET}$ (V_{RES})				1.3			V
	Trip threshold voltage				90	93	96	%V_O
	Hysteresis voltage					10		mV
	$t_{(RESET)}$ delay time				100	200	300	ms
	Rising edge deglitch					10		µs
	Output low voltage (at 700 µA)				–0.3		0.4	V
	Leakage current						100	nA
T_J	Operating junction temperature				–40		+125	°C

(1) Minimum V_{IN} is 1.800 V or $V_O + V_{DO}$, whichever is greater.
(2) Test condition includes, output voltage $V_O = V_O$ – 15% and pulse duration = 10 ms.
(3) $V_{Imin} = (V_O + 1)$ or 1.8 V whichever is greater.

$$\text{Line regulation (mV)} = (\%/\text{V}) \times \frac{V_O\left(5.5\text{ V} - V_{Imin}\right)}{100} \times 1000$$

(4) Dropout voltage is defined as the differential voltage between V_O and V_I when V_O drops 100 mV below the value measured with $V_I = V_O + 1$ V.

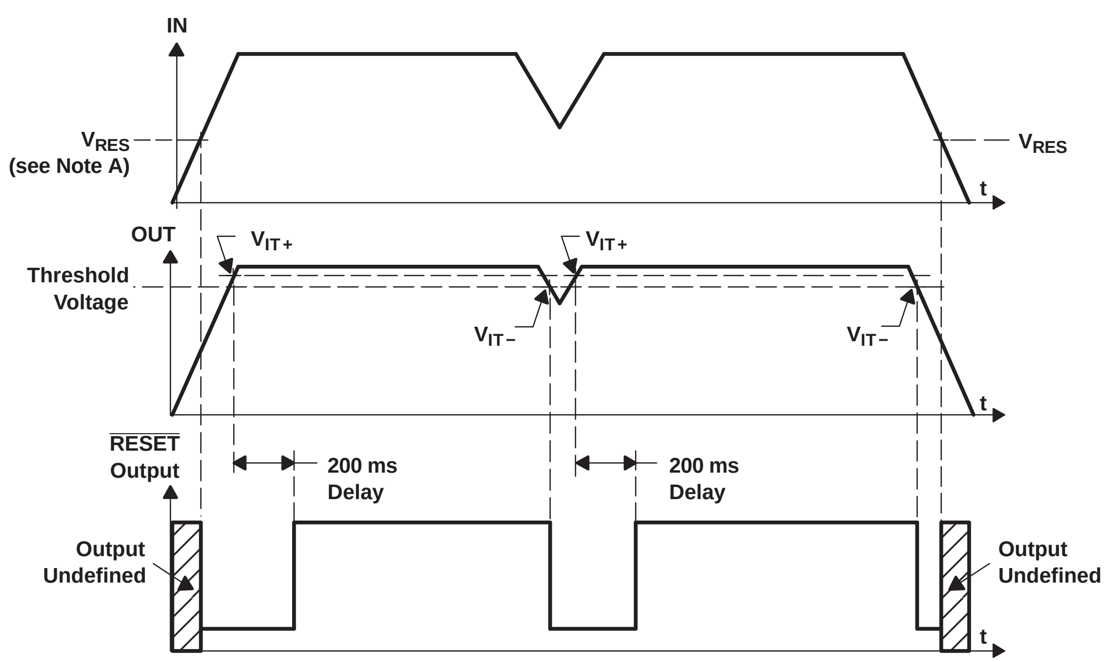
FUNCTIONAL BLOCK DIAGRAM



Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
GND	3	Ground
ENABLE	1	Enable input
IN	2	Input supply voltage
$\overline{\text{RESET}}$	5	This terminal is the $\overline{\text{RESET}}$ output. When used with a pull-up resistor, this open-drain output provides the active low $\overline{\text{RESET}}$ signal when the regulator output voltage drops more than 5% below its nominal output voltage. The $\overline{\text{RESET}}$ delay time is typically 200 ms.
OUT	4	Regulated output voltage

$\overline{\text{RESET}}$ TIMING DIAGRAM



NOTES:A. V_{RES} is the minimum input voltage for a valid $\overline{\text{RESET}}$.

TYPICAL CHARACTERISTICS

TPS72618 OUTPUT VOLTAGE vs OUTPUT CURRENT

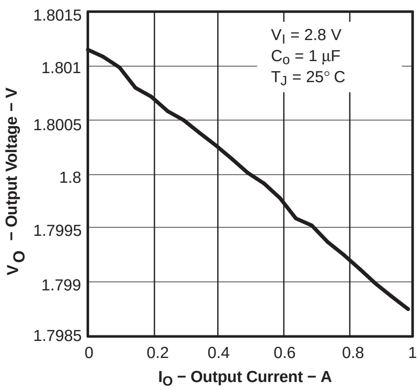


Figure 1.

TPS72618 OUTPUT VOLTAGE vs JUNCTION TEMPERATURE

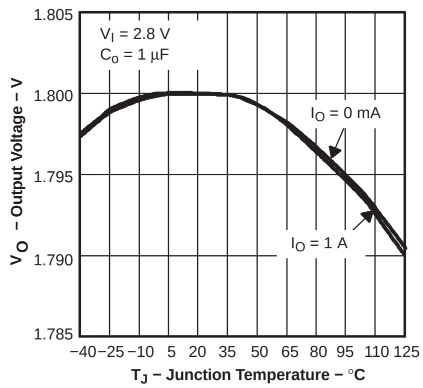


Figure 2.

TPS72618 GROUND CURRENT vs JUNCTION TEMPERATURE

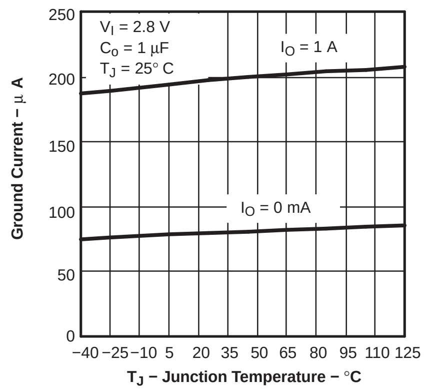


Figure 3.

TPS72618 GROUND CURRENT vs OUTPUT CURRENT

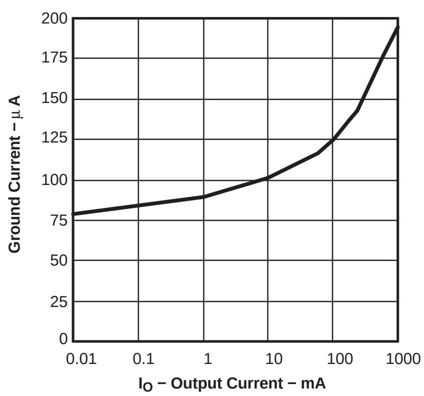


Figure 4.

TPS72625 DC DROPOUT VOLTAGE vs OUTPUT CURRENT

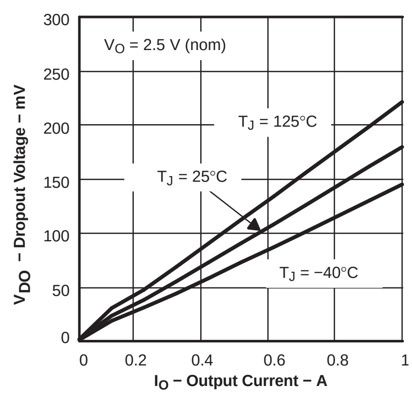


Figure 5.

TPS72618 DROPOUT VOLTAGE vs JUNCTION TEMPERATURE

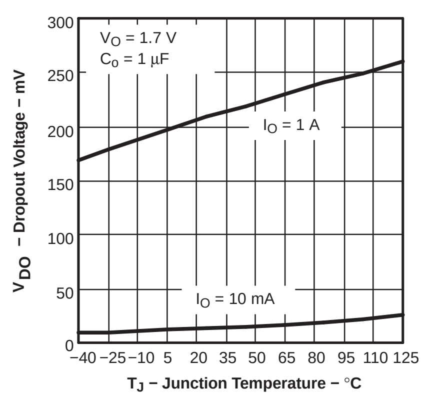


Figure 6.

MINIMUM REQUIRED INPUT VOLTAGE vs OUTPUT VOLTAGE

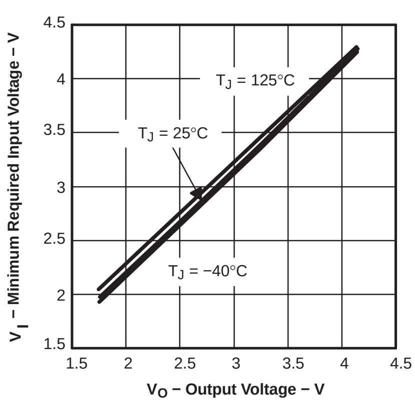


Figure 7.

TPS72618 LINE TRANSIENT RESPONSE

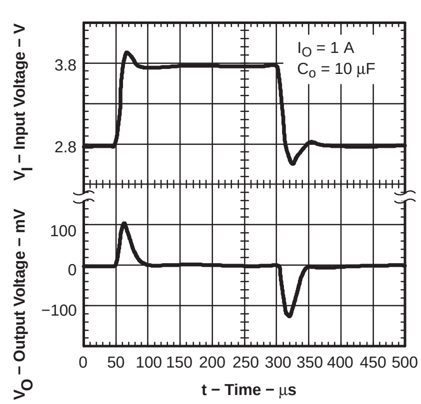


Figure 8.

TPS72618 LOAD TRANSIENT RESPONSE

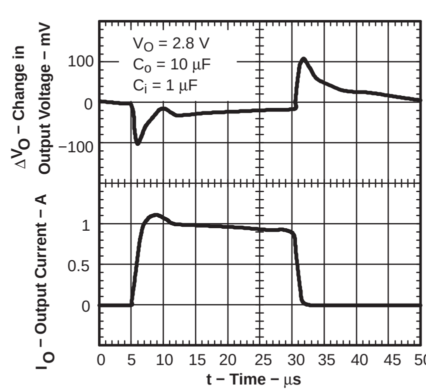


Figure 9.

TYPICAL CHARACTERISTICS (continued)

TPS72618 LOAD TRANSIENT RESPONSE

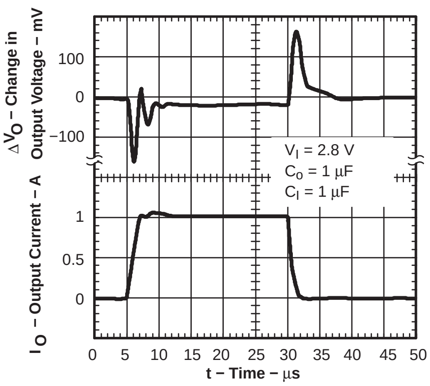


Figure 10.

TPS72618 OUTPUT VOLTAGE, ENABLE VOLTAGE vs TIME (START-UP)

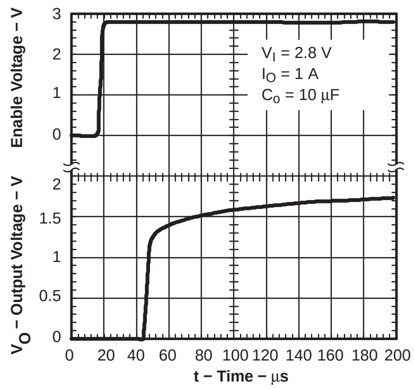


Figure 11.

TPS72618 POWER UP/POWER DOWN

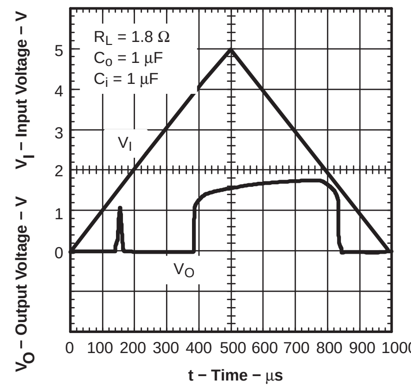


Figure 12.

TPS72618 OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

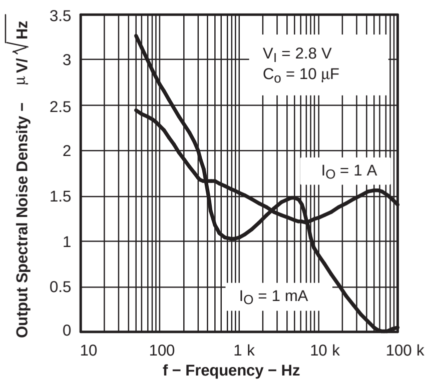


Figure 13.

OUTPUT IMPEDANCE vs FREQUENCY

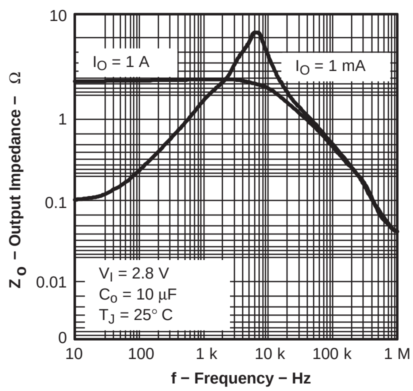


Figure 14.

TPS72618 RIPPLE REJECTION vs FREQUENCY

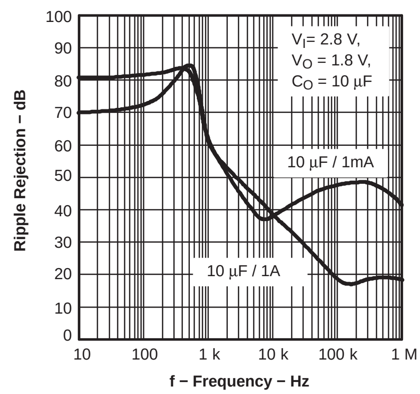


Figure 15.

CURRENT LIMIT vs INPUT VOLTAGE

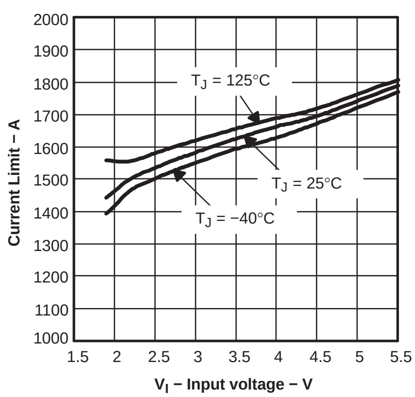


Figure 16.

TPS72615 GROUND CURRENT vs INPUT VOLTAGE

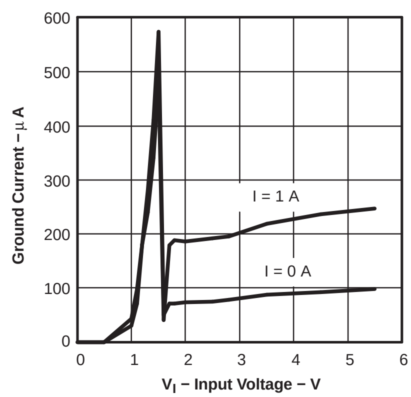


Figure 17.

DROPOUT VOLTAGE vs INPUT VOLTAGE

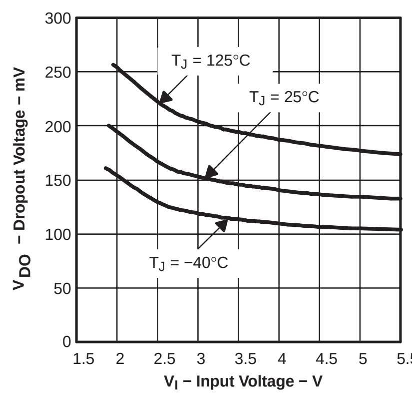


Figure 18.

APPLICATION INFORMATION

The TPS726xx family of low-dropout (LDO) regulators have numerous features that make it apply to a wide range of applications. The family operates with very low input voltage (≥1.8 V) and low dropout voltage (typically 200 mV at full load), making it an efficient stand-alone power supply or post regulator for battery or switch mode power supplies. Both the active low $\overline{\text{RESET}}$ and 1-A output current, make the TPS726xx family ideal for powering processor and FPGA supplies. The TPS726xx family also has low output noise (typically 150 μV_{RMS} with 10-µF output capacitor), making it ideal for use in telecom equipment.

External Capacitor Requirements

A 1-µF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS726xx, is required for stability. To improve transient response, noise rejection, and ripple rejection, an additional 10-µF or larger, low ESR capacitor is recommended. A higher-value, low ESR input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source, especially if the minimum input voltage of 1.8 V is used.

Although an output capacitor is not required for stability, transient response and output noise are improved with a 10-µF output capacitor.

Regulator Protection

The TPS726xx pass element has a built-in back diode that safely conducts reverse current when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage is anticipated, external limiting might be appropriate.

The TPS726xx also features internal current limiting and thermal protection. During normal operation, the TPS726xx limits output current to approximately 1.6 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below 145°C, regulator operation resumes.

THERMAL INFORMATION

The amount of heat that an LDO linear regulator generates is directly proportional to the amount of power it dissipates during operation. All integrated circuits have a maximum allowable junction temperature ($T_J$max) above which normal operation is not assured. A system designer must design the operating environment so that the operating junction temperature (T_J) does not exceed the maximum junction temperature ($T_J$max). The two main environmental variables that a designer can use to improve thermal performance are air flow and external heatsinks. The purpose of this information is to aid the designer in determining the proper operating environment for a linear regulator that is operating at a specific power level.

In general, the maximum expected power ($P_{D(max)}$) consumed by a linear regulator is computed as:

$$P_D max = \left(V_{I(avg)} - V_{O(avg)}\right) \times I_{O(avg)} + V_{I(avg)} \times I_{(Q)} \tag{1}$$

Where:

- $V_{I(avg)}$ is the average input voltage.
- $V_{O(avg)}$ is the average output voltage.
- $_{O(avg)}$ is the average output current.
- $I_{(Q)}$ is the quiescent current.

For most TI LDO regulators, the quiescent current is insignificant compared to the average output current; therefore, the term $V_{I(avg)}$ x $I_{(Q)}$ can be neglected. The operating junction temperature is computed by adding the ambient temperature (T_A) and the increase in temperature due to the regulator's power dissipation. The temperature rise is computed by multiplying the maximum expected power dissipation by the sum of the thermal resistances between the junction and the case ®$_{\theta JC}$), the case to heatsink ®$_{\theta CS}$), and the heatsink to ambient ®$_{\theta SA}$). Thermal resistances are measures of how effectively an object dissipates heat. Typically, the larger the device, the more surface area available for power dissipation and the lower the object's thermal resistance.

THERMAL INFORMATION (continued)

Figure 19 illustrates these thermal resistances for (a) a SOT223 package mounted in a JEDEC low-K board, and (b) a DDPAK package mounted on a JEDEC high-K board.

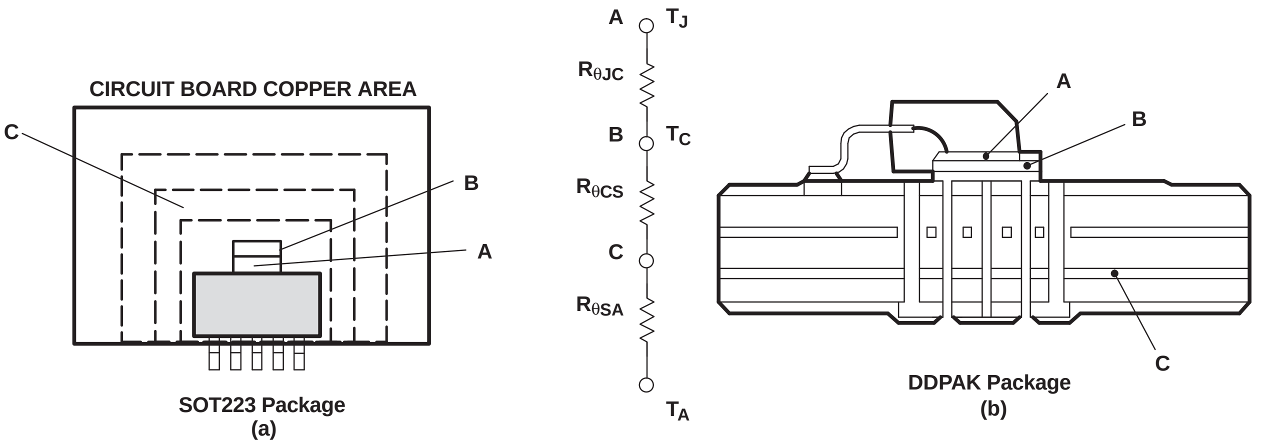


Figure 19. Thermal Resistances

Equation 2 summarizes the computation:

$$T_J = T_A + P_D\max \times \left(R_{\theta JC} + R_{\theta CS} + R_{\theta SA}\right) \tag{2}$$

The $R_{\theta JC}$ is specific to each regulator as determined by its package, lead frame, and die size provided in the regulator's data sheet. The $R_{\theta SA}$ is a function of the type and size of heatsink. For example, *black body radiator* type heatsinks can have $R_{\theta CS}$ values ranging from 5°C/W for very large heatsinks to 50°C/W for very small heatsinks. The $R_{\theta CS}$ is a function of how the package is attached to the heatsink. For example, if a thermal compound is used to attach a heatsink to a SOT223 package, $R_{\theta CS}$of 1°C/W is reasonable.

Even if no external *black body radiator* type heatsink is attached to the package, the board on which the regulator is mounted provides some heatsinking through the pin solder connections. Some packages, like the DDPAK and SOT223 packages, use a copper plane underneath the package or the circuit board's ground plane for additional heatsinking to improve their thermal performance. Computer-aided thermal modeling can be used to compute very accurate approximations of an integrated circuit's thermal performance in different operating environments (e.g., different types of circuit boards, different types and sizes of heatsinks, and different air flows, etc.). Using these models, the three thermal resistances can be combined into one thermal resistance between junction and ambient ®$_{\theta JA}$). This $R_{\theta JA}$is valid only for the specific operating environment used in the computer model.

Equation 2 simplifies into Equation 3:

$$T_J = T_A + P_D\max \times R_{\theta JA} \tag{3}$$

Rearranging Equation 3 gives Equation 4:

$$R_{\theta JA} = \frac{T_J - T_A}{P_D\max} \tag{4}$$

Using Equation 3 and the computer model generated curves shown in Figure 20 and Figure 23, a designer can quickly compute the required heatsink thermal resistance/board area for a given ambient temperature, power dissipation, and operating environment.

DDPAK Power Dissipation

The DDPAK package provides an effective means of managing power dissipation in surface mount applications. The DDPAK package dimensions are provided in the *Mechanical Data* section at the end of the data sheet. The addition of a copper plane directly underneath the DDPAK package enhances the thermal performance of the package.

THERMAL INFORMATION (continued)

To illustrate, the TPS72625 in a DDPAK package was chosen. For this example, the average input voltage is 5 V, the output voltage is 2.5 V, the average output current is 1 A, the ambient temperature 55°C, the air flow is 150 LFM, and the operating environment is the same as documented below. Neglecting the quiescent current, the maximum average power is:

$$P_D max = (5 - 2.5)\ V \times 1\ A = 2.5\ W \quad (5)$$

Substituting $T_J$max for T_J into Equation 4 gives Equation 6:

$$R_{\theta JA} max = (125 - 55)°C / 2.5\ W = 28°C/W \quad (6)$$

From Figure 20, *DDPAK Thermal Resistance vs Copper Heatsink Area*, the ground plane needs to be 1 cm^2 for the part to dissipate 2.5 W. The operating environment used in the computer model to construct Figure 20 consisted of a standard JEDEC High-K board (2S2P) with a 1 oz. internal copper plane and ground plane. The package is soldered to a 2 oz. copper pad. The pad is tied through thermal vias to the 1 oz. ground plane. Figure 21 shows the side view of the operating environment used in the computer model.

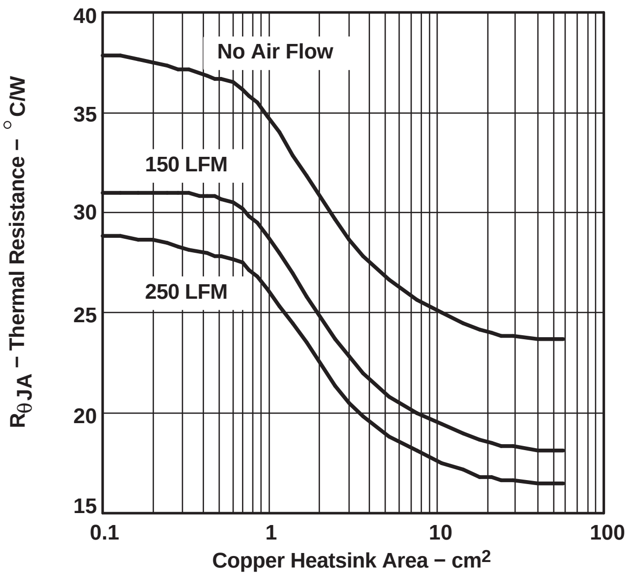


Figure 20. DDPAK Thermal Resistance vs Copper Heatsink Area

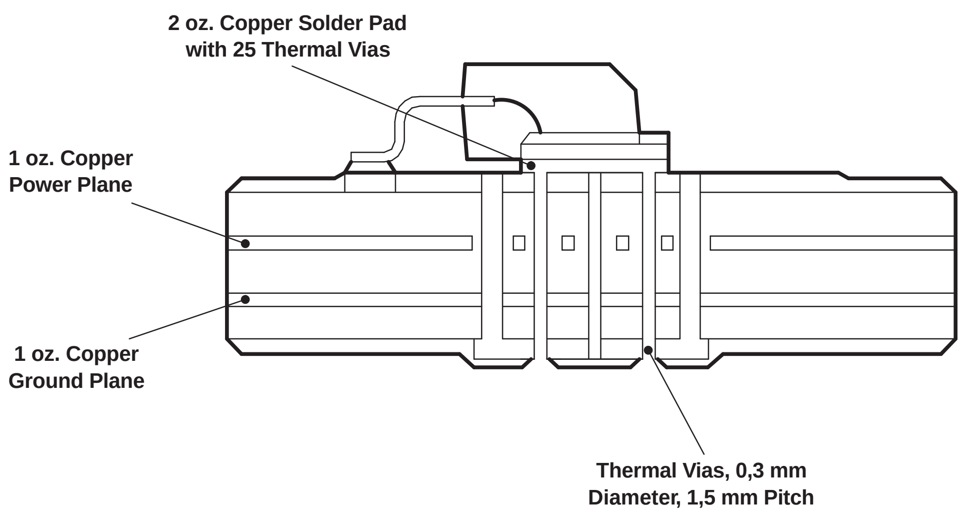


Figure 21. DDPAK Thermal Resistance

THERMAL INFORMATION (continued)

From the data in Figure 22 and rearranging Equation 4, the maximum power dissipation for a different ground plane area and a specific ambient temperature can be computed.

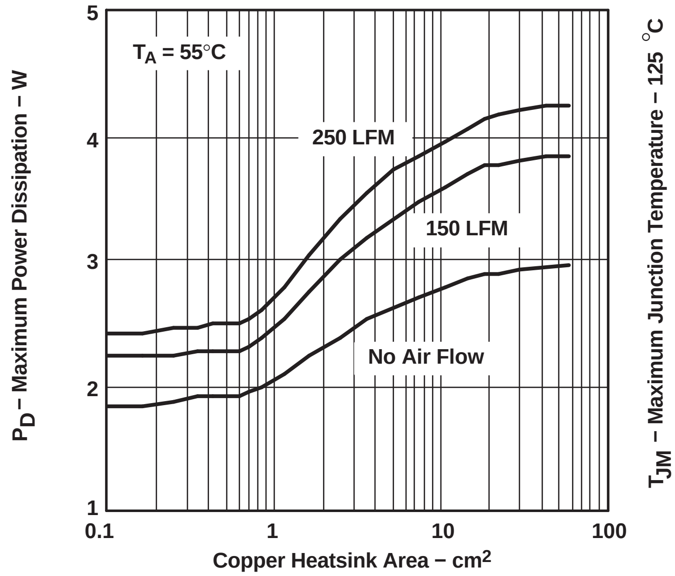


Figure 22. Maximum Power Dissipation vs Copper Heatsink Area

SOT223 Power Dissipation

The SOT223 package provides an effective means of managing power dissipation in surface mount applications. The SOT223 package dimensions are provided in the *Mechanical Data* section at the end of the data sheet. The addition of a copper plane directly underneath the SOT223 package enhances the thermal performance of the package.

To illustrate, the TPS72625 in a SOT223 package was chosen. For this example, the average input voltage is 3.3 V, the output voltage is 2.5 V, the average output current is 1 A, the ambient temperature 55°C, no air flow is present, and the operating environment is the same as documented below. Neglecting the quiescent current, the maximum average power is:

$$P_D max = (3.3 - 2.5) V \times 1 A = 800 mW \quad (7)$$

Substituting $T_J$max for T_J into Equation 4 gives Equation 8:

$$R_{\theta JA} max = (125 - 55)°C/800 mW = 87.5°C/W \quad (8)$$

From Figure 23, *$R_{\theta JA}$ vs PCB Copper Area*, the ground plane needs to be 0.55 in^2 for the part to dissipate 800 mW. The operating environment used to construct Figure 23 consisted of a board with 1 oz. copper planes. The package is soldered to a 1 oz. copper pad on the top of the board. The pad is tied through thermal vias to the 1 oz. ground plane.

THERMAL INFORMATION (continued)

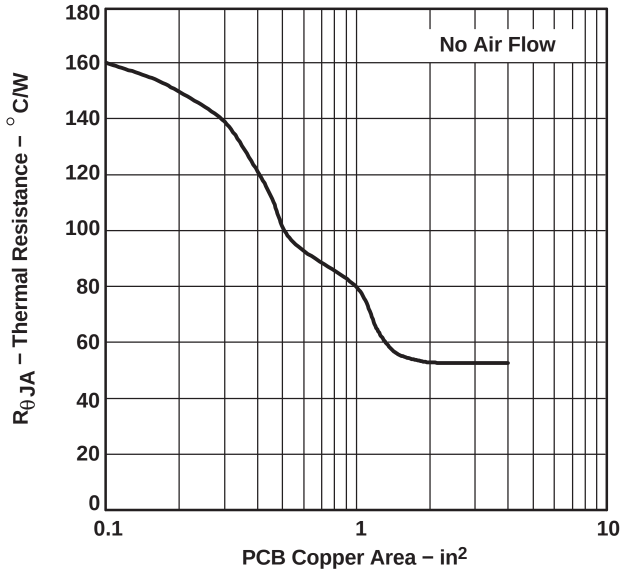


Figure 23. SOT223 Thermal Resistance vs PCB AREA

From the data in Figure 23 and rearranging Equation 4, the maximum power dissipation for a different ground plane area and a specific ambient temperature can be computed (as shown in Figure 24).

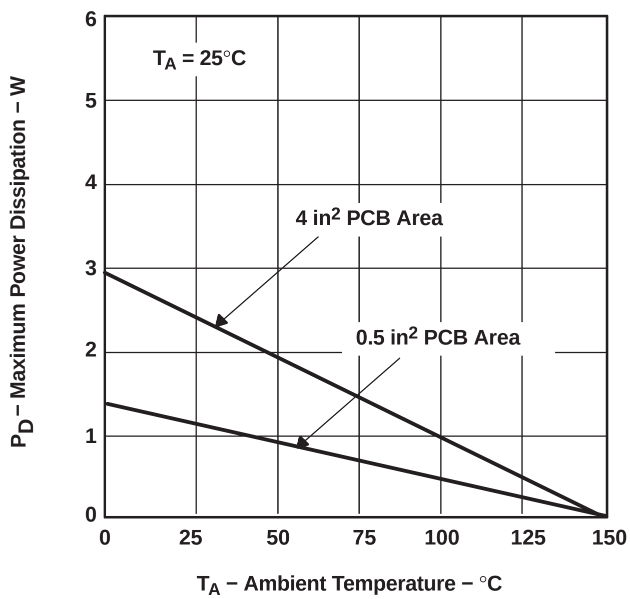


Figure 24. SOT223 Power Dissipation

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS726126DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS726126DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS726126DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS726126DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS72615DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS72615DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS72615DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS72615DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS72615KTT	OBSOLETE	DDPAK/ TO-263	KTT	5		TBD	Call TI	Call TI
TPS72615KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS72615KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS72615KTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS72615KTTTG3	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS72616DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS72616DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS72616DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS72616DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS72616KTT	OBSOLETE	DDPAK/ TO-263	KTT	5		TBD	Call TI	Call TI
TPS72616KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS72616KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS72616KTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS72616KTTTG3	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS72618DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS72618DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS72618DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS72618DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS72618KTT	OBSOLETE	DDPAK/ TO-263	KTT	5		TBD	Call TI	Call TI
TPS72618KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS72618KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS72618KTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS72618KTTTG3	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS72625DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS72625DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS72625DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS72625DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS72625KTT	OBSOLETE	DDPAK/ TO-263	KTT	5		TBD	Call TI	Call TI
TPS72625KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS72625KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS72625KTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
TPS72625KTTTG3	ACTIVE	DDPAK/ TO-263	KTT	5	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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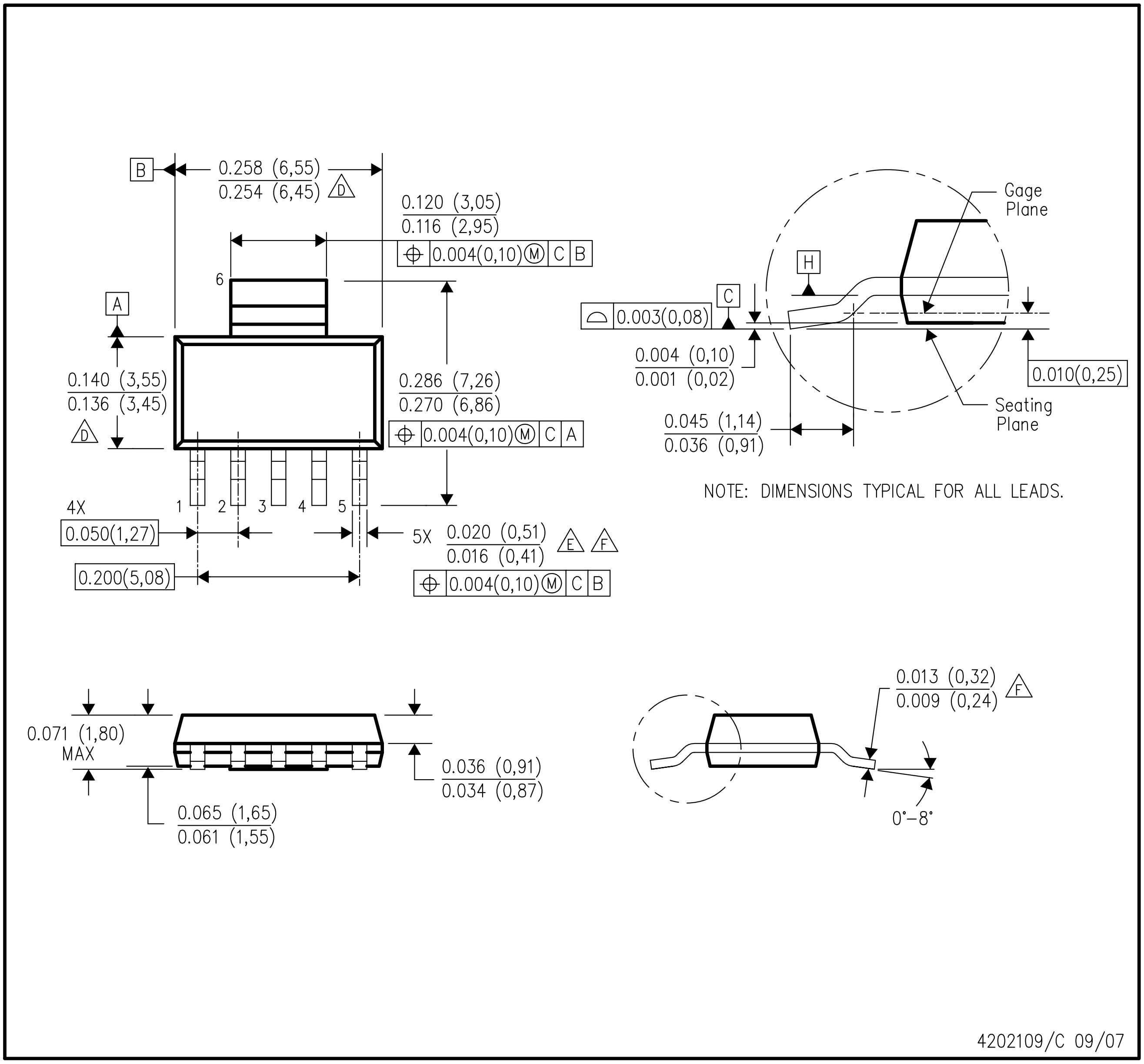
DCQ (R–PDSO–G6) PLASTIC SMALL–OUTLINE



NOTES:

A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Controlling dimension in inches.

D. Body length and width dimensions are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and the bottom of the plastic body.

E. Lead width dimension does not include dambar protrusion.

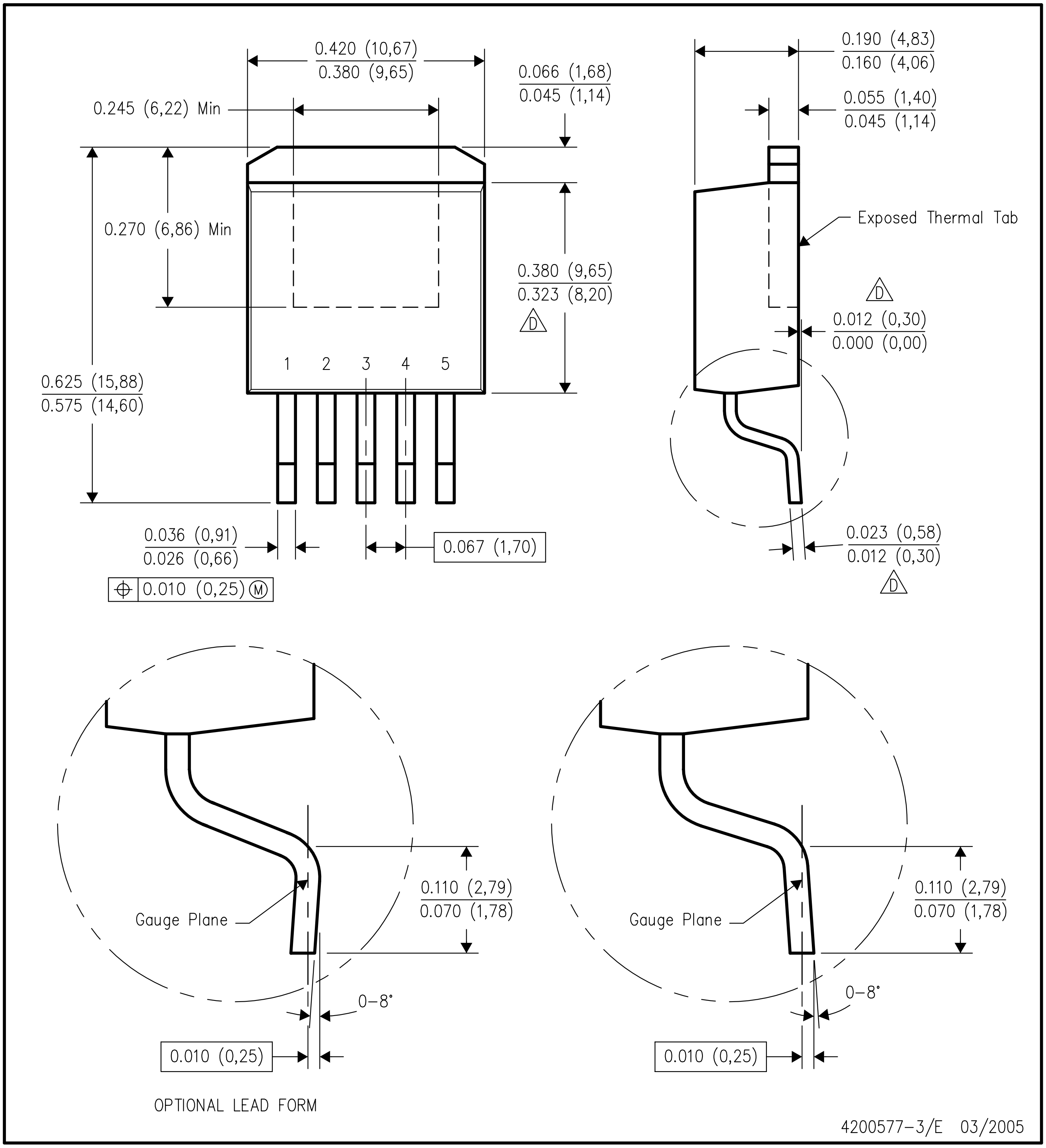
F. Lead width and thickness dimensions apply to solder plated leads.

G. Interlead flash allow 0.008 inch max.

H. Gate burr/protrusion max. 0.006 inch.

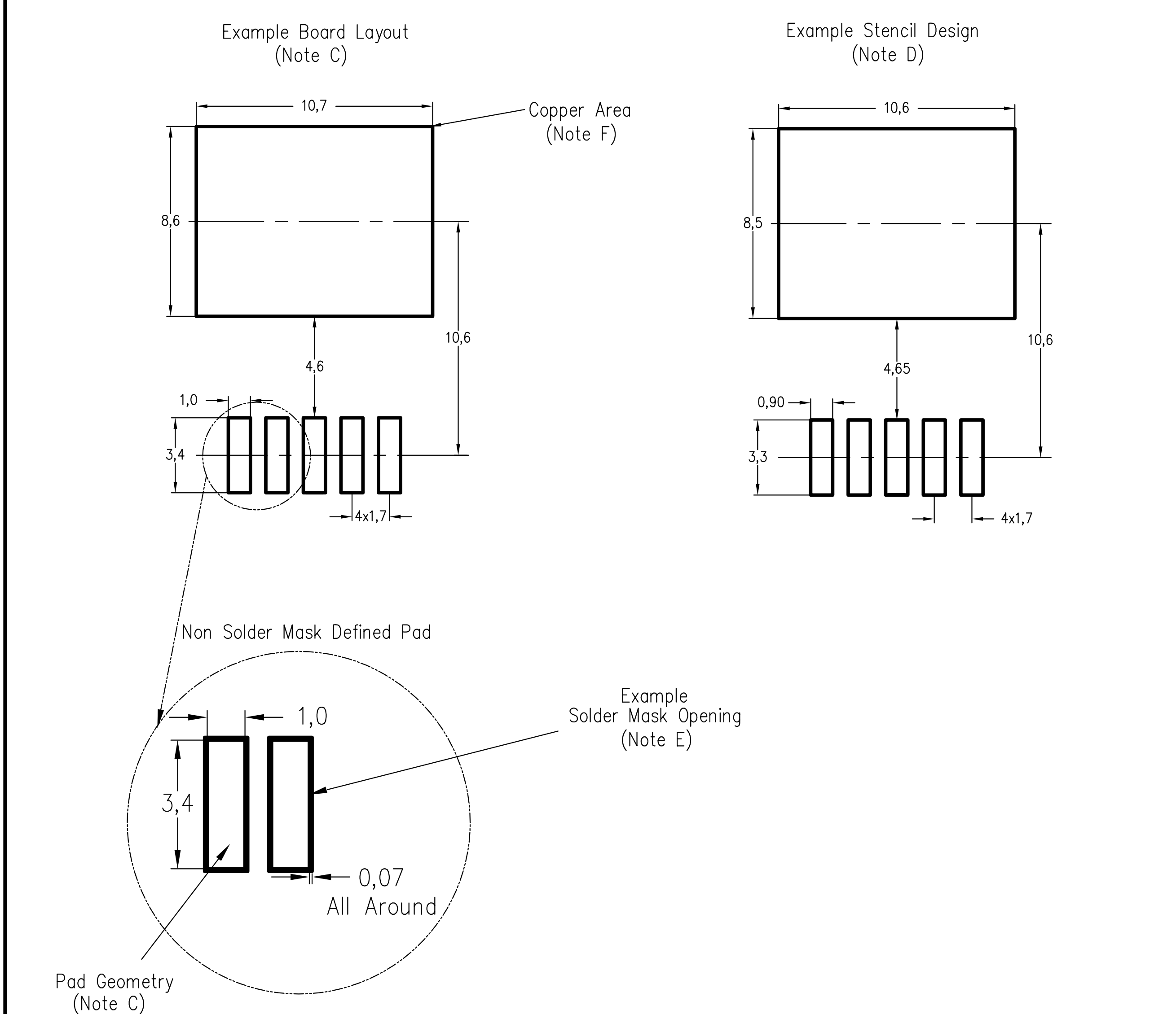
I. Datums A and B are to be determined at Datum H.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

KTT (R–PSFM–G5)



4208208–3/B 03/07

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

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