

TPS715 50mA、24V、3.2 μ A 静态电流、低压降线性稳压器

1 特性

- 输入电压范围：2.5 V 至 24 V (最大 30 V)
- 超低 I_Q ：50mA 负载电流下为 3.2 μ A
- 输出电流：高达 50 mA
- 与 $\geq 0.47 \mu$ F 的输出电容器一起工作时可保持稳定
- 可配置的输出电压选项：
 - 固定：1.8V、1.9V、2.3V、2.5V、3V、3.3V、3.45V、5V
 - 可调节：1.2 V 至 15 V
- 过流保护
- 封装：5 引脚 SC70 (DCK)
- 指定结温：-40°C 至 +125°C
- 有关 80mA 额定电流和更高功率的封装，请参阅 [TPS715A](#)

应用

- 家庭和楼宇自动化
- 零售自动化和支付
- 电网基础设施
- 医疗应用
- 照明应用

2 说明

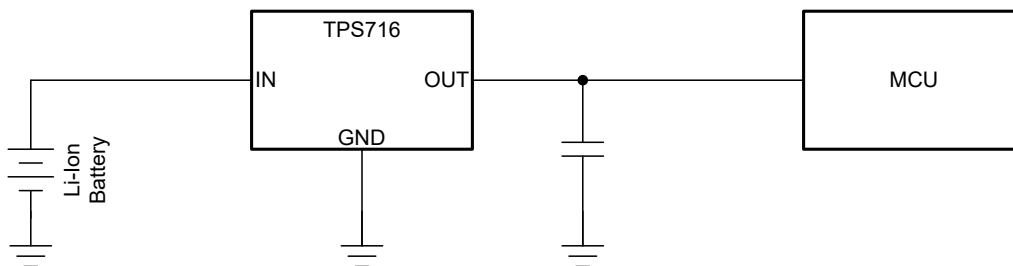
TPS715 低压降 (LDO) 线性稳压器是低静态电流器件，此器件在小型化封装中提供宽输入电压范围和低功耗运行的优势。TPS715 的低压降和低静态电流可实现超低功耗运行。因此，TPS715 专为电池供电型应用而设计，可用作低功耗微控制器的电源管理附件。

TPS715 有固定电压和可调节电压两种版本可供选用。为了获得更大的灵活性或更高的输出电压，可调节电压版本使用反馈电阻器将输出电压设置为 1.205V 至 15V。TPS715 LDO 在负载电流为 50mA 时支持典型值为 415mV 的低压降。低静态电流 (典型值为 3.2 μ A) 在整个输出负载电流 (0mA 至 50mA) 范围内都是稳定的。TPS715 还具有内部软启动功能，可降低浪涌电流。内置过流限制有助于在发生负载短路或故障时保护稳压器。

封装信息⁽¹⁾

| 器件型号 | 封装 | 封装尺寸 (标称值) |
|--------|----------|-----------------|
| TPS715 | SC70 (5) | 2.00mm × 1.25mm |

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。



典型应用原理图



Table of Contents

| | | | |
|--|----|---|-----------|
| 1 特性 | 1 | 6.4 Device Functional Modes..... | 12 |
| 应用 | 1 | 7 Application and Implementation | 13 |
| 2 说明 | 1 | 7.1 Application Information..... | 13 |
| 3 Revision History | 2 | 7.2 Typical Application..... | 13 |
| 4 Pin Configuration and Functions | 3 | 7.3 Best Design Practices..... | 18 |
| 5 Specifications | 4 | 7.4 Power Supply Recommendations..... | 18 |
| 5.1 Absolute Maximum Ratings..... | 4 | 7.5 Layout..... | 18 |
| 5.2 ESD Ratings..... | 4 | 8 Device and Documentation Support | 20 |
| 5.3 Recommended Operating Conditions..... | 4 | 8.1 Device Support..... | 20 |
| 5.4 Thermal Information..... | 5 | 8.2 Documentation Support..... | 20 |
| 5.5 Electrical Characteristics..... | 6 | 8.3 接收文档更新通知..... | 20 |
| 5.6 Typical Characteristics..... | 7 | 8.4 支持资源..... | 20 |
| 6 Detailed Description | 10 | 8.5 Trademarks..... | 20 |
| 6.1 Overview..... | 10 | 8.6 Electrostatic Discharge Caution..... | 20 |
| 6.2 Functional Block Diagrams..... | 10 | 8.7 术语表..... | 21 |
| 6.3 Feature Description..... | 10 | 9 Mechanical, Packaging, and Orderable Information.. | 21 |

3 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision R (February 2015) to Revision S (August 2022)

| | Page |
|---|------|
| • 更新了整个文档中的表格、图和交叉参考的编号格式..... | 1 |
| • 更改了文档标题..... | 1 |
| • 更改了 <i>特性</i> 部分..... | 1 |
| • 更改了 <i>应用</i> 部分..... | 1 |
| • 更改了 <i>说明</i> 部分..... | 1 |
| • Changed descriptions of FB and NC pins in <i>Pin Functions</i> table, split fixed and adjustable pin outs apart | 3 |
| • Added M3-specific plots to <i>Typical Characteristics</i> section..... | 7 |
| • Changed <i>Overview</i> section..... | 10 |
| • Changed block diagrams in <i>Functional Block Diagrams</i> section..... | 10 |
| • Changed <i>Low Quiescent Current</i> section and title..... | 10 |
| • Changed <i>Dropout Voltage</i> (V_{DO}) section..... | 11 |
| • Deleted <i>Disabled</i> row from <i>Device Functional Mode Comparison</i> table..... | 12 |
| • Changed <i>Dropout Operation</i> section..... | 12 |
| • Changed <i>External Capacitor Requirements</i> section..... | 14 |
| • Added <i>Input and Output Capacitor Requirements</i> section..... | 14 |
| • Changed <i>Reverse Current</i> section..... | 14 |
| • Changed output voltage value when no C_{FF} is used from 0.8 V to 1.205 V | 15 |
| • Added <i>Power Dissipation</i> (P_D) section..... | 15 |
| • Added M3-specific plots to <i>Application Curves</i> section..... | 17 |
| • Added second row and deleted second footnote from <i>Device Nomenclature</i> table..... | 20 |

Changes from Revision Q (January 2014) to Revision R (February 2015)

| | Page |
|---|------|
| • 新增了 <i>ESD</i> 等级表、 <i>特性说明</i> 部分、 <i>器件功能模式</i> 、 <i>应用和实现</i> 部分、 <i>电源相关建议</i> 部分、 <i>布局</i> 部分、 <i>器件和文档支持</i> 部分以及 <i>机械、封装和可订购信息</i> 部分..... | 1 |
| • 更改了首页图片..... | 1 |
| • Changed <i>Pin Configuration and Functions</i> section; updated table format | 3 |

4 Pin Configuration and Functions

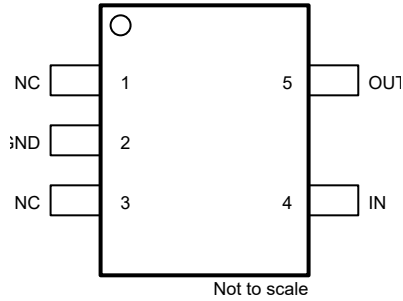


图 4-1. DCK Package (Fixed), 5-Pin SC70 (Top View)

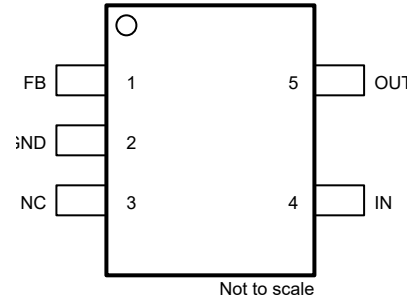


图 4-2. DCK Package (Adjustable), 5-Pin SC70 (Top View)

表 4-1. Pin Functions

| NAME | PIN | | TYPE | DESCRIPTION |
|------|-------|------------|------|--|
| | FIXED | ADJUSTABLE | | |
| FB | — | 1 | I | In the adjustable configuration, this pin is used to set the output voltage with help of the feedback divider. For the fixed output version, this pin can either be left floating or connected to GND. |
| GND | 2 | 2 | — | Ground |
| IN | 4 | 4 | I | Input supply |
| NC | 1, 3 | 3 | — | No connect pin. This pin is not connected internally. Connect to ground for best thermal performance or leave floating. |
| OUT | 5 | 5 | O | Output of the regulator. Any output capacitor $\geq 0.47 \mu\text{F}$ can be used for stability. |

5 Specifications

5.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)⁽¹⁾ ⁽²⁾

| | | MIN | MAX | UNIT |
|-------------|---------------------------|--------------------|-----------------------|------|
| Voltage | V _{IN} | - 0.3 | 30 | V |
| | V _{OUT} | - 0.3 | V _{IN} + 0.3 | |
| | V _{FB} | - 0.3 | 4.5 | |
| Current | Peak output current | Internally limited | | |
| Temperature | Junction, T _J | - 40 | 150 | °C |
| | Storage, T _{stg} | - 65 | 150 | |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

5.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|-------------------------|--|-------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | ±2000 |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | ±500 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | NOM | MAX | UNIT |
|------------------|---------------------------------|-------|-------|-----|------|
| V _{IN} | Input supply voltage | 2.5 | | 24 | V |
| V _{OUT} | Output voltage | 1.205 | | 15 | V |
| I _{OUT} | Output current | 0 | | 50 | mA |
| C _{IN} | Input capacitor ⁽²⁾ | 0 | 0.047 | | μF |
| C _{OUT} | Output capacitor ⁽³⁾ | 0.47 | 1 | | μF |
| T _J | Operating junction temperature | -40 | | 125 | °C |

- (1) All voltages are with respect to GND.
- (2) An input capacitor is not required for LDO stability. However, an input capacitor with an effective value of 0.047 μF is recommended to counteract the effect of source resistance and inductance, which may in some cases cause symptoms of system level instability such as ringing or oscillation, especially in the presence of load transients.
- (3) All capacitor values are assumed to derate to 50% of the nominal capacitor value.

5.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TPS715 | TPS715M3 | UNIT |
|-------------------------------|--|------------|------------|------|
| | | DCK [SC70] | DCK [SC70] | |
| | | 5 PINS | 5 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 253.8 | 195.7 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 73.7 | 88.2 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 84.6 | 40.7 | °C/W |
| ψ_{JT} | Junction-to-top characterization parameter | 1.1 | 11.2 | °C/W |
| ψ_{JB} | Junction-to-board characterization parameter | 83.9 | 40.5 | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics application report](#).

5.5 Electrical Characteristics

over operating junction temperature range ($T_J = -40^\circ\text{C}$ to 125°C), $V_{IN} = V_{OUT(nom)} + 1\text{ V}$, $I_{OUT} = 1\text{ mA}$, and $C_{OUT} = 1\ \mu\text{F}$ (unless otherwise noted); typical values are at $T_J = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------------|--|--|-----|-----|-----|------------------|
| V_{IN} | Input voltage TPS715 (1) | $I_O = 10\text{ mA}$ | 2.5 | | 24 | V |
| | | $I_O = 50\text{ mA}$ | 3 | | 24 | |
| V_{OUT} | Output voltage Range (TPS71501) | | 1.2 | | 15 | V |
| V_{OUT} | Accuracy (1) (2) | Over V_{IN} , I_{OUT} , and Temp $V_{OUT} + 1\text{ V} \leq V_{IN} \leq 24\text{ V}$, $100\ \mu\text{A} \leq I_{OUT} \leq 50\text{ mA}$ | -4 | | 4 | % |
| I_{GND} | Ground pin current (3) | $0 \leq I_{OUT} \leq 50\text{ mA}$, $T_J = -40^\circ\text{C}$ to 85°C | | 3.2 | 4.2 | μA |
| | | $0\text{ mA} \leq I_{OUT} \leq 50\text{ mA}$ | | 3.2 | 4.8 | |
| | | $0\text{ mA} \leq I_{OUT} \leq 50\text{ mA}$, $V_{IN} = 24\text{ V}$ | | | 5.8 | |
| $\Delta V_{OUT} (\Delta I_{OUT})$ | Load regulation | $I_{OUT} = 100\ \mu\text{A}$ to 50 mA | | 22 | | mV |
| $\Delta V_{OUT} (\Delta V_{IN})$ | Output voltage line regulation (1) | $V_{OUT(NOM)} + 1\text{ V} \leq V_{IN} \leq 24\text{ V}$ | | 20 | 60 | mV |
| V_n | Output noise voltage (non-M3 device) (4) | $BW = 200\text{ Hz}$ to 100 kHz , $C_{OUT} = 10\ \mu\text{F}$, $I_{OUT} = 50\text{ mA}$ | | 575 | | μVrms |
| V_n | Output noise voltage (M3 device) (4) | $BW = 200\text{ Hz}$ to 100 kHz , $C_{OUT} = 10\ \mu\text{F}$, $I_{OUT} = 50\text{ mA}$ | | 425 | | μVrms |
| I_{CL} | Output current limit (TPS715) | $V_{OUT} = 0\text{ V}$, $V_{IN} \geq 3.5\text{ V}$ | 125 | | 750 | mA |
| | | $V_{OUT} = 0\text{ V}$, $V_{IN} < 3.5\text{ V}$ | 90 | | 750 | |
| | Output current limit (TPS715M3) | $V_{OUT} = 0\text{ V}$, $V_{IN} \geq 3.5\text{ V}$ | 175 | | 450 | |
| | | $V_{OUT} = 0\text{ V}$, $V_{IN} < 3.5\text{ V}$ | 90 | | 450 | |
| PSRR | Power-supply ripple rejection | $f = 100\text{ kHz}$, $C_{OUT} = 10\ \mu\text{F}$ | | 60 | | dB |
| V_{DO} | Dropout voltage TPS715 | $V_{IN} = V_{OUT(nom)} - 0.1\text{ V}$ $I_{OUT} = 50\text{ mA}$ | | 415 | 750 | mV |
| | Dropout voltage TPS715M3 | | | 415 | 600 | |

- (1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or the value shown for *Input voltage* in this table, whichever is greater.
- (2) For adjustable device, output accuracy excludes the tolerance and mismatch associated with external resistors used for setting up the output voltage level.
- (3) See [Figure 6.1](#). The TPS715 family employs a leakage null control circuit. This circuit is active only if output current is less than pass FET leakage current. The circuit is typically active when output load is less than $5\ \mu\text{A}$, V_{IN} is greater than 18 V , and die temperature is greater than 100°C .
- (4) See [Section 10.1.2](#) for clarification about M3 and Non-M3 devices.

5.6 Typical Characteristics

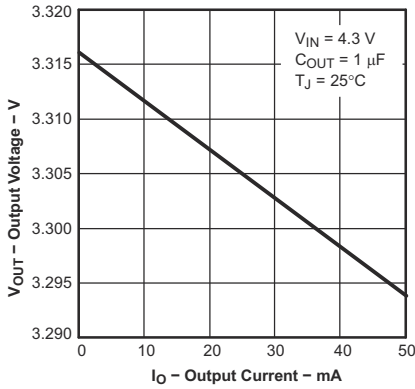


图 5-1. Output Voltage vs Output Current

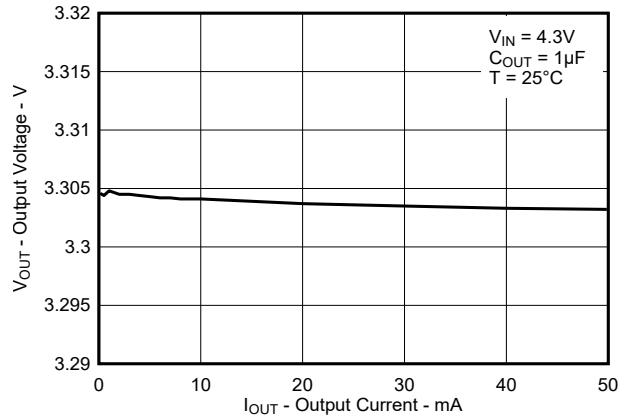


图 5-2. Output Voltage vs Output Current for M3 Devices

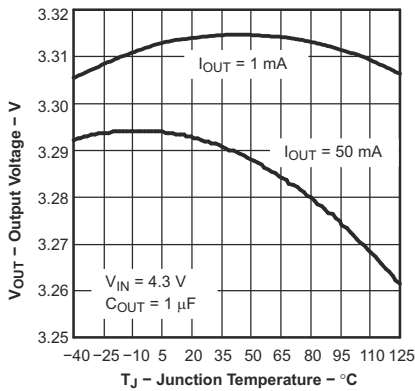


图 5-3. Output Voltage vs Junction Temperature

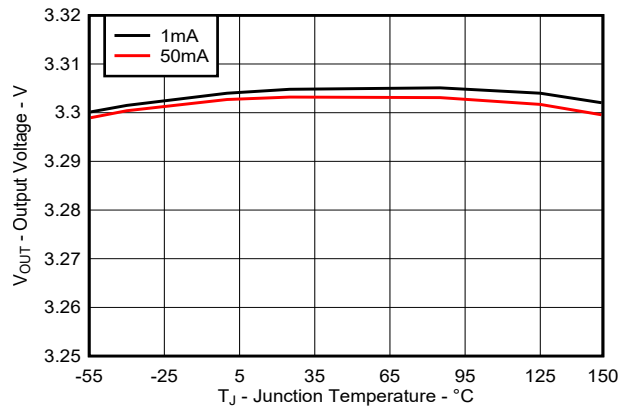


图 5-4. Output Voltage vs Junction Temperature for M3 Devices

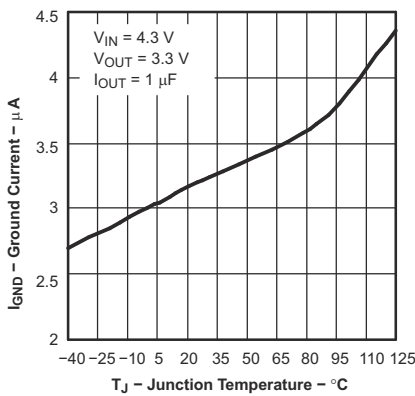


图 5-5. Quiescent Current vs Junction Temperature

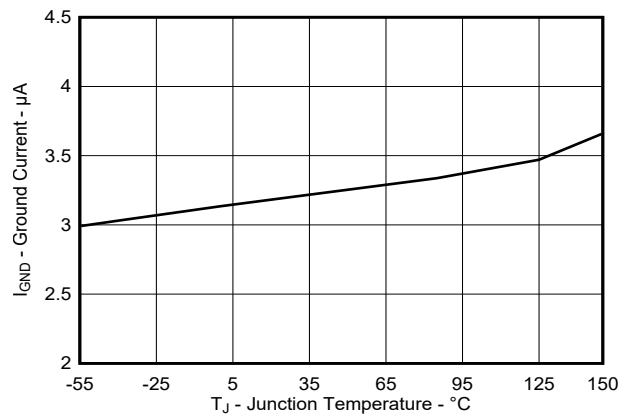


图 5-6. Quiescent Current vs Junction Temperature for M3 Devices

5.6 Typical Characteristics (continued)

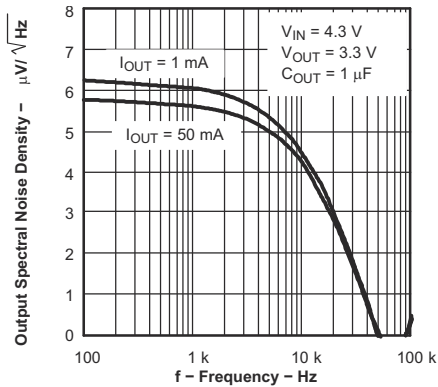


图 5-7. Output Voltage Spectral Noise Density vs Frequency

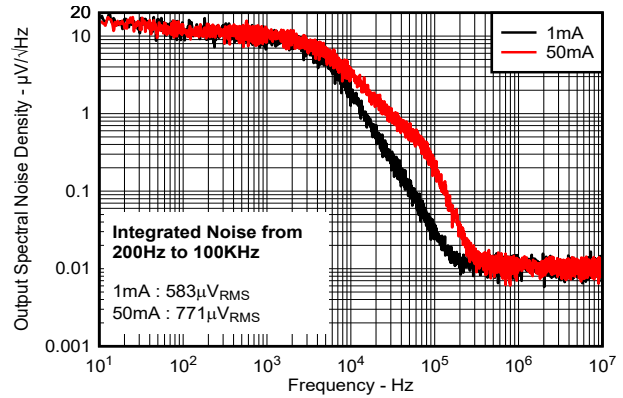


图 5-8. Output Voltage Spectral Noise Density vs Frequency for M3 Devices

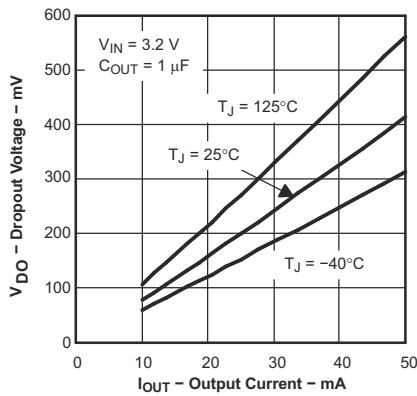


图 5-9. Dropout Voltage vs Output Current

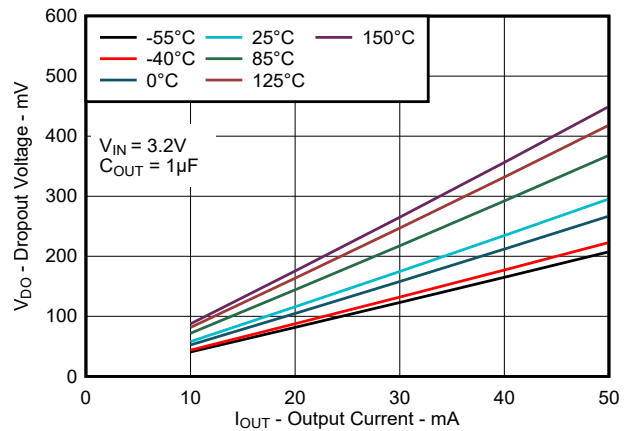


图 5-10. Dropout Voltage vs Output Current for M3 Devices

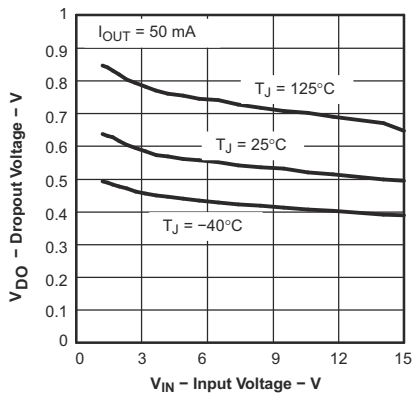


图 5-11. TPS71501 Dropout Voltage vs Input Voltage

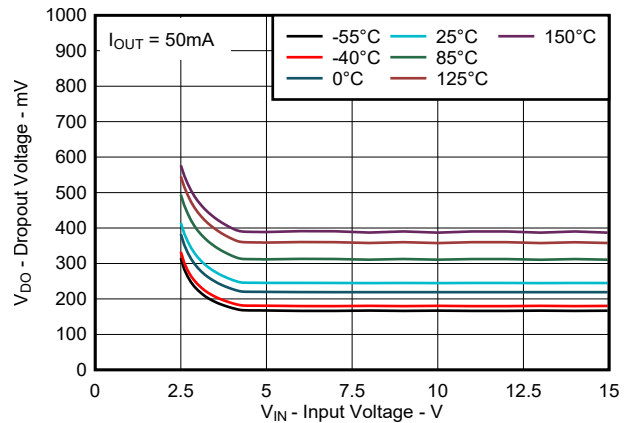


图 5-12. TPS71501 Dropout Voltage vs Input Voltage for M3 Devices

5.6 Typical Characteristics (continued)

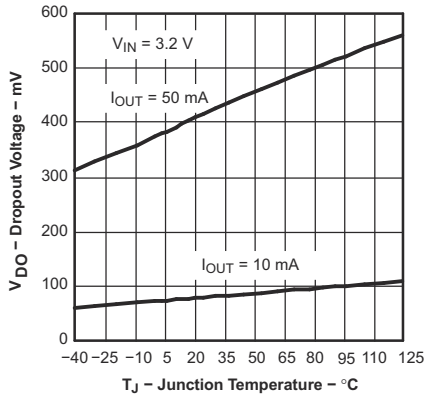


图 5-13. Dropout Voltage vs Junction Temperature

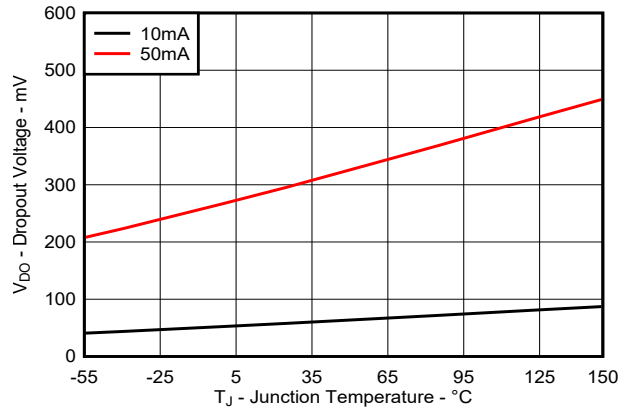


图 5-14. Dropout Voltage vs Junction Temperature for M3 Devices

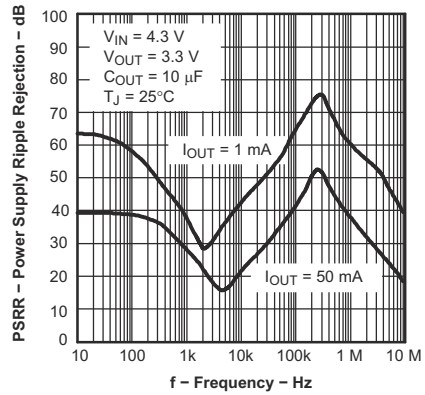


图 5-15. Power-Supply Ripple Rejection vs Frequency

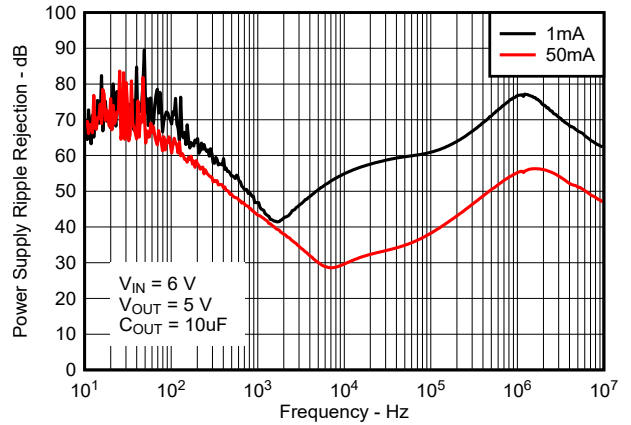


图 5-16. Power-Supply Ripple Rejection vs Frequency for M3 Devices

6 Detailed Description

6.1 Overview

The TPS715 family of low-dropout regulators (LDOs) consume only 3.2 μA of quiescent current across the entire output current range, while offering a wide input voltage range and low-dropout voltage in a small package. The devices, which operate over an input range of 2.5 V to 24 V, are stable with any output capacitor greater than or equal to 0.47 μF . The low quiescent current across the complete load current range, makes the TPS715 designed for powering battery-operated applications. The TPS715 family has internal soft-start to control inrush current into the output capacitor. These LDOs also have overcurrent protection during a load-short or fault condition on the output.

6.2 Functional Block Diagrams

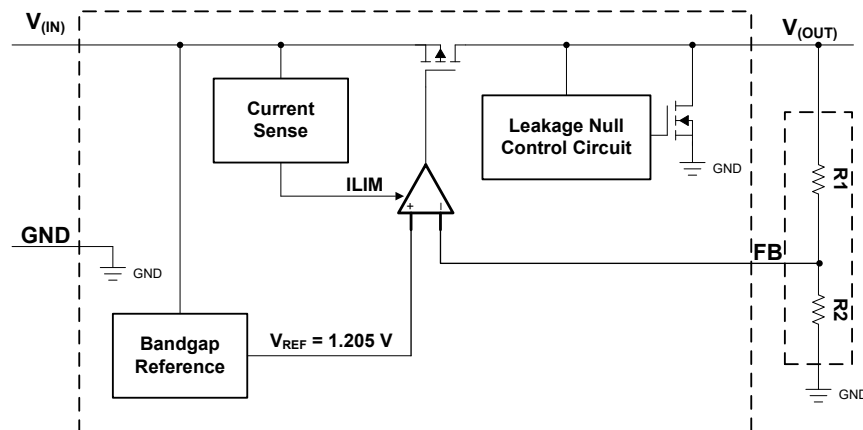


图 6-1. Functional Block Diagram—Adjustable Version

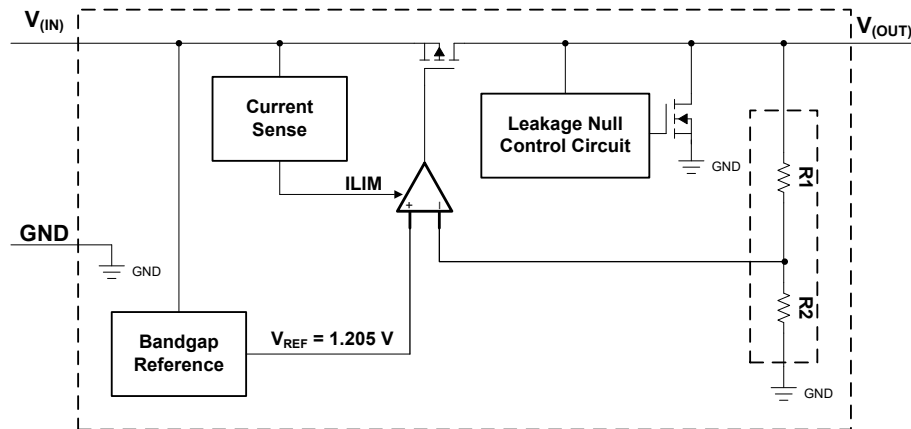


图 6-2. Functional Block Diagram—Fixed Version

6.3 Feature Description

6.3.1 Wide Supply Range

This device has an operational input supply range of 2.5 V to 24 V, allowing for a wide range of applications. This wide supply range is designed for applications that have either large transients or high DC voltage supplies.

6.3.2 Low Quiescent Current

This device only requires 3.2 μA (typical) of quiescent current across the complete load current range (0 mA to 50 mA) from -40°C to $+85^\circ\text{C}$ and has a maximum current consumption of 5.8 μA at -40°C to $+125^\circ\text{C}$.

6.3.3 Dropout Voltage (V_{DO})

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage ($V_{IN} - V_{OUT}$) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. In dropout operation, the pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the value required to maintain output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source, on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. Use [方程式 1](#) to calculate the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

6.3.4 Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brick-wall scheme. In a high-load current fault, the brick-wall scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power $[(V_{IN} - V_{OUT}) \times I_{CL}]$. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the [Know Your Limits application report](#).

图 6-3 shows a diagram of the current limit.

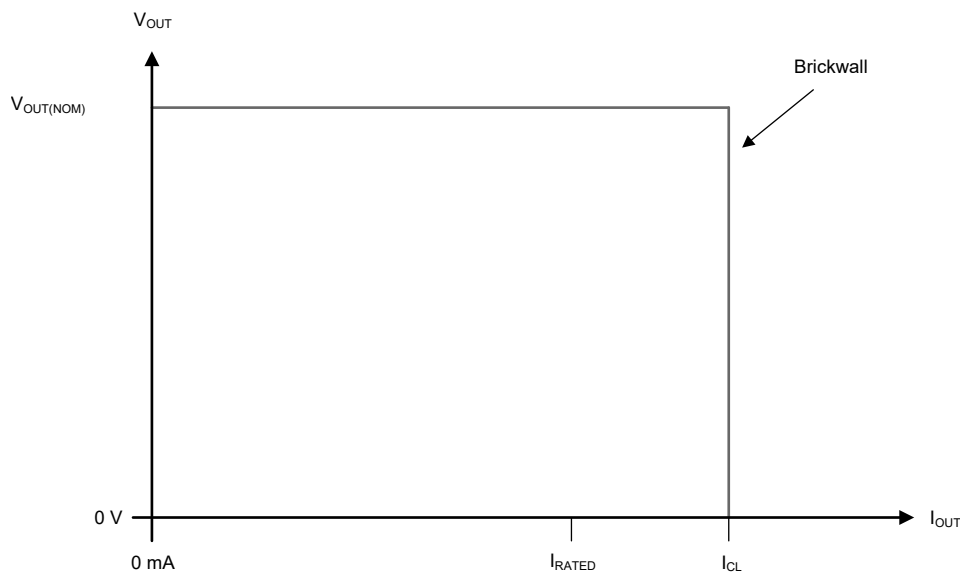


图 6-3. Current Limit

6.4 Device Functional Modes

表 6-1 provides a quick comparison between the normal, dropout, and disabled modes of operation.

表 6-1. Device Functional Mode Comparison

| OPERATING MODE | PARAMETER | |
|----------------|----------------------------------|--------------------|
| | V_{IN} | I_{OUT} |
| Normal | $V_{IN} > V_{OUT(nom)} + V_{DO}$ | $I_{OUT} < I_{CL}$ |
| Dropout | $V_{IN} < V_{OUT(nom)} + V_{DO}$ | $I_{OUT} < I_{CL}$ |

6.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than 125°C

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Application Information

The TPS715 family of LDO regulators is a good choice for battery powered applications as well as a good attachment to low power micro-controllers such as [MSP430](#), due to its low IQ performance across load current range. The ultra-low-supply current of the TPS715 device maximizes efficiency at light loads, its high input voltage range makes and flexibility of output voltage selection in adjustable configuration and fixed output levels makes the device suitable for supplies such as unconditioned solar panels.

7.2 Typical Application

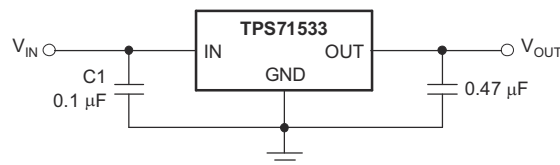


图 7-1. Typical Application Circuit (Fixed-Voltage Version)

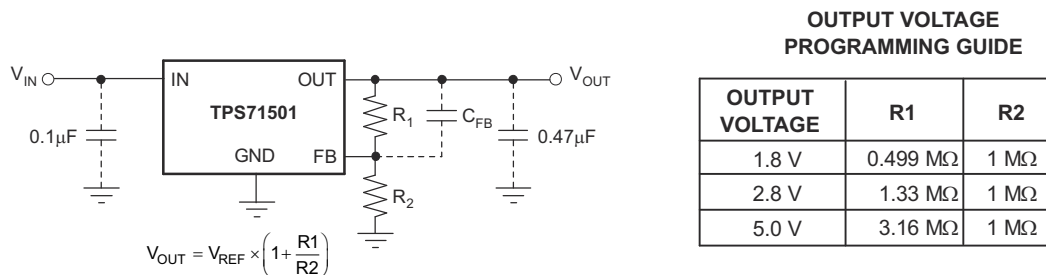


图 7-2. TPS71501 Adjustable LDO Regulator Programming

7.2.1 Detailed Design Procedure

7.2.1.1 Setting V_{OUT} for the TPS71501 Adjustable LDO

The TPS715 family contains an adjustable version, the TPS71501, which sets the output voltage using an external resistor divider as shown in [图 7-2](#). The output voltage operating range is 1.2 V to 15 V, and is calculated using:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2} \right) \quad (2)$$

where:

- $V_{REF} = 1.205 \text{ V}$ (typical)

Choose resistors R1 and R2 allows approximately 1.5 μ A of current through the resistor divider. Lower value resistors can be used for improved noise performance, but consume more power. Avoid higher resistor values because leakage current into or out of FB across R1 / R2 creates an offset voltage that is proportional to V_{OUT} divided by V_{REF} . The recommended design procedure is to choose $R2 = 1\text{ M}\Omega$ to set the divider current at 1.5 μ A, and then calculate R1 using [方程式 3](#):

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \times R2 \quad (3)$$

[图 7-2](#) depicts this configuration.

7.2.1.2 External Capacitor Requirements

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. As a rule of thumb, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

7.2.1.3 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. An input capacitor is recommended if the source impedance is more than 0.5 Ω . A higher value capacitor may be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

Dynamic performance of the device is improved with the use of an output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

7.2.1.4 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the intrinsic body diode of the PMOS pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} \leq V_{IN} + 0.3\text{ V}$. These conditions are:

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, external protection is recommended to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

图 7-3 显示了一种保护器件的方法。

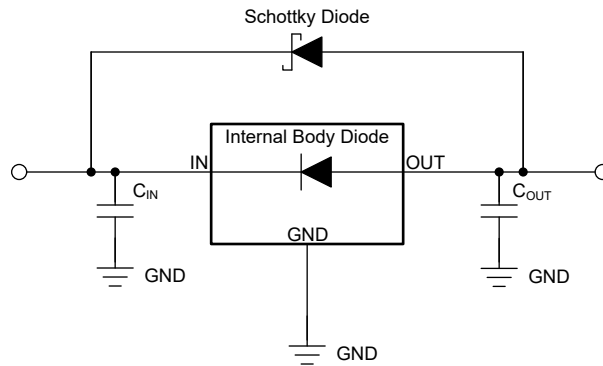


图 7-3. 使用肖特基二极管的反向电流保护示例电路

7.2.1.5 Feed-Forward Capacitor (C_{FF})

对于可调电压版本器件，可以在 OUT 引脚和 FB 引脚之间连接一个前馈电容 (C_{FF})。 C_{FF} 可以改善瞬态、噪声和 PSRR 性能，但不需要用于调节器稳定性。推荐 C_{FF} 值列在 *Recommended Operating Conditions* 表中。可以使用更高的电容值 C_{FF} ；然而，启动时间会增加。有关 C_{FF} 权衡的详细说明，请参阅 [Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator application note](#)。

C_{FF} 和 R_1 在环路增益中形成频率 f_z 处的零点，而 C_{FF} 、 R_1 和 R_2 在环路增益中形成频率 f_p 处的极点。 C_{FF} 零点和极点频率可以通过以下方程计算：

$$f_z = 1 / (2 \times \pi \times C_{FF} \times R_1) \quad (4)$$

$$f_p = 1 / (2 \times \pi \times C_{FF} \times (R_1 \parallel R_2)) \quad (5)$$

$C_{FF} \geq 10$ pF 是稳定性所必需的，如果反馈分压器电流小于 5μ A。 [方程式 6](#) 计算了反馈分压器电流。

$$I_{FB_Divider} = V_{OUT} / (R_1 + R_2) \quad (6)$$

为了避免启动时间增加，限制 C_{FF} 的乘积 $C_{FF} \times R_1 < 50 \mu$ s。

对于输出电压为 1.205 V 且 FB 引脚连接到 OUT 引脚的情况，不使用 C_{FF} 。

7.2.1.6 Power Dissipation (P_D)

电路可靠性需要考虑器件功耗、电路在印刷电路板 (PCB) 上的位置以及热平面的正确 sizing。 PCB 周围必须没有或很少有其他发热器件，以免造成额外的热应力。

作为一阶近似，调节器中的功耗取决于输入到输出之间的电压差和负载条件。以下方程计算了功耗 (P_D)。

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (7)$$

备注

功耗可以最小化，因此可以实现更高的效率，通过正确选择系统电压轨。为了最低的功耗，请使用正确输出调节所需的最小输入电压。

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (8)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

7.2.1.7 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1 mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \quad (9)$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \quad (10)$$

where:

- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the [Semiconductor and IC Package Thermal Metrics application note](#).

7.2.2 Application Curves

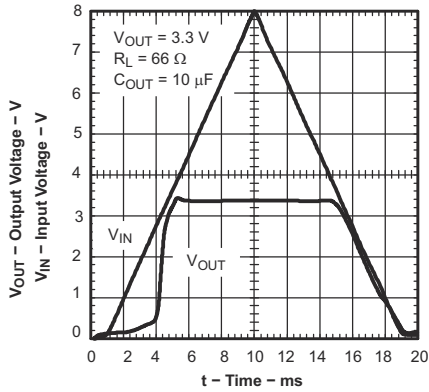


图 7-4. Power-Up and Power-Down

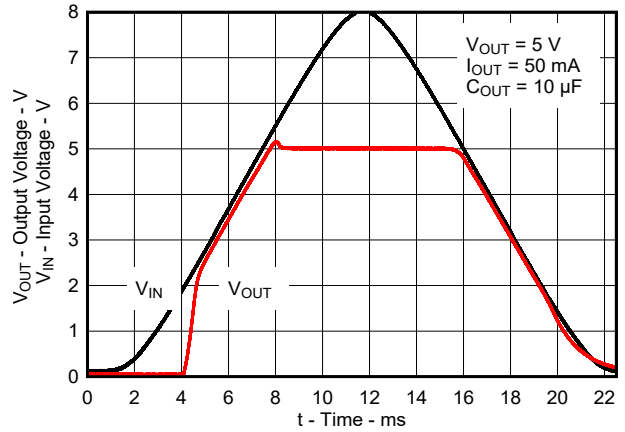


图 7-5. Power-Up and Power-Down for M3 Devices

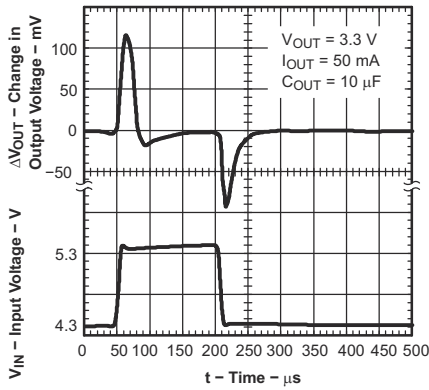


图 7-6. Line Transient Response

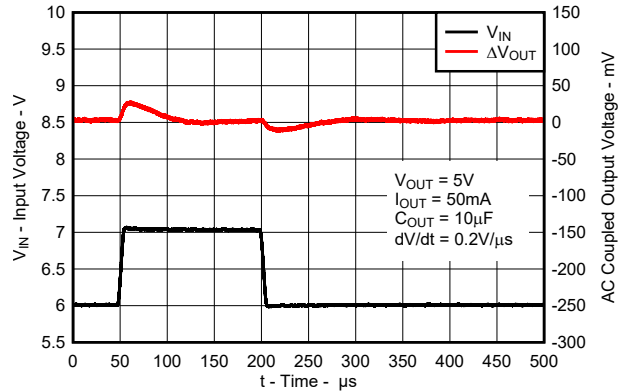


图 7-7. Line Transient Response for M3 Devices

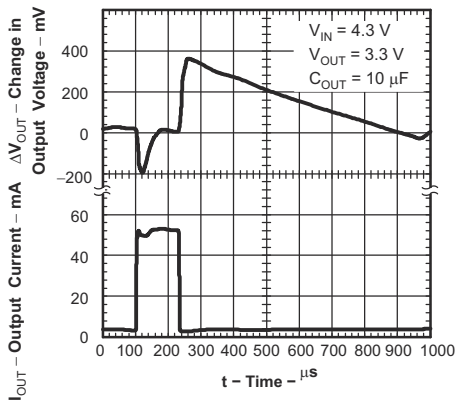


图 7-8. Load Transient Response

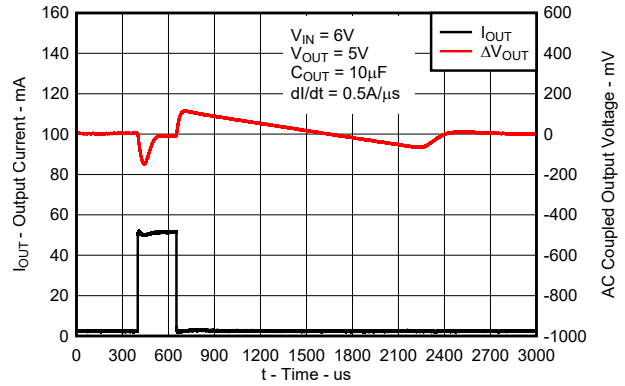
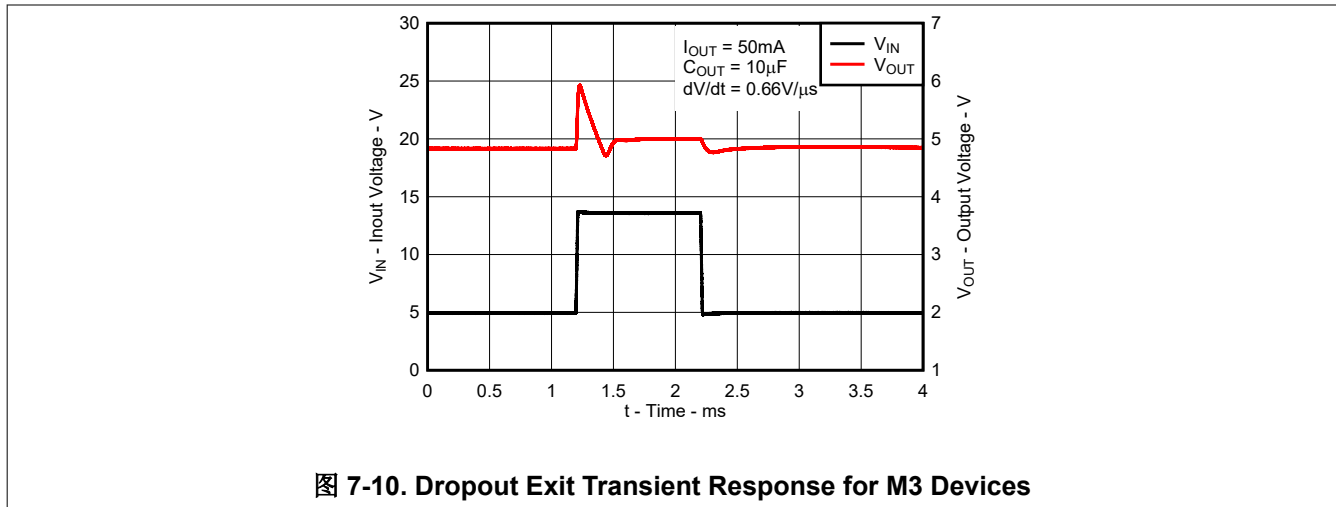


图 7-9. Load Transient Response for M3 Devices



7.3 Best Design Practices

Place at least one 0.47- μ F capacitor as close as possible to the OUT and GND terminals of the regulator.

Do not connect the output capacitor to the regulator using a long, thin trace.

Connect an input capacitor as close as possible to the IN and GND terminals of the regulator for best performance.

Do not exceed the absolute maximum ratings.

7.4 Power Supply Recommendations

The TPS715 is designed to operate from an input voltage supply range between 2.5 V and 24 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

7.5 Layout

7.5.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the printed-circuit-board and as near as practical to the respective LDO pin connections. Place ground return connections for the input and output capacitors as close to the GND pin as possible, using wide, component-side, copper planes. Do not use vias and long traces to create LDO circuit connections to the input capacitor, output capacitor, or the resistor divider because this practice negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage and shield the LDO from noise.

7.5.1.1 Power Dissipation

To ensure reliable operation, worst-case junction temperature must not exceed 125°C. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D , which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using [方程式 11](#):

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}} \quad (11)$$

where

- T_{Jmax} is the maximum allowable junction temperature
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package (see the [Thermal Information](#) table)
- T_A is the ambient temperature

The regulator dissipation is calculated using [方程式 12](#):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (12)$$

For a higher power package version of the TPS715, see the [TPS715A](#).

7.5.2 Layout Example

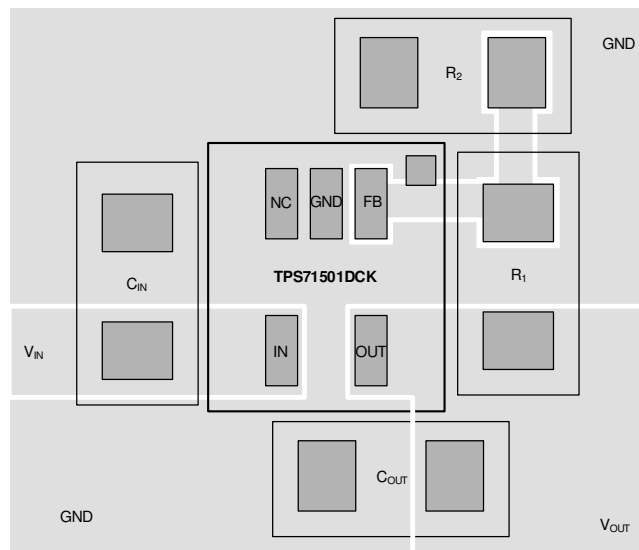


图 7-11. Example Layout for the TPS71501DCK

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS715. The [TPS71533EVM evaluation module](#) (and related [user's guide](#)) can be requested at the TI website through the product folders or purchased directly from [the TI eStore](#).

8.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS715 is available through the product folders under *Tools & Software*.

8.1.2 Device Nomenclature

表 8-1. Device Nomenclature⁽¹⁾

| PRODUCT | V _{OUT} |
|----------------|--|
| TPS715xx yyy z | XX is nominal output voltage (for example, 28 = 2.8 V, 285 = 2.85 V, 01 = Adjustable). YYY is package designator. Z is package quantity. |
| TPS715xyyyxM3 | M3 is a suffix designator for newer high density chip re-designs, fabricated on the latest TI process technology. Compared to Non-M3 devices, M3 devices support similar or better performance. |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](#).

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [TPS71533EVM LDO Evaluation Module user guide](#)
- Texas Instruments, [TPS735 High Input Voltage, Micropower SON-Packaged, 80-mA LDO Linear Regulators data sheet](#)

8.3 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](#) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.4 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

8.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| HPA00328DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | TBD | Call TI | Call TI | -40 to 85 | | Samples |
| HPA00423DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | Samples |
| HPA00681DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | Samples |
| PTPS71501DCKRM3 | ACTIVE | SC70 | DCK | 5 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | Samples |
| PTPS71533DCKRM3 | ACTIVE | SC70 | DCK | 5 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | Samples |
| PTPS71550DCKRM3 | ACTIVE | SC70 | DCK | 5 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | Samples |
| TPS71501DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | ARB | Samples |
| TPS71501DCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | ARB | Samples |
| TPS71518DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | ARD | Samples |
| TPS71518DCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | ARD | Samples |
| TPS71519DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | BOX | Samples |
| TPS71523DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | BNX | Samples |
| TPS71525DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | AQL | Samples |
| TPS71525DCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | AQL | Samples |
| TPS71530DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | AQM | Samples |
| TPS71530DCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | AQM | Samples |
| TPS71533DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | AQI | Samples |
| TPS71533DCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | AQI | Samples |
| TPS715345DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | BNY | Samples |
| TPS71550DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | T48 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| TPS71550DCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | T48 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS715 :

- Automotive : [TPS715-Q1](#)

NOTE: Qualified Version Definitions:

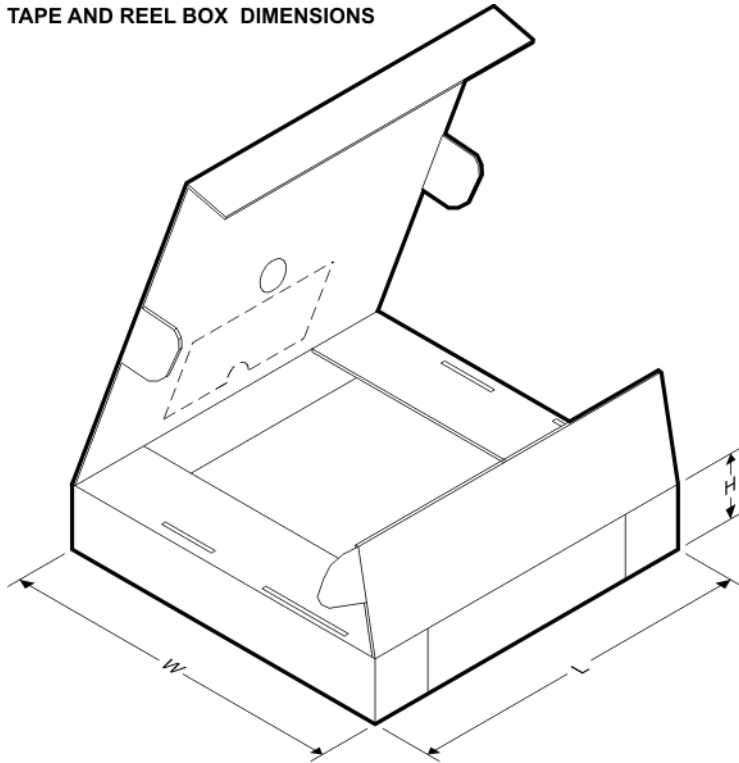
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS71501DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71501DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.41 | 2.41 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71518DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.41 | 2.41 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71519DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.41 | 2.41 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71523DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71523DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.41 | 2.41 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71525DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71525DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.41 | 2.41 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71530DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.41 | 2.41 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71530DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71533DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71533DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.41 | 2.41 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS715345DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.41 | 2.41 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71550DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71550DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.41 | 2.41 | 1.2 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS71501DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS71501DCKR | SC70 | DCK | 5 | 3000 | 183.0 | 183.0 | 20.0 |
| TPS71518DCKR | SC70 | DCK | 5 | 3000 | 183.0 | 183.0 | 20.0 |
| TPS71519DCKR | SC70 | DCK | 5 | 3000 | 183.0 | 183.0 | 20.0 |
| TPS71523DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS71523DCKR | SC70 | DCK | 5 | 3000 | 183.0 | 183.0 | 20.0 |
| TPS71525DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS71525DCKR | SC70 | DCK | 5 | 3000 | 183.0 | 183.0 | 20.0 |
| TPS71530DCKR | SC70 | DCK | 5 | 3000 | 183.0 | 183.0 | 20.0 |
| TPS71530DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS71533DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS71533DCKR | SC70 | DCK | 5 | 3000 | 183.0 | 183.0 | 20.0 |
| TPS715345DCKR | SC70 | DCK | 5 | 3000 | 183.0 | 183.0 | 20.0 |
| TPS71550DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS71550DCKR | SC70 | DCK | 5 | 3000 | 183.0 | 183.0 | 20.0 |

DCK (R-PDSO-G5)

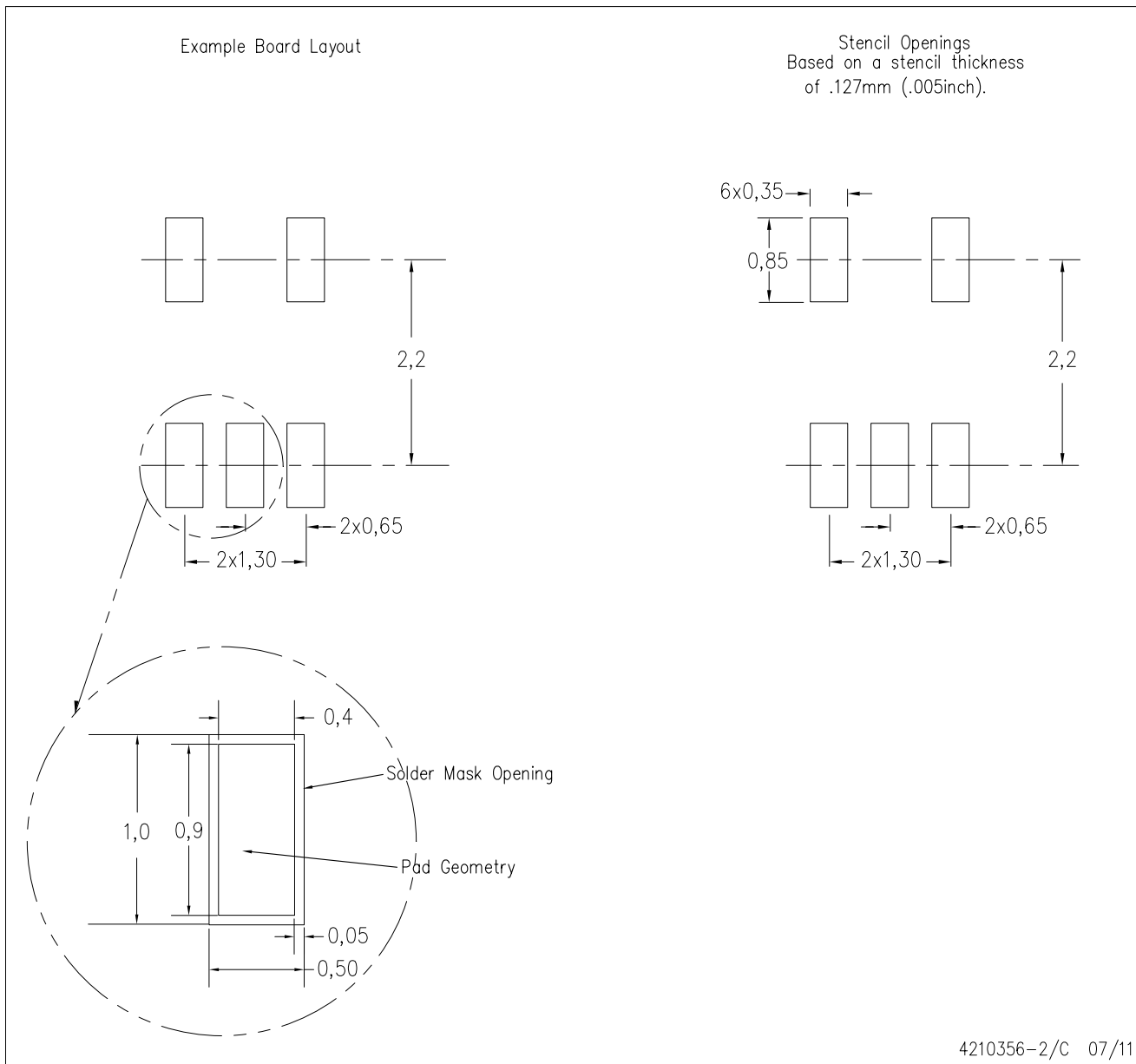
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2022，德州仪器 (TI) 公司