

150-mA, 30-V, Ultralow I_Q Voltage Regulators with Enable

FEATURES

- **Ultralow I_Q :** 1.35 μ A
- **Reverse Current Protection**
- **Low $I_{SHUTDOWN}$:** 150 nA
- **Input Voltage Range:** 2.7 V to 30 V
- **Supports 200-mA Peak Output**
- **Low Dropout:** 245 mV at 50 mA
- **2% Accuracy Over Temperature**
- **Available in Fixed-Output Voltages:** 1.2 V to 6.5 V
- **Thermal Shutdown and Overcurrent Protection**
- **Packages:** SOT23-5

APPLICATIONS

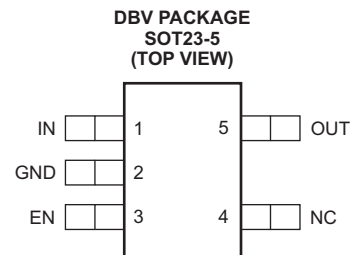
- **Zigbee™ Networks**
- **Home Automation**
- **Metering**
- **Weighing Scales**
- **Portable Power Tools**
- **Remote Control Devices**
- **Wireless Handsets, Smart Phones, PDAs, WLAN, and Other PC Add-On Cards**
- **White Goods**

DESCRIPTION

The TPS709xx series of linear regulators are ultralow, quiescent current devices designed for power-sensitive applications. A precision band-gap and error amplifier provides 2% accuracy over temperature. Quiescent current of only 1.35 μ A makes these devices ideal solutions for battery-powered, always-on systems that require very little idle-state power dissipation. These devices have thermal-shutdown, current-limit, and reverse-current protections for added safety.

These regulators can be put into shutdown mode by pulling the EN pin low. The leakage current in this mode goes down to 150 nA, typical.

The TPS709xx series is available in an SOT23-5 package.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE OPTIONS⁽¹⁾

PRODUCT	V _{OUT}
TPS709xxyyyz	XX is the nominal output voltage (for example 28 = 2.8 V). YYY is the package designator Z is the package quantity; R is for reel (3000 pieces), T is for tape (250 pieces)

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Specified at T_J = –40°C to +125°C, unless otherwise noted. All voltages are with respect to GND.

		VALUE		UNIT
		MIN	MAX	
Voltage	V _{IN}	–0.3	+32	V
	V _{EN}	–0.3	+7	V
	V _{OUT}	–0.3	+7	V
Maximum output current	I _{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation	P _{DISS}	See the Thermal Information table		
Temperature	Junction, T _J	–55	+150	°C
	Storage, T _{stg}	–55	+150	°C
Electrostatic discharge (ESD) ratings	Human body model (HBM)	2		kV
	Charged device model (CDM)	500		V

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		TPS709xx	UNITS
		DBV (SOT23)	
		5 PINS	
θ _{JA}	Junction-to-ambient thermal resistance	212.1	°C/W
θ _{JCtop}	Junction-to-case (top) thermal resistance	78.5	
θ _{JB}	Junction-to-board thermal resistance	39.5	
ψ _{JT}	Junction-to-top characterization parameter	2.86	
ψ _{JB}	Junction-to-board characterization parameter	38.7	
θ _{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

ELECTRICAL CHARACTERISTICS

At $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{IN} = V_{OUT(\text{typ})} + 1\text{ V}$ or 2.7 V (whichever is greater), $I_{OUT} = 1\text{ mA}$, $V_{EN} = 2\text{ V}$, and $C_{IN} = C_{OUT} = 2.2\text{-}\mu\text{F}$ ceramic, unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$.

PARAMETER		TEST CONDITIONS	TPS709xx			UNIT
			MIN	TYP	MAX	
V_{IN}	Input voltage range		2.7		30	V
V_{OUT}	Output voltage range		1.2		6.5	V
V_O	DC output accuracy	$V_{OUT} < 3.3\text{ V}$	-2		2	%
		$V_{OUT} \geq 3.3\text{ V}$	-1		1	%
ΔV_O	Line regulation	$(V_{OUT(\text{NOM})} + 1\text{ V}, 2.7\text{ V}) \leq V_{IN} \leq 30\text{ V}$		3	10	mV
	Load regulation	$V_{IN} = V_{OUT(\text{typ})} + 1.5\text{ V}$ or 3 V (whichever is greater), $100\text{ }\mu\text{A} \leq I_{OUT} \leq 150\text{ mA}$		20	50	mV
V_{DO}	Dropout voltage ⁽¹⁾⁽²⁾	TPS70933, $I_{OUT} = 50\text{ mA}$		295	650	mV
		TPS70933, $I_{OUT} = 150\text{ mA}$		960	1400	mV
		TPS70950, $I_{OUT} = 50\text{ mA}$		245	500	mV
		TPS70950, $I_{OUT} = 150\text{ mA}$		690	1200	mV
		TPS70965, $I_{OUT} = 50\text{ mA}$		180	500	mV
		TPS70965, $I_{OUT} = 150\text{ mA}$		460	1000	mV
I_{CL}	Output current limit ⁽³⁾	$V_{OUT} = 0.9 \times V_{OUT(\text{NOM})}$	200	320	500	mA
I_{GND}	Ground pin current	$I_{OUT} = 0\text{ mA}$, $V_{OUT} \leq 3.3\text{ V}$		1.35	2.05	μA
		$I_{OUT} = 0\text{ mA}$, $V_{OUT} > 3.3\text{ V}$		1.45	2.25	μA
		$I_{OUT} = 150\text{ mA}$		350		μA
$I_{SHUTDOWN}$	Shutdown current	$V_{EN} \leq 0.4\text{ V}$, $V_{IN} = 2.7\text{ V}$		150		nA
PSRR	Power-supply rejection ratio	$f = 10\text{ Hz}$		80		dB
		$f = 100\text{ Hz}$		62		dB
		$f = 1\text{ kHz}$		52		dB
V_N	Output noise voltage	$BW = 10\text{ Hz to }100\text{ kHz}$, $I_{OUT} = 10\text{ mA}$, $V_{IN} = 2.7\text{ V}$, $V_{OUT} = 1.2\text{ V}$		190		μV_{RMS}
t_{STR}	Start-up time ⁽⁴⁾	$V_{OUT(\text{NOM})} \leq 3.3\text{ V}$		200	600	μs
		$V_{OUT(\text{NOM})} > 3.3\text{ V}$		500	1500	μs
$V_{EN(\text{HI})}$	Enable pin high (enabled)		0.9			V
	Enable pin high (disabled)		0		0.4	V
I_{EN}	EN pin current	$EN = 1.0\text{ V}$, $V_{IN} = 5.5\text{ V}$		300		nA
I_{REV}	Reverse current (flowing out of IN pin)	$V_{OUT} = 3\text{ V}$, $V_{IN} = V_{EN} = 0\text{ V}$		10		nA
	Reverse current (flowing into OUT pin)	$V_{OUT} = 3\text{ V}$, $V_{IN} = V_{EN} = 0\text{ V}$		100		nA
t_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		+158		$^\circ\text{C}$
		Reset, temperature decreasing		+140		$^\circ\text{C}$
T_J	Operating junction temperature		-40		+125	$^\circ\text{C}$

(1) V_{DO} is measured with $V_{IN} = 0.98 \times V_{OUT(\text{NOM})}$.

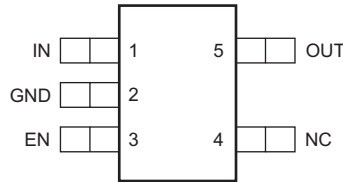
(2) Dropout is only valid when $V_{OUT} \geq 2.8\text{ V}$ because of the minimum input voltage limits.

(3) Measured with $V_{IN} = V_{OUT} + 3\text{ V}$ for $V_{OUT} \leq 2.5\text{ V}$. Measured with $V_{IN} = V_{OUT} + 2.5\text{ V}$ for $V_{OUT} > 2.5\text{ V}$.

(4) Startup time = time from EN assertion to $0.95 \times V_{OUT(\text{NOM})}$ and load = $47\text{ }\Omega$.

PIN CONFIGURATION

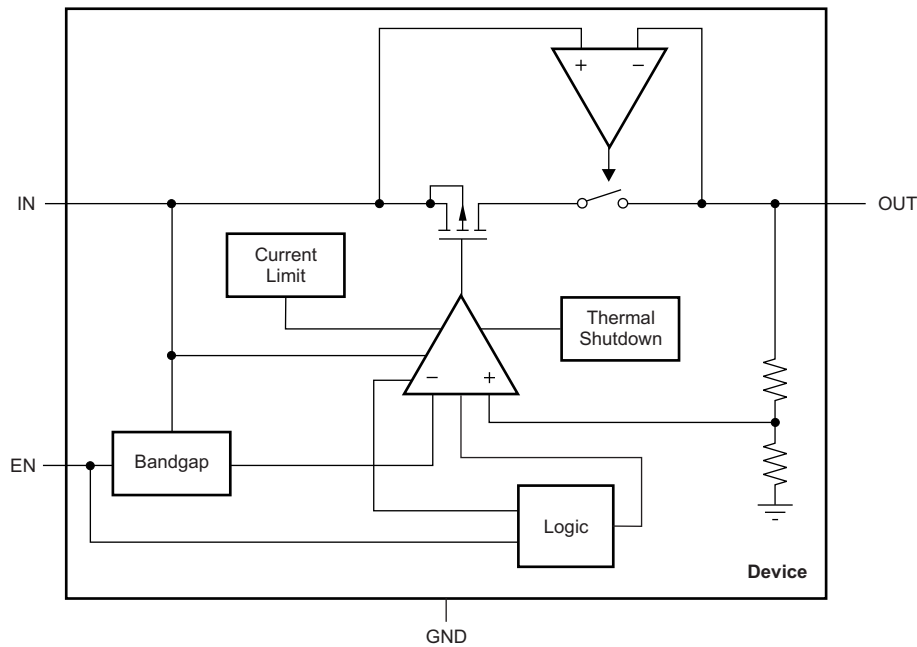
DBV PACKAGE
SOT23-5
(TOP VIEW)



PIN DESCRIPTIONS

NAME	PIN NO.	DESCRIPTION
EN	3	Enable Pin. Driving this pin high enables the device. Driving this pin low puts the device into low current shutdown. This pin has an internal pull-up resistor and can be left floating to enable the device.
GND	2	Ground
IN	1	Unregulated input to the device
NC	4	No internal connection
OUT	5	Regulated output voltage. A small 2.2- μ F or greater ceramic capacitor should be connected from this pin to ground to assure stability.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

Over operating temperature range ($T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$), $I_{OUT} = 10\text{ mA}$, $V_{EN} = 2\text{ V}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, and $V_{IN} = V_{OUT(TYP)} + 1\text{ V}$ or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at $T_J = +25^{\circ}\text{C}$.

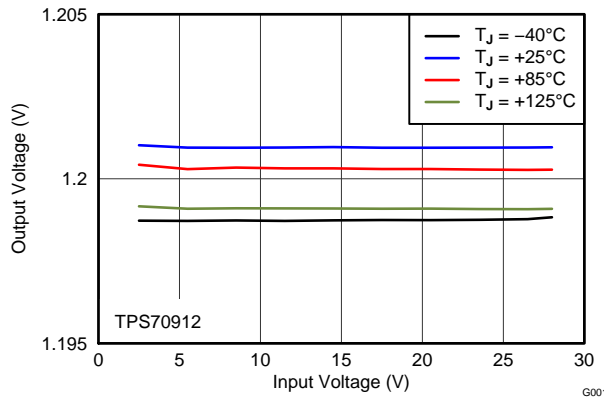


Figure 1. 1.2-V LINE REGULATION vs V_{IN} AND TEMPERATURE

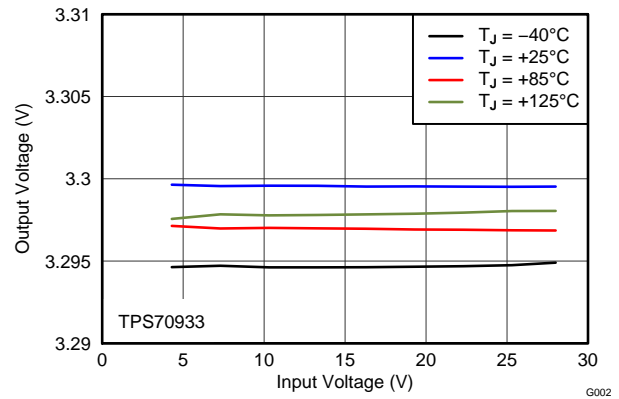


Figure 2. 3.3-V LINE REGULATION vs V_{IN} AND TEMPERATURE

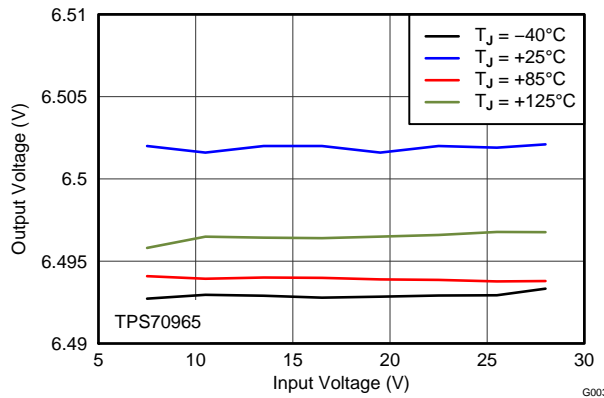


Figure 3. 6.5-V LINE REGULATION vs V_{IN} AND TEMPERATURE

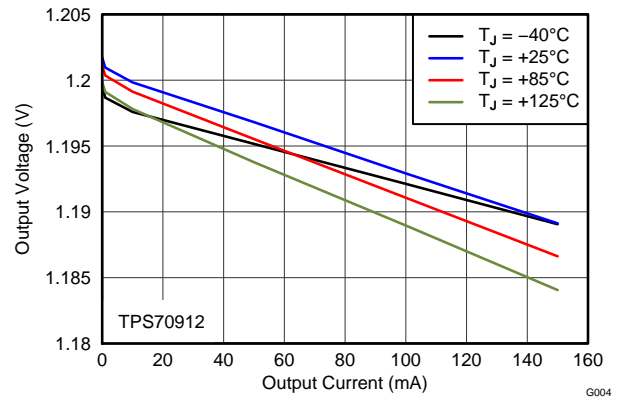


Figure 4. 1.2-V LOAD REGULATION vs I_{OUT} AND TEMPERATURE

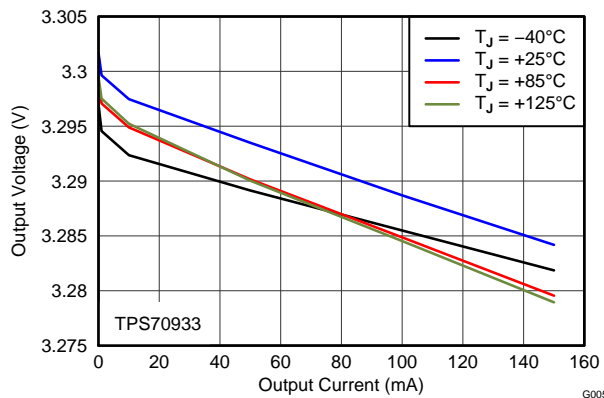


Figure 5. 3.3-V LOAD REGULATION vs I_{OUT} AND TEMPERATURE

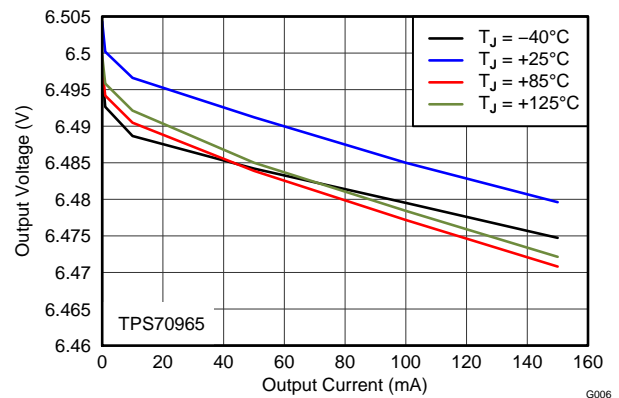


Figure 6. 6.5-V LOAD REGULATION vs I_{OUT} AND TEMPERATURE

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range ($T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$), $I_{OUT} = 10\text{ mA}$, $V_{EN} = 2\text{ V}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, and $V_{IN} = V_{OUT(TYP)} + 1\text{ V}$ or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at $T_J = +25^{\circ}\text{C}$.

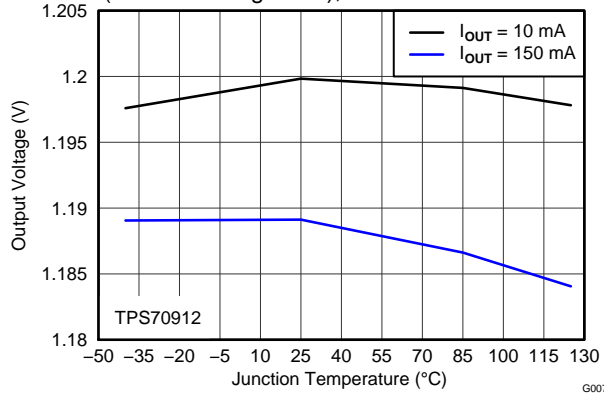


Figure 7. V_{OUT} vs TEMPERATURE

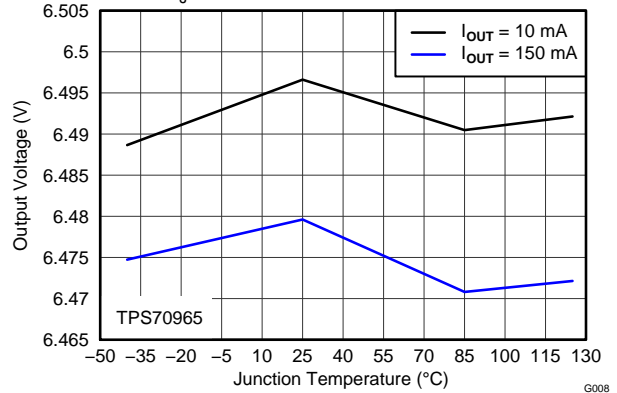


Figure 8. V_{OUT} vs TEMPERATURE

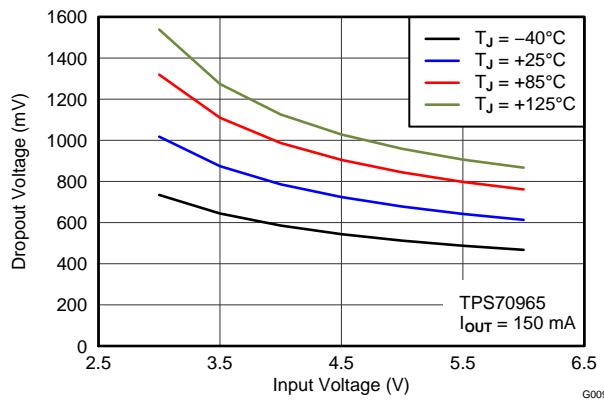


Figure 9. DROPOUT VOLTAGE vs V_{IN} AND TEMPERATURE

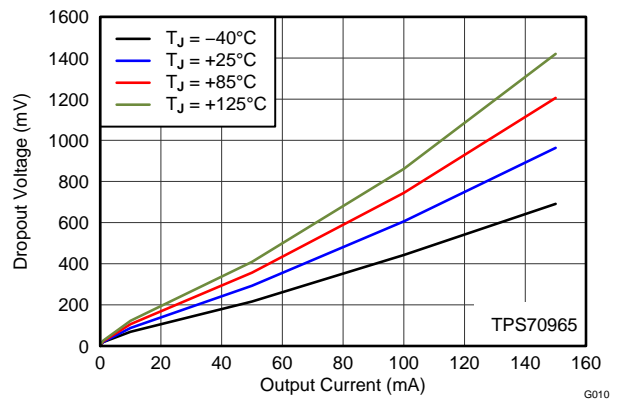


Figure 10. DROPOUT VOLTAGE vs I_{OUT} AND TEMPERATURE

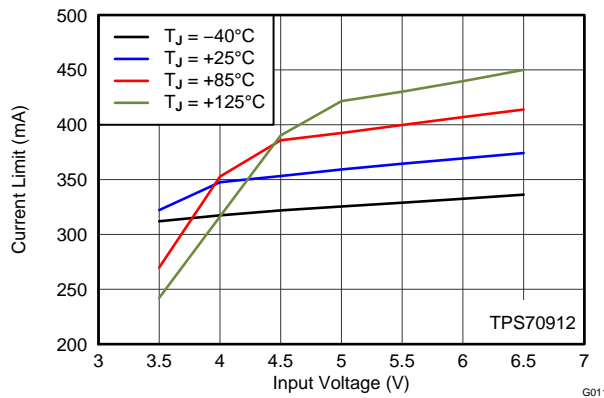


Figure 11. 1.2-V CURRENT LIMIT vs V_{IN} AND TEMPERATURE

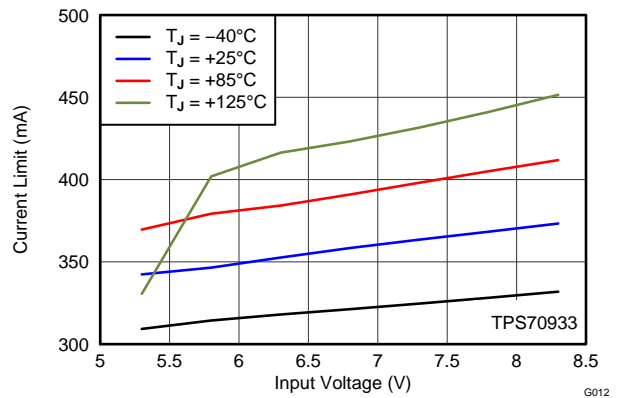


Figure 12. 3.3-V CURRENT LIMIT vs V_{IN} AND TEMPERATURE

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range ($T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$), $I_{OUT} = 10\text{ mA}$, $V_{EN} = 2\text{ V}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, and $V_{IN} = V_{OUT(TYP)} + 1\text{ V}$ or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at $T_J = +25^\circ\text{C}$.

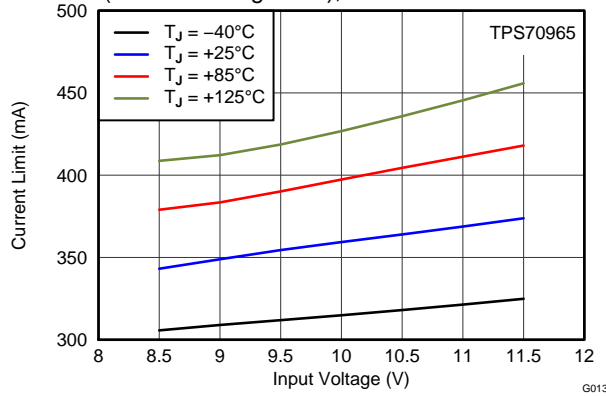


Figure 13. 6.5-V CURRENT LIMIT vs V_{IN} AND TEMPERATURE

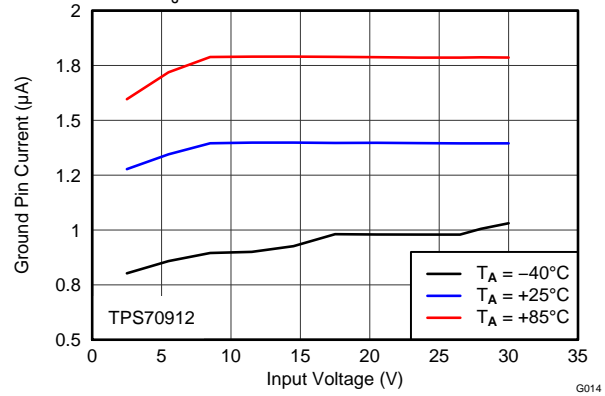


Figure 14. GND CURRENT vs V_{IN} AND TEMPERATURE

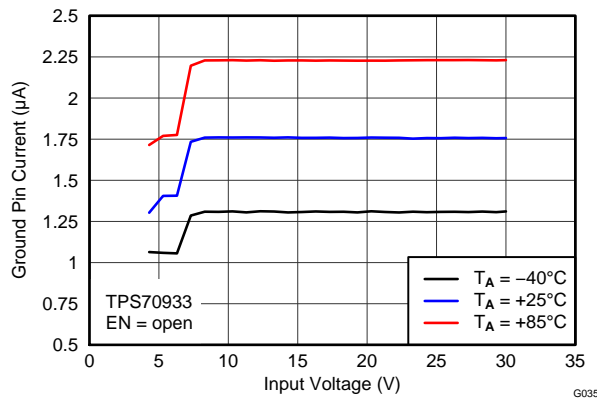


Figure 15. GND CURRENT vs V_{IN} AND TEMPERATURE

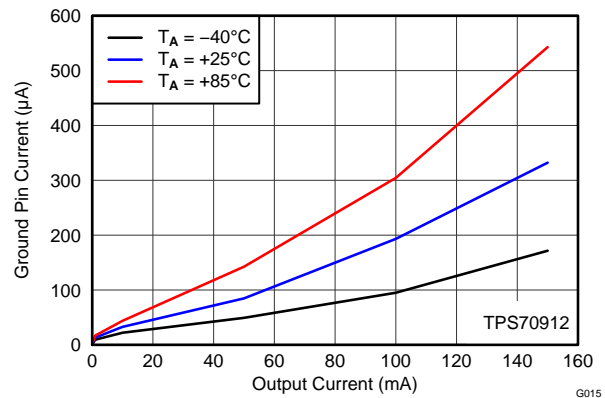


Figure 16. GND CURRENT vs I_{OUT} AND TEMPERATURE

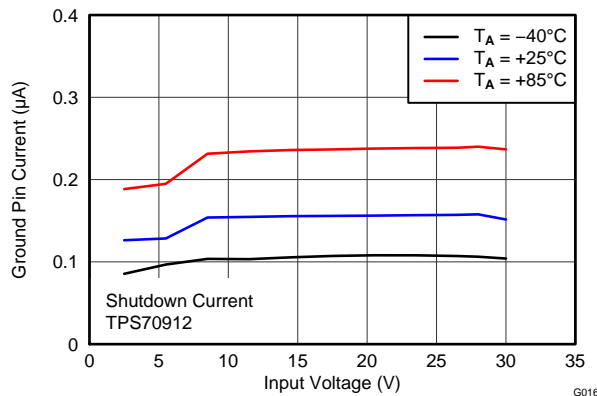


Figure 17. SHUTDOWN CURRENT vs V_{IN} AND TEMPERATURE

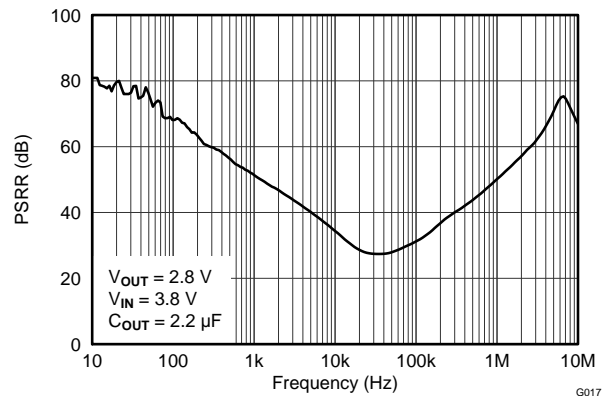


Figure 18. POWER-SUPPLY REJECTION RATIO vs FREQUENCY

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range ($T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$), $I_{OUT} = 10\text{ mA}$, $V_{EN} = 2\text{ V}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, and $V_{IN} = V_{OUT(TYP)} + 1\text{ V}$ or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at $T_J = +25^{\circ}\text{C}$.

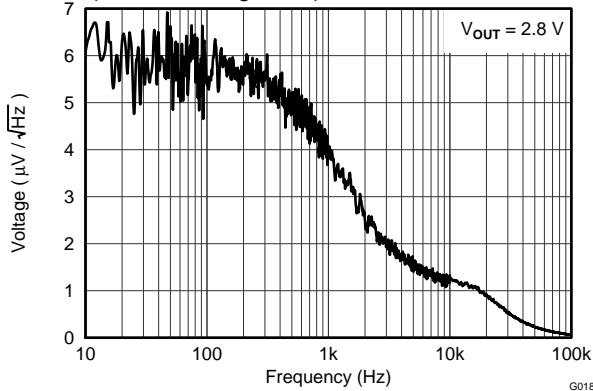


Figure 19. NOISE

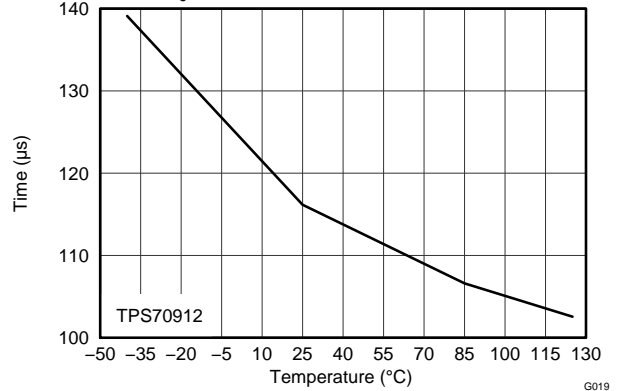


Figure 20. START-UP TIME vs TEMPERATURE

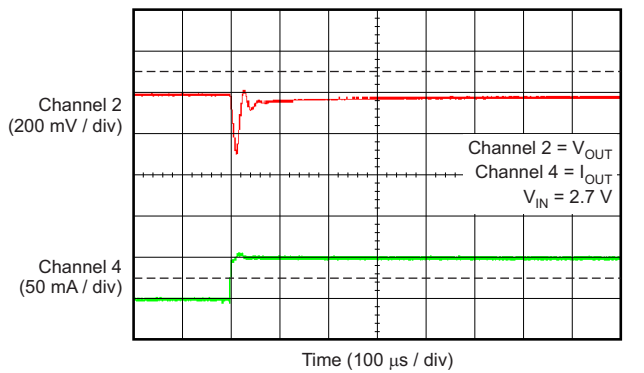


Figure 21. TPS70912 LOAD TRANSIENT (0 mA to 50 mA)

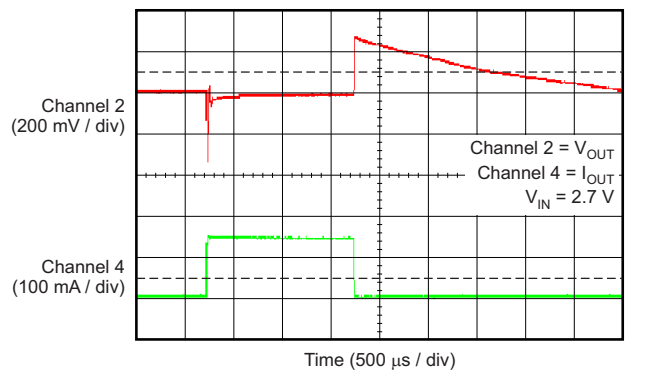


Figure 22. TPS70912 LOAD TRANSIENT (1 mA to 150 mA)

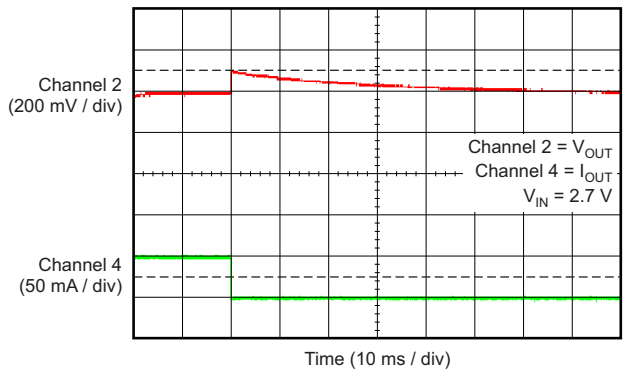


Figure 23. TPS70912 LOAD TRANSIENT (50 mA to 0 mA)

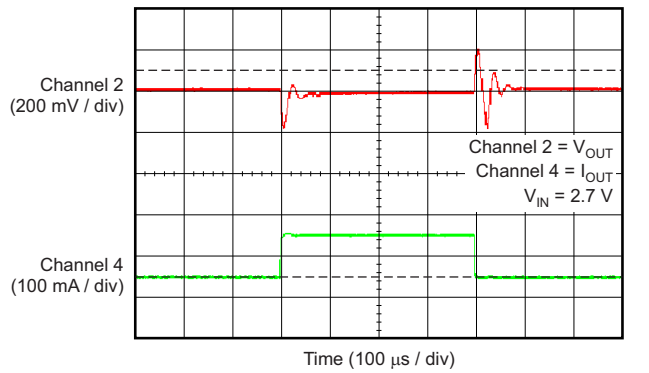


Figure 24. TPS70912 LOAD TRANSIENT (50 mA to 150 mA)

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range ($T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$), $I_{OUT} = 10\text{ mA}$, $V_{EN} = 2\text{ V}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, and $V_{IN} = V_{OUT(TYP)} + 1\text{ V}$ or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at $T_J = +25^{\circ}\text{C}$.

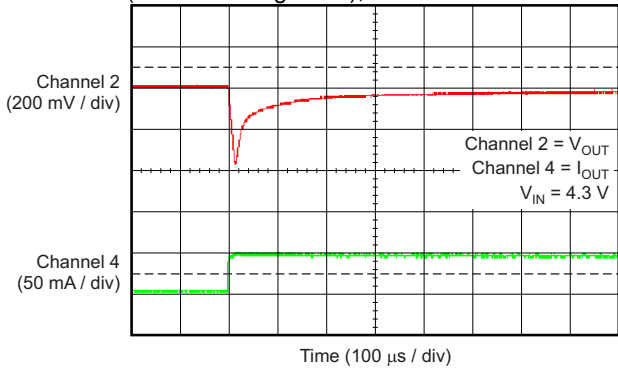


Figure 25. TPS70933 LOAD TRANSIENT (0 mA to 50 mA)

G024

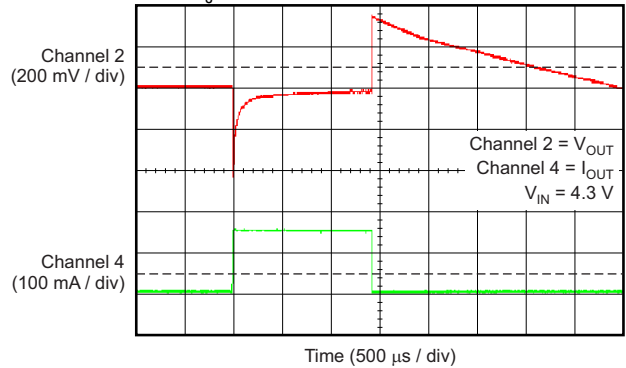


Figure 26. TPS70933 LOAD TRANSIENT (1 mA to 150 mA)

G025

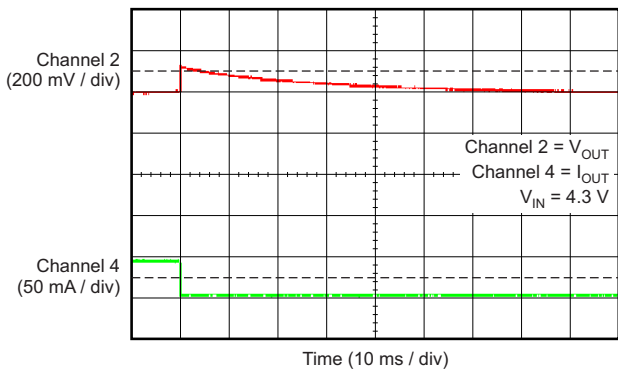


Figure 27. TPS70933 LOAD TRANSIENT (50 mA to 0 mA)

G026

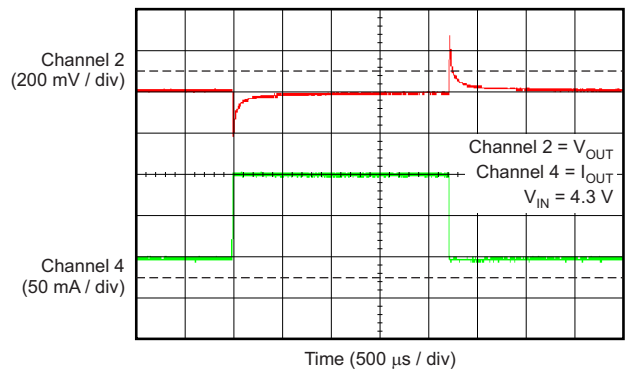


Figure 28. TPS70933 LOAD TRANSIENT (50 mA to 150 mA)

G027

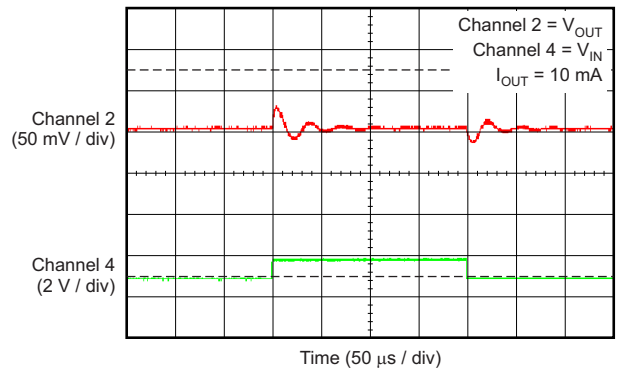


Figure 29. TPS70912 LINE TRANSIENT (2.7 V to 3.7 V)

G028

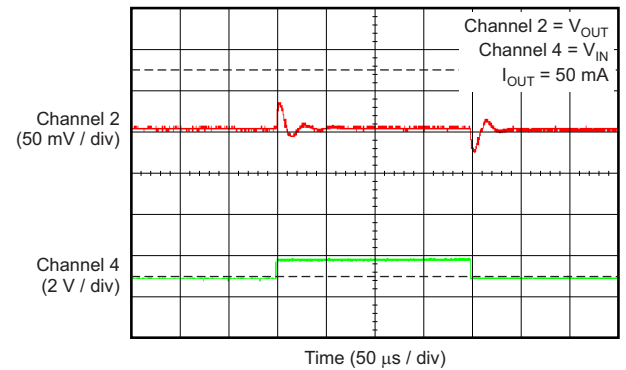


Figure 30. TPS70912 LINE TRANSIENT (2.7 V to 3.7 V)

G029

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range ($T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$), $I_{OUT} = 10\text{ mA}$, $V_{EN} = 2\text{ V}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, and $V_{IN} = V_{OUT(TYP)} + 1\text{ V}$ or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at $T_J = +25^{\circ}\text{C}$.

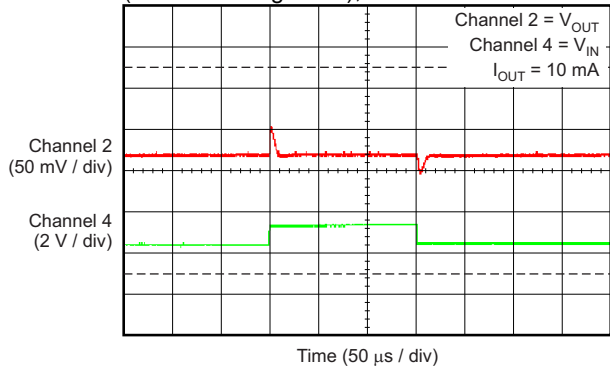


Figure 31. TPS70933 LINE TRANSIENT (4.3 V to 5.3 V)

G030

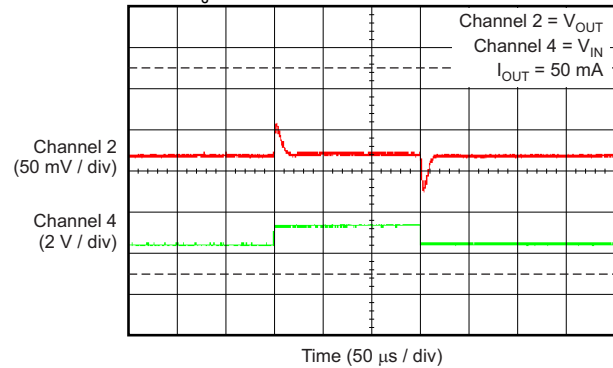


Figure 32. TPS70933 LINE TRANSIENT (4.3 V to 5.3 V)

G031

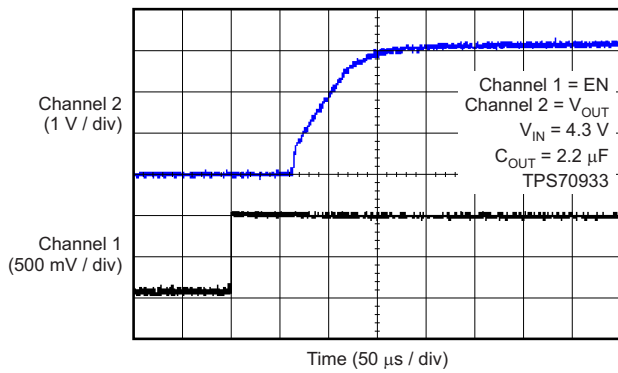


Figure 33. POWER-UP WITH ENABLE

G032

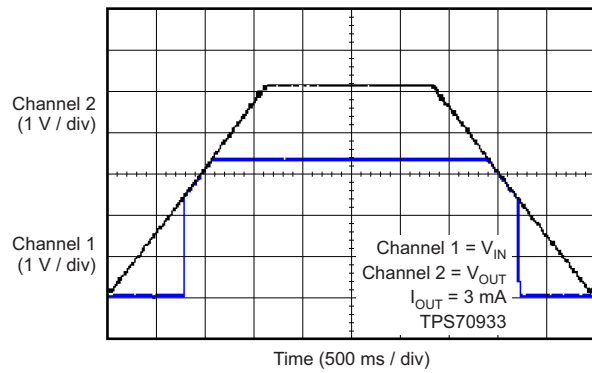


Figure 34. POWER-UP AND POWER-DOWN RESPONSE

G033

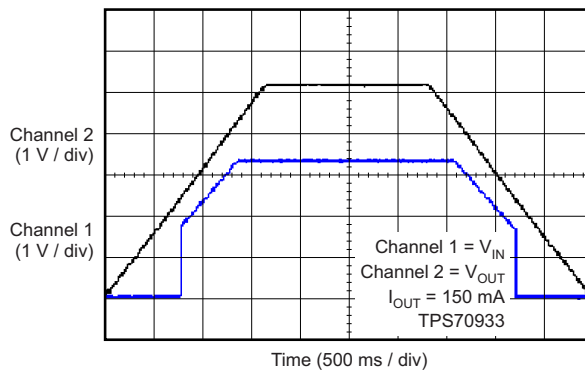


Figure 35. POWER-UP AND POWER-DOWN RESPONSE

G034

APPLICATION INFORMATION

The TPS709xx are a series of devices that belong to a new family of next-generation voltage regulators. These devices consume low quiescent current and deliver excellent line and load transient performance. This performance, combined with low noise, very good PSRR with little ($V_{IN} - V_{OUT}$) headroom, makes these devices ideal for RF portable applications, current limit, and thermal protection. The TPS709xx are specified from -40°C to $+125^{\circ}\text{C}$.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

Input and output capacitors should be placed as close to the device pins as possible. To improve ac performance (such as PSRR, output noise, and transient response), TI recommends that the board be designed with separate ground planes for V_{IN} and V_{OUT} , with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should be connected directly to the device GND pin.

INTERNAL CURRENT LIMIT

The TPS709xx internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. In such a case, the output voltage is not regulated, and can be measured as ($V_{OUT} = I_{LIMIT} \times R_{LOAD}$). The PMOS pass transistor dissipates [$(V_{IN} - V_{OUT}) \times I_{LIMIT}$] until a thermal shutdown is triggered and the device turns off. As the device cools down, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown; see the [Thermal Information](#) section for more details.

The TPS709xx are characterized over the recommended operating output current range up to 150 mA. The internal current limit begins to limit the output current at a minimum of 200 mA of output current. The TPS709xx continue to operate for output currents between 150 mA and 200 mA but some data sheet parameters may not be met.

DROPOUT VOLTAGE

The TPS709xx use a PMOS pass transistor to achieve low dropout. When ($V_{IN} - V_{OUT}$) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} approximately scales with the output current because the PMOS device behaves like a resistor in dropout.

The ground pin current of many linear voltage regulators increases substantially when the device is operated in dropout. This increase in ground pin current while operating in dropout can be several orders of magnitude larger than when the device is not in dropout. The TPS709xx employ a special control loop that limits the increase in ground pin current while operating in dropout. This functionality allows for the most efficient operation while in dropout conditions that can greatly increase battery run times.

INPUT AND OUTPUT CAPACITOR

The TPS709xx are stable with output capacitors with an effective capacitance of 2.0 μF or greater for output voltages below 1.5 V. For output voltages equal or greater than 1.5 V, the minimum effective capacitance for stability is 1.5 μF . The maximum capacitance for stability is 47 μF . The equivalent series resistance (ESR) of the output capacitor should be between 0 Ω and 0.2 Ω for stability.

The effective capacitance is the minimum capacitance value of a capacitor after taking into account variations resulting from tolerances, temperature, and dc bias effects. X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and ESR over temperature.

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1- μF to 2.2- μF capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. An input capacitor is necessary if line transients greater than 10 V in magnitude are anticipated.

TRANSIENT RESPONSE

As with any regulator, increasing the output capacitor size reduces over- and undershoot magnitude, but increases transient response duration.

UNDERVOLTAGE LOCK-OUT (UVLO)

The TPS709xx use an undervoltage lockout (UVLO) circuit to keep the output shut off until the internal circuitry operates properly.

REVERSE CURRENT PROTECTION

The TPS709xx have integrated reverse current protection. Reverse current protection prevents current from flowing from the OUT pin to the IN pin when output voltage is higher than input voltage. The reverse current protection circuitry places the power path in high impedance when it detects that the output voltage is higher than the input voltage. This setting reduces leakage current from the output to the input to 10 nA, typical. The reverse current protection is always active regardless of the enable pin logic state or if the OUT pin voltage is greater than 1.8 V. Reverse current can flow if the output voltage is less than 1.8 V and if input voltage is less than the output voltage.

If voltage is applied to the input pin, then the maximum voltage that can be applied to the OUT pin is the lower of three times the nominal output voltage or 6.5 V. For example, if the 1.2-V output voltage version is used, then the maximum reverse bias voltage that can be applied to the OUT pin is 3.6 V. If the 5.0-V output voltage version is used, then the maximum reverse bias voltage that can be applied to the OUT pin is 6.5 V.

THERMAL INFORMATION

Thermal protection disables the output when the junction temperature rises to approximately +165°C, allowing the device to cool. When the junction temperature cools to approximately +145°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C, maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The TPS709xx internal protection circuitry is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TPS709xx into thermal shutdown degrades device reliability.

POWER DISSIPATION

The ability to remove heat from the die is different for each package type, which presents different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to ambient air. Performance data for JEDEC low and high-K boards are given in the [Thermal Information](#) table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element, as shown in [Equation 1](#):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (1)$$

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2012) to Revision B	Page
• Changed <i>Line regulation</i> and <i>Load regulation</i> parameters in Electrical Characteristics table	3
• Changed I_{GND} parameter test conditions in Electrical Characteristics table	3
• Changed $I_{SHUTDOWN}$ parameter test conditions in Electrical Characteristics table	3
• Changed footnote 4 in Electrical Characteristics table	3
• Added Pin Configuration section	4
• Changed second paragraph of <i>Dropout Voltage</i> section	11
<hr/>	
Changes from Original (March 2012) to Revision A	Page
• Changed device status from Product Preview to Production Data	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS70912DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS70912DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS709135DBVR	PREVIEW	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS709135DBVT	PREVIEW	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS70916DBVR	PREVIEW	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS70916DBVT	PREVIEW	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS70918DBVR	PREVIEW	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS70918DBVT	PREVIEW	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS70919DBVR	PREVIEW	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS70919DBVT	PREVIEW	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS70925DBVR	PREVIEW	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS70925DBVT	PREVIEW	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS70927DBVR	PREVIEW	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS70927DBVT	PREVIEW	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS70928DBVR	PREVIEW	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS70928DBVT	PREVIEW	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS70930DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS70930DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS70933DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS70933DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS70936DBVR	PREVIEW	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS70936DBVT	PREVIEW	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS70938DBVR	PREVIEW	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS70938DBVT	PREVIEW	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS70939DBVR	PREVIEW	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS70939DBVT	PREVIEW	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS70950DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS70950DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS70912DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70912DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70930DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70930DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70933DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70933DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70950DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70950DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS70912DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70912DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70930DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70930DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70933DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70933DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70950DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70950DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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