Integrated Power Management Unit Top Specification

Check for Samples: TPS65910, TPS65910A, TPS659101, TPS659102, TPS659103, TPS659104, TPS659105, TPS659106, TPS659107, TPS659108, TPS659109

FEATURES

The purpose of the TPS65910 device is to provide the following resources:

- **Embedded power controller**
- **Two efficient step-down dc-dc converters for processor cores**
- **One efficient step-down dc-dc converter for I/O power**
- **One efficient step-up 5-V dc-dc converter**
- **SmartReflex™ compliant dynamic voltage management for processor cores**
- **8 LDO voltage regulators and one RTC LDO (internal purpose)**
- **One high-speed I^2C interface for general-purpose control commands (CTL-I^2C)**
- **One high-speed I^2C interface for SmartReflex Class 3 control and command (SR-I^2C)**
- **Two enable signals multiplexed with SR-I^2C, configurable to control any supply state and processor cores supply voltage**
- **Thermal shutdown protection and hot-die detection**
- **A real-time clock (RTC) resource with:**
  - **Oscillator for 32.768-kHz crystal or 32-kHz built-in RC oscillator**
  - **Date, time and calendar**
  - **Alarm capability**
- **One configurable GPIO**
- **DC-DC switching synchronization through internal or external 3-MHz clock**

APPLICATIONS

- **Portable and handheld systems**
- **OMAP3 power management**

DESCRIPTION

The TPS65910 is an integrated power-management IC available in 48-QFN package and dedicated to applications powered by one Li-Ion or Li-Ion polymer battery cell or 3-series Ni-MH cells, or by a 5-V input; it requires multiple power rails. The device provides three step-down converters, one step-up converter, and eight LDOs and is designed to support the specific power requirements of OMAP-based applications.

Two of the step-down converters provide power for dual processor cores and are controllable by a dedicated class-3 SmartReflex interface for optimum power savings. The third converter provides power for the I/Os and memory in the system.

The device includes eight general-purpose LDOs providing a wide range of voltage and current capabilities; they are fully controllable by the I^2C interface. The use of the LDOs is flexible; they are intended to be used as follows: Two LDOs are designated to power the PLL and video DAC supply rails on the OMAP based processors, four general-purpose auxiliary LDOs are available to provide power to other devices in the system, and two LDOs are provided to power DDR memory supplies in applications requiring these memories.

In addition to the power resources, the device contains an embedded power controller (EPC) to manage the power sequencing requirements of the OMAP systems and an (RTC).

Figure 1 shows the top-level diagram of the device.

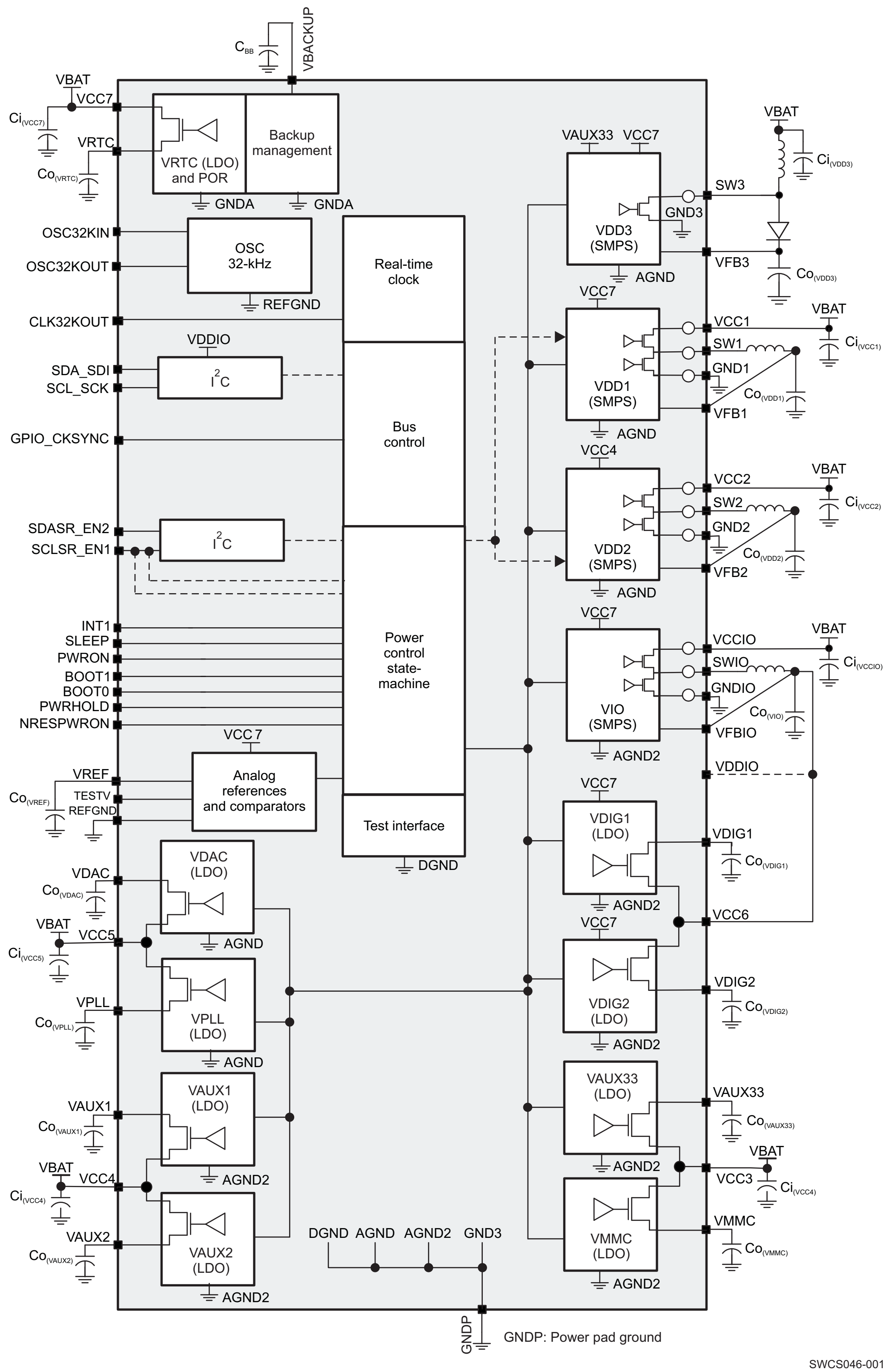


Figure 1. 48-QFN Top-Level Diagram

Table 1. SUPPORTED PROCESSORS AND CORRESPONDING PART NUMBERS

Compatible Processor(1)	Part Number(1)
TI processor - AM335x	TPS65910AA1RSL
TI processors - AM1705/07, AM1806/08, AM3505/17, AM3703/15, DM3730/25, OMAP-L137/38, OMAP3503/15/25/30, TMS320C6742/6/8	TPS65910A1RSL
Samsung - S5PV210, S5PC110	TPS659101A1RSL
Rockchip - RK29xx	TPS659102A1RSL
Samsung - S5PC100	TPS659103A1RSL
Samsung - S5P6440	TPS659104A1RSL
TI processors - DM643x, DM644x	TPS659105A1RSL
Reserved	TPS659106A1RSL
Freescale - i.MX27, Freescale - i.MX35	TPS659107A1RSL
Freescale - i.MX508	TPS659108A1RSL
Freescale - i.MX51	TPS659109A1RSL

(1) The RSL package is available in tape and reel. See for details for corresponding part numbers, quantities and ordering information.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)
Stresses beyond those listed under below may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated below are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
The absolute maximum ratings for the TPS65910 device are listed below:

PARAMETER	MIN	MAX	UNIT
Voltage range on pins/balls VCC1, VCC2, VCCIO, VCC3, VCC4, VCC5, VCC6, VCC7	–0.3	7	V
Voltage range on pins/balls VDDIO	–0.3	3.6	V
Voltage range on pins/balls OSC32KIN, OSC32KOUT, BOOT1, BOOT0	–0.3	$VRTC_{MAX}$ + 0.3	V
Voltage range on pins/balls SDA_SDI, SCL_SCK, SDASR_EN2, SCLSR_EN1, SLEEP, INT1, CLK32KOUT, NRESPWRON	–0.3	$VDDIO_{MAX}$ + 0.3	V
Voltage range on pins/balls PWRON	–0.3	7	V
Voltage range on pins/balls PWRHOLD(1) GPIO_CKSYNC(2)	–0.3	7	V
Functional junction temperature range	–45	150	°C
Peak output current on all other terminals than power resources	–5	5	mA

(1) I/O supplied from VDDIO but which can be driven from to a VBAT voltage level
(2) I/O supplied from VRTC but can be driven to a VBAT voltage level

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

Package	$R_{\theta ja}$ (°C/W)	TA < 25°C Power Rating (W)	DERATING FACTOR ABOVE 25 °C (mW/°C)	TA = 70°C Power (W)	TA = 85°C Power Rating (W)
RSL 48-QFN	37	2.6	37	1.48	1

The thermal resistance $R_{\theta JP}$ junction-to-power PAD of the RSL package is 1.1°C/W

The value of thermal resistance $R_{\theta JA}$ junction-to-ambient was measured on a high K.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)
Lists of the recommended operating maximum ratings for the TPS65910 device are given below.
Note1: VCC7 should be connected to the highest supply that is connected to the device VCCx pin. The exception is that VCC2 and VCC4 can be higher than VCC7.
Note2: VCC2 and VCC4 must be connected together (to the same voltage).
Note3: If VDD3 boost is used, VAUX33 must be set to 2.8 V or higher and enabled before VDD3.

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{CC}: Input voltage range on pins/balls VCC1, VCC2, VCCIO, VCC3, VCC4, VCC5, VCC7		2.7	3.6	5.5	V
V_{CCP}: Input voltage range on pins/balls VCC6		1.7	3.6	5.5	V
Input voltage range on pins/balls VDDIO		1.65	1.8/3.3	3.45	V
Input voltage range on pins/balls PWRON		0	3.6	5.5	V
Input voltage range on pins/balls SDA_SDI, SCL_SCK, SDASR_EN2, SCLSR_EN1, SLEEP		1.65	VDDIO	3.45	V
Input voltage range on pins/balls PWRHOLD, GPIO_CKSYNC		1.65	VDDIO	5.5	V
Input voltage range on balls BOOT1, BOOT0, OSC32KIN		1.65	VRTC	1.95	V
Operating free-air temperature, T_A		–40	27	85	°C
Junction temperature T_J		–40	27	125	°C
Storage temperature range		–65	27	150	°C
Lead temperature (soldering, 10 s)			260		°C
Power References					
VREF filtering capacitor $C_{O(VREF)}$	Connected from VREF to REFGND		100		nF
VDD1 SMPS					
Input capacitor $C_{I(VCC1)}$	X5R or X7R dielectric		10		µF
Filter capacitor $C_{O(VDD1)}$	X5R or X7R dielectric	4	10	12	µF
C_O filter capacitor ESR	f = 3 MHz		10	300	mΩ
Inductor $L_{O(VDD1)}$			2.2		µH
L_O inductor dc resistor DCR_L				125	mΩ
VDD2 SMPS					
Input capacitor $C_{I(VCC2)}$	X5R or X7R dielectric		10		µF
Filter capacitor $C_{O(VDD2)}$	X5R or X7R dielectric	4	10	12	µF
C_O filter capacitor ESR	f = 3 MHz		10	300	mΩ
Inductor $L_{O(VDD2)}$			2.2		µH
L_O inductor dc resistor DCR_L				125	mΩ
VIO SMPS					
Input capacitor $C_{I(VIO)}$	X5R or X7R dielectric		10		µF
Filter capacitor $C_{O(VIO)}$	X5R or X7R dielectric	4	10	12	µF
C_O filter capacitor ESR	f = 3 MHz		10	300	mΩ
Inductor $L_{O(VIO)}$			2.2		µH
L_O inductor dc resistor DCR_L				125	mΩ
VDIG1 LDO					
Input capacitor $C_{I(VCC6)}$	X5R or X7R dielectric		4.7		µF
Filtering capacitor $C_{O(VDIG1)}$		0.8	2.2	2.64	µF
C_O filtering capacitor ESR		0		500	mΩ
VDIG2 LDO					
Filtering capacitor $C_{O(VDIG2)}$		0.8	2.2	2.64	µF
C_O filtering capacitor ESR		0		500	mΩ
VPLL LDO					
Input capacitor $C_{I(VCC5)}$	X5R or X7R dielectric		4.7		µF
Filtering capacitor $C_{O(VPLL)}$		0.8	2.2	2.64	µF

RECOMMENDED OPERATING CONDITIONS (continued)

over operating free-air temperature range (unless otherwise noted)
Lists of the recommended operating maximum ratings for the TPS65910 device are given below.
Note1: VCC7 should be connected to the highest supply that is connected to the device VCCx pin. The exception is that VCC2 and VCC4 can be higher than VCC7.
Note2: VCC2 and VCC4 must be connected together (to the same voltage).
Note3: If VDD3 boost is used, VAUX33 must be set to 2.8 V or higher and enabled before VDD3.

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
C_O filtering capacitor ESR		0		500	mΩ
VDAC LDO					
Filtering capacitor $C_{O(VDAC)}$		0.8	2.2	2.64	µF
C_O filtering capacitor ESR		0		500	mΩ
VMMC LDO					
Input capacitor $C_{I(VCC4)}$	X5R or X7R dielectric		4.7		µF
Filtering capacitor $C_{O(VMMC)}$		0.8	2.2	2.64	µF
C_O filtering capacitor ESR		0		500	mΩ
VAUX33 LDO					
Filtering capacitor $C_{O(VAUX33)}$		0.8	2.2	2.64	µF
C_O filtering capacitor ESR		0		500	mΩ
VAUX1 LDO					
Input capacitor $C_{I(VCC3)}$	X5R or X7R dielectric		4.7		µF
Filtering capacitor $C_{O(VAUX1)}$		0.8	2.2	2.64	µF
C_O filtering capacitor ESR		0		500	mΩ
VAUX2 LDO					
Filtering capacitor $C_{O(VAUX2)}$		0.8	2.2	2.64	µF
C_O filtering capacitor ESR		0		500	mΩ
VRTC LDO					
Input capacitor $C_{I(VCC7)}$	X5R or X7R dielectric		4.7		µF
Filtering capacitor $C_{O(VRTC)}$		0.8	2.2	2.64	µF
C_O filtering capacitor ESR		0		500	mΩ
VDD3 SMPS					
Input capacitor $C_{I(VDD3)}$	X5R or X7R dielectric		4.7		
Filter capacitor $C_{O(VDD3)}$	X5R or X7R dielectric	4	10	12	µF
C_O filter capacitor ESR	f = 1 MHz		10	300	mΩ
Inductor $L_{O(VDD3)}$		2.8	4.7	6.6	µH
L_O inductor DC resistor DCR_L			50	500	mΩ
Backup Battery					
Backup battery capacitor C_{BB}	Battery or superCap supplying VBACKUP	5	10	2000	mF
	Capacitor supplying VBACKUP	1		40	µF
Series resistors	5 to 15 mF	10		1500	Ω
	100 to 2000 mF	5		15	
I^2C Interfaces					
SDA_SDI, SCL_SCK, SDASR_EN2, SCLSR_EN1 external pull-up resistor	Connected to VDDIO		1.2		kΩ
Crystal Oscillator (connected from OSC32KIN to OSC32KOUT)					
Crystal frequency	@ specified load cap value		32.768		kHz
Crystal tolerance	@ 27°C	–20	0	20	ppm
Frequency Temperature coefficient.	Oscillator contribution (not including crystal variation)	–0.5		0.5	ppm/°C
Secondary temperature coefficient		–0.04	–0.035	–0.03	ppm/°C^2
Voltage coefficient		–2		2	ppm/V

RECOMMENDED OPERATING CONDITIONS (continued)

over operating free-air temperature range (unless otherwise noted)
Lists of the recommended operating maximum ratings for the TPS65910 device are given below.
Note1: VCC7 should be connected to the highest supply that is connected to the device VCCx pin. The exception is that VCC2 and VCC4 can be higher than VCC7.
Note2: VCC2 and VCC4 must be connected together (to the same voltage).
Note3: If VDD3 boost is used, VAUX33 must be set to 2.8 V or higher and enabled before VDD3.

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Max crystal series resistor	@ Fundamental frequency			90	kΩ
Crystal load capacitor	According to crystal data sheet	6		12.5	pF
Load crystal oscillator Coscin ,Coscout	parallel mode Including parasitic PCB capacitor	12		25	pF
Quality factor		8000		80000	

ESD SPECIFICATIONS

over operating free-air temperature range (unless otherwise noted)

ESD METHOD	STANDARD REFERENCE	PERFORMANCE	TI STANDARD REQUIREMENTS
Human body model (HBM)	EIA/JESD22-A114D	2000 V	2000 V
Charge device model (CDM)	EIA/JESD22-C101C	500 V	500 V

I/O PULLUP AND PULLDOWN CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SDA_SDI, SCL_SCK, SDASR_EN2, SCLSR_EN1 Programmable pullup (DFT, default inactive)	Grounded, VDDIO = 1.8 V	–45%	8	+45%	kΩ
SLEEP programmable pulldown (default active)	@ 1.8 V, VRTC = 1.8 V	2	4.5	10	μA
PWRHOLD programmable pulldown (default active)	@ 1.8 V, VRTC = 1.8 V, VCC7 = 2.7 V	2	4.5	10	μA
	@ 5.5 V, VRTC = 1.8 V, VCC7 = 5.5 V	7	14	30	
BOOT0, BOOT1 programmable pulldown (default active)	@ 1.8 V, VRTC = 1.8 V	2	4.5	10	μA
NRESPWRON pulldown	@ 1.8 V, VCC7 = 5.5 V, OFF state	2	4.5	10	μA
32KCLKOUT pulldown (disabled in Active-sleep state)	@ 1.8 V, VRTC = 1.8 V, OFF state	2	4.5	10	μA
PWRON programmable pullup (default active)	Grounded, VCC7 = 5.5 V	–40	–31	–15	μA
GPIO_CKSYNC programmable pullup (default active)	Grounded, VRTC = 1.8 V	–27	–18	–9	μA

(1) The internal pullups on the CTL-I^2C and SR-I^2C balls are used for test purposes or when the SR-I^2C interface is not used. Discrete pullups to the VIO supply must be mounted on the board in order to use the I^2C interfaces. The internal I^2C pullups must not be used for functional applications

DIGITAL I/O VOLTAGE ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
Related I/O: PWRON					
Low-level input voltage V_{IL}				0.3 x VCC7	V
High-level input voltage V_{IH}		0.7 x VCC7			V
Related I/Os: PWRHOLD, GPIO_CKSYNC					
Low-level input voltage V_{IL}				0.45	V
High-level input voltage V_{IH}		1.3	VDDIO/VCC7	VCC7	V
Related I/Os: BOOT0, BOOT1, OSC32KIN					
Low-level input voltage V_{IL}				0.35 x VRTC	V
High-level input voltage V_{IH}		0.65 x VRTC			V
Related I/Os: SLEEP					
Low-level input voltage V_{IL}				0.35 x VDDIO	V
High-level input voltage V_{IH}		0.65 x VDDIO			V
Related I/Os: NRESPWRON, INT1, 32KCLKOUT					
Low-level output voltage V_{OL}	I_{OL} = 100 µA			0.2	V
	I_{OL} = 2 mA			0.45	V
High-level output voltage V_{OH}	I_{OH} = 100 µA	VDDIO – 0.2			V
	I_{OH} = 2 mA	VDDIO – 0.45			V
Related Open-Drain I/Os: GPIO0					
Low-level output voltage V_{OL}	I_{OL} = 100 µA			0.2	V
	I_{OL} = 2 mA			0.45	V
I²C-Specific Related I/Os: SCL, SDA, SCLSR_EN1, SDASR_EN2					
Low-level input voltage V_{IL}		–0.5		0.3 x VDDIO	V
High-level input voltage V_{IH}		0.7 x VDDIO			V
Hysteresis		0.1 x VDDIO			V
Low-level output voltage V_{OL} @ 3mA (sink current), VDDIO = 1.8 V				0.2 × VDDIO	V
Low-level output voltage V_{OL} @ 3mA (sink current), VDDIO = 3.3 V				0.4 x VDDIO	V

I²C INTERFACE AND CONTROL SIGNALS

over operating free-air temperature range (unless otherwise noted)

NO.	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX
		INT1 rise and fall times, C_L = 5 to 35 pF	5	10	ns
		NRESPWRON rise and fall times, C_L = 5 to 35 pF	5	10	ns
SLAVE HIGH–SPEED MODE					
		SCL/SCLSR_EN1 and SDA/SDASR_EN2 rise and fall time, C_L = 10 to 100 pF	10	80	ns
		Data rate		3.4	Mbps
I3	$t_{su(SDA-SCLH)}$	Setup time, SDA valid to SCL high	10		ns
I4	$t_{h(SCLL-SDA)}$	Hold time, SDA valid from SCL low	0	70	ns
I7	$t_{su(SCLH-SDAL)}$	Setup time, SCL high to SDA low	160		ns
I8	$t_{h(SDAL-SCLL)}$	Hold time, SCL low from SDA low	160		ns
I9	$t_{su(SDAH-SCLH)}$	Setup time, SDA high to SCL high	160		ns
SLAVE FAST MODE					
		SCL/SCLSR_EN1 and SDA/SDASR_EN2 rise and fall time, C_L = 10 to 400 pF	20 + 0.1 × C_L	250	ns
		Data rate		400	Kbps
I3	$t_{su(SDA-SCLH)}$	Setup time, SDA valid to SCL high	100		ns
I4	$t_{h(SCLL-SDA)}$	Hold time, SDA valid from SCL low	0	0.9	µs
I7	$t_{su(SCLH-SDAL)}$	Setup time, SCL high to SDA low	0.6		µs
I8	$t_{h(SDAL-SCLL)}$	Hold time, SCL low from SDA low	0.6		µs
I9	$t_{su(SDAH-SCLH)}$	Setup time, SDA high to SCL high	0.6		µs
SLAVE STANDARD MODE					
		SCL/SCLSR_EN1 and SDA/SDASR_EN2 rise and fall time, C_L = 10 to 400 pF		250	ns
		Data rate		100	Kbps
I3	$t_{su(SDA-SCLH)}$	Setup time, SDA valid to SCL high	250		ns
I4	$t_{h(SCLL-SDA)}$	Hold time, SDA valid from SCL low	0		µs
I7	$t_{su(SCLH-SDAL)}$	Setup time, SCL high to SDA low	4.7		µs
I8	$t_{h(SDAL-SCLL)}$	Hold time, SCL low from SDA low	4		µs
I9	$t_{su(SDAH-SCLH)}$	Setup time, SDA high to SCL high	4		µs
SWITCHING CHARACTERISTICS					
SLAVE HIGH–SPEED MODE					
I1	$t_{w(SCLL)}$	Pulse duration, SCL low	160		ns
I2	$t_{w(SCLH)}$	Pulse duration, SCL high	60		ns
SLAVE FAST MODE					
I1	$t_{w(SCLL)}$	Pulse duration, SCL low	1.3		µs
I2	$t_{w(SCLH)}$	Pulse duration, SCL high	0.6		µs
SLAVE STANDARD MODE					
I1	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		µs
I2	$t_{w(SCLH)}$	Pulse duration, SCL high	4		µs

POWER CONSUMPTION

over operating free-air temperature range (unless otherwise noted)
All current consumption measurements are relative to the FULL chip, all VCC inputs set to VBAT voltage.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device BACKUP state	VBAT = 2.4 V, VBACKUP = 0 V,		11	16	µA
	VBAT = 0 V, VBACKUP = 3.2 V		6	9	
Device OFF state	VBAT = 3.6 V, CK32K clock running				µA
	BOOT[1:0] = 00: 32-kHz RC oscillator		16.5	23	
	BOOT[1:0] = 01: 32-kHz quartz or bypass oscillator, BOOT0P = 0		15	20	
	BOOT[1:0] = 01, Backup Battery Charger on, VBACKUP = 3.2 V		32	42	
	VBAT = 5 V, CK32K clock running:		20	28	
	BOOT[1:0] = 00: RC oscillator				
Device SLEEP state	VBAT = 3.6 V, CK32K clock running, PWRHOLDP = 0				µA
	BOOT[1:0] = 00, 3 DC-DCs on, 5 LDOs and VRTC on, no load		295		
	BOOT[1:0] = 01, 3 DC-DCs on, 3 LDOs and VRTC on, no load, BOOT0P = 0		279		
Device ACTIVE state	VBAT = 3.6 V, CK32K clock running, PWRHOLDP = 0				mA
	BOOT[1:0] = 00, 3 DC-DCs on, 5 LDOs and VRTC on, no load		1		
	BOOT[1:0] = 01, 3 DC-DCs on, 3 LDOs and VRTC on, no load, BOOT0P = 0		0.9		
	BOOT[1:0] = 00, 3 DC-DCs on PWM mode (VDD1_PSKIP = VDD2_PSKIP = VIO_PSKIP = 0), 5 LDOs and VRTC on, no load		21		

POWER REFERENCES AND THRESHOLDS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output reference voltage (VREF terminal)	Device in active or low-power mode	–1%	0.85	+1%	V
Main battery charged threshold VMBCH (programmable)	Measured on VCC7 terminal Triggering monitored through NRESPRWON				V
	VMBCH_VSEL = 11, BOOT[1:0] = 11 or 00		3		
	VMBCH_VSEL = 10		2.9		
	VMBCH_VSEL = 01		2.8		
	VMBCH_VSEL = 00		bypassed		
Main battery discharged threshold VMBDCH (programmable)	Measured on VCC7 terminal (MTL prg) Triggering monitored through INT1		VMBCH – 100 mV		V
Main battery low threshold VMBLO (MB comparator)	Measured on VCC7 terminal (Triggering monitored on terminal NRESPWRON)	2.5	2.6	2.7	V
Main battery high threshold VMBHI	VBACKUP = 0 V, measured on terminal VCC7 (MB comparator)	2.6	2.75	3	V
	VBACKUP = 3.2 V, measured on terminal VCC7	2.5	2.55	3	
Main battery not present threshold VBNPR	Measured on terminal VCC7 (Triggering monitored on terminal VRTC)	1.9	2.1	2.2	V
Ground current (analog references + comparators + backup battery switch)	V_{CC} = 3.6 V				µA
	Device in OFF state		8		
	Device in ACTIVE or SLEEP state		20		

THERMAL MONITORING AND SHUTDOWN

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Hot-die temperature rising threshold	THERM_HDSEL[1:0] = 00	113	117	136	°C
	THERM_HDSEL[1:0] = 01		121		
	THERM_HDSEL[1:0] = 10		125		
	THERM_HDSEL[1:0] = 11		130		
Hot-die temperature hysteresis			10		°C
Thermal shutdown temperature rising threshold		136	148	160	°C
Thermal shutdown temperature hysteresis			10		°C
Ground current	Device in ACTIVE state, Temp = 27°C, VCC7 = 3.6 V		6		µA

32-kHz RTC CLOCK

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLK32KOUT rise and fall time	C_L = 35 pF			10	ns
Bypass Clock (OSC32KIN: input, OSC32KOUT floating)					
Input bypass clock frequency	OSCKIN input		32		kHz
Input bypass clock duty cycle	OSCKIN input	40%		60%	
Input bypass clock rise and fall time	10% – 90%, OSC32KIN input,		10	20	ns
CLK32KOUT duty cycle	Logic output signal	40%		60%	
Bypass clock setup time	32KCLKOUT output			1	ms
Ground current	Bypass mode			1.5	µA
Crystal oscillator (connected from OSC32KIN to OSC32KOUT)					
Output frequency	CK32KOUT output		32.768		kHz
Oscillator startup time	On power on			2	s
Ground current			1.5		µA
RC oscillator (OSC32KIN: grounded, OSC32KOUT floating)					
Output frequency	CK32KOUT output		32		kHz
Output frequency accuracy	@ 25°C	–15%	0%	+15%	
Cycle jitter (RMS)	Oscillator contribution			+10%	
Output duty cycle		+40%	+50%	+60%	
Settling time				150	µs
Ground current	Active @ fundamental frequency		4		µA

BACKUP BATTERY CHARGER

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Backup battery charging current	VBACKUP = 0 to 2.4 V, BBCHEN = 1	350	500	700	μA
End-of-charge backup battery voltage(1)	VCC7 = 3.6 V, BBSEL = 10	–3%	3.15	+3%	V
	VCC7 = 3.6 V, BBSEL = 00	–3%	3	+3%	
	VCC7 = 3.6 V, BBSEL = 01	–3%	2.52	+3%	
	VCC7 = 3.6 V, BBSEL = 11	VBAT – 0.3 V		VBAT	
Ground current	On mode		10		μA

(1) Note:
(a) BBSEL = 10, 00, or 01 intended to charge battery or superCap
(b) BBSEL = 11 intended to charge capacitor

VRTC LDO

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage V_{IN}	On mode	2.5		5.5	V
	Back-up mode	1.9		3	
DC output voltage V_{OUT}	On mode, 3.0 V < V_{IN} < 5.5 V	1.78	1.83	1.88	V
	Back-up mode, 2.3 V ≤ V_{IN} ≤ 2.6 V	1.72	1.78	1.84	
Rated output current I_{OUTmax}	On mode	20			mA
	Back-up mode	0.1			
DC load regulation	On mode, I_{OUT} = I_{OUTmax} to 0			50	mV
	Back-up mode, I_{OUT} = I_{OUTmax} to 0			50	
DC line regulation	On mode, V_{IN} = 3.0 V to V_{INmax} @ I_{OUT} = I_{OUTmax}			2.5	mV
	Back-up mode, V_{IN} = 2.3 V to 5.5 V @ I_{OUT} = I_{OUTmax}			25	
Transient load regulation	On mode, V_{IN} = V_{INmin} + 0.2 V to V_{INmax}			50 (1)	mV
	I_{OUT} = I_{OUTmax}/2 to I_{OUTmax} in 5 μs and I_{OUT} = I_{OUTmax} to I_{OUTmax}/2 in 5 μs				
Transient line regulation	On mode, V_{IN} = V_{INmin} + 0.5 V to V_{INmin} in 30 μs			25 (1)	mV
	And V_{IN} = V_{INmin} to V_{INmin} + 0.5 V in 30 μs, I_{OUT} = I_{OUTmax}/2				
Turn-on time	I_{OUT} = 0, V_{IN} rising from 0 up to 3.6 V, @ V_{OUT} = 0.1 V up to V_{OUTmin}		2.2		ms
Ripple rejection	V_{IN} = V_{INDC} + 100 mV_{pp} tone, V_{INDC+} = V_{INmin} + 0.1 V to V_{INmax} @ I_{OUT} = I_{OUTmax}/2				dB
	f = 217 Hz		55		
	f = 50 kHz		35		
Ground current	Device in ACTIVE state		23		μA
	Device in BACKUP or OFF state		3		

(1) These parameters are not tested. They are used for design specification only.

VIO SMPS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage (VCCIO and VCC7) V_{IN}	$I_{OUT} \leq 800$ mA	2.7		5.5	V
	V_{OUT} = 1.5 V or 1.8 V, I_{OUT} > 800 mA	3.2		5.5	
	V_{OUT} = 2.5 V, I_{OUT} > 800 mA	4.0		5.5	
	V_{OUT} = 3.3 V, I_{OUT} > 800 mA	4.4		5.5	
DC output voltage (V_{OUT})	PWM mode (VIO_PSKIP = 0) or pulse skip mode I_{OUT} to I_{MAX}				V
	VSEL=00	–3%	1.5	+3%	
	VSEL = 01, default BOOT[1:0] = 00 and 01	–3%	1.8	+3%	
	VSEL = 10	–3%	2.5	+3%	
	VSEL = 11	–3%	3.3	+3%	
	Power down		0		
Rated output current I_{OUTmax}	ILMAX[1:0] = 00, default	500			mA
	ILMAX[1:0] = 01	1000			
P-channel MOSFET	$V_{IN} = V_{INmin}$		300		mΩ
On-resistance $R_{DS(ON)\_PMOS}$	V_{IN} = 3.8 V		250	400	
P-channel leakage current I_{LK_PMOS}	$V_{IN} = V_{INMAX}$, SWIO = 0 V			2	µA
N-channel MOSFET	$V_{IN} = V_{MIN}$		300		mΩ
On-resistance $R_{DS(ON)\_NMOS}$	V_{IN} = 3.8 V		250	400	
N-channel leakage current I_{LK_NMOS}	$V_{IN} = V_{INmax}$, SWIO = V_{INmax}			2	µA
PMOS current limit (high-side)	$V_{IN} = V_{INmin}$ to V_{INmax}, ILMAX[1:0] = 00	650			mA
	$V_{IN} = V_{INmin}$ to V_{INmax}, ILMAX[1:0] = 01	1200			
	$V_{IN} = V_{INmin}$ to V_{INmax}, ILMAX[1:0] = 01	1700			
NMOS current limit (low-side)	Source current load:				mA
	$V_{IN} = V_{INmin}$ to V_{INmax}, ILMAX[1:0] = 00	650			
	$V_{IN} = V_{INmin}$ to V_{INmax}, ILMAX[1:0] = 01	1200			
	$V_{IN} = V_{INmin}$ to V_{INmax}, ILMAX[1:0] = 10	1700			
	Sink current load:				
	$V_{IN} = V_{INmin}$ to V_{INmax}, ILMAX[1:0] = 00	800			
	$V_{IN} = V_{INmin}$ to V_{INmax}, ILMAX[1:0] = 01	1200			
	$V_{IN} = V_{INmin}$ to V_{INmax}, ILMAX[1:0] = 10	1700			
DC load regulation	On mode, I_{OUT} = 0 to I_{OUTmax}			20	mV
DC line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax}			20	mV
Transient load regulation	V_{IN} = 3.8 V, V_{OUT} = 1.8 V I_{OUT} = 0 to 500 mA , Max slew = 100 mA/µs I_{OUT} = 700 to 1200 mA , Max slew = 100 mA/µs			50	mV
t on, off to on	I_{OUT} = 200 mA		350		µs
Overshoot	SMPS turned on		3%		
Power-save mode Ripple voltage	Pulse skipping mode, I_{OUT} = 1 mA		0.025 × V_{OUT}		V_{PP}
Switching frequency			3		MHz
Duty cycle				100	%
Minimum On Time $T_{ON(MIN)}$ P-channel MOSFET			35		ns
VFBIO internal resistance		0.5	1		MΩ
Discharge resistor for power-down sequence R_{DIS}	During device switch-off sequence Note: No discharge resistor is applied if VIO is turned off while the device is on.		30	50	Ω

VIO SMPS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Ground current (I_Q)	Off			1	μA
	PWM mode, I_{OUT} = 0 mA, V_{IN} = 3.8 V, VIO_PSKIP = 0		7500		
	Pulse skipping mode, no switching, 3-MHz clock on		250		
	Low-power (pulse skipping) mode, no switching				
	ST[1:0]=11		63		
Conversion efficiency	PWM mode, DCR_L < 50 mΩ, V_{OUT} = 1.8 V, V_{IN} = 3.6 V:				
	I_{OUT} = 10 mA		44%		
	I_{OUT} = 100 mA		87%		
	I_{OUT} = 400 mA		86%		
	I_{OUT} = 800 mA		76%		
	I_{OUT} = 1000 mA		72%		
	Pulse Skipping mode, DCR_L < 50 mΩ, V_{OUT} = 1.8 V, V_{IN} = 3.6 V:				
	I_{OUT} = 1 mA		71%		
	I_{OUT} = 10 mA		80%		
	I_{OUT} = 200 mA		87%		

VDD1 SMPS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage (VCC1 and VCC7) V_{IN}	I_{OUT} ≤ 1200 mA	2.7		5.5	V
	V_{OUT} = 0.6 V to 1.5 V, VGAIN_SEL = 00, I_{OUT} > 1200 mA	V_{OUT} + 2 V		5.5	
	2.5 V ≤ V_{OUT} ≤ 3.3 V, VGAIN_SEL = 10 or 11, I_{OUT} > 1200 mA	4.5		5.5	
DC output voltage (V_{OUT})	VGAIN_SEL = 00, I_{OUT} = 0 to I_{OUTmax}:				V
	max programmable voltage, SEL[6:0] = 1001011		1.5		
	default voltage, BOOT[1:0] = 00	–3%	1.2	+3%	
	default voltage, BOOT[1:0] = 01	–3%	1.2	+3%	
	min programmable voltage, SEL[6:0] = 0000011		0.6		
	SEL[6:0] = 000000: power down		0		
	VGAIN_SEL = 10, SEL = 0101011 = 43, I_{OUT} = 0 to I_{OUTmax}	–3%	2.2	+3%	V
	VGAIN_SEL = 11, SEL = 0101000 = 40, I_{OUT} = 0 to I_{OUTmax}	–3%	3.2	+3%	V
DC output voltage programmable step ($V_{OUTSTEP}$)	VGAIN_SEL = 00, 72 steps		12.5		mV
Rated output current I_{OUTmax}	ILMAX = 0, default	1000			mA
	ILMAX = 1	1500			
P-channel MOSFET On-resistance $R_{DS(ON)\_PMOS}$	V_{IN} = V_{INmin}		300		mΩ
	V_{IN} = 3.8 V		250	400	
P-channel leakage current I_{LK_PMOS}	V_{IN} = V_{INmax}, SW1 = 0 V			2	µA
N-channel MOSFET On-resistance $R_{DS(ON)\_NMOS}$	V_{IN} = V_{MIN}		300		mΩ
	V_{IN} = 3.8 V		250	400	
N-channel leakage current I_{LK_NMOS}	V_{IN} = V_{INmax}, SW1 = V_{INmax}			2	µA
PMOS current limit (high-side)	V_{IN} = V_{INmin} to V_{INmax}, ILMAX = 0	1150			mA
	V_{IN} = V_{INmin} to V_{INmax}, ILMAX = 1	2000			
NMOS current limit (low-side)	Source current load:				mA
	V_{IN} = V_{INmin} to V_{INmax}, ILMAX = 0	1150			
	V_{IN} = V_{INmin} to V_{INmax}, ILMAX = 1	2000			
	Sink current load:				
	V_{IN} = V_{INmin} to V_{INmax}, ILMAX = 0	1200			
	V_{IN} = V_{INmin} to V_{INmax}, ILMAX = 1	2000			
DC load regulation	On mode, I_{OUT} = 0 to I_{OUTmax}			20	mV
DC line regulation	On mode, V_{IN} = V_{INmin} to V_{INmax}			20	mV
Transient load regulation	V_{IN} = 3.8 V, V_{OUT} = 1.2 V			50	mV
	I_{OUT} = 0 to 500 mA , Max slew = 100 mA/µs				
	I_{OUT} = 700 mA to 1.2A , Max slew = 100 mA/µs				
t on, off to on	I_{OUT} = 200 mA		350		µs
Output voltage transition rate	From V_{OUT} = 0.6 V to 1.5 V and V_{OUT} = 1.5 V to 0.6 V I_{OUT} = 500 mA				mV/µs
	TSTEP[2:0] = 001		12.5		
	TSTEP[2:0] = 011 (default)		7.5		
	TSTEP[2:0] = 111		2.5		
Overshoot	SMPS turned on		3%		
Power-save mode ripple voltage	Pulse skipping mode, I_{OUT} = 1 mA		0.025 × V_{OUT}		V_{PP}
Switching frequency			3		MHz

VDD1 SMPS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Duty cycle				100	%
Minimum on time $t_{ON(MIN)}$ P-channel MOSFET			35		ns
VFB1 internal resistance		0.5	1		MΩ
Discharge resistor for power-down sequence R_{DIS}			30	50	Ω
Ground current (I_Q)	Off			1	µA
	PWM mode, I_{OUT} = 0 mA, V_{IN} = 3.8 V, VDD1_PSKIP = 0		7500		
	Pulse skipping mode, no switching		78		
	Low-power (pulse skipping) mode, no switching				
	ST[1:0] = 11		63		
Conversion efficiency	PWM mode, DCR_L < 0.1 Ω, V_{OUT} = 1.2 V, V_{IN} = 3.6 V:				
	I_{OUT} = 10 mA		35%		
	I_{OUT} = 200 mA		82%		
	I_{OUT} = 400 mA		81%		
	I_{OUT} = 800 mA		74%		
	I_{OUT} = 1500 mA		62%		
	Pulse skipping mode, DCR_L < 0.1Ω, V_{OUT} = 1.2 V, V_{IN} = 3.6 V:				
	I_{OUT} = 1 mA		59%		
	I_{OUT} = 10 mA		70%		
	I_{OUT} = 200 mA		82%		

VDD2 SMPS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage (VCC2 and VCC4) V_{IN}	I_{OUT} ≤ 1200 mA	2.7		5.5	V
	V_{OUT} = 0.6 V to 1.5 V, VGAIN_SEL = 00, I_{OUT} > 1200 mA	V_{OUT} + 2 V		5.5	
	2.5 V ≤ V_{OUT} ≤ 3.3 V, VGAIN_SEL = 10 or 11, I_{OUT} > 1200 mA	4.5		5.5	
DC output voltage (V_{OUT})	VGAIN_SEL = 00, I_{OUT} = 0 to I_{OUTmax}:				V
	max programmable voltage, SEL[6:0] = 1001011		1.5		
	default, BOOT[1:0] = 01	–3%	1.2	+3%	
	min programmable voltage, SEL[6:0] = 0000011		0.6		
	SEL[6:0] = 000000: power down		0		
	VGAIN_SEL = 10, SEL = 0101011 = 43	–3%	2.2	+3%	
	VGAIN_SEL = 11, default, BOOT[1:0] = 00	–3%	3.3	+3%	
DC output voltage programmable step ($V_{OUTSTEP}$)	VGAIN_SEL = 00, 72 steps		12.5		mV
Rated output current I_{OUTmax}	ILMAX = 0, default	1000			mA
	ILMAX = 1	1500			
P-channel MOSFET	V_{IN} = V_{INmin}		300		mΩ
On-resistance $R_{DS(ON)\_PMOS}$	V_{IN} = 3.8 V		250	400	
P-channel leakage current I_{LK_PMOS}	V_{IN} = V_{INmax}, SW2 = 0 V			2	μA
N-channel MOSFET	V_{IN} = V_{MIN}		300		mΩ
On-resistance $R_{DS(ON)\_NMOS}$	V_{IN} = 3.8 V		250	400	
N-channel leakage current I_{LK_NMOS}	V_{IN} = V_{INmax}, SW2 = V_{INmax}			2	μA
PMOS current limit (high-side)	V_{IN} = V_{INmin} to V_{INmax}, ILMAX = 0	1150			mA
	V_{IN} = V_{INmin} to V_{INmax}, ILMAX = 1	2200			
NMOS current limit (low-side)	Source current load:	1150			mA
	V_{IN} = V_{INmin} to V_{INmax}, ILMAX = 0	2000			
	V_{IN} = V_{INmin} to V_{INmax}, ILMAX = 1				
	Sink current load:				
	V_{IN} = V_{INmin} to V_{INmax}, ILMAX = 0	1200			
	V_{IN} = V_{INmin} to V_{INmax}, ILMAX = 1	2000			
DC load regulation	On mode, I_{OUT} = 0 to I_{OUTmax}			20	mV
DC line regulation	On mode, V_{IN} = V_{INmin} to V_{INmax} @ I_{OUT} = I_{OUTmax}			20	mV
Transient load regulation	V_{IN} = 3.8 V, V_{OUT} = 1.2 V			50	mV
	I_{OUT} = 0 to 500 mA , Max slew = 100 mA/μs				
	I_{OUT} = 700 mA to 1.2 A , Max slew = 100 mA/μs				
t on, Off to on	I_{OUT} = 200 mA		350		μs
Output voltage transition rate	From V_{OUT} = 0.6 V to 1.5 V and V_{OUT} = 1.5 V to 0.6 V I_{OUT} = 500 mA				μs
	TSTEP[2:0] = 001		12.5		
	TSTEP[2:0] = 011 (default)		7.5		
	TSTEP[2:0] = 111		2.5		
Power-save mode ripple voltage	Pulse skipping mode, I_{OUT} = 1 mA		0.025 V_{OUT}		V_{PP}
Overshoot			3%		
Switching frequency			3		MHz
Duty cycle				100	%
Minimum On time P-Channel MOSFET			35		ns

VDD2 SMPS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VFB2 internal resistance		0.5	1		MΩ
Discharge resistor for power-down sequence R_{DIS}			30	50	Ω
Ground current (I_Q)	Off			1	µA
	PWM mode, I_{OUT} = 0 mA, V_{IN} = 3.8 V, VDD2_PSKIP = 0		7500		
	Pulse skipping mode, no switching		78		
	Low-power (pulse skipping) mode, no switching				
	ST[1:0] = 11		63		
Conversion efficiency	PWM mode, DCR_L < 50 mΩ, V_{OUT} = 1.2 V, V_{IN} = 3.6 V:				
	I_{OUT} = 10 mA		35%		
	I_{OUT} = 200 mA		82%		
	I_{OUT} = 400 mA		81%		
	I_{OUT} = 800 mA		74%		
	I_{OUT} = 1200 mA		66%		
	I_{OUT} = 1500 mA		62%		
	Pulse skipping mode mode, DCR_L < 50 mΩ, V_{OUT} = 1.2 V, V_{IN} = 3.6 V:				
	I_{OUT} = 1 mA		59%		
	I_{OUT} = 10 mA		70%		
	I_{OUT} = 200 mA		82%		
	PWM mode, DCR_L < 50 mΩ, V_{OUT} = 3.3 V, V_{IN} = 5 V:				
	I_{OUT} = 10 mA		44%		
	I_{OUT} = 200 mA		90%		
	I_{OUT} = 400 mA		91%		
	I_{OUT} = 800 mA		88%		
	I_{OUT} = 1200 mA		84%		
	I_{OUT} = 1500 mA		81%		
	Pulse skipping mode mode, DCR_L < 50 mΩ, V_{OUT} = 3.3 V, V_{IN} = 5 V:				
	I_{OUT} = 1 mA		75%		
	I_{OUT} = 10 mA		83%		
	I_{OUT} = 200 mA		90%		

VDD3 SMPS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage V_{IN}		3		5.5	V
DC output voltage (V_{OUT})		4.65	5	5.25	V
Rated output current I_{OUTmax}		100			mA
N-channel MOSFET On-resistance $R_{DS(ON)\_NMOS}$	V_{IN} = 3.6 V		500		mΩ
N-channel MOSFET leakage current I_{LK_NMOS}	V_{IN} = V_{INmax}, SW3 = V_{INmax}			2	µA
N-channel MOSFET DC current limit	V_{IN} = V_{INmin} to V_{INmax}, sink current load	430	550		mA
Turn-on inrush current	V_{IN} = V_{INmin} to V_{INmax}			850	mA
Ripple voltage			20		mV
DC load regulation	On mode, I_{OUT} = 0 to I_{OUTmax}			100	mV
DC line regulation	On mode, V_{IN} = V_{INmin} to 5 V @ I_{OUT} = I_{OUTmax}			100	mV
Turn-on time	I_{OUT} = 8 mA, V_{OUT} = 0 to 4.4 V		200		µs
Overshoot			3%		
Switching frequency			1		MHz
VFB3 internal resistance			088		MΩ
Ground current (I_Q)	Off			1	µA
	I_{OUT} = 0 mA to I_{OUTmax}, V_{IN} = 3.6 V		360		µA
Conversion efficiency	V_{IN} = 3.6 V:				
	I_{OUT} = 10 mA		81%		
	I_{OUT} = 50 mA		85%		
	I_{OUT} = 100 mA		85%		

VDIG1 AND VDIG2 LDO

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage (VCC6) V_{IN}	V_{OUT} (VDIG1) = 1.2 V / 1.5 V @ 100 mA and				V
	V_{OUT} (VDIG2) =1.2 V / 1.1 V / 1.0 V	1.7		5.5	
	V_{OUT}(VDIG1) = 1.5 V and V_{OUT}(VDIG1,VDIG2) = 1.8 V @ 200mA	2.1		5.5	
	V_{OUT}(VDIG1) = 1.8 V and V_{OUT}(VDIG1) = 1.8 V	2.7		5.5	
	V_{OUT}(VDIG1) = 2.7 V	3.2		5	
VDIG1					
DC output voltage V_{OUT}	ON and Low-power mode, V_{IN} = V_{INmin} to V_{INmax}				V
	SEL = 11, I_{OUT} = 0 to I_{OUTmax}	–3%	2.7	+3%	
	SEL = 10 I_{OUT} = 0 to I_{OUTmax}	–3%	1.8	+3%	
	SEL = 01 I_{OUT} = 0 to 100 mA/I_{OUTmax}	–3%	1.5	+3%	
	SEL = 00, I_{OUT} = 0 to I_{OUTmax}, V_{IN} = V_{INmin} to 4 V, default BOOT[1:0] = 00 or 01	–3%	1.2	+3%	
Rated output current I_{OUTmax}	On mode	300			mA
	Low-power mode	1			
Load current limitation (short-circuit protection)	On mode, V_{OUT} = V_{OUTmin} – 100 mV	350	600		mA
Dropout voltage V_{DO}	ON mode, VDO = V_{IN} – V_{OUT}				mV
	V_{OUTtyp} = 2.7 V, V_{IN} = 2.8 V, I_{OUT} = I_{OUTmax}, T = 25°C		150		
	V_{OUTtyp} = 1.5 V, V_{IN} = 1.7 V, I_{OUT} = I_{OUTmax}, T = 25°C		300		
DC load regulation	On mode, I_{OUT} = I_{OUTmax} to 0			25	mV
DC line regulation	On mode, V_{IN} = V_{INmin} to V_{INmax} @ I_{OUT} = I_{OUTmax}			3	mV
Transient load regulation	ON mode, V_{IN} = 3.8 V		10		mV
	I_{OUT} = 20 mA to 180 mA in 5µs and I_{OUT} = 180 mA to 20 mA in 5 µs				
Transient line regulation	On mode, V_{IN} = 2.7 + 0.5 V to 2.7 in 30 µs,		2		mV
	And V_{IN} = 2.7 to 2.7 + 0.5 V in 30 µs, I_{OUT} = I_{OUTmax}/2				
Turn-on time	I_{OUT} = 0, @ V_{OUT} = 0.1 V up to V_{OUTmin}		100		µs
Turn-on inrush current			300		mA
Ripple rejection	V_{IN} = V_{INDC} + 100 mV_{pp} tone, $_{VINDC+}$= 3.8 V, I_{OUT} = I_{OUTmax}/2				dB
	f = 217 Hz		70		
	f = 50 kHz		40		
VDIG1 internal resistance	LDO off		400		Ω
Ground current	On mode, I_{OUT} = 0, VCC6 = VBAT, V_{OUT} = 2.7 V		54		µA
	On mode, I_{OUT} = 0, VCC6 = 1.8 V, V_{OUT} = 1.2 V		67		
	On mode, I_{OUT} = I_{OUTmax}, VCC6 = VBAT, V_{OUT} = 2.7 V		1870		
	On mode, I_{OUT} = I_{OUTmax}, VCC6 = 1.8 V, V_{OUT} = 1.2 V		1300		
	Low-power mode, VCC6 = VBAT, V_{OUT} = 2.7 V		13		
	Low-power mode, VCC6 = 1.8 V, V_{OUT} = 1.2 V		10		
	Off mode			1	
VDIG2					
DC output voltage V_{OUT}	On and low-power mode, V_{IN} = V_{INmin} to V_{INmax}				

VDIG1 AND VDIG2 LDO (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	SEL = 11, I_{OUT} = 0 to I_{OUTmax}	–3%	1.8	+3%	V
	SEL = 10 I_{OUT} = 0 to I_{OUTmax}, V_{IN} = V_{INmin} to 4 V	–3%	1.2	+3%	
	SEL = 01 I_{OUT} = 0 to 100 mA/I_{OUTmax}, V_{IN}= V_{INmin} to 4 V	–3%	1.1	+3%	
	SEL = 00, I_{OUT} = 0 to I_{OUTmax}, V_{IN} = V_{INmin} to 4 V, default BOOT[1:0] = 00 or 01	–3%	1	+3%	
Rated output current I_{OUTmax}	On mode	300			mA
	Low-power mode	1			
Load current limitation (short-circuit protection)	On mode, V_{OUT} = V_{OUTmin} – 100 mV	350	600		mA
Dropout voltage V_{DO}	ON mode, V_{DO} = V_{IN} – V_{OUT},				
	V_{OUTtyp} = 1.8 V, V_{IN} = 2.1 V, IOUT=I_{OUTmax}, T = 25°C		250		mV
DC load regulation	On mode, I_{OUT} = I_{OUTmax} to 0			25	mV
DC line regulation	On mode, V_{IN} = V_{INmin} to V_{INmax} @ I_{OUT} = I_{OUTmax}			3	mV
Transient load regulation	ON mode, V_{IN} = 3.8 V		10		mV
	I_{OUT} = 20 mA to 180 mA in 5μs and I_{OUT} = 180 mA to 20 mA in 5 μs				
Transient line regulation	On mode, V_{IN} = 2.7 + 0.5 V to 2.7 in 30 μs,		2		mV
	And V_{IN} = 2.7 to 2.7 + 0.5 V in 30 μs, I_{OUT} = I_{OUTmax}/2				
Turn-on time	I_{OUT} = 0, @ V_{OUT} = 0.1 V up to V_{OUTmin}		100		μs
Turn-on inrush current			300		mA
Ripple rejection	V_{IN} = V_{INDC} + 100 mV_{pp} tone, $_{VINDC+}$= 3.8 V, I_{OUT} = I_{OUTmax}/2				dB
	f = 217 Hz		70		
	f = 50 kHz		40		
VDIG2 internal resistance	LDO off		400		Ω
Ground current	On mode, I_{OUT} = 0, VCC6 = VBAT, V_{OUT} = 1.8 V		52		μA
	On mode, I_{OUT} = 0, VCC6 = 1.8 V, V_{OUT} = 1.0 V		67		
	On mode, I_{OUT} = I_{OUTmax}, VCC6 = VBAT, V_{OUT} = 1.8 V		1750		
	On mode, I_{OUT} = I_{OUTmax}, VCC6 = 1.8 V, V_{OUT} = 1.0 V		1300		
	Low-power mode, VCC6 = VBAT, V_{OUT} = 1.8 V		11		
	Low-power mode, VCC6 = 1.8 V, V_{OUT} = 1.0 V		10		
	Off mode			1	

VAUX33 AND VMMC LDO

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage (VCC3) V_{IN}	V_{OUT} (VAUX33) = 1.8 V / 2 V and V_{OUT} (VMMC) = 1.8 V	2.7		5.5	V
	V_{OUT} (VAUX33) = 2.8 V	3.2		5.5	
	V_{OUT} (VAUX33) = 3.3 V	3.6		5.5	
	V_{OUT} (VMMC) = 2.8 V @ 200 mA	3.2		5.5	
	V_{OUT} (VMMC) = 3.0 V	3.6		5.5	
	V_{OUT} (VMMC) = 3.3 V @ 200 mA	3.6		5.5	
VAUX33					
DC output voltage V_{OUT}	On and low-power mode, $V_{IN} = V_{INmin}$ to V_{INmax}				V
	SEL = 11, I_{OUT} = 0 to I_{OUTmax}, Default BOOT[1:0] = 01	–3%	3.3	+3%	
	SEL = 10, I_{OUT} = 0 to I_{OUTmax}	–3%	2.8	+3%	
	SEL = 01, I_{OUT} = 0 to I_{OUTmax}	–3%	2.0	+3%	
	SEL = 00, I_{OUT} = 0 to I_{OUTmax}, default BOOT[1:0] = 00	–3%	1.8	+3%	
Rated output current I_{OUTmax}	On mode	150			mA
	Low-power mode	1			
Load current limitation (short-circuit protection)	On mode, $V_{OUT} = V_{OUTmin}$ – 100 mV	350	500		mA
Dropout Voltage V_{DO}	On mode, V_{OUTtyp} = 2.8 V, $V_{DO} = V_{IN} – V_{OUT}$,				
	V_{IN} = 2.9 V, $I_{OUT} = I_{OUTmax}$, T = 25°C		150		mV
DC load regulation	On mode, $I_{OUT} = I_{OUTmax}$ to 0			20	mV
DC line regulation	On mode, $I_{OUT} = I_{OUTmax}$			3	mV
Transient load regulation	On mode, V_{IN} = 3.8 V		12		mV
	I_{OUT} = 0.1 × I_{OUTmax} to 0.9 × I_{OUTmax} in 5 µs and I_{OUT} = 0.9 × I_{OUTmax} to 0.1 × I_{OUTmax} in 5 µs				
Transient line regulation	On mode, $I_{OUT} = I_{OUTmax}$,$V_{IN} = V_{INmin}$ + 0.5 V to V_{INmin} in 30 µs		2		mV
	and $V_{IN} = V_{INmin}$ to V_{INmin} + 0.5 V in 30 µs, $I_{OUT} = I_{OUTmax}/2$				
Turn-on time	I_{OUT} = 0, @ V_{OUT} = 0.1 V up to V_{OUTmin}		100		µs
Turn-on inrush current			600		mA
Ripple Rejection	$V_{IN} = V_{INDC}$ + 100 mV_{pp} tone, V_{INDC+} = 3.8 V, $I_{OUT} = I_{OUTmax}/2$				dB
	f = 217 Hz		70		
	f = 50 kHz		40		
VAUX33 internal resistance	LDO off		70		Ω
Ground current	On mode, I_{OUT} = 0		55		µA
	On mode, $I_{OUT} = I_{OUTmax}$		1600		
	Low-power mode		15		
	Off mode			1	
VMMC					
DC output voltage V_{OUT}	On and low-power mode, $V_{IN} = V_{INmin}$ to V_{INmax}				V
	SEL = 11, I_{OUT} = 0 to 200 mA, default BOOT[1:0] = 00	–3%	3.3	+3%	
	SEL = 10, I_{OUT} = 0 to I_{OUTmax}	–3%	3.0	+3%	
	SEL = 01, I_{OUT} = 0 to 200 mA	–3%	2.8	+3%	
	SEL = 00, I_{OUT} = 0 to I_{OUTmax}, default BOOT[1:0] = 01	–3%	1.8	+3%	

VAUX33 AND VMMC LDO (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Rated output current I_{OUTmax}	On mode	300			mA
	Low-power mode	1			
Load current limitation (short-circuit protection)	On mode, $V_{OUT} = V_{OUTmin} - 100$ mV	350	500		mA
Dropout voltage V_{DO}	Dropout voltage V_{DO}				
	V_{IN} = 3.0 V, I_{OUT} = 200 mA, T = 25°C		200		mV
DC load regulation	On mode, $I_{OUT} = I_{OUTmax}$ to 0			25	mV
DC line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} @ $I_{OUT} = I_{OUTmax}$			3	mV
Transient load regulation	On mode, V_{IN} = 3.8 V		12		mV
	I_{OUT} = 20 mA to 180 mA in 5 µs and I_{OUT} = 180 mA to 20 mA in 5 µs				
Transient line regulation	On mode, I_{OUT} = 200 mA, $V_{IN} = V_{INmin}$ + 0.5 V to V_{INmin} in 30 µs		2		mV
	And $V_{IN} = V_{INmin}$ to V_{INmin} + 0.5 V in 30 µs, $I_{OUT} = I_{OUTmax}/2$				
Turn-on time	I_{OUT} = 0, @ V_{OUT} = 0.1 V up to V_{OUTmin}		100		µs
Ripple rejection	$V_{IN} = V_{INDC}$ + 100 mV_{pp} tone, V_{INDC+}= 3.8 V, $I_{OUT} = I_{OUTmax}/2$				
	f = 217 Hz		70		dB
	f = 50 kHz		40		
VMMC internal resistance	LDO Off		70		Ω
Ground current	On mode, I_{OUT} = 0		55		µA
	On mode, $I_{OUT} = I_{OUTmax}$		2700		
	Low-power mode		15		
	Off mode			1	

VAUX1 AND VAUX2 LDO

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage (VCC4) V_{IN}	V_{OUT} (VAUX1) = 1.8 V and V_{OUT} (AUX2) = 1.8 V	2.7		5.5	V
	V_{OUT} (VAUX1) = 2.5 V	3.2		5.5	
	V_{OUT} (VAUX1) = 2.8 V @ I_{load} = 200 mA and 2.85 V @ I_{load} = 200mA	3.2		5.5	
	V_{OUT} (VAUX2) = 2.8 V	3.2		5.5	
	V_{OUT} (VAUX2) = 2.9 V @ I_{load} = 100mA	3.2		5.5	
	V_{OUT} (VAUX2) = 3.3 V	3.6		5.5	
VAUX1					
DC output voltage V_{OUT}	On and low-power mode, V_{IN} = V_{INmin} to V_{INmax}				V
	SEL = 11, I_{OUT} = 0 to 200 mA	–3%	2.85	+3%	
	SEL = 10, I_{OUT} = 0 to 200 mA	–3%	2.8	+3%	
	SEL = 01, I_{OUT} = 0 to I_{OUTmax}	–3%	2.5	+3%	
	SEL = 00, I_{OUT} = 0 to I_{OUTmax}, default BOOT[1:0] = 00 or 01	–3%	1.8	+3%	
Rated output current I_{OUTmax}	On mode	300			mA
	Low-power mode	1			
Load current limitation (short-circuit protection)	On mode, V_{OUT} = V_{OUTmin} – 100 mV	350	500		mA
Dropout voltage V_{DO}	On mode, V_{OUTtyp} = 2.8 V, V_{DO} = V_{IN} – V_{OUT},				
	V_{IN} = 3.0 V, I_{OUT} = 200 mA, T = 25°C		200		mV
DC load regulation	On mode, I_{OUT} = 200 mA to 0			15	mA
DC line regulation	On mode, I_{OUT} = 200 mA			5	V
Transient load regulation	On mode, V_{IN} = 3.8 V, I_{OUT} = 20 mA to 180 mA in 5 µs		15		mV
	and I_{OUT} = 180 mA to 20 mA in 5µs				
Transient line regulation	On mode, I_{OUT} = 200 mA, V_{IN}= V_{INmin} + 0.5 V to V_{INmin} in 30 µs		2		mV
	and V_{IN} = V_{INmin} to V_{INmin} + 0.5v in 30 µs, I_{OUT} = I_{OUTmax}/2				
Turn-on time	I_{OUT} = 0, @ V_{OUT} = 0.1 V up to V_{OUTmin}, no load		100		µs
Turn-on inrush current			600		mA
Ripple Rejection	V_{IN} = V_{INDC} + 100 mV_{pp} tone, V_{INDC+} = 3.8 V, I_{OUT} = I_{OUTmax}/2				dB
	f = 217 Hz		70		
	f = 50 kHz		40		
VAUX1 internal resistance	LDO Off		80		Ω
Ground current	On mode, I_{OUT} = 0		60		µA
	On mode, I_{OUT} = I_{OUTmax}		2700		
	Low-power mode		12		
	Off mode			1	
VAUX2					
	On and low-power mode, V_{IN} = V_{INmin} to V_{INmax}				V
	SEL = 11, I_{OUT} = 0 to I_{OUTmax}	–3%	3.3	+3%	
	SEL = 10, I_{OUT} = 0 to 100 mA	–3%	2.9	+3%	
	SEL = 01, I_{OUT} = 0 to I_{OUTmax}	–3%	2.8	+3%	
	SEL = 00, I_{OUT} = 0 to I_{OUTmax}, default BOOT[1:0] = 00 or 01	–3%	1.8	+3%	
Rated output current I_{OUTmax}	On mode	150			mA
	Low-power mode	1			

VAUX1 AND VAUX2 LDO (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Load current limitation (short-circuit protection)	On mode, $V_{OUT} = V_{OUTmin}$ – 100 mV	350	500		mA
Dropout voltage V_{DO}	On mode, V_{OUTtyp} = 2.8 V, $V_{DO} = V_{IN} - V_{OUT}$ V_{IN} = 2.9 V, $I_{OUT} = I_{OUTmax}$, T = 25°C		150		mV
DC load regulation	On mode, $I_{OUT} = I_{OUTmax}$ to 0			15	mV
DC line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} @ $I_{OUT} = I_{OUTmax}$			2	mV
Transient load regulation	On mode, V_{IN} = 3.8 V, I_{OUT} = 0.1 × I_{OUTmax} to 0.9 × I_{OUTmax} in 5µs And I_{OUT} = 0.9 × IOUTmax to 0.1 × IOUTmax in 5us		12		mV
Transient line regulation	On mode, $I_{OUT} = I_{OUTmax}$, $V_{IN} = V_{INmin}$ + 0.5 V to V_{INmin} in 30 µs And $V_{IN} = V_{INmin}$ to V_{INmin} + 0.5 V in 30 µs, $I_{OUT} = I_{OUTmax}/2$		2		mV
Turn-on time	I_{OUT} = 0, @ V_{OUT} = 0.1 V up to V_{OUTmin}		100		µs
Turn-on Inrush current			600		mA
Ripple rejection	$V_{IN} = V_{INDC}$ + 100 mV_{pp} tone, V_{INDC+} = 3.8 V, $I_{OUT} = I_{OUTmax}/2$ f = 217 Hz f = 50 kHz		 70 40		dB
VAUX2 internal resistance	LDO off		80		Ω
Ground current	On mode, I_{OUT} = 0 On mode, $I_{OUT} = I_{OUTmax}$ Low-power mode Off mode		60 1600 12 	 1	µA

VDAC AND VPLL LDO

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage (VCC5) V_{IN}	V_{OUT}(VDAC) = 1.8 V and V_{OUT}(VPLL) = 1.8 V / 1.1 V / 1.0 V	2.7		5.5	V
	V_{OUT}(VDAC) = 2.6 V and V_{OUT}(VPLL) = 2.5 V	3.0		5.5	
	V_{OUT}(VDAC) = 2.8 V / 2.85 V	3.2		5.5	
VDAC					
DC Output voltage V_{OUT}	On and low-power mode, $V_{IN} = V_{INmin}$ to V_{INmax}				V
	SEL = 11, I_{OUT} = 0 to I_{OUTmax}	–3%	2.85	+3%	
	SEL = 10, I_{OUT} = 0 to I_{OUTmax}	–3%	2.8	+3%	
	SEL = 01, I_{OUT} = 0 to I_{OUTmax}	–3%	2.6	+3%	
	SEL = 00, I_{OUT} = 0 to I_{OUTmax}, default BOOT[1:0] = 00 or 01	–3%	1.8	+3%	
Rated output current I_{OUTmax}	On mode	150			mA
	Low-power mode	1			
Load current limitation (short-circuit protection)	On mode, $V_{OUT} = V_{OUTmin}$ – 100 mV	350	500		mA
Dropout Voltage V_{DO}	On mode, V_{OUTtyp} = 2.8 V, $V_{DO} = V_{IN} – V_{OUT}$,		150		mV
	V_{IN} = 2.9 V, $I_{OUT} = I_{OUTmax}$, T = 25°C				
DC load regulation	On mode, $V_{OUT} = V_{OUTmin}$ – 100 mV			15	mV
DC line regulation	On mode, V_{OUT} = 1.8 V, $I_{OUT} = I_{OUTmax}$			2	mV
Transient load regulation	On mode, V_{IN} = 3.8 V, I_{OUT} = 0.1 × I_{OUTmax} to 0.9 × I_{OUTmax} in 5 µs		15		mV
	And I_{OUT} = 0.9 × I_{OUTmax} to 0.1 × I_{OUTmax} in 5 µs				
Transient line regulation	On mode, $I_{OUT} = I_{OUTmax}$, $V_{IN} = V_{INmin}$ + 0.5 V to V_{INmin} in 30 µs		0.5		mV
	And $V_{IN} = V_{INmin}$ to V_{INmin} + 0.5 V in 30 µs, $I_{OUT} = I_{OUTmax}/2$				
Turn-on time	I_{OUT} = 0, @ V_{OUT} = 0.1 V up to V_{OUTmin}		100		µs
Turn-on Inrush current			600		mA
Ripple Rejection	$V_{IN} = V_{INDC}$ + 100 mV_{pp} tone, V_{INDC+} = 3.8 V, $I_{OUT} = I_{OUTmax}/2$				dB
	f = 217 Hz		70		
	f = 50 kHz		40		
VDAC internal resistance	LDO off		360		kΩ
Ground current	On mode, I_{OUT} = 0		60		µA
	On mode, $I_{OUT} = I_{OUTmax}$		1600		
	Low-power mode		12		
	Off mode			1	
VPLL					
DC output voltage V_{OUT}	On and low-power mode, $V_{IN} = V_{INmin}$ to V_{INmax}				V
	SEL = 11, I_{OUT} = 0 to I_{OUTmax}	–3%	2.5	+3%	
	SEL = 10, I_{OUT} = 0 to I_{OUTmax}, default BOOT[1:0 = 00 or 01	–3%	1.8	+3%	
	SEL = 01, I_{OUT} = 0 to I_{OUTmax}	–3%	1.1	+3%	
	SEL = 00, I_{OUT} = 0 to I_{OUTmax}	–3%	1.0	+3%	
Rated output current I_{OUTmax}	On mode	50			mA
	Low-power mode	1			
Load current limitation (short-circuit protection)	On mode, $V_{OUT} = V_{OUTmin}$ – 100 mV	200	400		mA
Dropout voltage V_{DO}	On mode, V_{OUTtyp} = 2.5 V, $V_{DO} = V_{IN} – V_{OUT}$,		100		mV

VDAC AND VPLL LDO (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	V_{IN} = 2.5 V, I_{OUT} = I_{OUTmax}, T = 25°C				
DC load regulation	On mode, I_{OUT} = I_{OUTmax} to 0			10	mV
DC line regulation	On mode, V_{IN} = V_{INmin} to V_{INmax} @ I_{OUT} = I_{OUTmax}			1	mV
Transient load regulation	On mode, V_{IN} = 3.8 V, I_{OUT} = 0.1 × I_{OUTmax} to 0.9 × I_{OUTmax} in 5 µs And I_{OUT} = 0.9 × I_{OUTmax} to 0.1 × I_{OUTmax} in 5 µs		9		mV
Transient line regulation	On mode, V_{IN} = V_{INmin} + 0.5 V to V_{INmin} in 30 µs And V_{IN} = V_{INmin} to V_{INmin} + 0.5 V in 30 µs, I_{OUT} = I_{OUTmax}/2		0.5		mV
Turn-on time	I_{OUT} = 0, @ V_{OUT} = 0.1 V up to V_{OUTmin}		100		µs
Turn-on inrush current			300		mA
Ripple rejection	V_{IN} = V_{INDC} + 100 mV_{pp} tone, V_{INDC+} = 3.8 V, I_{OUT} = I_{OUTmax}/2 f = 217 Hz f = 50 kHz		 70 40		dB
VPLL internal resistance	LDO off		535		kΩ
Ground current	On mode, I_{OUT} = 0 On mode, I_{OUT} = I_{OUTmax} Low-power mode Off mode		60 1600 12 	 1	µA

SWITCH-ON/-OFF SEQUENCES AND TIMING

Time slot length can be selected to be 0.5 ms or 2 ms through the EEPROM for an OFF-to-ACTIVE transition or through the value programmed in the register DEVCTRL2_REG for a SLEEP-to-ACTIVE transition.

BOOT1 = 0, BOOT0 = 0

Table 2 provides details about the EEPROM setting for the BOOT modes. The power-up sequence for this boot mode is provided in Figure 2.

Table 2. Fixed Boot Mode: 00

Register	Bit	Description	TPS65910 Boot 00
VDD1_OP_REG	SEL	VDD1 voltage level selection for boot	1.2 V
VDD1_REG	VGAIN_SEL	VDD1 Gain selection, x1 or x2	x1
EEPROM		VDD1 time slot selection	3
DCDCCTRL_REG	VDD1_PSKIP	VDD1 pulse skip mode enable	skip enabled
VDD2_OP_REG/VDD2_SR_REG	SEL	VDD2 voltage level selection for boot	1.1 V
VDD2_REG	VGAIN_SEL	VDD2 Gain selection, x1 or x3	x3
EEPROM		VDD2 time slot selection	2
DCDCCTRL_REG	VDD2_PSKIP	VDD2 pulse skip mode enable	skip enabled
VIO_REG	SEL	VIO voltage selection	1.8 V
EEPROM		VIO time slot selection	1
DCDCCTRL_REG	VIO_PSKIP	VIO pulse skip mode enable	skip enabled
EEPROM		VDD3 time slot	OFF
VDIG1_REG	SEL	LDO voltage selection	1.2 V
EEPROM		LDO time slot	OFF
VDIG2_REG	SEL	LDO voltage selection	1.0 V
EEPROM		LDO time slot	OFF

SWITCH-ON/-OFF SEQUENCES AND TIMING (continued)

Table 2. Fixed Boot Mode: 00 (continued)

VDAC_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	5
VPLL_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	4
VAUX1_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	1
VMMC_REG	SEL	LDO voltage selection	3.3 V
EEPROM		LDO time slot	6
VAUX33_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	OFF
VAUX2_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	5
CLK32KOUT pin		CLK32KOUT time slot	7
NRESPWRON pin		NRESPWRON time slot	7 + 1
VRTC_REG	VRTC_OFFMASK	0: VRTC LDO will be in low-power mode during OFF state 1: VRC LDO will be in full-power mode during OFF state	Low-power mode
DEVCTRL_REG	RTC_PWDN	0: RTC in normal power mode 1: Clock gating of RTC register and logic, low-power mode	1
DEVCTRL_REG	CK32K_CTRL	0: Clock source is crystal/external clock 1: Clock source is internal RC oscillator	RC
DEVCTRL2_REG	TSLOT_LENGTH[0]	Boot sequence time slot duration: 0: 0.5 ms 1: 2 ms	2 ms
DEVCTRL2_REG	IT_POL	0: INT1 signal will be active-low 1: INT1 signal will be active-high	Active-low
INT_MSK_REG	VMBHI_IT_MSK	0: Device will automatically switch-on at NOSUPPLY to OFF or BACKUP to OFF transition 1: Startup reason required before switch-on	0: Automatic switch-on from supply insertion
VMBCH_REG	VMBCH_SEL[1:0]	Select threshold for main battery comparator threshold VMBCH.	3 V

Figure 2 shows the 00 Boot mode timing characteristics.

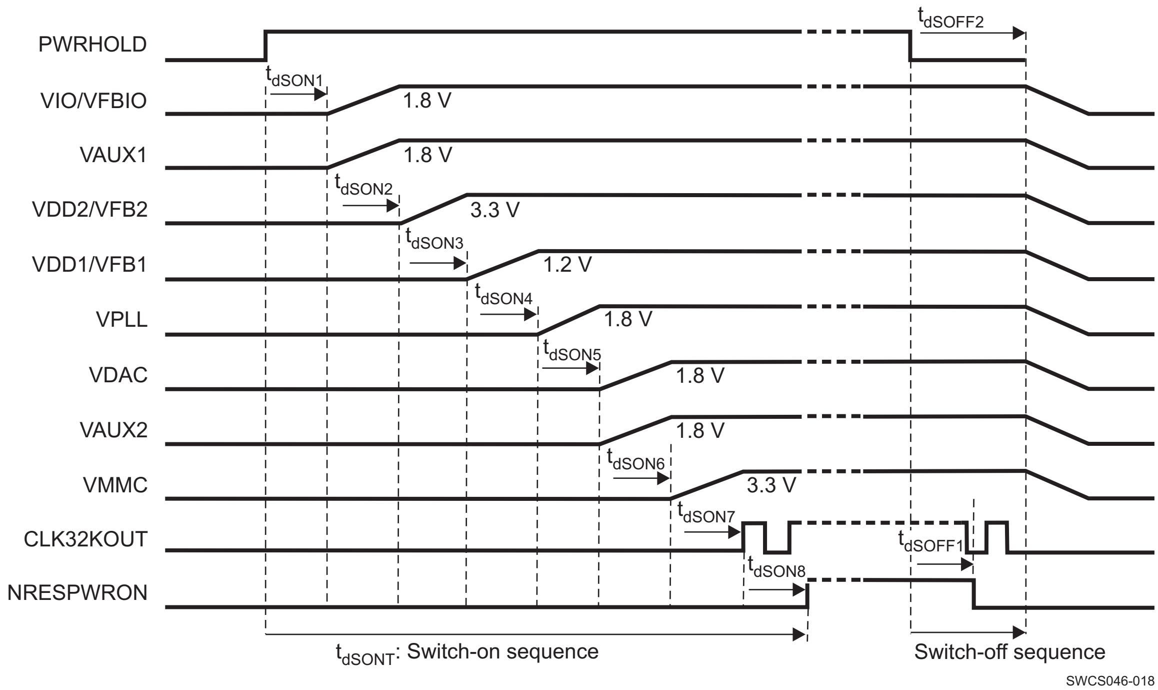


Figure 2. Boot Mode: BOOT1 = 0, BOOT0 = 0

Table 3 lists the 00 Boot mode timing characteristics.

Table 3. Boot Mode: BOOT1 = 0, BOOT0 = 0 Timing Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{dSON1}	PWRHOLD rising edge to VIO, VAUX1 enable delay		$66 \times t_{CK32k} = 2060$		µs
t_{dSON2}	VIO to VDD2 enable delay		$64 \times t_{CK32k} = 2000$		µs
t_{dSON3}	VDD2 to VDD1 enable delay		$64 \times t_{CK32k} = 2000$		µs
t_{dSON4}	VDD1 to VPLL enable delay		$64 \times t_{CK32k} = 2000$		µs
t_{dSON5}	VPLL to VDAC,VAUX2 enable delay		$64 \times t_{CK32k} = 2000$		µs
t_{dSON6}	VDAC to VMMC enable delay		$64 \times t_{CK32k} = 2000$		µs
	VMMC to CLK32KOUT rising edge delay		$64 \times t_{CK32k} = 2000$		µs
t_{dSON8}	CLK32KOUT to NRESPWRON rising edge delay		$64 \times t_{CK32k} = 2000$		µs
t_{dSONT}	Total switch-on delay		16		ms
t_{dSOFF1}	PWRHOLD falling edge to NRESPWRON falling edge delay		$2 \times t_{CK32k} = 62.5$		µs
$t_{dSOFF1B}$	NRESPWRON falling edge to CLK32KOUT low delay		$3 \times t_{CK32k} = 92$		µs
t_{dSOFF2}	PWRHOLD falling edge to supplies and reference disable delay		$5 \times t_{CK32k} = 154$		µs

Registers default setting: CK32K_CTRL = 1 (32-kHz RC oscillator is used), RTC_PWDN = 1 (RTC domain off), IT_POL = 0 (INt2 interrupt flag active low), VMBHI_IT_MSK = 0 (automatic switch-on on Battery plug), VMBCH_SEL = 11.

BOOT1 = 0, BOOT0 = 1

Table 4 provides details about the EEPROM setting for the BOOT modes. The power-up sequence for this boot mode is provided in Figure 3.

Table 4. Fixed Boot Mode: 01

Register	Bit	Description	TPS65910 Boot 01
VDD1_OP_REG	SEL	VDD1 voltage level selection for boot	1.2 V
VDD1_REG	VGAIN_SEL	VDD1 Gain selection, x1 or x2	x1
EEPROM		VDD1 time slot selection	3
DCDCCTRL_REG	VDD1_PSKIP	VDD1 pulse skip mode enable	Skip enabled
VDD2_OP_REG/VDD2_SR_REG	SEL	VDD2 voltage level selection for boot	1.2 V
VDD2_REG	VGAIN_SEL	VDD2 Gain selection, x1 or x3	x1
EEPROM		VDD2 time slot selection	4
DCDCCTRL_REG	VDD2_PSKIP	VDD2 pulse skip mode enable	Skip enabled
VIO_REG	SEL	VIO voltage selection	1.8 V
EEPROM		VIO time slot selection	1
DCDCCTRL_REG	VIO_PSKIP	VIO pulse skip mode enable	Skip enabled
EEPROM		VDD3 time slot	OFF
VDIG1_REG	SEL	LDO voltage selection	1.2 V
EEPROM		LDO time slot	OFF
VDIG2_REG	SEL	LDO voltage selection	1.0 V
EEPROM		LDO time slot	OFF
VDAC_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	OFF
VPLL_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	2
VAUX1_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	OFF
VMMC_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	OFF
VAUX33_REG	SEL	LDO voltage selection	3.3 V
EEPROM		LDO time slot	6
VAUX2_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	5
CLK32KOUT pin		CLK32KOUT time slot	7
NRESPWRON pin		NRESPWRON time slot	7+1
VRTC_REG	VRTC_OFFMASK	0: VRTC LDO will be in low-power mode during OFF state 1: VRC LDO will be in full-power mode during OFF state	low-power mode
DEVCTRL_REG	RTC_PWDN	0: RTC in normal power mode 1: Clock gating of RTC register and logic, low-power mode	1
DEVCTRL_REG	CK32K_CTRL	0: Clock source is crystal/external clock 1: Clock source is internal RC oscillator	Crystal
DEVCTRL2_REG	TSLOT_LENGTH [0]	Boot sequence time slot duration: 0: 0.5 ms 1: 2 ms	2 ms
DEVCTRL2_REG	IT_POL	0: INT1 signal will be active-low 1: INT1 signal will be active-high	Active-low
INT_MSK_REG	VMBHI_IT_MSK	0: Device will automatically switch-on at NOSUPPLY to OFF or BACKUP to OFF transition 1: Startup reason required before switch-on	0: Automatic switch-on from supply insertion
VMBCH_REG	VMBCH_SEL[1:0]	Select threshold for main battery comparator threshold VMBCH.	3 V

Figure 3 shows the 01 Boot mode timing characteristics.

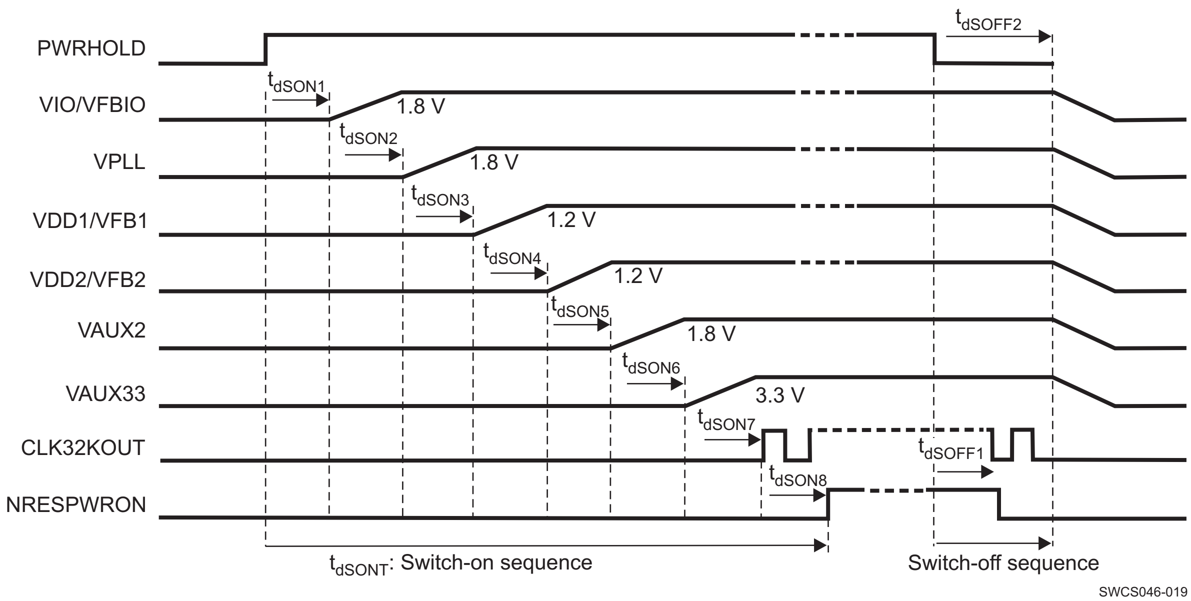


Figure 3. Boot Mode: BOOT1 = 0, BOOT0 = 1

Table 5 lists the 01 Boot mode timing characteristics.

Table 5. Boot Mode: BOOT1 = 0, BOOT0 = 1 Timing Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{dSON1}	PWRHOLD rising edge to VIO enable delay		66 × t_{CK32k} = 2060		µs
t_{dSON2}	VIO to VPLL enable delay		64 × t_{CK32k} = 2000		µs
t_{dSON3}	VPLL to VDD1 enable delay		64 × t_{CK32k} = 2000		µs
t_{dSON4}	VDD1 to VDD2 enable delay		64 × t_{CK32k} = 2000		µs
t_{dSON5}	VDD2 to VAUX2 enable delay		64 × t_{CK32k} = 2000		µs
	VAUX2 to VAUX33 enable delay		64 × t_{CK32k} = 2000		µs
t_{dSON7}	VAUX33 to CLK32KOUT enable delay		64 × t_{CK32k} = 2000		µs
t_{dSON8}	CLK32KOUT to NRESPWRON enable delay		64 × t_{CK32k} = 2000		µs
t_{dSONT}	Total switch-on delay		16		ms
t_{dSOFF1}	PWRHOLD falling edge to NRESPWRON falling edge		2 × t_{CK32k} = 62.5		µs
$t_{dSOFF1B}$	NRESPWRON falling edge to CLK32KOUT low delay		3 × t_{CK32k} = 92		µs
t_{dSOFF2}	PWRHOLD falling edge to supplies disable delay		5 × t_{CK32k} = 154		µs

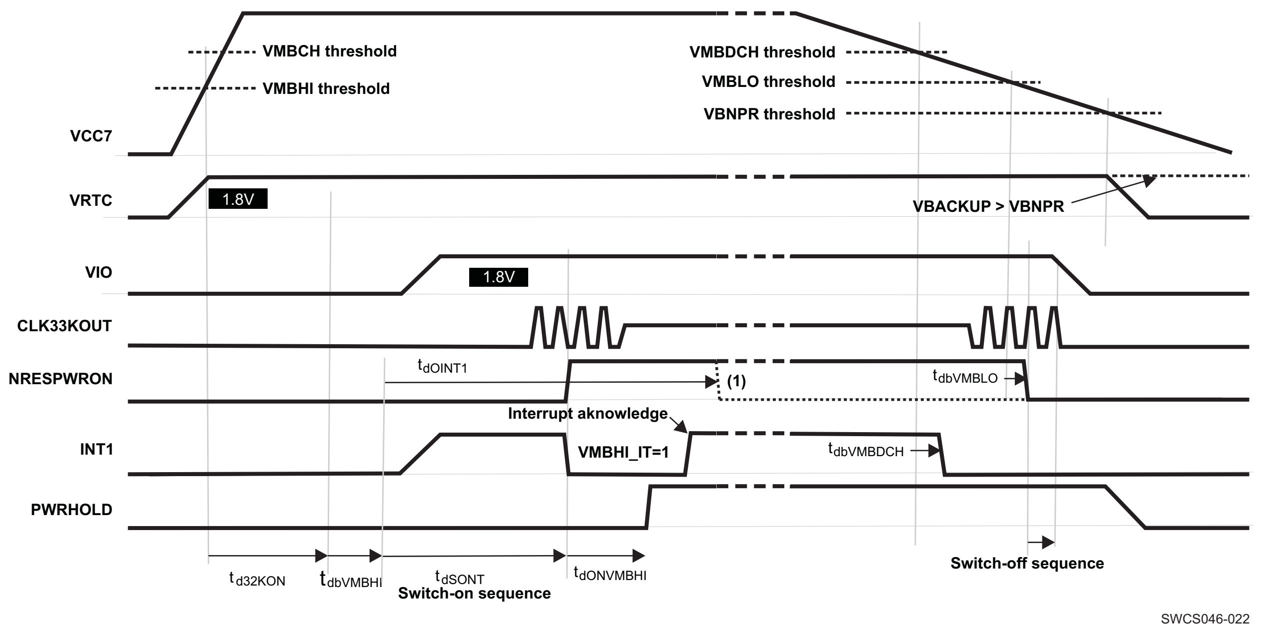
Registers default setting: CK32K_CTRL = 0 (32-kHz quartz or external bypass clock is used), RTC_PWDN = 1 (RTC domain off), IT_POL = 0 (INt2 interrupt flag active low), VMBHI_IT_MSK = 0 (automatic switch-on on battery plug), VMBCH_SEL = 11.

POWER CONTROL TIMING

Device Turn-On/Off With Rising/Falling Input Voltage

Figure 4 shows the device turn-on/-off with rising/falling input voltage.

POWER CONTROL TIMING (continued)

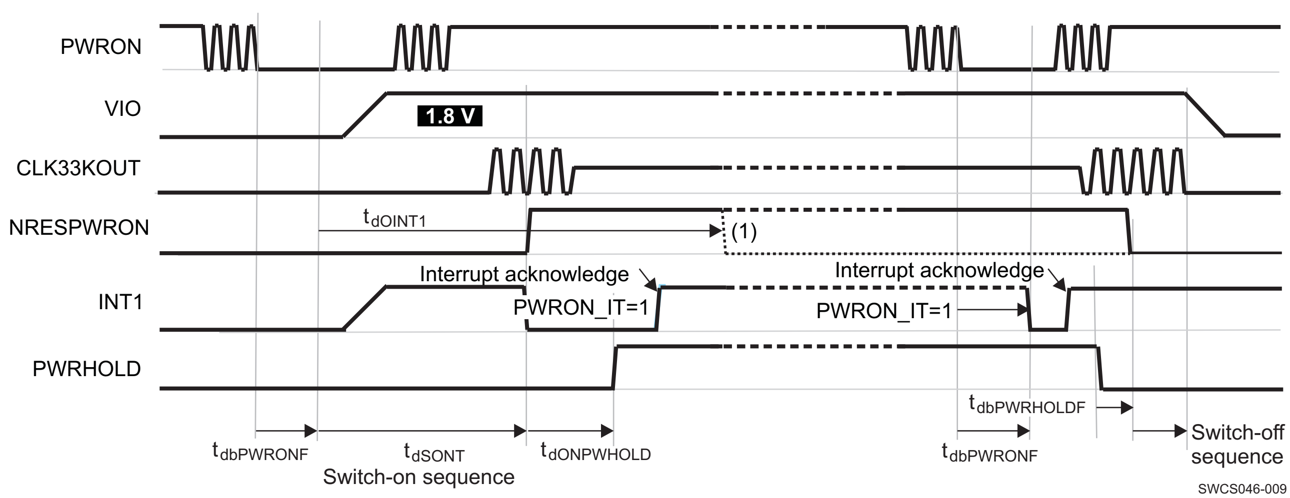


NOTE: (1) The DEV_ON control bit (set to 1) or the PWRHOLD signal (set high) can be used to maintain supplies on after the switch-on sequence. If none of these devce Power On enable conditions is set, the supplies will be turned off after t_{dOINT1} delay.

Figure 4. Device Turn-On/Off with Rising/Falling Input Voltage

Device State Control Through PWRON Signal

Figure 5 shows the device state control through PWRON signal.

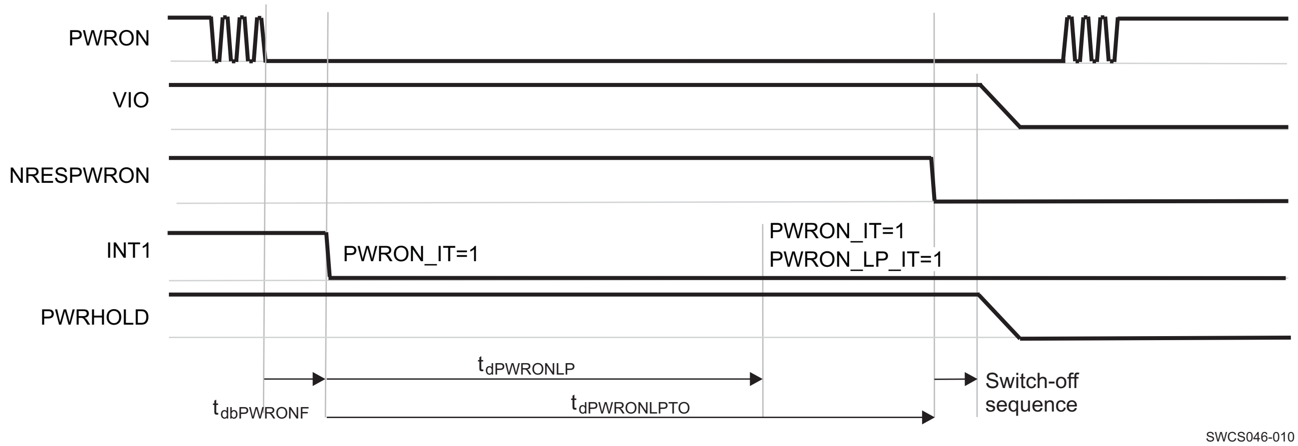


NOTE: (1) The DEV_ON control bit (set to 1) or the PWRHOLD signal (set high) can be used to maintain supplies on after switch-on sequence, If none of these device POWER ON enable condition is set the supplies will be turned off after T_{dOINT1} delay.

Figure 5. PWRON Turn-On/Turn-Off

Figure 6 shows the long-press turn-off timing characteristics.

POWER CONTROL TIMING (continued)



NOTE: If the DEV_ON control bit is set to 1 or PWRHOLD is kept high, the device will be turned on again after PWRON long press turn-off and PWRON released.

Figure 6. PWRON Long-Press Turn-Off

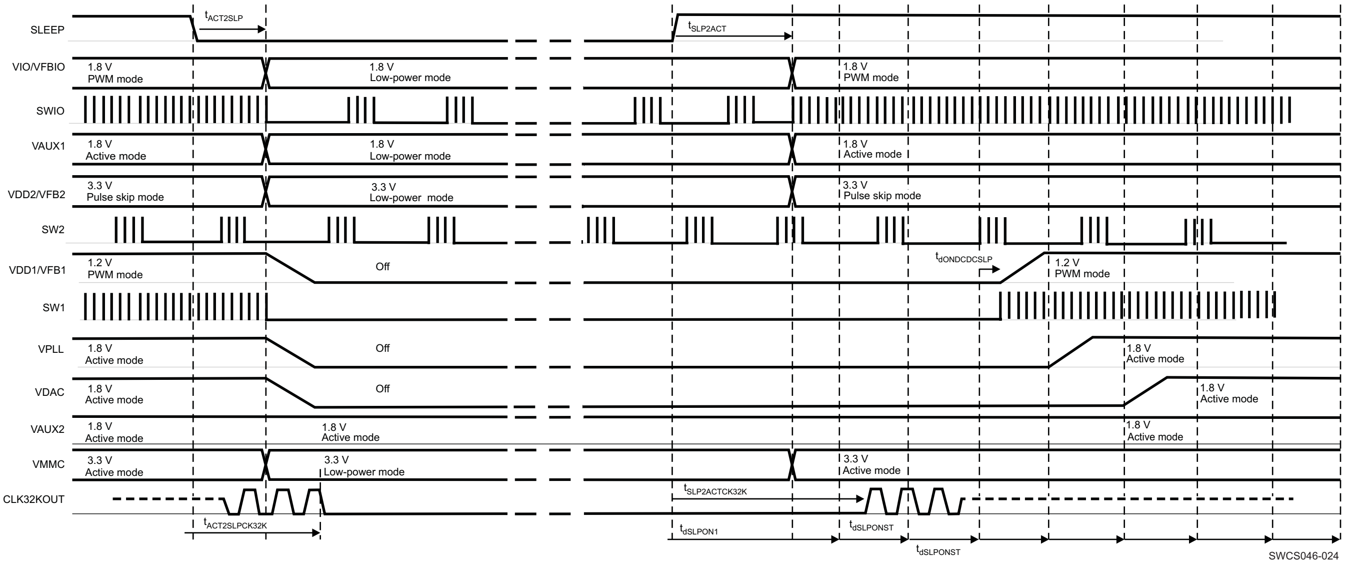
Table 6 lists the power control timing characteristics.

Table 6. Power Control Timing Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d32KON}: 32-kHz Oscillator turn-on time	BOOT[1:0] = 00, RC oscillator		0.1		ms
	BOOT[1:0] = 01, Quartz oscillator		400	2000	
	BOOT[1:0] = 01, Bypass clock		0.1		
$t_{dbVMBHI}$: VMBHI rising-edge debouncing delay		3 × t_{CK32k} = 94		4 × t_{CK32k} = 125	µs
$t_{dbVMBDCH}$: Main Battery voltage = VMBDCH threshold to INT1 falling-edge delay		3 × t_{CK32k} = 94		4 × t_{CK32k} = 125	s
$t_{dbVMBLO}$: Main Battery voltage = VMBLO threshold to NRESPWRON falling-edge delay		3 × t_{CK32k} = 94		4 × t_{CK32k} = 125	s
$t_{dbPWRONF}$: PWRON falling-edge debouncing delay		500		550	µs
$t_{dbPWRONR}$: PWRON rising-edge debouncing delay		3 × t_{CK32k}= 94		4 × t_{CK32k} = 125	µs
$t_{dbPWRHOLD}$: PWRON rising-edge debouncing delay		2 × t_{CK32k} = 63		3 × t_{CK32k}= 94	µs
t_{dOINT}: INT1 (internal) Power-on pulse duration after PWRON low-level (debounced) event			1		s
$t_{dONPWHOLD}$: delay to set high PWRHOLD signal or DEV_ON control bit after NRESPWRON released to keep on the supplies			984		ms
$t_{dPWRONLP}$: PWRON long-press delay to interrupt	PWRON falling edge to PWON_LP_IT = 1		6		s
$t_{dPWRONLPTO}$: PWRON long-press delay to turn-off	PWRON falling edge to NRESPWRON falling edge		8		s

Device SLEEP State Control

Figure 7 shows the device SLEEP state control timing characteristics.



NOTE: Registers programming: VIO_PSKIP = 0, VDD1_PSKIP = 0, VDD1_SETOFF = 1, VDAC_SETOFF = 1, VPLL_SETOFF = 1, VAUX2_KEEPON = 1

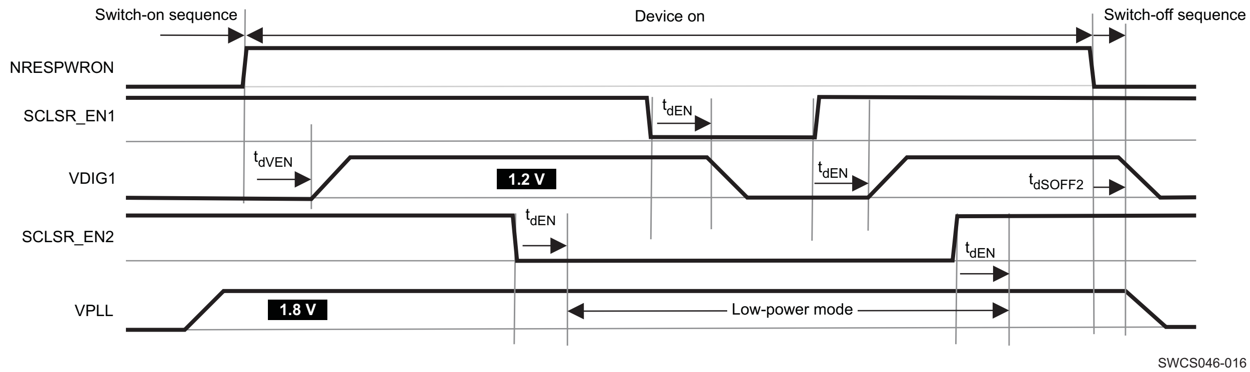
Figure 7. Device SLEEP State Control

Table 7. Device SLEEP State Control Timing Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{ACT2SLP}$	SLEEP falling edge to supply in low power mode (SLEEP resynchronization delay)	2 × t_{CK32k} = 62		3 × t_{CK32k} = 94	µs
$t_{ACT2SLP}$	SLEEP falling edge to CLK32KOUT low	156	$t_{ACT2SLP}$ + 3 × t_{CK32k}	188	µs
$t_{SLP2ACT}$	SLEEP rising edge to supply in high power mode	8 × t_{CK32k} = 250		9 × t_{CK32k} = 281	µs
$t_{SLP2ACTCK32K}$	SLEEP rising edge to CLK32KOUT running	344	$t_{SLP2ACT}$ + 3 × t_{CK32k}	375	µs
$t_{dSLPON1}$	SLEEP rising edge to time step 1 of the tun-on sequence from SLEEP state	281	$t_{SLP2ACT}$ + 1 × t_{CK32k}	312	µs
$t_{dSLPONST}$	turn-on sequence step duration, from SLEEP state				µs
	TSLOT_LENGTH[1:0] = 00		0		
	TSLOT_LENGTH[1:0] = 01		200		
	TSLOT_LENGTH[1:0] = 10		500		
	TSLOT_LENGTH[1:0] = 11		2000		
$t_{dSLPONDCDC}$	VDD1, VDD2 or VIO tun-on delay from tun-on sequence time step		2 × t_{CK32k} = 62		us

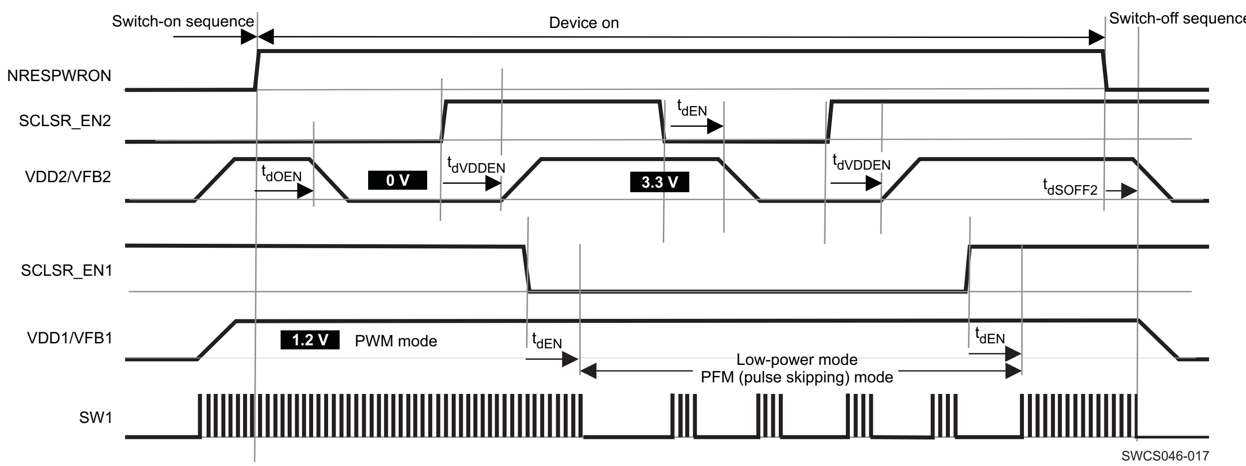
Power Supplies State Control Through the SCLSR_EN1 and SDASR_EN2 Signals

Figure 8 andFigure 9 show the power supplies state control through the SCLSR_EN1 and SDASR_EN2 signals timing characteristics.



NOTE: Register setting: VDIG1_EN1 = 1, VPLL_EN2 = 1, and VPLL_KEEPON = 1

Figure 8. LDO Type Supplies State Control Through SCLSR_EN1 and SCLSR_EN2



NOTE: Register setting: VDD2_EN2 = 1, VDD1_EN1 = 1, VDD1_KEEPON = 1, VDD1_PSKIP = 0, and SEL[6:0] = hex00 in VDD2_SR_REG

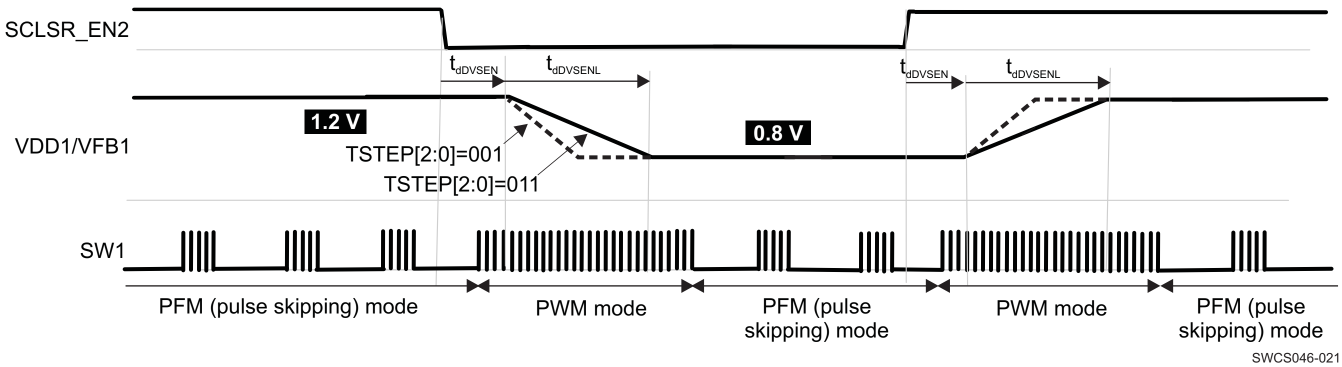
Figure 9. VDD1 and VDD2 Supplies State Control Through SCLSR_EN1 and SCLSR_EN2

Table 8. Supplies State Control Though SCLSR_EN1 and SCLSR_EN2 Timing Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{dEN}: NREPSWON to supply state change delay, SCLSR_EN1 or SCLSR_EN2 driven			0		ms
t_{dEN}: SCLSR_EN1 or SCLSR_EN2 edge to supply state change delay			$1 \times t_{CK32k} = 31$		µs
t_{dVDDEN}: SCLSR_EN1 or SCLSR_EN2 edge to VDD1 or VDD2 dc-dc turn on delay			$3 \times t_{CK32k} = 63$		µs

VDD1 and VDD2 Voltage Control Through SCLSR_EN1 and SDASR_EN2 Signals

Figure 10 shows the VDD1 and VDD2 voltage control through the SCLSR_EN1 and SDASR_EN2 signals timing characteristics.



NOTE: Register setting: VDD1_EN1 = 1, SEL[6:0] = hex13 in VDD1_SR_REG

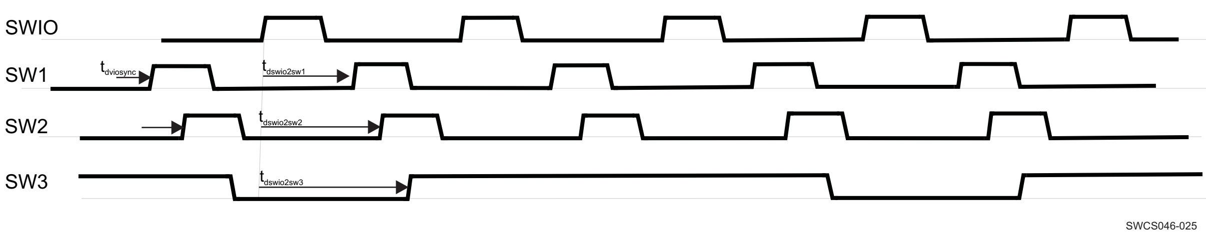
Figure 10. VDD1 Supply Voltage Control Though SCLSR_EN1

Table 9. VDD1 Supply Voltage Control Through SCLSR_EN1 Timing Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{dDVSEN}: SCLSR_EN1 or SCLSR_EN2 edge to VDD1 or VDD2 voltage change delay			$2 \times t_{CK32k} = 62$		µs
$t_{dDVSENL}$: VDD1 or VDD2 voltage settling delay	TSTEP[2:0] = 001 TSTEP[2:0] = 011 (default) TSTEP[2:0] = 111		32 0.4/7.5 = 53 160		µs

SMPS Switching Synchronization

Figure 11 shows the SMPS switching synchronization timing characteristics.



NOTE: VDD1 or VDD2 switching synchronization is available in PWM mode (VDD1_PSKIP = 0 or VDD2_PSKIP = 0). SMPS external clock (GPIO_CKSYNC) synchronization is available when VIO PWM mode is set (VIO_PSKIP = 0).

Figure 11. SMPS Switching Synchronization

Table 10. SMPS Switching Synchronization Timing Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{dSWIO2SW1}$: delay from SWIO rising edge to SW1 rising edge	VDD1_PSKIP = 0, DCDCCKSYNC[1:0] = 11 DCDCCKSYNC[1:0] = 01		 160 220		ns
$t_{dSWIO2SW2}$: delay from SWIO rising edge to SW1 rising edge	VDD2_PSKIP = 0, DCDCCKSYNC[1:0] = 11 DCDCCKSYNC[1:0] = 01		 160 290		ns
$t_{dSWIO2SW3}$: delay from SWIO rising edge to SW3 rising edge			206		ns

DEVICE INFORMATION

Table 11. Terminal Functions

NAME	QFN PIN	SUPPLIES	TYPE	I/O	DESCRIPTION	PU/PD
VDDIO		VDDIO/DGND	Power	I	Digital I/Os supply	No
SDA_SDI		VDDIO/DGND	Digital	I/O	I^2C bidirectional data signal/serial peripheral interface data input (multiplexed)	External PU
SCL_SCK		VDDIO/DGND	Digital	I/O	I^2C bidirectional clock signal/serial peripheral interface Clock Input (multiplexed)	External PU
SDASR_EN2		VDDIO/DGND	Digital	I/O	I^2C SmartReflex bidirectional data signal/enable of supplies (multiplexed)	External PU
SCLSR_EN1		VDDIO/DGND	Digital	I/O	I^2C SmartReflex bidirectional clock signal/enable of supplies (multiplexed)	External PU
SLEEP		VDDIO/DGND	Digital	I	Active-sleep state transition control signal	Programmable PD (default active)
GPIO_CKSYNC		VDDIO/DGND	Digital	I/O	Configurable general-purpose I/O or DC-DCs synchronization clock input signal	Programmable PD (default active)
PWRHOLD		VRTC/DGND	Digital	I	Switch-on/-off control signal	Programmable PD (default active)
PWRON		VBAT/DGND	Digital	I	External switch-on control (ON button)	Programmable PU (default active)
NRESPWRON		VDDIO/DGND	Digital	O	Power off reset	PD active during device OFF state
INT1		VDDIO/DGND	Digital	O	Interrupt flag	No
BOOT0		VRTC/DGND	Digital	I	Power-up sequence selection	Programmable PD (default active)
BOOT1		VRTC/DGND	Digital	I	Power-up sequence selection	Programmable PD (default active)
CLK32KOUT		VDDIO/DGND	Digital	O	32-kHz clock output	PD disable in ACTIVE or SLEEP state
OSC32KIN		VRTC/REFGND	Analog	I	32-kHz crystal oscillator	No
OSC32KOUT		VRTC/REFGND	Analog	I	32-kHz crystal oscillator	No
VREF		VCC7/REFGND	Analog	O	Bandgap voltage	No
REFGND		REFGND	Analog	I/O	Reference ground	No
TESTV		VCC7/AGND	Analog	O	Analog test output (DFT)	No
VBACKUP		VBACKUP/AGND	Power	I	Backup battery input (short to VCC5 if not used)	No
VCC1		VCC1/GND1	Power	I	VDD1 dc-dc power input	No
GND1		VCC1/GND1	Power	I/O	VDD1 dc-dc power ground	No
SW1		VCC1/GND1	Power	O	VDD1 dc-dc switched output	No
VFB1		VCC7/AGND	Analog	I	VDD1 feedback voltage	PD
VCC2		VCC2/GND2	Power	I	VDD2 dc-dc power input	No
GND2		VCC2/GND2	Power	I/O	VDD2 dc-dc power ground	No
SW2		VCC2/GND2	Power	O	VDD2 dc-dc switched output	No
VFB2		VCC4/AGND2	Analog	I	VDD2 dc-dc feedback voltage	PD
VCCIO		VCCIO/GNDIO	Power	I	VIO dc-dc power input	No
GNDIO		VCCIO/GNDIO	Power	I/O	VIO dc-dc power ground	No
SWIO		VCCIO/GNDIO	Power	O	VIO dc-dc switched output	No
VFBIO		VCC7/AGND	Analog	I	VIO feedback voltage	PD
VCC3		VCC3/AGND2	Power	I	VMMC VAUX33 power input	No
VMMC		VCC3/REFGND	Power	O	LDO regulator output	PD

Table 11. Terminal Functions (continued)

NAME	QFN PIN	SUPPLIES	TYPE	I/O	DESCRIPTION	PU/PD
VAUX33		VCC3/REFGND	Power	O	LDO regulator output, VDD3 internal regulated supply	PD
VCC4		VCC4/AGND2	Power	I	VAUX1, VAUX2 power input	No
VAUX1		VCC4/REFGND	Power	O	LDO regulator output	PD
VAUX2		VCC4/REFGND	Power	O	LDO regulator output	PD
VCC5		VCC5/AGND	Power	I	VDAC, VPLL power input	No
VDAC		VCC5/REFGND	Power	O	LDO regulator output	PD
VPLL		VCC5/REFGND	Power	O	LDO regulator output	PD
VRTC		VCC7/REFGND	Power	O	LDO regulator output	PD
VCC6		VCC6/AGND2	Power	I	VDIG1, VDIG2 power input	No
VDIG1		VCC6/REFGND	Power	O	LDO regulator output	No
VDIG2		VCC6/REFGND	Power	O	LDO regulator output	No
VCC7		VCC7/REFGND	Power	I	VRTC power input, VDD3 internal and analog references supply	No
VFB3		VCC7/AGND	Analog	I	VDD3 feedback voltage	No
SW3		VCC7/GND3	Power	O	VDD3 dc-dc switched output	No
GND3	Power PAD	AGND	Power	I/O	VDD3 dc-dc power ground	No
AGND	Power PAD	AGND	Power	I/O	Analog ground	No
AGND2	Power PAD	AGND	Power	I/O	Analog ground	No
DGND	Power PAD	DGND	Power	I/O	Digital ground	No

PIN ASSIGNMENT (TOP VIEW)

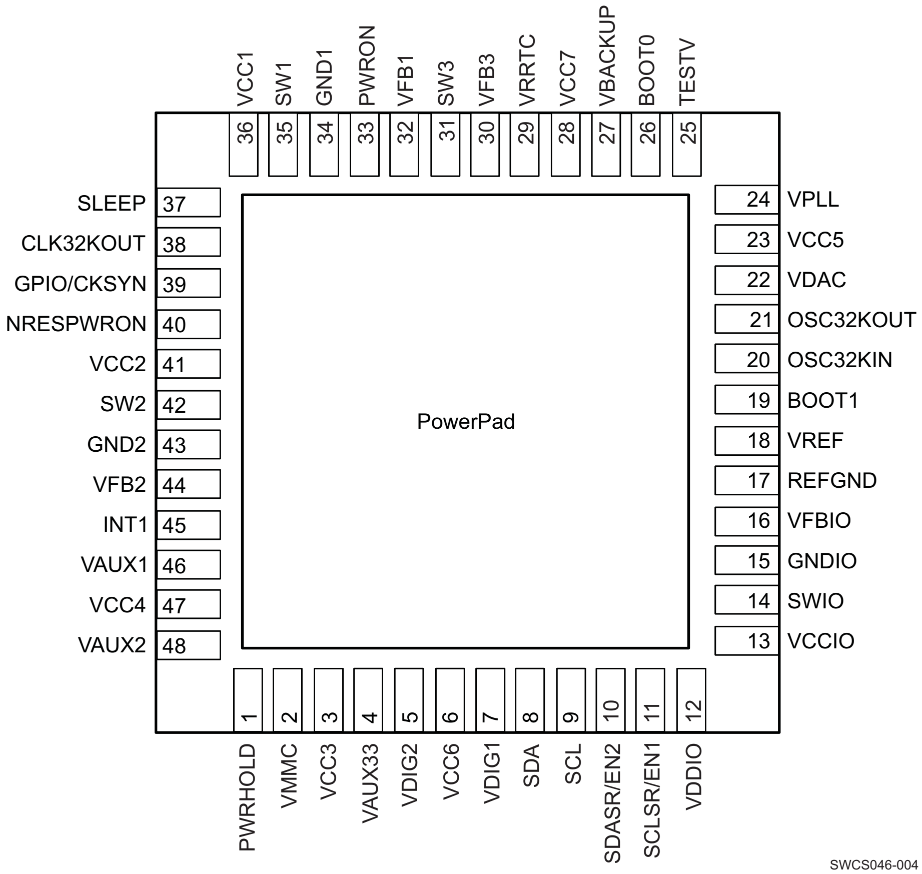


Figure 12. 48-QFN Top View Pin Assignment

DETAILED DESCRIPTION

POWER REFERENCE

The bandgap voltage reference is filtered by using an external capacitor connected across the VREF output and the analog ground REFGND (see RECOMMENDED OPERATING CONDITIONS, Recommended Operating Conditions). The VREF voltage is distributed and buffered inside the device.

POWER SOURCES

The power resources provided by the TPS65910 device include inductor-based switched mode power supplies (SMPS) and linear low drop-out voltage regulators (LDOs). These supply resources provide the required power to the external processor cores and external components, and to modules embedded in the TPS65910 device.

Two of these SMPS have DVS capability SmartReflex Class 3 compatible. These SMPS provide independent core voltage domains to the host processor. The remaining SMPS provides supply voltage for the host processor I/Os.

Table 12 lists the power sources provided by the TPS65910 device.

Table 12. Power Sources

RESOURCE	TYPE	VOLTAGES	POWER
VIO	SMPS	1.5 V / 1.8 V / 2.5 V / 3.3 V	1000 mA
VDD1	SMPS	0.6 ... 1.5 in 12.5-mV steps Programmable multiplication factor: x2, x3	1500 mA
VDD2	SMPS	0.6 ... 1.5 in 12.5-mV steps Programmable multiplication factor: x2, x3	1500 mA
VDD3	SMPS	5 V	100 mA
VDIG1	LDO	1.2 V, 1.5 V, 1.8 V, 2.7 V	300 mA
VDIG2	LDO	1 V, 1.1 V, 1.2 V, 1.8 V	300 mA
VPLL	LDO	1.0 V, 1.1 V, 1.8 V, 2.5 V	50 mA
VDAC	LDO	1.8 V, 2.6 V, 2.8 V, 2.85 V	150 mA
VAUX1	LDO	1.8 V, 2.5 V, 2.8 V, 2.85 V	300 mA
VAUX2	LDO	1.8 V, 2.8 V, 2.9 V, 3.3 V	150 mA
VAUX33	LDO	1.8 V, 2.0 V, 2.8 V, 3.3 V	150 mA
VMMC	LDO	1.8 V, 2.8 V, 3.0 V, 3.3 V	300 mA

EMBEDED POWER CONTROLLER

The embedded power controller manages the state of the device and controls the power-up sequence.

STATE-MACHINE

The EPC supports the following states:

No supply: The main battery supply voltage is not high enough to power the VRTC regulator. A global reset is asserted in this case. Everything on the device is off.

Backup: The main battery supply voltage is high enough to enable the VRTC domain but not enough to switch on all the resources. In this state, the VRTC regulator is in backup mode and only the 32-K oscillator and RTC module are operating (if enabled). All other resources are off or under reset.

Off: The main battery supply voltage is high enough to start the power-up sequence but device power on is not enabled. All power supplies are in OFF state except VRTC.

Active: Device power-on enable conditions are met and regulated power supplies are on or can be enabled with full current capability.

Sleep: Device SLEEP enable conditions are met and some selected regulated power supplies are in low-power mode.

Figure 13 shows the transitions of the state-machine.

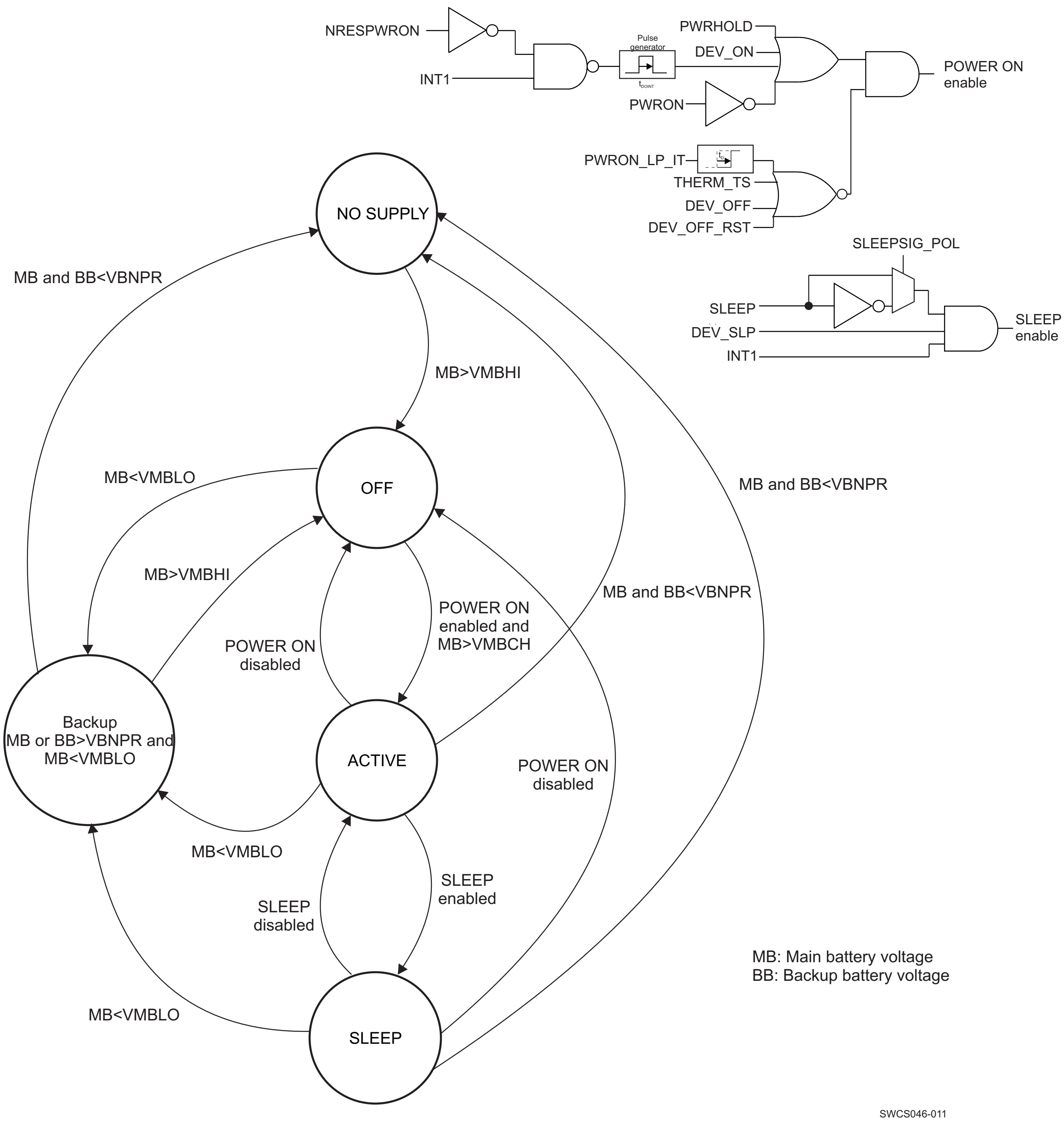


Figure 13. Embebded Power Control State-Machine

Device power-on enable conditions:

If none of the device power-on disable conditions is met, the following conditions are available to turn on and/or maintain the ON state of the device:

- PWRON signal low level.
- Or PWRHOLD signal high level.
- Or DEV_ON control bit set to 1 (default inactive).

- Or interrupt flag active (default INT1 low) while the device is off (NRESPWRON = 0) generates a power-on enable condition during a fixed delay (T_{DOINT1} pulse duration defined in POWER CONTROL TIMING, Power Control Timing).

  The power-on enable condition pulse occurs only if the interrupt status bit is initially low (no previous identical interrupt pending in the status register).

  The Interrupt sources expected when the device is off are:
  - PWRON low-level interrupt (PWRON_IT = 1 in INT_STS_REG register)
  - PWRHOLD rising-edge interrupt (PWRHOLD_IT = 1 in INT_STS_REG register)

  The Interrupt sources expected if enabled when the device is off are:
  - RTC Alarm interrupt (RTC_ALARM_IT = 1 or RTC_PERIOD_IT = 1 in INT_STS_REG register)
  - First-time input voltage rising above VMBHI threshold (Boot mode or EEPROM dependent) and input voltage > VMBCH threshold (VMBCH_IT = 1 in INT_STS_REG register).

GPIO_CKSYNC cannot be used to turn on the device (OFF-to-ACTIVE state transition), even if its associated interrupt is not masked, but can be used as an interrupt source to wake up the device from SLEEP-to-ACTIVE state.

Device power-on disable conditions:

- PWRON signal low level during more than the long-press delay: $t_{dPWRONLP}$ (can be disabled though register programming). The interrupt corresponding to this condtion is PWRON_LP_IT in the INT_STS_REG register.
- Or Die temperature has reached the thermal shutdown threshold.
- Or DEV_OFF or DEV_OFF_RST control bit set to 1 (value of DEV_OFF is cleared when the device is in OFF state).

Device SLEEP enable conditions:

- SLEEP signal low level (default, or high level depending on the programmed polarity)
- And DEV_SLP control bit set to 1
- And interrupt flag inactive (default INT1 high): no nonmasked interrupt pending

SLEEP state can be controlled by programming DEV_SLP and keeping the SLEEP signal floating, or it can be controlled through the SLEEP signal setting DEV_SLP = 1 once after device turn-on .

SWITCH-ON/-OFF SEQUENCES

The power sequence is the automated switching on of the device resources when an off-to-active transition takes place.

The device supports three embedded power sequences selectable by the device BOOT pins.

BOOT0	BOOT1	Processor Supported
0	0	AM3517, AM3505
1	0	OMAP3 Family, AM3715/03, DM3730/25
0	1	EEPROM sequence

Details of the boot sequence timing are given in SWITCH-ON/-OFF SEQUENCES AND TIMING. EEPROM sequences can be used for specific power up sequence for corresponding application processor. For details of EEPROM sequence refer to the user guides on the product folder: http://focus.ti.com/docs/prod/folders/print/tps65910.html.

CONTROL SIGNALS

SLEEP

When none of the device sleep-disable conditions are met, a falling edge (default, or rising edge, depending on the programmed polarity) of this signal causes an ACTIVE-to-SLEEP state transition of the device. A rising edge (default, or falling edge, depending on the programmed polarity) causes a transition back to ACTIVE state. This input signal is level sensitive and no debouncing is applied.

While the device is in SLEEP state, predefined resources are automatically set in their low-power mode or off.

Resources can be kept in their active mode: (full-load capability), programming the SLEEP_KEEP_LDO_ON and the SLEEP_KEEP_RES_ON registers. These registers contain 1 bit per power resource. If the bit is set to 1, then that resource stays in active mode when the device is in SLEEP state. 32KCLKOUT is also included in the SLEEP_KEEP_RES_ON register and the 32-kHz clock output is maintained in SLEEP state if the corresponding mask bit is set.

PWRHOLD

When none of the device power-on disable conditions are met, a rising edge of this signal causes an OFF-to-ACTIVE state transition of the device and a falling edge causes a transition back to OFF state. Typically, this signal is used to control the device in a slave configuration. It can be connected to the SYSEN output signal from other TPS659xx devices, or the NRESPWRON signal of another TPS65910 device. This input signal is level sensitive and no debouncing is applied.

A rising edge of PWRHOLD is highlighted though an associated interrupt.

BOOT0/BOOT1

These signals determine which processor the device is working with and hence which power-up sequence is needed. See SWITCH-ON/-OFF SEQUENCES AND TIMING for more details. There is no debouncing on this input signal.

NRESPWRON

This signal is used as the reset to the processor. It is held low until the ACTIVE state is reached. See POWER CONTROL TIMING to get detailed timing.

CLK32KOUT

This signal is the output of the 32K oscillator, which can be enabled or not during the power-on sequence, depending on the Boot mode. It can be enabled and disabled by register bit, during ACTIVE state of the device. CLK32KOUT output can also be enabled or not during SLEEP state of the device depending on the SLEEPMASK register programming.

PWRON

A falling edge on this signal causes after $t_{dbPWRONF}$ debouncing delay (defined in Figure 5 and Table 6) an OFF-to-ACTIVE state or SLEEP-to-ACTIVE state transition of the device and makes the corresponding interrupt (PWRON_IT) active. The PWRON input is connected to an external push-button. The built-in debouncing time defines a minimum button press duration that is required for button press detection. Any button press duration which is lower than this value is ignored, considered an accidental touch.

After an OFF-to-ACTIVE state transition, the PMIC maintains ACTIVE during t_{dOINT} delay, if the button is released. After this delay if none of the device enabling conditions is set by the processor supplied, the PMIC automatically turns off. If the button is not released, the PMIC maintains ACTIVE up to $t_{dPWRONLPTO}$, because PWRON low is a device enabling condition. After a SLEEP-to-ACTIVE state transition, the PMIC maintains ACTIVE as long as an interrupt is pending.

If the device is already in ACTIVE state, a PWRON low level makes the corresponding interrupt (PWRON_IT) active.

When the PMIC is in ACTIVE mode, if the button is pressed for longer time than $t_{dPWRONLP}$, the PMIC generates the PWON_LP_IT interrupt. If the processor does not acknowledge the long press interrupt within a period of $t_{dPWRONLPTO} - t_{dPWRONLP}$, the PMIC goes to OFF mode and shuts down the DCDCs and LDOs.

INT1

INT1 signal (default active low) warns the host processor of any event that occurred on the TPS65910 device. The host processor can then poll the interrupt from the interrupt status register through I^2C to identify the interrupt source. A low level (default setting) indicates an active interrupt, highlighted in the INT_STS_REG register. The polarity of INT1 can be set by programming the IT_POL control bit.

Any (not masked or masked) interrupt detection causes a POWER ON enable condition during a fixed delay t_{DOINT1} (only) when the device is in OFF state (when NRESPWON signal is low). Any (not masked) interrupt detection is causing a device wakeup from SLEEP state up to acknowledge of the pending interrupt. Any of the interrupt sources can be masked by programming the INT_MSK_REG register. When an interrupt is masked, its corresponding interrupt status bit is still updated, but the INT1 flag is not activated.

Interrupt source masking can be used to mask a device switch-on event. Because interrupt flag active is a POWER ON enable condition during t_{DOINT1} delay, any interrupt not masked must be cleared to allow turn off of the device after the t_{DOINT1} POWER ON enable pulse duration.. See section: Interrupts, for interrupt sources definition.

SDASR_EN2 and SCLSR_EN1

SDASR_EN2 and SCLSR_EN1 are the data and clock signals of the serial control interface (SR-I^{2}C) dedicated to SmartReflex applications. These signals can also be programmed to be used as enable signals of one or several supplies, when the device is on (NRESPWRON high). A resource assigned to SDASR_EN2 or SCLSR_EN1 control automatically disables the serial control interface.

Programming EN1_LDO_ASS_REG, EN2_LDO_REG, and SLEEP_KEEP_LDO_ON_REG registers: SCLSR_EN1 and SDASR_EN2 signals can be used to control the turn on/off or sleep state of any LDO type supplies.

Programming EN1_SMPS_ASS_REG, EN2_SMPS_ASS_REG, and SLEEP_KEEP_RES_ON registers: SCLSR_EN1 and SDASR_EN2 signals can be used to control the turn on/off or low-power state (PFM mode) of SMPS type supplies.

SDASR_EN2 and SCLSR_EN1 can be used to set output voltage of VDD1 and VDD2 SMPS from a roof to a floor value, preprogrammed in the VDD1_OP_REG, VDD2_OP_REG, and teh VDD1_SR_REG, VDD2_SR_REG registers. Tun-off of VDD1 and VDD2 can also be programmed either in VDD1_OP_REG, VDD2_OP_REG or in VDD1_SR_REG, VDD2_SR_REG registers.

When a supply is controlled through SCLSR_EN1 or SCLSR_EN2 signals, its state is no longer driven by the device SLEEP state.

GPIO_CKSYNC

GPIO_CKSYNC is a configurable open-drain digital I/O: directivity, debouncing delay and internal pullup can be programmed in the GPIO0_REG register. GPIO_CKSYNC cannot be used to turn on the device (OFF-to-ACTIVE state transition), even if its associated interrupt is not masked, but can be used as an interrupt source to wake up the device from SLEEP-to-ACTIVE state.

Programming DCDCCKEXT = 1, VDD1, VDD2, VIO, and VDD3 dc-dc switching can be synchronized using a 3-MHz clock set though the GPIO_CKSYNC pin.

DYNAMIC VOLTAGE FREQUENCY SCALING AND ADAPTIVE VOLTAGE SCALING OPERATION

Dynamic voltage frequency scaling (DVFS) operation: a supply voltage value corresponding to a targeted frequency of the digital core supplied is programmed in VDD1_OP_REG or VDD2_OP_REG registers.

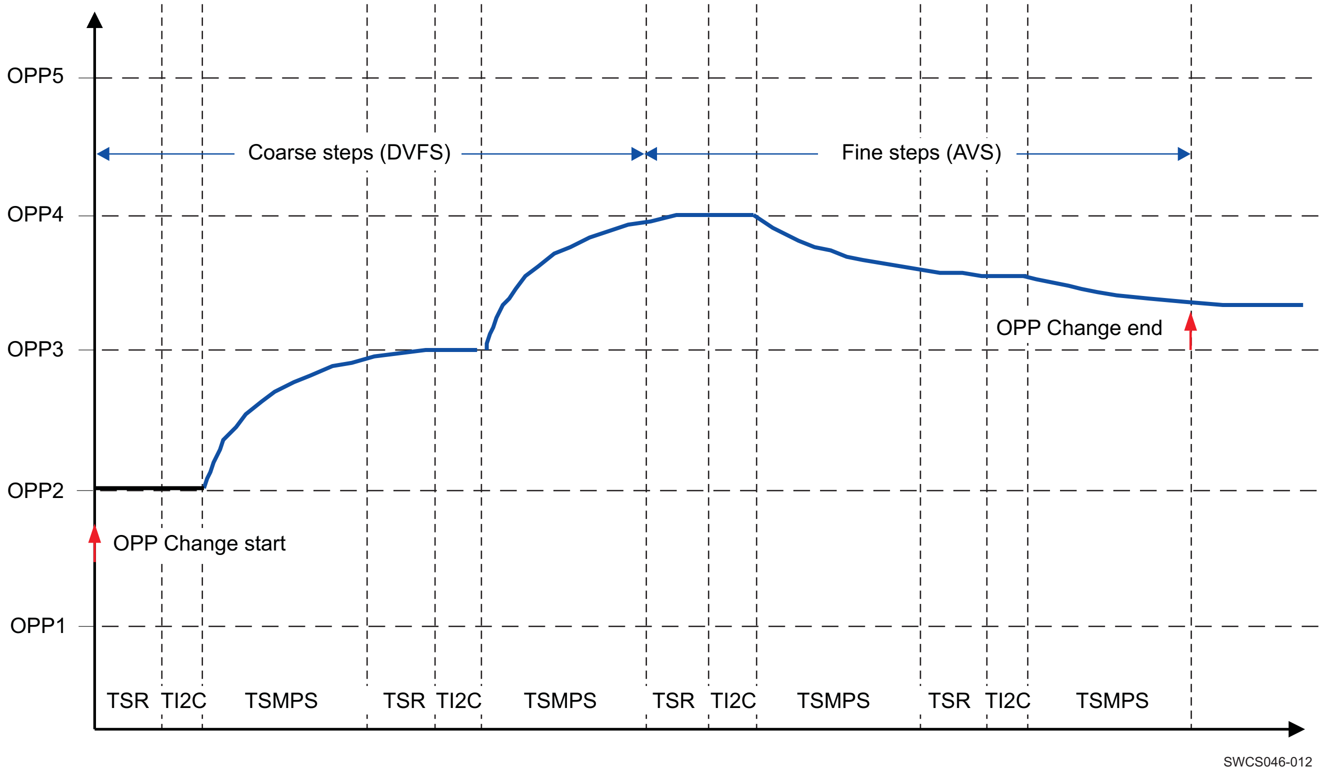
The slew rate of the voltage supply reaching a new VDD1_OP_REG or VDD2_OP_REG programmed value is limited to 12.5 mV/μs, fixed value. Adaptative voltage scaling (AVS) operation: a supply voltage value corresponding to a supply voltage adjustment is programmed in VDD1_SR_REG or VDD2_SR_REG registers. The supply voltage is then intended to be tuned by the digital core supplied, based its performance self-evaluation. The slew rate of VDD1 or VDD2 voltage supply reaching a new programmed value is programmable though the VDD1_REG or VDD2_REG register, respectively.

A serial control interface (SR-I^{2}C) is dedicated to SmartReflex applications such as DVFS and class 3 AVS, and thus gives access to the VDD1_OP_REG, VDD1_SR_REG, and VDD2_OP_REG, VDD2_SR_REG register.

A general-purpose serial control interface (CTL-I^{2}C) also gives access to these registers, if SR_CTL_I2C_SEL control bit is set to 1 in the DEVCTRL_REG register (default inactive).

Both control interfaces are compliant with HS-I^{2}C specification (100 kbps, 400 kbps, or 3.4 Mbps).

Figure 14 shows an example of a SmartReflex operation. To optimize power efficiency, the voltage domains of the host processor uses the DVFS and AVS features provided by SmartReflex.



(1) T_{SR}: Time used by the SmartReflex controller

(2) T_{I2C}: Time used for data transfer through the I^2C interface

(3) T_{SMPS}: Time required by the SMPS to converge to new voltage value

Figure 14. SmartReflex Operation Example

32-kHz RTC CLOCK

The TPS65910 device can provide a 32-kHz clock to the platform through the CLK32KOUT output, the source of this 32-kHz clock can be:

- 32-kHz crystal connected from OSC32IN to OSC32KOUT pins
- A square-wave 32-kHz clock signal applied to OSC32IN input (OSC32KOUT kept floating).
- Internal 32-kHz RC oscillator, to reduce the BOM, if an accurate clock is not needed by the system.

Default selection of a 32-kHz RC oscillator versus 32-kHz crystal oscillator or external square-wave 32-kHz clock depends on the Boot mode or device version (EEPROM programming):

- BOOT1 = 0, BOOT0 = 1: quartz oscillator or external square wave 32-kHz clock default
- BOOT1 = 0, BOOT0 = 0: 32-kHz RC oscillator default

Switching from the 32-kHz RC oscillator to the 32-kHz crystal oscillator or external square-wave 32-kHz clock can also be programmed though DEVCTRL_REG register, taking benefit of the shorter turn-on time of the internal RC oscillator.

Switching from the 32-kHz crystal oscillator or external square-wave clock to the RC oscillator is not supported.

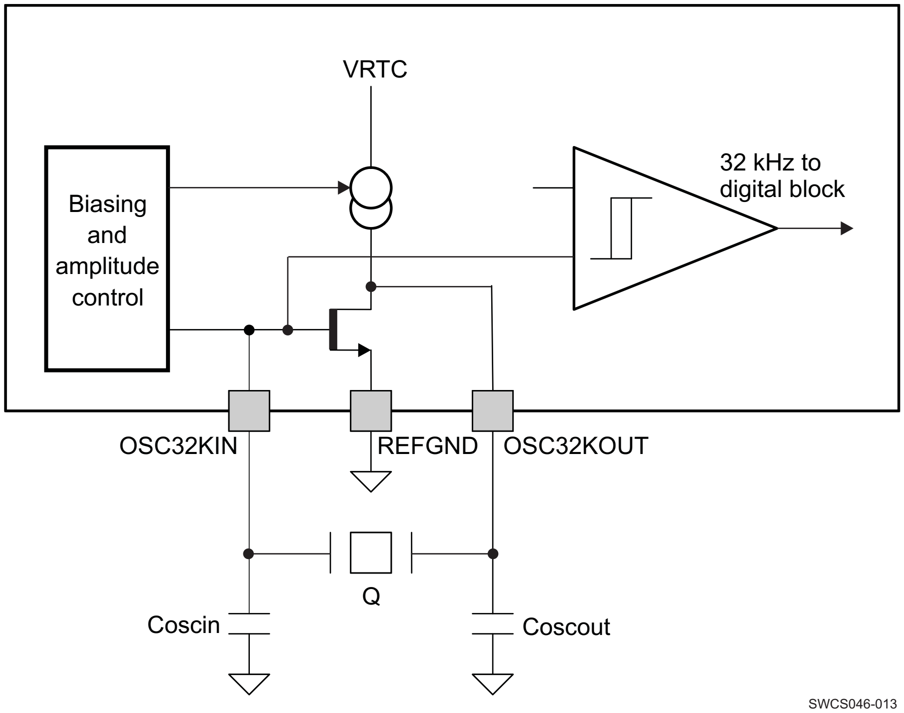


Figure 15. Crystal Oscillator 32-kHz Clock

RTC

The RTC, which is driven by the 32-kHz clock, provides the alarm and timekeeping functions. The RTC is kept supplied when the device is in the OFF or the BACKUP state.

The main functionalities of the RTC block are:

- Time information (seconds/minutes/hours) directly in binary-coded decimal (BCD) format
- Calendar information (Day/Month/Year/Day of the week) directly in BCD code up to year 2099
- Programmable interrupts generation: The RTC can generate two interrupts: a timer interrupt RTC_PERIOD_IT periodically (1s/1m/1h/1d period) and an alarm interrupt RTC_ALARM_IT at a precise time of the day (alarm function). These interrupts are enabled using IT_ALARM and IT_TIMER control bits. Periodically interrupts can be masked during the SLEEP period to avoid host interruption and are automatically unmasked after SLEEP wakeup (using the IT_SLEEP_MASK_EN control bit).
- Oscillator frequency calibration and time correction

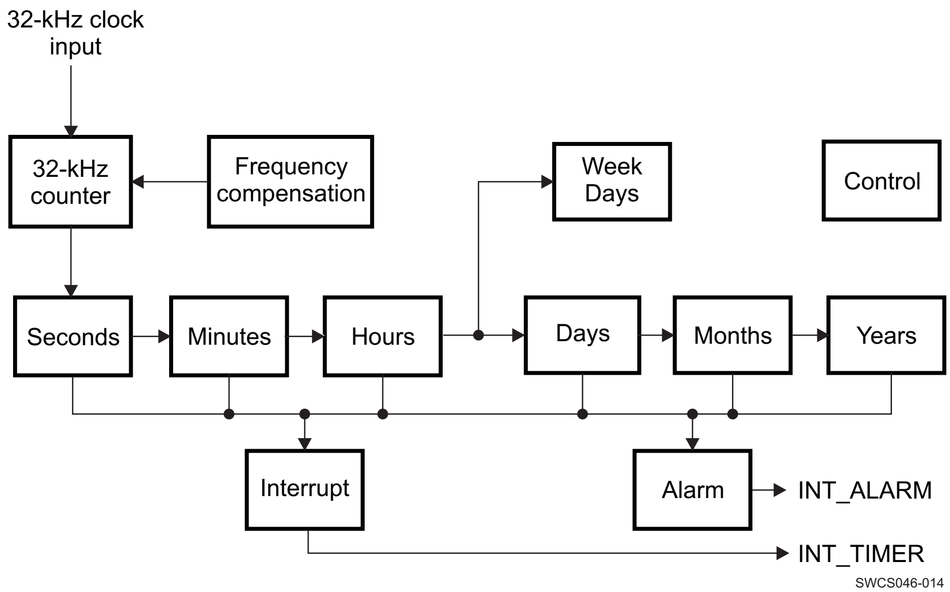


Figure 16. RTC Digital Section Block Diagram

NOTE

INT_ALARM can generate a wakeup of the platform.

INT_TIMER cannot generate a wakeup of the platform.

TIME CALENDAR REGISTERS

All the time and calendar information are available in these dedicated registers, called TC registers. Values of the TC registers are written in BCD format.

1. Year data ranges from 00 to 99
   - Leap year = Year divisible by four (2000, 2004, 2008, 2012...)
   - Common year = other years
2. Month data ranges from 01 to 12
3. Day value ranges from:
   - 1 to 31 when months are 1, 3, 5, 7, 8, 10, 12
   - 1 to 30 when months are 4, 6, 9, 11
   - 1 to 29 when month is 2 and year is a leap year
   - 1 to 28 when month is 2 and year is a common year
4. Week value ranges from 0 to 6
5. Hour value ranges from 00 to 23 in 24-hour mode and ranges from 1 to 12 in AM/PM mode
6. Minutes value ranges from 0 to 59
7. Seconds value ranges from 0 to 59

To modify the current time, software writes the new time into TC registers to fix the time/calendar information. The DBB can write into TC registers without stopping the RTC. In addition, software can stop the RTC by clearing the STOP_RTC bit of the control register and check the RUN bit of the status to be sure that the RTC is frozen. Then update TC values, and then restart the RTC by setting the STOP_RTC bit.

Example: Time is 10H54M36S PM (PM_AM mode set), 2008 September 5, previous register values are:

Register	Value
SECONDS_REG	0x36
MINUTES_REG	0x54
HOURS_REG	0x90
DAYS_REG	0x05
MONTHS_REG	0x09
YEARS_REG	0x08

The user can round to the closest minute, by setting the ROUND_30S register bit. TC values are set to the closest minute value at the next second. The ROUND_30S bit is automatically cleared when the rounding time is performed.

Example:

- If current time is 10H59M45S, a round operation changes time to 11H00M00S.
- if current time is 10H59M29S, a round operation changes time to 10H59M00S.

GENERAL REGISTERS

Software can access the RTC_STATUS_REG and RTC_CTRL_REG registers at any time (except for the RTC_CTRL_REG[5] bit, which must be changed only when the RTC is stopped).

COMPENSATION REGISTERS

The RTC_COMP_MSB_REG and RTC_COMP_LSB_REG registers must respect the available access period. These registers must be updated before each compensation process. For example, software can load the compensation value into these registers after each hour event, during an available access period.

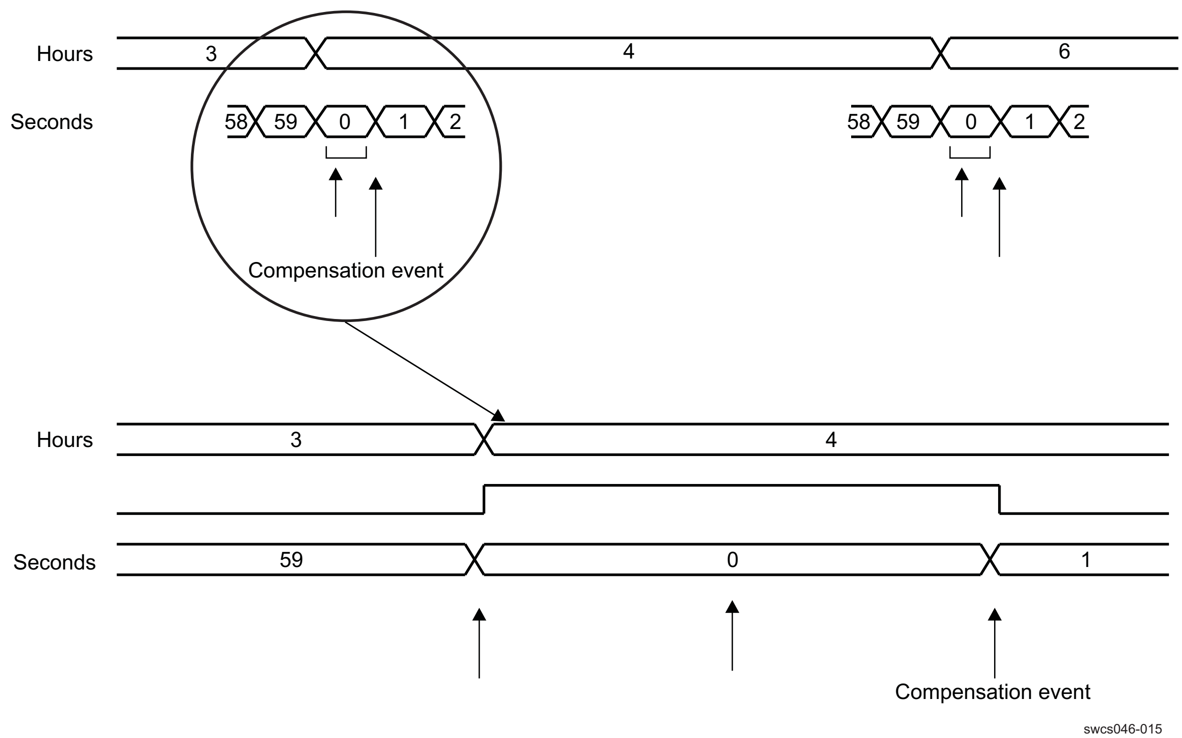


Figure 17. RTC Compensation Scheduling

This drift can be balanced to compensate for any inaccuracy of the 32-kHz oscillator. Software must calibrate the oscillator frequency, calculate the drift compensation versus one time hour period; and then load the compensation registers with the drift compensation value. Indeed, if the AUTO_COMP_EN bit in the RTC_CTRL_REG is enabled, the value of COMP_REG (in twos-complement) is added to the RTC 32-kHz counter at each hour and one second. When COMP_REG is added to the RTC 32-kHz counter, the duration of the current second becomes (32768 - COMP_REG)/32768s; so, the RTC can be compensated with a 1/32768 s/hour time unit accuracy.

NOTE

The compensation is considered once written into the registers.

BACKUP BATTERY MANAGEMENT

The device includes a back-up battery switch connecting the VRTC regulator input to a main battery (VCC7) or to a back-up battery (VBACKUP), depending on the batteries voltage value.

The VRTC supply can then be maintained during a BACKUP state as far as the input voltage is high enough (>VBNPR threshold). Below the VBNPR voltage threshold the digital core of the device is set under reset by internal signal POR (PowerOnReset).

The back-up domain functions which are always supplied from VRTC comprehend:

- The internal 32-kHz oscillator
- Backup registers

The back-up battery can be charged from the main battery through an embedded charger. The back-up battery charge voltage and enable is controlled through BBCH_REG register programming. This register content is maintained during the device Backup state.

Hence enabled the back-up battery charge is maintained as far as the main battery voltage is higher than the VMBLO threshold and the back-up battery voltage.

BACKUP REGISTERS

As part of the RTC the device contains five 8-bit registers which can be used for storage by the application firmware when the external host is powered down. These registers retain their content as long as the VRTC is active.

I^{2}C INTERFACE

A general-purpose serial control interface (CTL-I^{2}C) allows read and write access to the configuration registers of all resources of the system.

A second serial control interface (SR-I^{2}C) is dedicated to SmartReflex applications such as DVFS or AVS.

Both control interfaces are compliant with HS-I^{2}C specification.

These interfaces support the standard slave mode (100 Kbps), Fast mode (400 Kbps), and high-speed mode (3.4 Mbps). The general-purpose I^{2}C module using one slave hard-coded addresse (ID1 = 2Dh). The SmartReflex I^{2}C module uses one slave hard-coded address (ID0 = 12h). The master mode is not supported.

Addressing: Seven-bit mode addressing device

They do not support the following features:

- 10-bit addressing
- General call

THERMAL MONITORING AND SHUTDOWN

A thermal protection module monitors the junction temperature of the device versus two thesholds:

- Hot-die temperature threshold
- Thermal shutdown temperature theshold

When the hot-die temperature threshold is reached an interrupt is sent to software to close the noncritical running tasks.

When the thermal shutdown temperature theshold is reached, the TPS65910 device is set under reset and a transition to OFF state is initiated. Then the power-on enable conditions of the device is not considered until the die temperature has decreased below the hot-die threshold. An hysteresis is applied to the hot-die and shutdown threshold, when detecting a falling edge of temperature, and both detection are debounced to avoid any parasitic detection. The TPS65910 device allows programming of four hot-die temperature thresholds to increase the flexibility of the system.

By default, the thermal protection is enabled in ACTIVE state, but can be disabled through programming register THERM_REG. The thermal protection can be enabled in SLEEP state programming register SLEEP_KEEP_RES_ON. The thermal protection is automatically enabled during an OFF-to-ACTIVE state transition and is kept enabled in OFF state after a switch-off sequence caused by a thermal shutdown event. Transition to OFF state sequence caused by a thermal shutdown event is highlighted in the INT_STS_REG status register. Recovery from this OFF state is initiated (switch-on sequence) when the die temperature falls below the hot-die temperature threshold.

Hot-die and thermal shutdown temperature threshold detections state can be monitored or masked by reading or programming the THERM_REG register. Hot-die interrupt can be masked by programming the INT_MSK_REG register.

INTERRUPTS

Table 13. Interrupt Sources

Interrupt	Description
RTC_ALARM_IT	RTC alarm event: Occurs at programmed determinate date and time (running in ACTIVE, OFF, and SLEEP state, default inactive)
RTC_PERIOD_IT	RTC periodic event: Occurs at programmed regular period of time (every second or minute) (running in ACTIVE, OFF, and SLEEP state, default inactive)
HOT_DIE_IT	The embedded thermal monitoring module has detected a die temperature above the hot-die detection threshold (running in ACTIVE and SLEEP state)
	Level sensitive interrupt.
PWRHOLD_IT	PWRHOLD signal rising edge
PWRON_LP_IT	PWRON is low during more than the long-press delay: $t_{dPWRONLP}$ (can be disable though register programming).
PWRON_IT	PWRON is low while the device is on (running in ACTIVE and SLEEP state) or PWON was low while the device was off (causing a device turn-on). Level-sensitive interrupt
VMBHI_IT	The battery voltage rise above the VMBHI threshold: NOSUPPLY to Off or Backup-to-Off device states transition (first battery plug or battery voltage bounce detection). This interrupt source can be disabled through EEPROM programming (VMBHI_IT_DIS). Edge-sensitive interrupt
VMBDCH_IT	The battery voltage falls down below the VMBDCH threshold(running in ACTIVE and SLEEP state, if enabled programming VMBCH_VSEL). Edge-sensitive interrupt
GPIO0_R_IT	GPIO_CKSYNC rising-edge detection (available in ACTIVE and SLEEP state)
GPIO0_F_IT	GPIO_CKSYNC falling-edge detection (available in ACTIVE and SLEEP state)

INT1 signal (active low) warns the host processor of any event that occurred on the TPS65910 device. The host processor can then poll the interrupt from the interrupt status register via I^2C to identify the interrupt source. Each interrupt source can be individually masked via the interrupt mask register.

PACKAGE DESCRIPTION

The following are the package descriptions of the TPS65910 PMU devices:

- Package type:

Package	TPS65910
Type	RSL QFN-N48
Size (mm)	6x6
Substrate layers	1 layer
Pitch ball array (mm)	0.4 mm
ViP (via-in-pad)	No
Number of balls	48
Thickness (mm) (max. height including balls)	1
Others	Green, ROHS-compliant

- Moisture sensitivity level target: JEDEC MSL3 @ 260°C

APPENDIX A: FUNCTIONAL REGISTERS

TPS65910_FUNC_REG REGISTERS MAPPING SUMMARY

Table 14. TPS65910_FUNC_REG Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	Address Offset
SECONDS_REG	RW	8	0x00	0x00
MINUTES_REG	RW	8	0x00	0x01
HOURS_REG	RW	8	0x00	0x02
DAYS_REG	RW	8	0x01	0x03
MONTHS_REG	RW	8	0x01	0x04
YEARS_REG	RW	8	0x00	0x05
WEEKS_REG	RW	8	0x00	0x06
ALARM_SECONDS_REG	RW	8	0x00	0x08
ALARM_MINUTES_REG	RW	8	0x00	0x09
ALARM_HOURS_REG	RW	8	0x00	0x0A
ALARM_DAYS_REG	RW	8	0x01	0x0B
ALARM_MONTHS_REG	RW	8	0x01	0x0C
ALARM_YEARS_REG	RW	8	0x00	0x0D
RTC_CTRL_REG	RW	8	0x00	0x10
RTC_STATUS_REG	RW	8	0x80	0x11
RTC_INTERRUPTS_REG	RW	8	0x00	0x12
RTC_COMP_LSB_REG	RW	8	0x00	0x13
RTC_COMP_MSB_REG	RW	8	0x00	0x14
RTC_RES_PROG_REG	RW	8	0x27	0x15
RTC_RESET_STATUS_REG	RW	8	0x00	0x16
BCK1_REG	RW	8	0x00	0x17
BCK2_REG	RW	8	0x00	0x18
BCK3_REG	RW	8	0x00	0x19
BCK4_REG	RW	8	0x00	0x1A
BCK5_REG	RW	8	0x00	0x1B
PUADEN_REG	RW	8	0x9F	0x1C
REF_REG	RW	8	0x01	0x1D
VRTC_REG	RW	8	0x01	0x1E
VIO_REG	RW	8	0x00	0x20

Table 14. TPS65910_FUNC_REG Register Summary (continued)

Register Name	Type	Register Width (Bits)	Register Reset	Address Offset
VDD1_REG	RW	8	0x0C	0x21
VDD1_OP_REG	RW	8	0x00	0x22
VDD1_SR_REG	RW	8	0x00	0x23
VDD2_REG	RW	8	0x04	0x24
VDD2_OP_REG	RW	8	0x00	0x25
VDD2_SR_REG	RW	8	0x00	0x26
VDD3_REG	RW	8	0x04	0x27
VDIG1_REG	RW	8	0x00	0x30
VDIG2_REG	RW	8	0x00	0x31
VAUX1_REG	RW	8	0x00	0x32
VAUX2_REG	RW	8	0x00	0x33
VAUX33_REG	RW	8	0x00	0x34
VMMC_REG	RW	8	0x00	0x35
VPLL_REG	RW	8	0x00	0x36
VDAC_REG	RW	8	0x00	0x37
THERM_REG	RW	8	0x0D	0x38
BBCH_REG	RW	8	0x00	0x39
DCDCCTRL_REG	RW	8	0x3B	0x3E
DEVCTRL_REG	RW	8	0x40	0x3F
DEVCTRL2_REG	RW	8	0x34	0x40
SLEEP_KEEP_LDO_ON_REG	RW	8	0x00	0x41
SLEEP_KEEP_RES_ON_REG	RW	8	0x00	0x42
SLEEP_SET_LDO_OFF_REG	RW	8	0x00	0x43
SLEEP_SET_RES_OFF_REG	RW	8	0x00	0x44
EN1_LDO_ASS_REG	RW	8	0x00	0x45
EN1_SMPS_ASS_REG	RW	8	0x00	0x46
EN2_LDO_ASS_REG	RW	8	0x00	0x47
EN2_SMPS_ASS_REG	RW	8	0x00	0x48
RESERVED	RW	8	0x00	0x49
RESERVED	RW	8	0x00	0x4A
INT_STS_REG	RW	8	0x00	0x50
INT_MSK_REG	RW	8	0x02	0x51
INT_STS2_REG	RW	8	0x00	0x52
INT_MSK2_REG	RW	8	0x00	0x53
GPIO0_REG	RW	8	0x0A	0x60
JTAGVERNUM_REG	RO	8	0x00	0x80

TPS65910_FUNC_REG REGISTER DESCRIPTIONS

Table 15. SECONDS_REG

Address Offset	0x00	
Physical Address		**Instance**
Description	RTC register for seconds	
Type	RW	

7	6	5	4	3	2	1	0
Reserved	SEC1			SEC0			

Bits	Field Name	Description	Type	Reset
7	Reserved	Reserved bit	RO R returns 0s	0
6:4	SEC1	Second digit of seconds (range is 0 up to 5)	RW	0x0
3:0	SEC0	First digit of seconds (range is 0 up to 9)	RW	0x0

Table 16. MINUTES_REG

Address Offset	0x01	
Physical Address		**Instance**
Description	RTC register for minutes	
Type	RW	

7	6	5	4	3	2	1	0
Reserved	MIN1			MIN0			

Bits	Field Name	Description	Type	Reset
7	Reserved	Reserved bit	RO R returns 0s	0
6:4	MIN1	Second digit of minutes (range is 0 up to 5)	RW	0x0
3:0	MIN0	First digit of minutes (range is 0 up to 9)	RW	0x0

Table 17. HOURS_REG

Address Offset	0x02	
Physical Address		**Instance**
Description	RTC register for hours	
Type	RW	

7	6	5	4	3	2	1	0
PM_NAM	Reserved	HOUR1		HOUR0			

Bits	Field Name	Description	Type	Reset
7	PM_NAM	Only used in PM_AM mode (otherwise it is set to 0) 0 is AM 1 is PM	RW	0
6	Reserved	Reserved bit	RO R returns 0s	0
5:4	HOUR1	Second digit of hours(range is 0 up to 2)	RW	0x0
3:0	HOUR0	First digit of hours (range is 0 up to 9)	RW	0x0

Table 18. DAYS_REG

Address Offset	0x03	
Physical Address		**Instance**
Description	RTC register for days	
Type	RW	

7	6	5	4	3	2	1	0
Reserved		DAY1		DAY0			

Bits	Field Name	Description	Type	Reset
7:6	Reserved	Reserved bit	RO R returns 0s	0x0
5:4	DAY1	Second digit of days (range is 0 up to 3)	RW	0x0
3:0	DAY0	First digit of days (range is 0 up to 9)	RW	0x1

Table 19. MONTHS_REG

Address Offset	0x04	
Physical Address		**Instance**
Description	RTC register for months	
Type	RW	

7	6	5	4	3	2	1	0
Reserved			MONTH1	MONTH0			

Bits	Field Name	Description	Type	Reset
7:5	Reserved	Reserved bit	RO R returns 0s	0x0
4	MONTH1	Second digit of months (range is 0 up to 1)	RW	0
3:0	MONTH0	First digit of months (range is 0 up to 9)	RW	0x1

Table 20. YEARS_REG

Address Offset	0x05	
Physical Address		**Instance**
Description	RTC register for day of the week	
Type	RW	

7	6	5	4	3	2	1	0
YEAR1				YEAR0			

Bits	Field Name	Description	Type	Reset
7:4	YEAR1	Second digit of years (range is 0 up to 9)	RW	0x0
3:0	YEAR0	First digit of years (range is 0 up to 9)	RW	0x0

Table 21. WEEKS_REG

Address Offset	0x06	
Physical Address		**Instance**
Description	RTC register for day of the week	
Type	RW	

7	6	5	4	3	2	1	0
Reserved					WEEK		

Bits	Field Name	Description	Type	Reset
7:3	Reserved	Reserved bit	RO R returns 0s	0x00
2:0	WEEK	First digit of day of the week (range is 0 up to 6)	RW	0

Table 22. ALARM_SECONDS_REG

Address Offset	0x08
Physical Address	**Instance**
Description	RTC register for alarm programmation for seconds
Type	RW

7	6	5	4	3	2	1	0
Reserved	ALARM_SEC1			ALARM_SEC0			

Bits	Field Name	Description	Type	Reset
7	Reserved	Reserved bit	RO R returns 0s	0
6:4	ALARM_SEC1	Second digit of alarm programmation for seconds (range is 0 up to 5)	RW	0x0
3:0	ALARM_SEC0	First digit of alarm programmation for seconds (range is 0 up to 9)	RW	0x0

Table 23. ALARM_MINUTES_REG

Address Offset	0x09
Physical Address	**Instance**
Description	RTC register for alarm programmation for minutes
Type	RW

7	6	5	4	3	2	1	0
Reserved	ALARM_MIN1			ALARM_MIN0			

Bits	Field Name	Description	Type	Reset
7	Reserved	Reserved bit	RO R returns 0s	0
6:4	ALARM_MIN1	Second digit of alarm programmation for minutes (range is 0 up to 5)	RW	0x0
3:0	ALARM_MIN0	First digit of alarm programmation for minutes (range is 0 up to 9)	RW	0x0

Table 24. ALARM_HOURS_REG

Address Offset	0x0A
Physical Address	**Instance**
Description	RTC register for alarm programmation for hours
Type	RW

7	6	5	4	3	2	1	0
ALARM_PM_NAM	Reserved	ALARM_HOUR1		ALARM_HOUR0			

Bits	Field Name	Description	Type	Reset
7	ALARM_PM_NAM	Only used in PM_AM mode for alarm programmation (otherwise it is set to 0) 0 is AM 1 is PM	RW	0
6	Reserved	Reserved bit	RO R returns 0s	0
5:4	ALARM_HOUR1	Second digit of alarm programmation for hours(range is 0 up to 2)	RW	0x0
3:0	ALARM_HOUR0	First digitof alarm programmation for hours (range is 0 up to 9)	RW	0x0

Table 25. ALARM_DAYS_REG

Address Offset	0x0B
Physical Address	**Instance**
Description	RTC register for alarm programmation for days
Type	RW

7	6	5	4	3	2	1	0
Reserved		ALARM_DAY1		ALARM_DAY0			

Bits	Field Name	Description	Type	Reset
7:6	Reserved	Reserved bit	RO R Special	0x0
5:4	ALARM_DAY1	Second digit of alarm programmation for days (range is 0 up to 3)	RW	0x0
3:0	ALARM_DAY0	First digit of alarm programmation for days (range is 0 up to 9)	RW	0x1

Table 26. ALARM_MONTHS_REG

Address Offset	0x0C
Physical Address	**Instance**
Description	RTC register for alarm programmation for months
Type	RW

7	6	5	4	3	2	1	0
Reserved			ALARM_MONTH1	ALARM_MONTH0			

Bits	Field Name	Description	Type	Reset
7:5	Reserved	Reserved bit	RO R returns 0s	0x0
4	ALARM_MONTH1	Second digit of alarm programmation for months (range is 0 up to 1)	RW	0
3:0	ALARM_MONTH0	First digit of alarm programmation for months (range is 0 up to 9)	RW	0x1

Table 27. ALARM_YEARS_REG

Address Offset	0x0D
Physical Address	**Instance**
Description	RTC register for alarm programmation for years
Type	RW

7	6	5	4	3	2	1	0
ALARM_YEAR1				ALARM_YEAR0			

Bits	Field Name	Description	Type	Reset
7:4	ALARM_YEAR1	Second digit of alarm programmation for years (range is 0 up to 9)	RW	0x0
3:0	ALARM_YEAR0	First digit of alarm programmation for years (range is 0 up to 9)	RW	0x0

Table 28. RTC_CTRL_REG

Address Offset	0x10
Physical Address	**Instance**
Description	RTC control register: NOTES: A dummy read of this register is necessary before each I^{2}C read in order to update the ROUND_30S bit value.
Type	RW

7	6	5	4	3	2	1	0
RTC_V_OPT	GET_TIME	SET_32_COUNTER	TEST_MODE	MODE_12_24	AUTO_COMP	ROUND_30S	STOP_RTC

Bits	Field Name	Description	Type	Reset
7	RTC_V_OPT	RTC date / time register selection: 0: Read access directly to dynamic registers (SECONDS_REG, MINUTES_REG, HOURS_REG, DAYS_REG, MONTHS_REG, YEAR_REG, WEEKS_REG) 1: Read access to static shadowed registers: (see GET_TIME bit).	RW	0
6	GET_TIME	When writing a 1 into this register, the content of the dynamic registers (SECONDS_REG, MINUTES_REG, HOURS_REG, DAYS_REG, MONTHS_REG, YEAR_REG and WEEKS_REG) is transferred into static shadowed registers. Each update of the shadowed registers needs to be done by re-asserting GET_TIME bit to 1 (i.e.: reset it to 0 and then re-write it to 1)	RW	0
5	SET_32_COUNTER	0: No action 1: set the 32-kHz counter with COMP_REG value. It must only be used when the RTC is frozen.	RW	0
4	TEST_MODE	0: functional mode 1: test mode (Auto compensation is enable when the 32kHz counter reaches at its end)	RW	0
3	MODE_12_24	0: 24 hours mode 1: 12 hours mode (PM-AM mode) It is possible to switch between the two modes at any time without disturbed the RTC, read or write are always performed with the current mode.	RW	0
2	AUTO_COMP	0: No auto compensation 1: Auto compensation enabled	RW	0
1	ROUND_30S	0: No update 1: When a one is written, the time is rounded to the closest minute. This bit is a toggle bit, the micro-controller can only write one and RTC clears it. If the micro-controller sets the ROUND_30S bit and then read it, the micro-controller will read one until the rounded to the closet.	RW	0
0	STOP_RTC	0: RTC is frozen 1: RTC is running	RW	0

Table 29. RTC_STATUS_REG

Address Offset	0x11
Physical Address	**Instance**
Description	RTC status register: NOTES: A dummy read of this register is necessary before each I^2C read in order to update the status register value.
Type	RW

7	6	5	4	3	2	1	0
POWER_UP	ALARM	EVENT_1D	EVENT_1H	EVENT_1M	EVENT_1S	RUN	Reserved

Bits	Field Name	Description	Type	Reset
7	POWER_UP	Indicates that a reset occurred (bit cleared to 0 by writing 1). POWER_UP is set by a reset, is cleared by writing one in this bit.	RW	1
6	ALARM	Indicates that an alarm interrupt has been generated (bit clear by writing 1). The alarm interrupt keeps its low level, until the micro-controller write 1 in the ALARM bit of the RTC_STATUS_REG register. The timer interrupt is a low-level pulse (15 µs duration).	RW	0
5	EVENT_1D	One day has occurred	RO	0
4	EVENT_1H	One hour has occurred	RO	0
3	EVENT_1M	One minute has occurred	RO	0
2	EVENT_1S	One second has occurred	RO	0
1	RUN	0: RTC is frozen 1: RTC is running This bit shows the real state of the RTC, indeed because of STOP_RTC signal was resynchronized on 32-kHz clock, the action of this bit is delayed.	RO	0
0	Reserved	Reserved bit	RO R returns 0s	0

Table 30. RTC_INTERRUPTS_REG

Address Offset	0x12
Physical Address	**Instance**
Description	RTC interrupt control register
Type	RW

7	6	5	4	3	2	1	0
Reserved			IT_SLEEP_MASK_EN	IT_ALARM	IT_TIMER	EVERY	

Bits	Field Name	Description	Type	Reset
7:5	Reserved	Reserved bit	RO R returns 0s	0x0
4	IT_SLEEP_MASK_EN	1: Mask periodic interrupt while the TPS65910 device is in SLEEP mode. Interrupt event is back up in a register and occurred as soon as the TPS65910 device is no more in SLEEP mode. 0: Normal mode, no interrupt masked	RW	0

Bits	Field Name	Description	Type	Reset
3	IT_ALARM	Enable one interrupt when the alarm value is reached (TC ALARM registers) by the TC registers	RW	0
2	IT_TIMER	Enable periodic interrupt 0: interrupt disabled 1: interrupt enabled	RW	0
1:0	EVERY	Interrupt period 00: every second 01: every minute 10: every hour 11: every day	RW	0x0

Table 31. RTC_COMP_LSB_REG

Address Offset	0x13
Physical Address	**Instance**
Description	RTC compensation register (LSB) Notes: This register must be written in 2-complement. This means that to add one 32kHz oscillator period every hour, micro-controller needs to write FFFF into RTC_COMP_MSB_REG & RTC_COMP_LSB_REG. To remove one 32-kHz oscillator period every hour, micro-controller needs to write 0001 into RTC_COMP_MSB_REG & RTC_COMP_LSB_REG. The 7FFF value is forbidden.
Type	RW

7	6	5	4	3	2	1	0
RTC_COMP_LSB							

Bits	Field Name	Description	Type	Reset
7:0	RTC_COMP_LSB	This register contains the number of 32-kHz periods to be added into the 32-kHz counter every hour [LSB]	RW	0x00

Table 32. RTC_COMP_MSB_REG

Address Offset	0x14
Physical Address	**Instance**
Description	RTC compensation register (MSB) Notes: See RTC_COMP_LSB_REG Notes.
Type	RW

7	6	5	4	3	2	1	0
RTC_COMP_MSB							

Bits	Field Name	Description	Type	Reset
7:0	RTC_COMP_MSB	This register contains the number of 32-kHz periods to be added into the 32-kHz counter every hour [MSB]	RW	0x00

Table 33. RTC_RES_PROG_REG

Address Offset	0x15
Physical Address	**Instance**
Description	RTC register containing oscillator resistance value
Type	RW

7	6	5	4	3	2	1	0
Reserved		SW_RES_PROG					

Bits	Field Name	Description	Type	Reset
7:6	Reserved	Reserved bit	RO R returns 0s	0x0
5:0	SW_RES_PROG	Value of the oscillator resistance	RW	0x27

Table 34. RTC_RESET_STATUS_REG

Address Offset	0x16	
Physical Address		**Instance**
Description	RTC register for reset status	
Type	RW	

7	6	5	4	3	2	1	0
Reserved							RESET_STATUS

Bits	Field Name	Description	Type	Reset
7:6	Reserved	Reserved bit	RO R returns 0s	0x0
5:0	RESET_STATUS		RW	0x27

Table 35. BCK1_REG

Address Offset	0x17	
Physical Address		**Instance**
Description	Backup register which can be used for storage by the application firmware when the external host is powered down. These registers will retain their content as long as the VRTC is active.	
Type	RW	

7	6	5	4	3	2	1	0
BCKUP							

Bits	Field Name	Description	Type	Reset
7:0	BCKUP	Backup bit	RW	0x00

Table 36. BCK2_REG

Address Offset	0x18	
Physical Address		**Instance**
Description	Backup register which can be used for storage by the application firmware when the external host is powered down. These registers will retain their content as long as the VRTC is active.	
Type	RW	

7	6	5	4	3	2	1	0
BCKUP							

Bits	Field Name	Description	Type	Reset
7:0	BCKUP	Backup bit	RW	0x00

Table 37. BCK3_REG

Address Offset	0x19
Physical Address	**Instance**
Description	Backup register which can be used for storage by the application firmware when the external host is powered down. These registers will retain their content as long as the VRTC is active.
Type	RW

7	6	5	4	3	2	1	0
BCKUP							

Bits	Field Name	Description	Type	Reset
7:0	BCKUP	Backup bit	RW	0x00

Table 38. BCK4_REG

Address Offset	0x1A
Physical Address	**Instance**
Description	Backup register which can be used for storage by the application firmware when the external host is powered down. These registers will retain their content as long as the VRTC is active.
Type	RW

7	6	5	4	3	2	1	0
BCKUP							

Bits	Field Name	Description	Type	Reset
7:0	BCKUP	Backup bit	RW	0x00

Table 39. BCK5_REG

Address Offset	0x1B
Physical Address	**Instance**
Description	Backup register which can be used for storage by the application firmware when the external host is powered down. These registers will retain their content as long as the VRTC is active.
Type	RW

7	6	5	4	3	2	1	0
BCKUP							

Bits	Field Name	Description	Type	Reset
7:0	BCKUP	Backup bit	RW	0x00

Table 40. PUADEN_REG

Address Offset	0x1C
Physical Address	**Instance**
Description	Pull-up/pull-down control register.
Type	RW

7	6	5	4	3	2	1	0
RESERVED	I2CCTLP	I2CSRP	PWRONP	SLEEPP	PWRHOLDP	BOOT1P	BOOT0P

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved bit	RW	1
6	I2CCTLP	SDACTL and SCLCTL pull-up control: 1: Pull-up is enabled 0: Pull-up is disabled	RW	0
5	I2CSRP	SDASR and SCLSR pull-up control: 1: Pull-up is enabled 0: Pull-up is disabled	RW	0
4	PWRONP	PWRON pad pull-up control: 1: Pull-up is enabled 0: Pull-up is disabled	RW	1
3	SLEEPP	SLEEP pad pull-down control: 1: Pull-down is enabled 0: Pull-down is disabled	RW	1
2	PWRHOLDP	PWRHOLD pad pull-down control: 1: Pull-down is enabled 0: Pull-down is disabled	RW	1
1	BOOT1P	BOOT1 pad control: 1: Pull-down is enabled 0: Pull-down is disabled	RW	1
0	BOOT0P	BOOT0 pad control: 1: Pull-down is enabled 0: Pull-down is disabled	RW	1

Table 41. REF_REG

Address Offset	0x1D	
Physical Address		**Instance**
Description	Reference control register	
Type	RW	

7	6	5	4	3	2	1	0
Reserved				VMBCH_SEL		ST	

Bits	Field Name	Description	Type	Reset
7:4	Reserved	Reserved bit	RO R returns 0s	0x0
3:2	VMBCH_SEL	Main Battery comparator VMBCH programmable threshold (EEPROM bits): VMBCH_SEL[1:0] = 00 : bypass VMBCH_SEL[1:0] = 01 : VMBCH = 2.8 V VMBCH_SEL[1:0] = 10 : VMBCH = 2.9 V VMBCH_SEL[1:0] = 11 : VMBCH = 3.0 V	RW	0x0
1:0	ST	Reference state: ST[1:0] = 00 : Off ST[1:0] = 01 : On high power (ACTIVE) ST[1:0] = 10 : Reserved ST[1:0] = 11 : On low power (SLEEP) (Write access available in test mode only)	RO	0x1

Table 42. VRTC_REG

Address Offset	0x1E	
Physical Address		**Instance**
Description	VRTC internal regulator control register	
Type	RW	

7	6	5	4	3	2	1	0
Reserved				VRTC_OFFMASK	Reserved	ST	

Bits	Field Name	Description	Type	Reset
7:4	Reserved	Reserved bit	RO R returns 0s	0x0
3	VRTC_OFFMASK	VRTC internal regulator off mask signal: when 1, the regulator keeps its full-load capability during device OFF state. when 0, the regulator will enter in low-power mode during device OFF state.(EEPROM bit)	RW	0
2	Reserved	Reserved bit	RO R returns 0s	0
1:0	ST	Reference state: ST[1:0] = 00 : Reserved ST[1:0] = 01 : On high power (ACTIVE) ST[1:0] = 10 : Reserved ST[1:0] = 11 : On low power (SLEEP) (Write access available in test mode only)	RO	0x1

Table 43. VIO_REG

Address Offset	0x20	
Physical Address		**Instance**
Description	VIO control register	
Type	RW	

7	6	5	4	3	2	1	0
ILMAX		Reserved		SEL		ST	

Bits	Field Name	Description	Type	Reset
7:6	ILMAX	Select maximum load current: when 00: 0.5 A when 01: 1.0 A when 10: 1.0 A when 11: 1.0 A	RW	0x0
5:4	Reserved	Reserved bit	RO R returns 0s	0x0
3:2	SEL	Output voltage selection (EEPROM bits): SEL[1:0] = 00 : 1.5 V SEL[1:0] = 01 : 1.8 V SEL[1:0] = 10 : 2.5 V SEL[1:0] = 11 : 3.3 V	RW	See (1)
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00 : Off ST[1:0] = 01 : On high power (ACTIVE) ST[1:0] = 10 : Off ST[1:0] = 11 : On low power (SLEEP) (Write access available in test mode only)	RW	0x0

(1) The reset value for this field varies with boot mode selection and the processor support. Please refer to the corresponding processor user guide to find the correct default value.

Table 44. VDD1_REG

Address Offset	0x21
Physical Address	**Instance**
Description	VDD1 control register
Type	RW

7	6	5	4	3	2	1	0
VGAIN_SEL		ILMAX	TSTEP			ST	

Bits	Field Name	Description	Type	Reset
7:6	VGAIN_SEL	Select output voltage multiplication factor: G (EEPROM bits): when 00: x1 when 01: x1 when 10: x2 when 11: x3	RW	0x0
5:4	ILMAX	Select maximum load current: when 0: 1.0 A when 1: 1.5 A	RW	0
3:2	TSTEP	Time step: when changing the output voltage, the new value is reached through successive 12.5 mV voltage steps (if not bypassed). The equivalent programmable slew rate of the output voltage is then: TSTEP[2:0] = 000 : step duration is 0, step function is bypassed TSTEP[2:0] = 001 : 12.5 mV/μs (sampling 3 Mhz) TSTEP[2:0] = 010 : 9.4 mV/μs (sampling 3 Mhz × 3/4) TSTEP[2:0] = 011 : 7.5 mV/μs (sampling 3 Mhz × 3/5) (default) TSTEP[2:0] = 100 : 6.25 mV/μs(sampling 3 Mhz/2) TSTEP[2:0] = 101 : 4.7 mV/μs(sampling 3 Mhz/3) TSTEP[2:0] = 110 : 3.12 mV/μs(sampling 3 Mhz/4) TSTEP[2:0] = 111 : 2.5 mV/μs(sampling 3 Mhz/5)	RW	0x3
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00 : Off ST[1:0] = 01 : On, high power mode ST[1:0] = 10 : Off ST[1:0] = 11 : On, low power mode	RW	0x0

Table 45. VDD1_OP_REG

Address Offset	0x22
Physical Address	**Instance**
Description	VDD1 voltage selection register. This register can be accessed by both control and smartreflex I^2C interfaces depending on SR_CTL_I2C_SEL register bit value.
Type	RW

7	6	5	4	3	2	1	0
CMD	SEL						

Bits	Field Name	Description	Type	Reset
7	CMD	Smart-Reflex command: when 0: VDD1_OP_REG voltage is applied when 1: VDD1_SR_REG voltage is applied	RW	0
6:0	SEL	Output voltage (EEPROM bits) selection with GAIN_SEL = 00 (G = 1, 12.5 mV per LSB): SEL[6:0] = 1001011 to 1111111 : 1.5 V ... SEL[6:0] = 0111111 : 1.35 V ... SEL[6:0] = 0110011 : 1.2 V ... SEL[6:0] = 0000001 to 0000011 : 0.6 V SEL[6:0] = 0000000 : Off (0.0 V) Note: from SEL[6:0] = 3 to 75 (dec) Vout = (SEL[6:0] × 12.5 mV + 0.5625 mV) × G	RW	See (1)

(1) The reset value for this field varies with boot mode selection and the processor support. Please refer to the corresponding processor user guide to find the correct default value.

Table 46. VDD1_SR_REG

Address Offset	0x23
Physical Address	**Instance**
Description	VDD1 voltage selection register for smartreflex. This register can be accessed by both control and smartreflex I^2C interfaces depending on SR_CTL_I2C_SEL register bit value.
Type	RW

7	6	5	4	3	2	1	0
Reserved	SEL						

Bits	Field Name	Description	Type	Reset
7	Reserved	Reserved bit	RO R returns 0s	0
6:0	SEL	Output voltage (EEPROM bits) selection with GAIN_SEL = 00 (G = 1, 12.5 mV per LSB): SEL[6:0] = 1001011 to 1111111 : 1.5V ... SEL[6:0] = 0111111 : 1.35V ... SEL[6:0] = 0110011 : 1.2V ... SEL[6:0] = 0000001 to 0000011 : 0.6V SEL[6:0] = 0000000 : Off (0.0V) Note: from SEL[6:0] = 3 to 75 (dec) Vout = (SEL[6:0] × 12.5 mV + 0.5625 mV) × G	RW	See (1)

(1) The reset value for this field varies with boot mode selection and the processor support. Please refer to the corresponding processor user guide to find the correct default value.

Table 47. VDD2_REG

Address Offset	0x24
Physical Address	**Instance**
Description	VDD2 control register
Type	RW

7	6	5	4	3	2	1	0
VGAIN_SEL		ILMAX	TSTEP			ST	

Bits	Field Name	Description	Type	Reset
7:6	VGAIN_SEL	Select output voltage multiplication factor: G (EEPROM bits): when 00: x1 when 01: x1 when 10: x2 when 11: x3	RW	0x0
5:4	ILMAX	Select maximum load current: when 0: 1.0 A when 1: 1.5 A	RW	0
3:2	TSTEP	Time step: when changing the output voltage, the new value is reached through successive 12.5 mV voltage steps (if not bypassed). The equivalent programmable slew rate of the output voltage is then: TSTEP[2:0] = 000: step duration is 0, step function is bypassed TSTEP[2:0] = 001: 12.5 mV/µs (sampling 3 Mhz) TSTEP[2:0] = 010: 9.4 mV/µs (sampling 3 Mhz × 3/4) TSTEP[2:0] = 011: 7.5 mV/µs (sampling 3 Mhz × 3/5) (default) TSTEP[2:0] = 100: 6.25 mV/µs(sampling 3 Mhz/2) TSTEP[2:0] = 101: 4.7 mV/µs(sampling 3 Mhz/3) TSTEP[2:0] = 110: 3.12 mV/µs(sampling 3 Mhz/4) TSTEP[2:0] = 111: 2.5 mV/µs(sampling 3 Mhz/5)	RW	0x1
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00 : Off ST[1:0] = 01 : On, high power mode ST[1:0] = 10 : Off ST[1:0] = 11 : On, low power mode	RW	0x0

Table 48. VDD2_OP_REG

Address Offset	0x25
Physical Address	**Instance**
Description	VDD2 voltage selection register. This register can be accessed by both control and smartreflex I^2C interfaces depending on SR_CTL_I2C_SEL register bit value.
Type	RW

7	6	5	4	3	2	1	0
CMD	SEL						

Bits	Field Name	Description	Type	Reset
7	CMD	Smart-Reflex command: when 0: VDD2_OP_REG voltage is applied when 1: VDD2_SR_REG voltage is applied	RW	0
6:0	SEL	Output voltage (EEPROM bits) selection with GAIN_SEL = 00 (G = 1, 12.5 mV per LSB): SEL[6:0] = 1001011 to 1111111 : 1.5 V ... SEL[6:0] = 0111111 : 1.35 V ... SEL[6:0] = 0110011 : 1.2 V ... SEL[6:0] = 0000001 to 0000011 : 0.6 V SEL[6:0] = 0000000 : Off (0.0 V) Note: from SEL[6:0] = 3 to 75 (dec) Vout= (SEL[6:0] × 12.5 mV + 0.5625 mV) × G	RW	See [(1)]

(1) The reset value for this field varies with boot mode selection and the processor support. Please refer to the corresponding processor user guide to find the correct default value.

Table 49. VDD2_SR_REG

Address Offset	0x26
Physical Address	**Instance**
Description	VDD2 voltage selection register for smartreflex. This register can be accessed by both control and smartreflex I^2C interfaces depending on SR_CTL_I2C_SEL register bit value.

Table 49. VDD2_SR_REG (continued)

Type	RW

7	6	5	4	3	2	1	0
Reserved	SEL						

Bits	Field Name	Description	Type	Reset
7	Reserved	Reserved bit	RO R returns 0s	0
6:0	SEL	Output voltage (EEPROM bits) selection with GAIN_SEL = 00 (G = 1, 12.5 mV per LSB): SEL[6:0] = 1001011 to 1111111: 1.5 V ... SEL[6:0] = 0111111: 1.35V ... SEL[6:0] = 0110011: 1.2V ... SEL[6:0] = 0000001 to 0000011: 0.6V SEL[6:0] = 0000000: Off (0.0V) Note: from SEL[6:0] = 3 to 75 (dec) Vout= (SEL[6:0] × 12.5 mV + 0.5625 mV) ×G	RW	See (1)

(1) The reset value for this field varies with boot mode selection and the processor support. Please refer to the corresponding processor user guide to find the correct default value.

Table 50. VDD3_REG

Address Offset	0x27
Physical Address	**Instance**
Description	VDD2 voltage selection register for smartreflex. This register can be accessed by both control and smartreflex I^2C interfaces depending on SR_CTL_I2C_SEL register bit value.
Type	RW

7	6	5	4	3	2	1	0
Reserved					CKINEN	ST	

Bits	Field Name	Description	Type	Reset
7:3	Reserved	Reserved bit	RO R returns 0s	0x00
2	CKINEN	Enable 1Mhz clock synchronization	RW	1
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00 : Off ST[1:0] = 01 : On high power (ACTIVE) ST[1:0] = 10 : Off ST[1:0] = 11 : On low power (SLEEP)	RW	0x0

Table 51. VDIG1_REG

Address Offset	0x30
Physical Address	**Instance**
Description	VDIG1 regulator control register
Type	RW

7	6	5	4	3	2	1	0
Reserved				SEL		ST	

Bits	Field Name	Description	Type	Reset
7:4	Reserved	Reserved bit	RO R returns 0s	0x0
3:2	SEL	Supply voltage (EEPROM bits): SEL[1:0] = 00 : 1.2 V SEL[1:0] = 01 : 1.5 V SEL[1:0] = 10 : 1.8 V SEL[1:0] = 11 : 2.7 V	RW	See (1)
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00 : Off ST[1:0] = 01 : On high power (ACTIVE) ST[1:0] = 10 : Off ST[1:0] = 11 : On low power (SLEEP)	RW	0x0

(1) The reset value for this field varies with boot mode selection and the processor support. Please refer to the corresponding processor user guide to find the correct default value.

Table 52. VDIG2_REG

Address Offset	0x31	
Physical Address		**Instance**
Description	VDIG2 regulator control register	
Type	RW	

7	6	5	4	3	2	1	0
Reserved				SEL		ST	

Bits	Field Name	Description	Type	Reset
7:4	Reserved	Reserved bit	RO R returns 0s	0x0
3:2	SEL	Supply voltage (EEPROM bits): SEL[1:0] = 00 : 1.0 V SEL[1:0] = 01 : 1.1 V SEL[1:0] = 10 : 1.2 V SEL[1:0] = 11 : 1.8 V	RW	See (1)
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00 : Off ST[1:0] = 01 : On high power (ACTIVE) ST[1:0] = 10 : Off ST[1:0] = 11 : On low power (SLEEP)	RW	0x0

(1) The reset value for this field varies with boot mode selection and the processor support. Please refer to the corresponding processor user guide to find the correct default value.

Table 53. VAUX1_REG

Address Offset	0x32	
Physical Address		**Instance**
Description	VAUX1 regulator control register	
Type	RW	

7	6	5	4	3	2	1	0
Reserved				SEL		ST	

Bits	Field Name	Description	Type	Reset
7:4	Reserved	Reserved bit	RO R returns 0s	0x0
3:2	SEL	Supply voltage (EEPROM bits): SEL[1:0] = 00 : 1.8 V SEL[1:0] = 01 : 2.5 V SEL[1:0] = 10 : 2.8 V SEL[1:0] = 11 : 2.85 V	RW	See (1)
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00 : Off ST[1:0] = 01 : On high power (ACTIVE) ST[1:0] = 10 : Off ST[1:0] = 11 : On low power (SLEEP)	RW	0x0

(1) The reset value for this field varies with boot mode selection and the processor support. Please refer to the corresponding processor user guide to find the correct default value.

Table 54. VAUX2_REG

Address Offset	0x33	
Physical Address		**Instance**
Description	VAUX2 regulator control register	
Type	RW	

7	6	5	4	3	2	1	0
Reserved				SEL		ST	

Bits	Field Name	Description	Type	Reset
7:4	Reserved	Reserved bit	RO R returns 0s	0x0
3:2	SEL	Supply voltage (EEPROM bits): SEL[1:0] = 00 : 1.8 V SEL[1:0] = 01 : 2.8 V SEL[1:0] = 10 : 2.9 V SEL[1:0] = 11 : 3.3 V	RW	See (1)
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00 : Off ST[1:0] = 01 : On high power (ACTIVE) ST[1:0] = 10 : Off ST[1:0] = 11 : On low power (SLEEP)	RW	0x0

(1) The reset value for this field varies with boot mode selection and the processor support. Please refer to the corresponding processor user guide to find the correct default value.

Table 55. VAUX33_REG

Address Offset	0x34	
Physical Address		**Instance**
Description	VAUX33 regulator control register	
Type	RW	

7	6	5	4	3	2	1	0
Reserved				SEL		ST	

Bits	Field Name	Description	Type	Reset
7:4	Reserved	Reserved bit	RO R returns 0s	0x0
3:2	SEL	Supply voltage (EEPROM bits): SEL[1:0] = 00 : 1.8 V SEL[1:0] = 01 : 2.0 V SEL[1:0] = 10 : 2.8 V SEL[1:0] = 11 : 3.3 V	RW	See (1)
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00 : Off ST[1:0] = 01 : On high power (ACTIVE) ST[1:0] = 10 : Off ST[1:0] = 11 : On low power (SLEEP)	RW	0x0

(1) The reset value for this field varies with boot mode selection and the processor support. Please refer to the corresponding processor user guide to find the correct default value.

Table 56. VMMC_REG

Address Offset	0x35	
Physical Address		**Instance**
Description	VMMC regulator control register	
Type	RW	

7	6	5	4	3	2	1	0
Reserved				SEL		ST	

Bits	Field Name	Description	Type	Reset
7:4	Reserved	Reserved bit	RO R returns 0s	0x0
3:2	SEL	Supply voltage (EEPROM bits): SEL[1:0] = 00 : 1.8 V SEL[1:0] = 01 : 2.8 V SEL[1:0] = 10 : 3.0 V SEL[1:0] = 11 : 3.3 V	RW	See (1)
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00: Off ST[1:0] = 01: On high power (ACTIVE) ST[1:0] = 10: Off ST[1:0] = 11: On low power (SLEEP)	RW	0x0

(1) The reset value for this field varies with boot mode selection and the processor support. Please refer to the corresponding processor user guide to find the correct default value.

Table 57. VPLL_REG

Address Offset	0x36	
Physical Address		**Instance**
Description	VPLL regulator control register	
Type	RW	

7	6	5	4	3	2	1	0
Reserved				SEL		ST	

Bits	Field Name	Description	Type	Reset
7:4	Reserved	Reserved bit	RO R returns 0s	0x0
3:2	SEL	Supply voltage (EEPROM bits): SEL[1:0] = 00 : 1.0V SEL[1:0] = 01 : 1.1 V SEL[1:0] = 10 : 1.8 V SEL[1:0] = 11 : 2.5 V	RW	See (1)
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00 : Off ST[1:0] = 01 : On high power (ACTIVE) ST[1:0] = 10 : Off ST[1:0] = 11 : On low power (SLEEP)	RW	0x0

(1) The reset value for this field varies with boot mode selection and the processor support. Please refer to the corresponding processor user guide to find the correct default value.

Table 58. VDAC_REG

Address Offset	0x37	
Physical Address		**Instance**
Description	VDAC regulator control register	
Type	RW	

7	6	5	4	3	2	1	0
Reserved				SEL		ST	

Bits	Field Name	Description	Type	Reset
7:4	Reserved	Reserved bit	RO R returns 0s	0x0
3:2	SEL	Supply voltage (EEPROM bits): SEL[1:0] = 00 : 1.8 V SEL[1:0] = 01 : 2.6 V SEL[1:0] = 10 : 2.8 V SEL[1:0] = 11 : 2.85 V	RW	See (1)
1:0	ST	Supply state (EEPROM bits): ST[1:0] = 00 : Off ST[1:0] = 01 : On high power (ACTIVE) ST[1:0] = 10 : Off ST[1:0] = 11 : On low power (SLEEP)	RW	0x0

(1) The reset value for this field varies with boot mode selection and the processor support. Please refer to the corresponding processor user guide to find the correct default value.

Table 59. Therm_REG

Address Offset	0x38	
Physical Address		**Instance**
Description	Thermal control register	
Type	RW	

7	6	5	4	3	2	1	0
Reserved		THERM_HD	THERM_TS	THERM_HDSEL		RSVD1	THERM_STATE

Bits	Field Name	Description	Type	Reset
7:6	Reserved	Reserved bit	RO R returns 0s	0x0
5	THERM_HD	Hot die detector output: when 0: the hot die threshold is not reached when 1: the hot die threshold is reached	RO	0
4	THERM_TS	Thermal shutdown detector output: when 0: the thermal shutdown threshold is not reached when 1: the thermal shutdown threshold is reached	RO	0
3:2	THERM_HDSEL	Temperature selection for Hot Die detector: when 00: Low temperature threshold … when 11: High temperature threshold	RW	0x3
1	RSVD1	Reserved bit	RW	0
0	THERM_STATE	Thermal shutdown module enable signal: when 0: thermal shutdown module is disable when 1: thermal shutdown module is enable	RW	1

Table 60. BBCH_REG

Address Offset	0x39	
Physical Address		**Instance**
Description	Back-up battery charger control register	
Type	RW	

7	6	5	4	3	2	1	0
Reserved					BBSEL		BBCHEN

Bits	Field Name	Description	Type	Reset
7:4	Reserved	Reserved bit	RO R returns 0s	0x00
2:1	BBSEL	Back up battery charge voltage selection: BBSEL[1:0] = 00 : 3.0 V BBSEL[1:0] = 01 : 2.52 V BBSEL[1:0] = 10 : 3.15 V BBSEL[1:0] = 11 : VBAT	RW	0x0
0	BBCHEN	Back up battery charge enable	RW	0

Table 61. DCDCCTRL_REG

Address Offset	0x3E	
Physical Address		**Instance**
Description	DCDC control register	
Type	RW	

7	6	5	4	3	2	1	0
Reserved		VDD2_PSKIP	VDD1_PSKIP	VIO_PSKIP	DCDCCKEXT	DCDCCKSYNC	

Bits	Field Name	Description	Type	Reset
7:6	Reserved	Reserved bit	RO R returns 0s	0x0
5	VDD2_PSKIP	VDD2 pulse skip mode enable (EEPROM bit)	RW	1
4	VDD1_PSKIP	VDD1 pulse skip mode enable (EEPROM bit)	RW	1
3	VIO_PSKIP	VIO pulse skip mode enable (EEPROM bit)	RW	1

Bits	Field Name	Description	Type	Reset
2	DCDCCKEXT	This signal control the muxing of the GPIO0 pad: When 0: this pad is a GPIO When 1: this pad is used as input for an external clock used for the synchronisation of the DCDCs	RW	0
1:0	DCDCCKSYNC	DCDC clock configuration: DCDCCKSYNC[1:0] = 00 : no synchronization of DCDC clocks DCDCCKSYNC[1:0] = 01 : DCDC synchronous clock with phase shift DCDCCKSYNC[1:0] = 10 : no synchronization of DCDC clocks DCDCCKSYNC[1:0] = 11 : DCDC synchronous clock	RW	0x3

Table 62. DEVCTRL_REG

Address Offset	0x3F	
Physical Address		**Instance**
Description	Device control register	
Type	RW	

7	6	5	4	3	2	1	0
Reserved	RTC_PWDN	CK32K_CTRL	SR_CTL_I2C_SEL	DEV_OFF_RST	DEV_ON	DEV_SLP	DEV_OFF

Bits	Field Name	Description	Type	Reset
7	Reserved	Reserved bit	RO R returns 0s	0
6	RTC_PWDN	When 1, disable the RTC digital domain (clock gating and reset of RTC registers and logic). This register bit is not reset in BACKUP state. (EEPROM bit)	RW	1
5	CK32K_CTRL	Internal 32-kHz clock source control bit (EEPROM bit): when 0, the internal 32-kHz clock source is the crystal oscillator or an external 32-kHz clock in case the crystal oscillator is used in bypass mode when 1, the internal 32-kHz clock source is the RC oscillator.	RW	0
4	SR_CTL_I2C_SEL	Smartreflex registers access control bit: when 0: access to smartreflex registers by smartreflex I2C when 1: access to smartreflex registers by control I2C The smartreflex registers are: VDD1_OP_REG, VDD1_SR_REG, VDD2_OP_REG and VDD2_SR_REG.	RW	0
3	DEV_OFF_RST	Write 1 will start an ACTIVE to OFF or SLEEP to OFF device state transition (switch-off event) and activate reset of the digital core.	RW	0
2	DEV_ON	Write 1 will maintain the device on (ACTIVE or SLEEP device state) (if DEV_OFF = 0 and DEV_OFF_RST = 0).	RW	0
1	DEV_SLP	Write 1 allows SLEEP device state (if DEV_OFF = 0 and DEV_OFF_RST = 0). Write ‘0’ will start an SLEEP to ACTIVE device state transition (wake-up event) (if DEV_OFF = 0 and DEV_OFF_RST = 0). This bit is cleared in OFF state.	RW	0
0	DEV_OFF	Write 1 will start an ACTIVE to OFF or SLEEP to OFF device state transition (switch-off event). This bit is cleared in OFF state.	RW	0

Table 63. DEVCTRL2_REG

Address Offset	0x40	
Physical Address		**Instance**
Description	Device control register	

Table 63. DEVCTRL2_REG (continued)

Type	RW

7	6	5	4	3	2	1	0
Reserved		TSLOT_LENGTH		SLEEPSIG_POL	PWRON_LP_OFF	PWRON_LP_RST	IT_POL

Bits	Field Name	Description	Type	Reset
7:6	Reserved	Reserved bit	RO R returns 0s	0x0
5:4	TSLOT_LENGTH	Time slot duration programming (EEPROM bit): When 00 : 0 μs When 01 : 200 μs When 10 : 500 μs When 11 : 2 ms	RW	0x3
3	SLEEPSIG_POL	When 1, SLEEP signal active high When 0, SLEEP signal active low	RW	0
2	PWRON_LP_OFF	When 1, allows device turn-off after a PWRON long press (signal low).	RW	1
1	PWRON_LP_RST	When 1, allows digital core reset when the device is OFF after a PWRON long press (signal low).	RW	0
0	IT_POL	INT1 interrupt pad polarity control signal (EEPROM bit): When 0, active low When 1, active high	RW	0

Table 64. SLEEP_KEEP_LDO_ON_REG

Address Offset	0x41
Physical Address	**Instance**
Description	When corresponding control bit=0 in EN1/2_ LDO_ASS register (default setting): Configuration Register keeping the full load capability of LDO regulator (ACTIVE mode) during the SLEEP state of the device. When control bit=1, LDO regulator full load capability (ACTIVE mode) is maintained during device SLEEP state. When control bit=0, the LDO regulator is set or stay in low power mode during device SLEEP state(but then supply state can be overwritten programming ST[1:0]). Control bit value has no effect if the LDO regulator is off. When corresponding control bit=1 in EN1/2_ LDO_ASS register: Configuration Register setting the LDO regulator state driven by SCLSR_EN1/2 signal low level (when SCLSR_EN1/2 is high the regulator is on, full power): - the regulator is set off if its corresponding Control bit = 0 in SLEEP_KEEP_LDO_ON register (default) - the regulator is set in low power mode if its corresponding control bit = 1 in SLEEP_KEEP_LDO_ON register
Type	RW

7	6	5	4	3	2	1	0
VDAC_KEEPON	VPLL_KEEPON	VAUX33_KEEPON	VAUX2_KEEPON	VAUX1_KEEPON	VDIG2_KEEPON	VDIG1_KEEPON	VMMC_KEEPON

Bits	Field Name	Description	Type	Reset
7	VDAC_KEEPON	Setting supply state during device SLEEP state or when SCLSR_EN1/2 is low	RW	0
6	VPLL_KEEPON	Setting supply state during device SLEEP state or when SCLSR_EN1/2 is low	RW	0
5	VAUX33_KEEPON	Setting supply state during device SLEEP state or when SCLSR_EN1/2 is low	RW	0
4	VAUX2_KEEPON	Setting supply state during device SLEEP state or when SCLSR_EN1/2 is low	RW	0
3	VAUX1_KEEPON	Setting supply state during device SLEEP state or when SCLSR_EN1/2 is low	RW	0
2	VDIG2_KEEPON	Setting supply state during device SLEEP state or when SCLSR_EN1/2 is low	RW	0
1	VDIG1_KEEPON	Setting supply state during device SLEEP state or when SCLSR_EN1/2 is low	RW	0
0	VMMC_KEEPON	Setting supply state during device SLEEP state or when SCLSR_EN1/2 is low	RW	0

Table 65. SLEEP_KEEP_RES_ON_REG

Address Offset	0x42
Physical Address	**Instance**
Description	Configuration Register keeping, during the SLEEP state of the device (but then supply state can be overwritten programming ST[1:0]): - the full load capability of LDO regulator (ACTIVE mode), - The PWM mode of DCDC converter - 32KHz clock output - Register access though I2C interface (keeping the internal high speed clock on) - Die Thermal monitoring on Control bit value has no effect if the resource is off.
Type	RW

7	6	5	4	3	2	1	0
THERM_KEEPON	CLKOUT32K_KEEPON	VRTC_KEEPON	I2CHS_KEEPON	VDD3_KEEPON	VDD2_KEEPON	VDD1_KEEPON	VIO_KEEPON

Bits	Field Name	Description	Type	Reset
7	THERM_KEEPON	When 1, thermal monitoring is maintained during device SLEEP state. When 0, thermal monitoring is turned off during device SLEEP state.	RW	0
6	CLKOUT32K_KEEPON	When 1, CLK32KOUT output is maintained during device SLEEP state. When 0, CLK32KOUT output is set low during device SLEEP state.	RW	0
5	VRTC_KEEPON	When 1, LDO regulator full load capability (ACTIVE mode) is maintained during device SLEEP state. When 0, the LDO regulator is set or stays in low power mode during device SLEEP state.	RW	0
4	I2CHS_KEEPON	When 1, high speed internal clock is maintained during device SLEEP state. When 0, high speed internal clock is turned off during device SLEEP state.	RW	0
3	VDD3_KEEPON	When 1, VDD3 SMPS high power mode is maintained during device SLEEP state. No effect if VDD3 working mode is low power. When 0, VDD3 SMPS low power mode is set during device SLEEP state.	RW	0

Bits	Field Name	Description	Type	Reset
2	VDD2_KEEPON	If VDD2_EN1&2 control bit = 0 (default setting): When 1, VDD2 SMPS PWM mode is maintained during device SLEEP state. No effect if VDD2 working mode is PFM. When 0, VDD2 SMPS PFM mode is set during device SLEEP state.	RW	0
1	VDD1_KEEPON	If VDD1_EN1&2 control bit=0 (default setting): When 1, VDD1 SMPS PWM mode is maintained during device SLEEP state. No effect if VDD1 working mode is PFM. When 0, VDD1 SMPS PFM mode is set during device SLEEP state.	RW	0
0	VIO_KEEPON	If VIO_EN1&2 control bit=0 (default setting): When 1, VIO SMPS PWM mode is maintained during device SLEEP state. No effect if VIO working mode is PFM. When 0, VIO SMPS PFM mode is set during device SLEEP state.	RW	0

Table 66. SLEEP_SET_LDO_OFF_REG

Address Offset	0x43
Physical Address	**Instance**
Description	Configuration Register turning-off LDO regulator during the SLEEP state of the device. Corresponding *_KEEP_ON control bit in SLEEP_KEEP_RES_ON register should be 0 to make this *_SET_OFF control bit effective
Type	RW

7	6	5	4	3	2	1	0
VDAC_SETOFF	VPLL_SETOFF	VAUX33_SETOFF	VAUX2_SETOFF	VAUX1_SETOFF	VDIG2_SETOFF	VDIG1_SETOFF	VMMC_SETOFF

Bits	Field Name	Description	Type	Reset
7	VDAC_SETOFF	When 1, LDO regulator is turned off during device SLEEP state. When 0, No effect	RW	0
6	VPLL_SETOFF	When 1, LDO regulator is turned off during device SLEEP state. When 0, No effect	RW	0
5	VAUX33_SETOFF	When 1, LDO regulator is turned off during device SLEEP state. When 0, No effect	RW	0
4	IVAUX2_SETOFF	When 1, LDO regulator is turned off during device SLEEP state. When 0, No effect	RW	0
3	VAUX1_SETOFF	When 1, LDO regulator is turned off during device SLEEP state. When 0, No effect	RW	0
2	VDIG2_SETOFF	When 1, LDO regulator is turned off during device SLEEP state. When 0, No effect	RW	0
1	VDIG1_SETOFF	When 1, LDO regulator is turned off during device SLEEP state. When 0, No effect	RW	0
0	VMMC_SETOFF	When 1, LDO regulator is turned off during device SLEEP state. When 0, No effect	RW	0

Table 67. SLEEP_SET_RES_OFF_REG

Address Offset	0x44
Physical Address	**Instance**
Description	Configuration Register turning-off SMPS regulator during the SLEEP state of the device. Corresponding *_KEEP_ON control bit in SLEEP_KEEP_RES_ON2 register should be 0 to make this *_SET_OFF control bit effective. Supplies voltage expected after their wake-up (SLEEP to ACTIVE state transition) can also be programmed.
Type	RW

7	6	5	4	3	2	1	0
DEFAULT_VOLT	RSVD		SPARE_SETOFF	VDD3_SETOFF	VDD2_SETOFF	VDD1_SETOFF	VIO_SETOFF

Bits	Field Name	Description	Type	Reset
7	DEFAULT_VOLT	When 1, default voltages (registers value after switch-on) will be used to turned-on supplies during SLEEP to ACTIVE state transition. When 0, voltages programmed before the ACTIVE to SLEEP state transition will be used to turned-on supplies during SLEEP to ACTIVE state transition.	RW	0
6:5	RSVD	Reserved bit	RO R returns 0s	0x0
4	SPARE_SETOFF	Spare bit	RW	0
3	VDD3_SETOFF	When 1, SMPS is turned off during device SLEEP state. When 0, No effect.	RW	0
2	VDD2_SETOFF	When 1, SMPS is turned off during device SLEEP state. When 0, No effect.	RW	0
1	VDD1_SETOFF	When 1, SMPS is turned off during device SLEEP state. When 0, No effect.	RW	0
0	VIO_SETOFF	When 1, SMPS is turned off during device SLEEP state. When 0, No effect.	RW	0

Table 68. EN1_LDO_ASS_REG

Address Offset	0x45
Physical Address	**Instance**
Description	Configuration Register setting the LDO regulators, driven by the multiplexed SCLSR_EN1 signal. When control bit = 1, LDO regulator state is driven by the SCLSR_EN1 control signal and is also defined though SLEEP_KEEP_LDO_ON register setting: When SCLSR_EN1 is high the regulator is on, When SCLSR_EN1 is low: - the regulator is off if its corresponding Control bit = 0 in SLEEP_KEEP_LDO_ON register - the regulator is working in low power mode if its corresponding control bit = 1 in SLEEP_KEEP_LDO_ON register When control bit = 0 no effect : LDO regulator state is driven though registers programming and the device state Any control bit of this register set to 1 will disable the I2C SR Interface functionality
Type	RW

7	6	5	4	3	2	1	0
VDAC_EN1	VPLL_EN1	VAUX33_EN1	VAUX2_EN1	VAUX1_EN1	VDIG2_EN1	VDIG1_EN1	VMMC_EN1

Bits	Field Name	Description	Type	Reset
7	VDAC_EN1	Setting supply state control though SCLSR_EN1 signal	RW	0
6	VPLL_EN1	Setting supply state control though SCLSR_EN1 signal	RW	0
5	VAUX33_EN1	Setting supply state control though SCLSR_EN1 signal	RW	0
4	VAUX2_EN1	Setting supply state control though SCLSR_EN1 signal	RW	0
3	VAUX1_EN1	Setting supply state control though SCLSR_EN1 signal	RW	0
2	VDIG2_EN1	Setting supply state control though SCLSR_EN1 signal	RW	0
1	VDIG1_EN1	Setting supply state control though SCLSR_EN1 signal	RW	0
0	VMMC_EN1	Setting supply state control though SCLSR_EN1 signal	RW	0

Table 69. EN1_SMPS_ASS_REG

Address Offset	0x46
Physical Address	**Instance**
Description	Configuration Register setting the SMPS Supplies driven by the multiplexed SCLSR_EN1 signal. When control bit = 1, SMPS Supply state and voltage is driven by the SCLSR_EN1 control signal and is also defined though SLEEP_KEEP_RES_ON register setting. When control bit = 0 no effect : SMPS Supply state is driven though registers programming and the device state. Any control bit of this register set to 1 will disable the I2C SR Interface functionality
Type	RW

7	6	5	4	3	2	1	0
RSVD			SPARE_EN1	VDD3_EN1	VDD2_EN1	VDD1_EN1	VIO_EN1

Bits	Field Name	Description	Type	Reset
7:5	RSVD	Reserved bit	RW	0
4	SPARE_EN1	Spare bit	Rw	0
3	VDD3_EN1	When 1: When SCLSR_EN1 is high the supply is on. When SCLSR_EN1 is low and SLEEP_KEEP_RES_ON = '0' the supply voltage is off. When SCLSR_EN1 is low and SLEEP_KEEP_RES_ON = '1' the SMPS is working in low power mode. When control bit = 0 no effect: supply state is driven though registers programming and the device state	RW	0
2	VDD2_EN1	When control bit = 1: When SCLSR_EN1 is high the supply voltage is programmed though VDD2_OP_REG register, and it can also be programmed off. When SCLSR_EN1 is low the supply voltage is programmed though VDD2_SR_REG register, and it can also be programmed off. When SCLSR_EN1 is low and VDD2_KEEPON = 1 the SMPS is working in low power mode, if not tuned off through VDD2_SR_REG register. When control bit = 0 no effect: supply state is driven though registers programming and the device state	RW	0
1	VDD1_EN1	When 1: When SCLSR_EN1 is high the supply voltage is programmed though VDD1_OP_REG register, and it can also be programmed off. When SCLSR_EN1 is low the supply voltage is programmed though VDD1_SR_REG register, and it can also be programmed off. When SCLSR_EN1 is low and VDD1_KEEPON = 1 the SMPS is working in low power mode, if not tuned off though VDD1_SR_REG register. When control bit = 0 no effect: supply state is driven though registers programming and the device state	RW	0
0	VIO_EN1	When control bit = 1, supply state is driven by the SCLSR_EN1 control signal and is also defined though SLEEP_KEEP_RES_ON register setting: When SCLSR_EN1 is high the supply is on, When SCLSR_EN1 is low: - the supply is off (default) or the SMPS is working in low power mode if VIO_KEEPON = 1 When control bit = 0 no effect: SMPS state is driven though registers programming and the device state	RW	0

Table 70. EN2_LDO_ASS_REG

Address Offset	0x47
Physical Address	**Instance**
Description	Configuration Register setting the LDO regulators, driven by the multiplexed SDASR_EN2 signal. When control bit = 1, LDO regulator state is driven by the SDASR_EN2 control signal and is also defined though SLEEP_KEEP_LDO_ON register setting: When SDASR_EN2 is high the regulator is on, When SCLSR_EN2 is low: - the regulator is off if its corresponding Control bit = 0 in SLEEP_KEEP_LDO_ON register - the regulator is working in low power mode if its corresponding control bit = 1 in SLEEP_KEEP_LDO_ON register When control bit = 0 no effect: LDO regulator state is driven though registers programming and the device state Any control bit of this register set to 1 will disable the I2C SR Interface functionality
Type	RW

7	6	5	4	3	2	1	0
VDAC_EN2	VPLL_EN2	VAUX33_EN2	VAUX2_EN2	VAUX1_EN2	VDIG2_EN2	VDIG1_EN2	VMMC_EN2

Bits	Field Name	Description	Type	Reset
7	VDAC_EN2	Setting supply state control though SDASR_EN2 signal	RW	0
6	VPLL_EN2	Setting supply state control though SDASR_EN2 signal	RW	0
5	VAUX33_EN2	Setting supply state control though SDASR_EN2 signal	RW	0
4	VAUX2_EN2	Setting supply state control though SDASR_EN2 signal	RW	0
3	VAUX1_EN2	Setting supply state control though SDASR_EN2 signal	RW	0
2	VDIG2_EN2	Setting supply state control though SDASR_EN2 signal	RW	0
1	VDIG1_EN2	Setting supply state control though SDASR_EN2 signal	RW	0
0	VMMC_EN2	Setting supply state control though SDASR_EN2 signal	RW	0

Table 71. EN2_SMPS_ASS_REG

Address Offset	0x48
Physical Address	**Instance**
Description	Configuration Register setting the SMPS Supplies driven by the multiplexed SDASR_EN2 signal. When control bit = 1, SMPS Supply state and voltage is driven by the SDASR_EN2 control signal and is also defined though SLEEP_KEEP_RES_ON register setting. When control bit = 0 no effect: SMPS Supply state is driven though registers programming and the device state Any control bit of this register set to 1 will disable the I2C SR Interface functionality
Type	RW

7	6	5	4	3	2	1	0
RSVD			SPARE_EN2	VDD3_EN2	VDD2_EN2	VDD1_EN2	VIO_EN2

Bits	Field Name	Description	Type	Reset
7:5	RSVD	Reserved bit	RO R returns 0s	0x0
4	SPARE_EN2	Spare bit	RW	0
3	VDD3_EN2	When 1: When SDASR_EN2 is high the supply is on. When SDASR_EN2 is low and SLEEP_KEEP_RES_ON = 0 the supply voltage is off. When SDASR_EN2 is low and SLEEP_KEEP_RES_ON = 1 the SMPS is working in low power mode. When control bit = 0 no effect: supply state is driven though registers programming and the device state	RW	0

Bits	Field Name	Description	Type	Reset
2	VDD2_EN2	When control bit = 1: When SDASR_EN2 is high the supply voltage is programmed though VDD2_OP_REG register, and it can also be programmed off. When SDASR_EN2 is low the supply voltage is programmed though VDD2_SR_REG register, and it can also be programmed off. When SDASR_EN2 is low and and VDD2_KEEPON = 1 the SMPS is working in low power mode, if not tuned off though VDD2_SR_REG register. When control bit = 0 no effect: supply state is driven though registers programming and the device state	RW	0
1	VDD1_EN2	When control bit = 1: When SDASR_EN2 is high the supply voltage is programmed though VDD1_OP_REG register, and it can also be programmed off. When SDASR_EN2 is low the supply voltage is programmed though VDD1_SR_REG register, and it can also be programmed off. When SDASR_EN2 is low and and VDD1_KEEPON = 1 the SMPS is working in low power mode, if not tuned off though VDD1_SR_REG register. When control bit = 0 no effect: supply state is driven though registers programming and the device state	RW	0
0	VIO_EN2	When control bit = 1, supply state is driven by the SCLSR_EN2 control signal and is also defined though SLEEP_KEEP_RES_ON register setting: When SDASR _EN2 is high the supply is on, When SDASR _EN2 is low : - the supply is off (default) or the SMPS is working in low power mode if VIO_KEEPON = 1 When control bit = 0 no effect: SMPS state is driven though registers programming and the device state	RW	0

Table 72. RESERVED

Address Offset	0x49	
Physical Address		**Instance**
Description	Reserved register	
Type	RW	

7	6	5	4	3	2	1	0
RESERVED							

Bits	Field Name	Description	Type	Reset
7:0	RESERVED	Reserved bit	RW	0

Table 73. RESERVED

Address Offset	0x4A	
Physical Address		**Instance**
Description	Reserved register	
Type	RW	

7	6	5	4	3	2	1	0
RESERVED							

Bits	Field Name	Description	Type	Reset
7:0	RESERVED	Reserved bit	RW	0x00

Table 74. INT_STS_REG

Address Offset	0x50
Physical Address	**Instance**
Description	Interrupt status register: The interrupt status bit is set to 1 when the associated interrupt event is detected. Interrupt status bit is cleared by writing 1.
Type	RW

7	6	5	4	3	2	1	0
RTC_PERIOD_IT	RTC_ALARM_IT	HOTDIE_IT	PWRHOLD_IT	PWRON_LP_IT	PWRON_IT	VMBHI_IT	VMBDCH_IT

Bits	Field Name	Description	Type	Reset
7	RTC_PERIOD_IT	RTC period event interrupt status.	RW W1 to Clr	0
6	RTC_ALARM_IT	RTC alarm event interrupt status.	RW W1 to Clr	0
5	HOTDIE_IT	Hot die event interrupt status.	RW W1 to Clr	0
4	PWRHOLD_IT	PWRHOLD event interrupt status.	RW W1 to Clr	0
3	PWRON_LP_IT	PWRON Long Press event interrupt status.	RW W1 to Clr	0
2	PWRON_IT	PWRON event interrupt status.	RW W1 to Clr	0
1	VMBHI_IT	VBAT > VMHI event interrupt status	RW W1 to Clr	0
0	VMBDCH_IT	VBAT > VMBDCH event interrupt status. Active only if Main Battery comparator VMBCH programmable threshold is not bypassed (VMBCH_SEL[1:0] ≠ 00)	RW W1 to Clr	0

Table 75. INT_MSK_REG

Address Offset	0x51
Physical Address	**Instance**
Description	Interrupt mask register: When *_IT_MSK is set to 1, the associated interrupt is masked: INT1 signal is not activated, but *_IT interrupt status bit is updated. When *_IT_MSK is set to 0, the associated interrupt is enabled: INT1 signal is activated, *_IT is updated.
Type	RW

7	6	5	4	3	2	1	0
RTC_PERIOD_IT_MSK	RTC_ALARM_IT_MSK	HOTDIE_IT_MSK	PWRHOLD_IT_MSK	PWRON_LP_IT_MSK	PWRON_IT_MSK	VMBHI_IT_MSK	VMBDCH_IT_MSK

Bits	Field Name	Description	Type	Reset
7	RTC_PERIOD_IT_MSK	RTC period event interrupt mask.	RW	0
6	RTC_ALARM_IT_MSK	RTC alarm event interrupt mask.	RW	0
5	HOTDIE_IT_MSK	Hot die event interrupt mask.	RW	0
4	PWRHOLD_IT_MSK	PWRHOLD rising edge event interrupt mask.	RW	0
3	PWRON_LP_IT_MSK	PWRON Long Press event interrupt mask.	RW	0
2	PWRON_IT_MSK	PWRON event interrupt mask.	RW	0
1	VMBHI_IT_MSK	VBAT > VMBHI event interrupt mask. When 0, enable the device automatic switch on at BACKUP to OFF or NOSUPPLY to OFF device state transition (EEPROM bit)	RW	1
0	VMBDCH_IT_MSK	VBAT < VMBDCH event interrupt status. Active only if the main battery comparator VMBCH programmable threshold is not bypassed (VMBCH_SEL[1:0] ≠ 00).	RW	0

Table 76. INT_STS2_REG

Address Offset	0x52
Physical Address	**Instance**
Description	Interrupt status register: The interrupt status bit is set to 1 when the associated interrupt event is detected. Interrupt status bit is cleared by writing 1.
Type	RW

7	6	5	4	3	2	1	0
Reserved						GPIO0_F_IT	GPIO0_R_IT

Bits	Field Name	Description	Type	Reset
7:2	Reserved	Reserved bit	RW W1 to Clr	0
1	GPIO0_F_IT	GPIO_CKSYNC falling edge detection interrupt status	RW W1 to Clr	0
0	GPIO0_R_IT	GPIO_CKSYNC rising edge detection interrupt status	RW W1 to Clr	0

Table 77. INT_MSK2_REG

Address Offset	0x53
Physical Address	**Instance**
Description	Interrupt mask register: When *_IT_MSK is set to 1, the associated interrupt is masked: INT1 signal is not activated, but *_IT interrupt status bit is updated. When *_IT_MSK is set to 0, the associated interrupt is enabled: INT1 signal is activated, *_IT is updated.
Type	RW

7	6	5	4	3	2	1	0
Reserved						GPIO0_F_IT_MSK	GPIO0_R_IT_MSK

Bits	Field Name	Description	Type	Reset
7:2	Reserved	Reserved bit	RW	0
1	GPIO0_F_IT_MSK	GPIO_CKSYNC falling edge detection interrupt mask.	RW	0
0	GPIO0_R_IT_MSK	GPIO_CKSYNC rising edge detection interrupt mask.	RW	0

Table 78. GPIO0_REG

Address Offset	0x60	
Physical Address		**Instance**
Description	GPIO0 configuration register	
Type	RW	

7	6	5	4	3	2	1	0
Reserved			GPIO_DEB	GPIO_PUEN	GPIO_CFG	GPIO_STS	GPIO_SET

Bits	Field Name	Description	Type	Reset
7:5	Reserved	Reserved bit	RO R returns 0s	0x0
4	GPIO_DEB	GPIO_CKSYNC input debouncing time configuration: When 0, the debouncing is 91.5 μs using a 30.5 μs clock rate When 1, the debouncing is 150 ms using a 50 ms clock rate	RW	0
3	GPIO_PUEN	GPIO_CKSYNC pad pull-up control: 1: Pull-up is enabled 0: Pull-up is disabled	RW	1
2	GPIO_CFG	Configuration of the GPIO_CKSYNC pad direction: When 0, the pad is configured as an input When 1, the pad is configured as an output	RW	0
1	GPIO_STS	Status of the GPIO_CKSYNC pad	RO	1
0	GPIO_SET	Value set on the GPIO output when configured in output mode	RW	0

Table 79. JTAGVERNUM_REG

Address Offset	0x80	
Physical Address		**Instance**
Description	Silicon version number	
Type	RO	

7	6	5	4	3	2	1	0
Reserved				VERNUM			

Bits	Field Name	Description	Type	Reset
7:4	Reserved	Reserved bit	RO R returns 0s	0x0
3:0	VERNUM	Value depending on silicon version number 0000 - Revision 1.0	RO	0x0

GLOSSARY

ACRONYMS, ABBREVIATIONS, AND DEFINITIONS

ACRONYM	DEFINITION
DDR	Dual-Data Rate (memory)
ES	Engineering Sample
ESD	Electrostatic Discharge
FET	Field Effect Transistor
EPC	Embedded Power Controller
FSM	Finite State Machine
GND	Ground
GPIO	General-Purpose I/O
HBM	Human Body Model
HD	Hot-Die
HS-I^{2}C	High-Speed I^{2}C
I^{2}C	Inter-Integrated Circuit
IC	Integrated Circuit
ID	Identification
IDDQ	Quiescent supply current
IEEE	Institute of Electrical and Electronics Engineers
IR	Instruction Register
I/O	Input/Output
JEDEC	Joint Electron Device Engineering Council
JTAG	Joint Test Action Group
LBC7	Lin Bi-CMOS 7 (360 nm)
LDO	Low Drop Output voltage linear regulator
LP	Low-Power application mode
LSB	Least Significant Bit
MMC	Multimedia Card
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NVM	Nonvolatile Memory
OMAP™	Open Multimedia Application Platform™
RTC	Real-Time Clock
SMPS	Switched Mode Power Supply
SPI	Serial Peripheral Interface
POR	Power-On Reset

Table 80. REVISION HISTORY

VERSION	DATE	NOTES
*	03/2010	See (1).
A	05/2010	See (2).
B	06/2010	See (3).
C	06/2010	See (4).
D	11/2010	See (5).
E	01/2011	See (6).
F	01/2011	See (7).
G	05/2011	See (8).
H	06/2011	See (9).
I	07/2011	See (10)
J	10/2011	See (11)
K	10/2011	See (12)

(1) Initial release
(2) SWCS046A: Updated register tables VMMC_REG and VDAC_REG. Added register table VPLL_REG
(3) SWCS046B: Update Absolute Maximum Ratings, Recommended Operating Conditions, I/O Pullup and Pulldown Characteristics, DigitaL I/Os Voltage Electrical Characteristics, Power Consumption, Power References and Thresholds, Thermal Monitoring and Shutdown, 32-kHz RTC Clock, VRTC LDO, VIO SMPS, VDD1 SMPS, VDD2 SMPS, VDD3 SMPS, Switch-On/-Off Sequences and Timing
(4) SWCS046C: Associate parts; no change.
(5) SWCS046D: Update Recommended Operating Conditions - Backup Battery, I/O Pullup and Pulldown Characteristics, Backup Battery Charger. Update Rated output current, PMOS current limit (High-Side), NMOS current limit (Low-Side), and Conversion Efficiency for VIO SMPS, VDD1/VDD2/VDD3 SMPS and VDIG1/VDIG2 LDO. Update Input Voltage for VIO/VDD1/VDD2 SMPS. Update DC and Transient Load and Line Regulatio and Internal Resistance for VDIG1/VDIG2 LDO, VAUX33/VMMC LDO, VAUX1,VAUX2, LDO, and VDAC/VPLL LDO. Update DC Load Regulation for VAUX3/VMMC/VDAC. Update Power Control Timing. Add Device SLEEP State Control. Add SMPS Switching Synchronization. Update VIO_REG, VDD1_REG, and VDD2_REG.
(6) SWCS046E: Manually added Thermal Pad Mechanical Data.
(7) SWCS046F: UpdateTable 1, *SUPPORTED PROCESSORS AND CORRESPONDING PART NUMBERS*.
(8) SWCS046G: Update PACKAGE DESCRIPTION, RECOMMENDED OPERATING CONDITIONS, DIGITAL I/O VOLTAGE ELECTRICAL CHARACTERISTICS, and PWRON.
(9) SWCS046H: Update Table 40, PUADEN_REG, Table 72, RESERVED, and Table 73, RESERVED.
(10) SWCS046I: Update DC Output voltage V_{OUT} in VAUX1 AND VAUX2 LDO.
(11) SWCS046J: UpdateTable 1, *SUPPORTED PROCESSORS AND CORRESPONDING PART NUMBERS*.
(12) SWCS046K: UpdateTable 1, *SUPPORTED PROCESSORS AND CORRESPONDING PART NUMBERS - Add AM35x*.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS659101A1RSL	ACTIVE	VQFN	RSL	48	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TPS659101A1RSLR	ACTIVE	VQFN	RSL	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TPS659102A1RSL	ACTIVE	VQFN	RSL	48	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TPS659102A1RSLR	ACTIVE	VQFN	RSL	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TPS659103A1RSL	PREVIEW	VQFN	RSL	48	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TPS659103A1RSLR	PREVIEW	VQFN	RSL	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TPS659104A1RSL	PREVIEW	VQFN	RSL	48	60	TBD	Call TI	Call TI	
TPS659104A1RSLR	PREVIEW	VQFN	RSL	48	2500	TBD	Call TI	Call TI	
TPS659105A1RSL	PREVIEW	VQFN	RSL	48	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TPS659105A1RSLR	PREVIEW	VQFN	RSL	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TPS659106A1RSL	ACTIVE	VQFN	RSL	48	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TPS659106A1RSLR	ACTIVE	VQFN	RSL	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TPS659107A1RSL	PREVIEW	VQFN	RSL	48	60	TBD	Call TI	Call TI	
TPS659107A1RSLR	PREVIEW	VQFN	RSL	48	2500	TBD	Call TI	Call TI	
TPS659108A1RSL	ACTIVE	VQFN	RSL	48	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TPS659108A1RSLR	ACTIVE	VQFN	RSL	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TPS659109A1RSL	ACTIVE	VQFN	RSL	48	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TPS659109A1RSLR	ACTIVE	VQFN	RSL	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS65910A1RSL	ACTIVE	VQFN	RSL	48	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TPS65910A1RSLR	ACTIVE	VQFN	RSL	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TPS65910AA1RSL	ACTIVE	VQFN	RSL	48	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TPS65910AA1RSLR	ACTIVE	VQFN	RSL	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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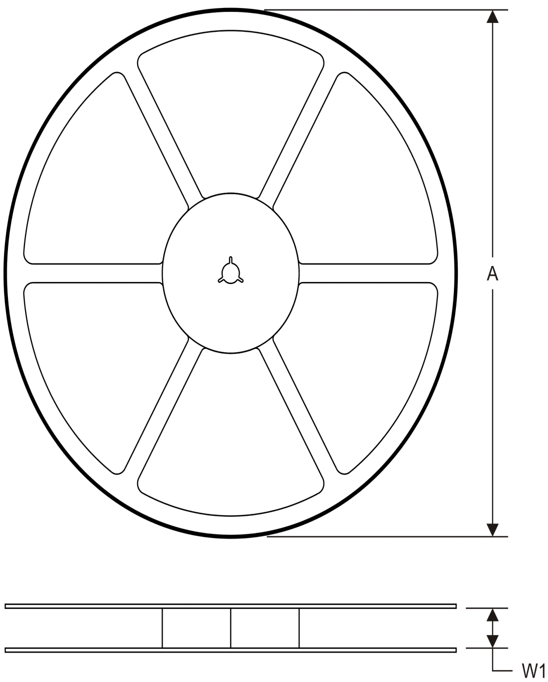
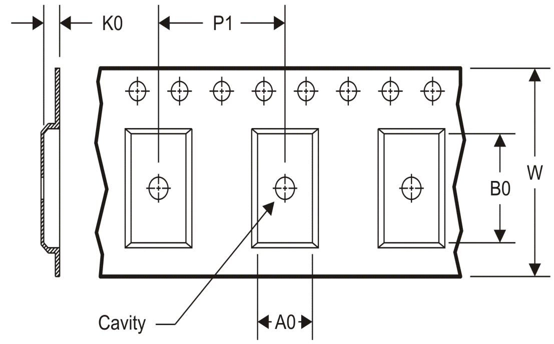
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



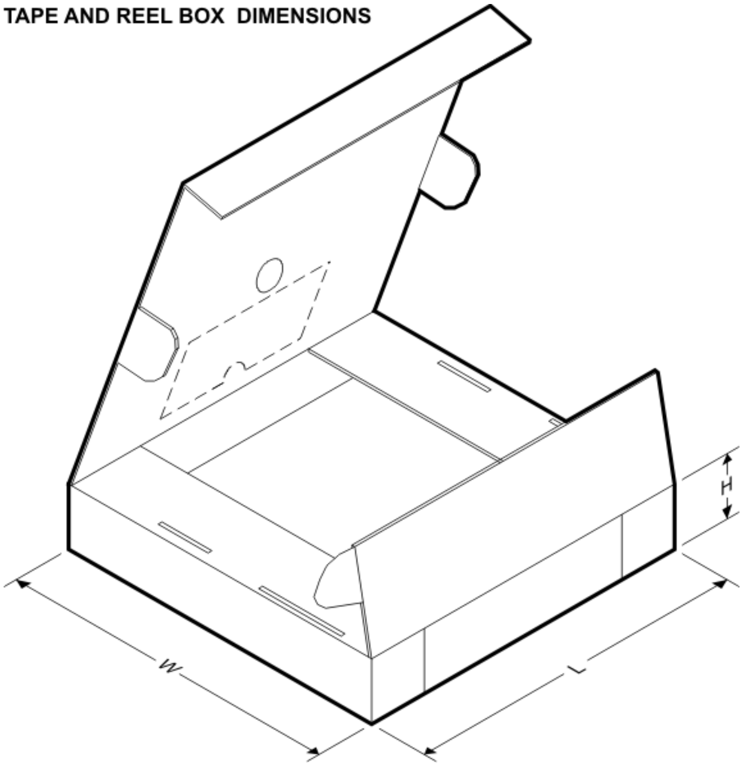
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS659101A1RSLR	VQFN	RSL	48	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS659102A1RSLR	VQFN	RSL	48	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS659106A1RSLR	VQFN	RSL	48	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS659108A1RSLR	VQFN	RSL	48	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65910AA1RSLR	VQFN	RSL	48	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

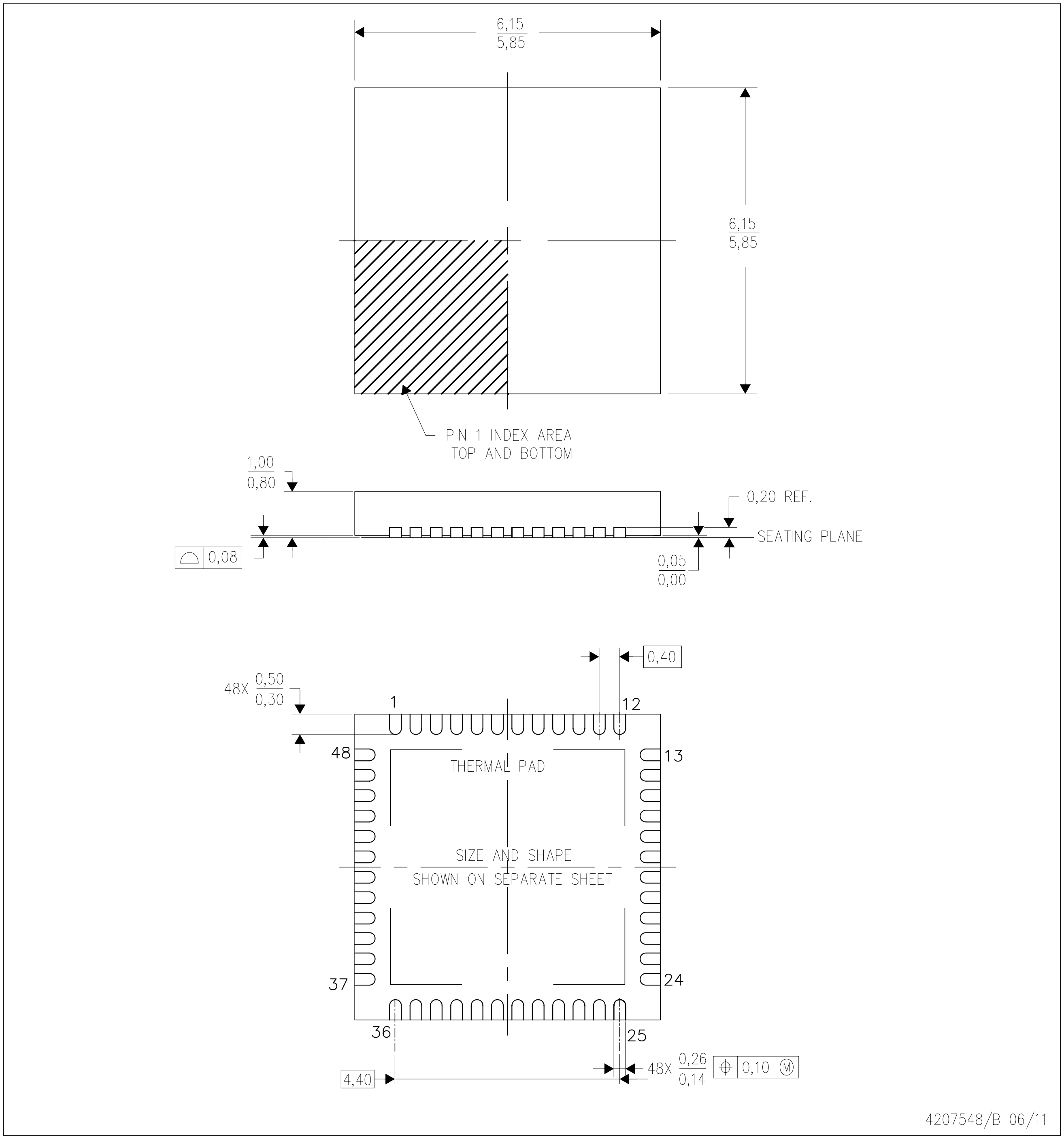
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS659101A1RSLR	VQFN	RSL	48	2500	346.0	346.0	33.0
TPS659102A1RSLR	VQFN	RSL	48	2500	346.0	346.0	33.0
TPS659106A1RSLR	VQFN	RSL	48	2500	346.0	346.0	33.0
TPS659108A1RSLR	VQFN	RSL	48	2500	346.0	346.0	33.0
TPS65910AA1RSLR	VQFN	RSL	48	2500	346.0	346.0	33.0

RSL (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

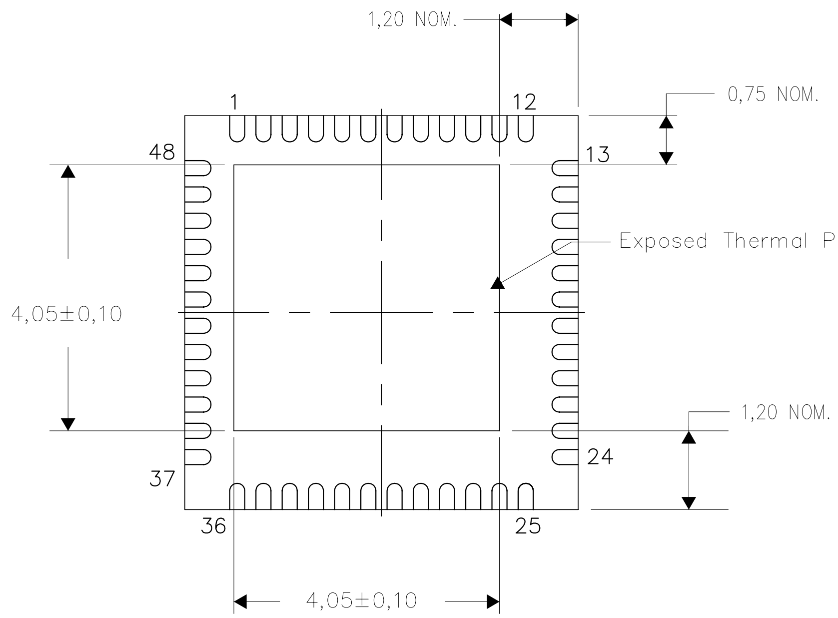
RSL (S-PVQFN-N48) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



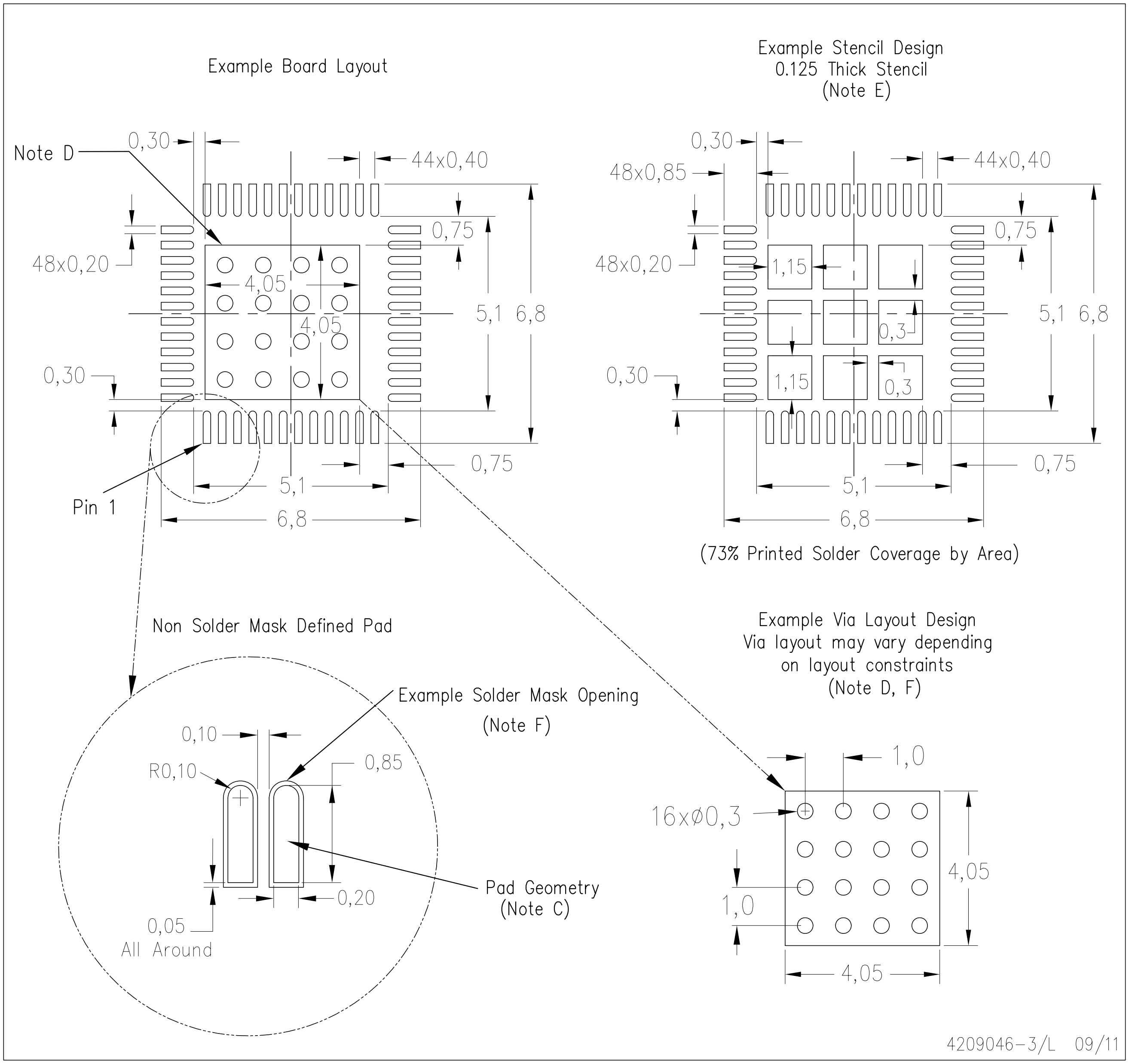
Bottom View

Exposed Thermal Pad Dimensions

4207841-4/N 10/11

NOTE: All linear dimensions are in millimeters

RSL (S-PVQFN-N48) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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