

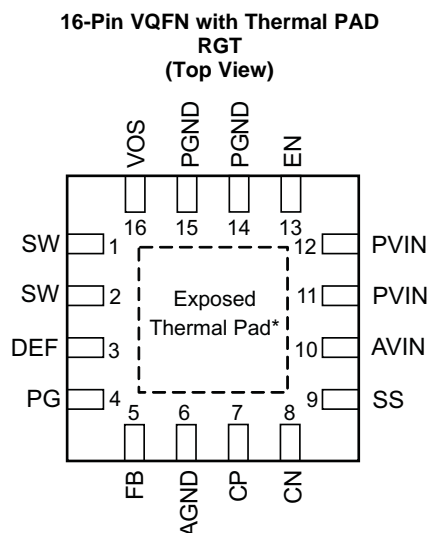
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4 Revision History

DATE	REVISION	NOTES
April 2014	*	Initial release.

5 Pin Configuration and Functions



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
SW	1, 2	Switch pin of the power stage.
DEF	3	This pin is used for internal logic and needs to be pulled high. This pin must be connected to the AVIN pin.
PG	4	Power good open drain output. A pull up resistor can not be connected to any voltage higher than the input voltage.
FB	5	Feedback pin, for regulating the output voltage.
AGND	6	Analog ground.
CP	7	Internal charge pump's flying capacitor. Connect a 10nF capacitor between CP and CN.
CN	8	Internal charge pump's flying capacitor. Connect a 10nF capacitor between CP and CN.
SS	9	Soft-start control pin. A capacitor is connected to this pin and sets the soft startup time. Leaving this pin floating sets the minimum start-up time.
AVIN	10	Analog supply input voltage pin.
PVIN	11,12	Power supply input voltage pin.
EN	13	Enable pin. This pin has an active pull down resistor of typically 400kΩ.
PGND	14,15	Power ground.
VOS	16	Output voltage sense pin. This pin must be directly connected to the output voltage.
Thermal Pad		The exposed thermal pad must be connected to AGND.

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6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾

		MIN	MAX	UNIT
Voltage at pins ⁽²⁾	PVIN, AVIN, FB, SS, EN, DEF, VOS	-0.3	7.0	V
	SW, PG	-0.3	V _{IN} +0.3	
Sink current	PG		1.0	mA
Operating junction temperature		-40	150	°C

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground pin.

6.2 Handling Ratings

		MIN	MAX	UNIT	
T _{stg}	Storage temperature range	-65	150	°C	
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	0	500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommend Operating Conditions

Over operating free-air temperature range, unless otherwise noted.

		MIN	MAX	UNIT
V _{IN}	Input voltage range	2.5	5.5	V
V _{PG}	Power good pull-up resistor voltage		V _{IN}	V
V _{OUT}	Output voltage range	0.8	V _{IN}	V
I _{OUT}	Output current range	0	4.0	A
T _J	Operating junction temperature	-40	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		RGT (16 PINS)	UNIT
R _{θJA}	Junction-to-ambient thermal resistance	47	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	60	
R _{θJB}	Junction-to-board thermal resistance	20	
ψ _{JT}	Junction-to-top characterization parameter	1.5	
ψ _{JB}	Junction-to-board characterization parameter	20	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	5.3	

- (1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, [SPRA953](#)

6.5 Electrical Characteristics

 $V_{IN} = 3.6V$, $T_A = -40^{\circ}C$ to $85^{\circ}C$, typical values are at $T_A = 25^{\circ}C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		2.5		5.5	V
I_{QIN}	Quiescent current	Not switching, No Load, Into PVIN and AVIN		20		μA
I_{sd}	Shutdown current	Into PVIN and AVIN		0.6	5	μA
UVLO	Undervoltage lockout threshold	V_{IN} falling	2.1	2.2	2.3	V
	Undervoltage lockout hysteresis			200		mV
	Thermal shutdown	Temperature rising		150		$^{\circ}C$
	Thermal shutdown hysteresis			20		$^{\circ}C$
CONTROL SIGNAL EN						
V_H	High level input voltage	$V_{IN} = 2.5 V$ to $5.5 V$	1			V
V_L	Low level input voltage	$V_{IN} = 2.5 V$ to $5.5 V$			0.4	V
I_{lkg}	Input leakage current	EN = V_{IN}		10	100	nA
R_{PD}	Pull down resistance	EN = Low		400		k Ω
SOFT STARTUP						
I_{SS}	Softstart current		6.3	7.5	8.7	μA
POWER GOOD						
V_{th}	Power good threshold	Output voltage rising	93%	95%	97%	
		Output voltage falling	88%	90%	92%	
V_L	Low level voltage	$I_{(sink)} = 1 mA$			0.4	V
I_{lkg}	Leakage current	$V_{PG} = 3.6 V$		10	100	nA
POWER SWITCH						
$R_{DS(on)}$	High side FET on-resistance	$I_{SW} = 500 mA$		50		m Ω
	Low side FET on-resistance	$I_{SW} = 500 mA$		40		m Ω
I_{LIM}	High side FET switch current limit		4.7	5.5	6.7	A
f_{SW}	Switching frequency	$I_{OUT} = 3 A$		1.4		MHz
OUTPUT						
V_{OUT}	Output voltage range		0.8		V_{IN}	V
R_{DIS}	Output discharge resistor	EN = GND, $V_{OUT} = 1.8 V$		200		Ω
V_{FB}	Feedback regulation voltage			0.8		V
	Feedback voltage accuracy ⁽¹⁾	$I_{OUT} = 1 A$, PWM mode	-1.4%		+1.4%	
		$I_{OUT} = 1 mA$, PFM mode, $V_{OUT} \geq 1.8 V$	-1.4%		+2.0%	
	$I_{OUT} = 1 mA$, PFM mode, $V_{OUT} < 1.8 V$	-1.4%		+2.5%		
I_{FB}	Feedback input bias current	$V_{FB} = 0.8 V$		10	100	nA
	Line regulation	$V_{OUT} = 1.8 V$, PWM operation		0.016		%/V
	Load regulation	$V_{OUT} = 1.8 V$, PWM operation		0.04		%/A

(1) Conditions: $L = 1 \mu H$, $C_{OUT} = 2 \times 22 \mu F$.

6.6 Typical Characteristics

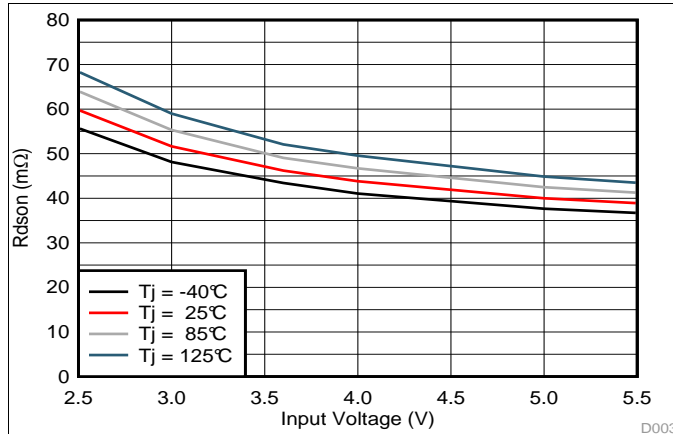


Figure 1. High Side FET On Resistance

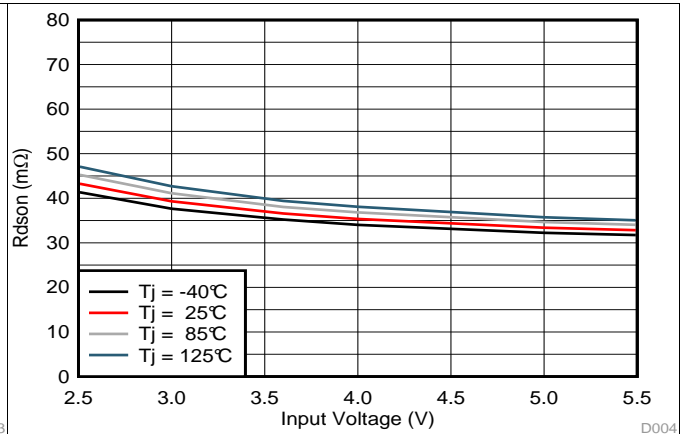


Figure 2. Low Side FET On Resistance

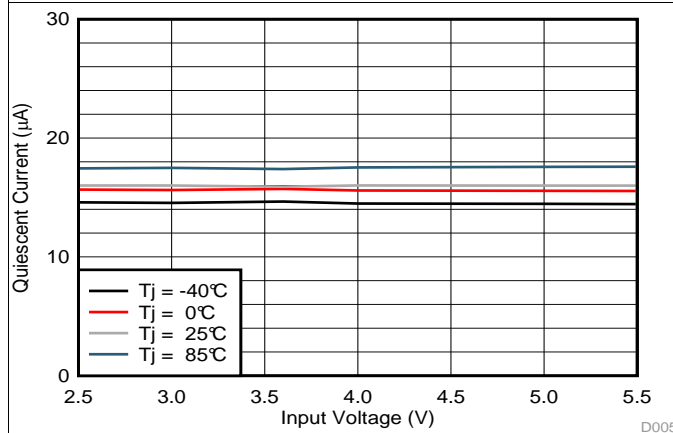


Figure 3. Quiescent Current

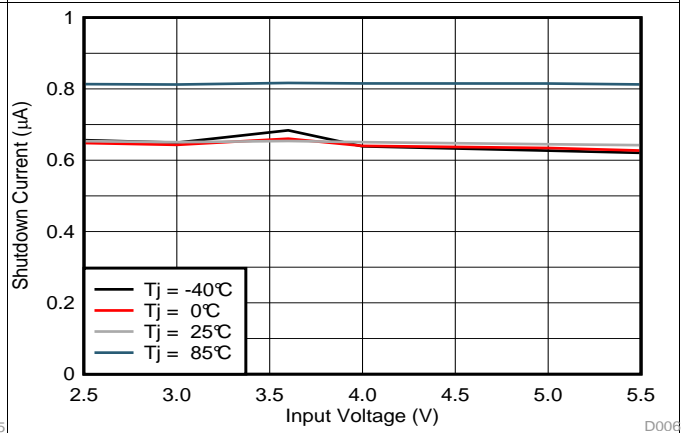


Figure 4. Shutdown Current

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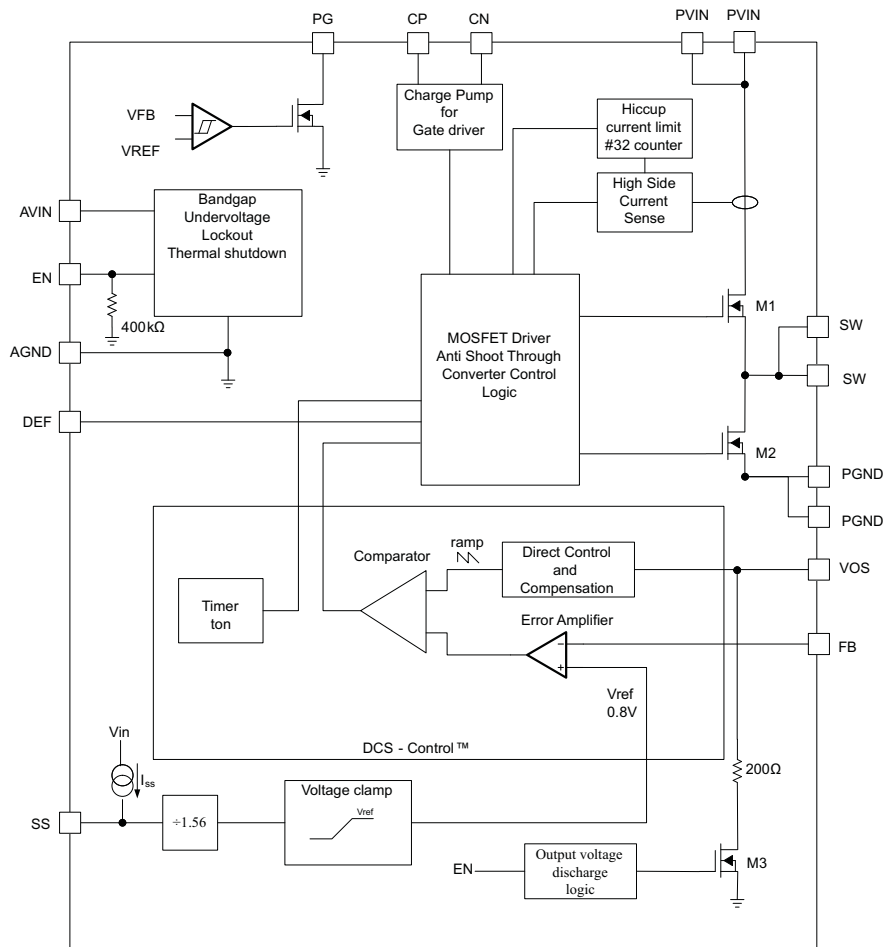
7 Detailed Description

7.1 Overview

The TPS62095 synchronous step down converter is based on DCS-Control™ (Direct Control with Seamless transition into Power Save Mode). This is an advanced regulation topology that combines the advantages of hysteretic and voltage mode control.

The DCS-Control™ topology operates in PWM (Pulse Width Modulation) mode for medium to heavy load conditions and in Power Save Mode at light load currents. In PWM, the converter operates with its nominal switching frequency of 1.4 MHz having a controlled frequency variation over the input voltage range. As the load current decreases, the converter enters Power Save Mode, reducing the switching frequency and minimizing the IC's quiescent current to achieve high efficiency over the entire load current range. DCS-Control™ supports both operation modes using a single building block and therefore has a seamless transition from PWM to Power Save Mode without effects on the output voltage. The TPS62095 offers excellent DC voltage regulation and load transient regulation, combined with low output voltage ripple, minimizing interference with RF circuits.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 PWM Operation

In PWM mode, the device operates with a fixed ON-time switching pulse at medium to heavy load currents. A quasi fixed switching frequency of typical 1.4MHz over the input and output voltage range is achieved by using an input feed forward. The ON-time is calculated as shown in [Equation 2](#). As the load current decreases, the converter enters Power Save Mode operation reducing its switching frequency. The device enters Power Save Mode at the boundary to discontinuous conduction mode (DCM).

7.3.2 Low Dropout Operation (100% Duty Cycle)

The device offers low input to output voltage difference by entering 100% duty cycle mode. In this mode the high side MOSFET switch is constantly turned on. This is particularly useful in battery powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage where the output voltage falls below set point is given by:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT} \times (R_{DS(on)} + R_L) \quad (1)$$

Where

$R_{DS(on)}$ = High side FET on-resistance

R_L = DC resistance of the inductor

$V_{OUT(min)}$ = Minimum output voltage the load can accept

7.3.3 Power Save Mode Operation

As the load current decreases, the converter enters Power Save Mode operation. During Power Save Mode, the converter operates with reduced switching frequency and with a minimum quiescent current to maintain high efficiency. The Power Save Mode is based on a fixed on-time architecture following [Equation 2](#).

$$t_{on} = \frac{V_{OUT}}{V_{IN}} \times 360ns \times 2$$

$$f = \frac{2 \times I_{OUT}}{t_{on}^2 \left(1 + \frac{V_{IN} - V_{OUT}}{V_{OUT}} \right) \times \frac{V_{IN} - V_{OUT}}{L}} \quad (2)$$

In Power Save Mode, the output voltage rises slightly above the nominal output voltage in PWM mode. This effect is reduced by increasing the output capacitance or the inductor value. This effect is also reduced by programming the output voltage of the TPS62095 lower than the target value. As an example, if the target output voltage is 3.3V, then the TPS62095 can be programmed to 3.3V - 0.3%. As a result, the output voltage accuracy is now -1.7% to +1.7% instead of -1.4% to 2%. The output voltage accuracy in PFM operation is reflected in the electrical specification table and given for a 2 x 22µF output capacitance.

7.4 Device Functional Modes

7.4.1 Soft Startup

To minimize inrush current during startup, the device has an adjustable startup time depending on the capacitor value connected to the SS pin. The device charges the SS capacitor with a constant current of typically 7.5µA. The feedback voltage follows this voltage divided by 1.56, until the internal reference voltage of 0.8V is reached. The soft startup operation is completed once the voltage at the SS capacitor has reached typically 1.25V. The soft startup time is calculated using [Equation 3](#). The larger the SS capacitor, the longer the soft startup time. The relation between the SS pin voltage and the FB pin voltage is estimated using [Equation 4](#). Leaving the SS pin floating sets the minimum startup time.

$$t_{SS} = C_{SS} \times \frac{1.25V}{7.5\mu A} \quad (3)$$

$$V_{FB} = \frac{V_{SS}}{1.56} \quad (4)$$

Device Functional Modes (continued)

During startup the switch current limit is reduced to 1/3 of its typical current limit of 5.5A when the output voltage is less than 0.6V. Once the output voltage exceeds typically 0.6V, the switch current limit is released to its nominal value. Thus, the device provides a reduced load current of 1.8A when the output voltage is below 0.6V. A small or no soft startup time may trigger this reduced switch current limit during startup, especially for larger output capacitor applications. This is avoided by using a larger soft start up capacitance which extends the soft startup time. See Short Circuit Protection (Hiccup-Mode) for details of the reduced current limit during startup.

7.4.2 Voltage Tracking

The SS pin can also be used to implement output voltage tracking with other supply rails, as shown in Figure 5.

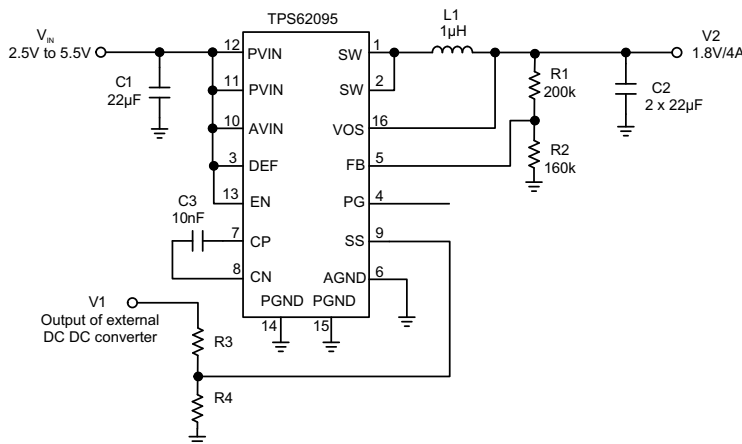


Figure 5. Output Voltage Tracking

In voltage tracking applications, the resistance R4 should be set properly to achieve accurate voltage tracking by taking 7.5µA soft startup current into account. 4.3kΩ is a sufficient value for R4. The relationship between V1 and V2 is shown in Equation 5. To achieve V1 startup leading V2, as shown in Figure 6, Equation 5 should be less than 1. To achieve simultaneous tracking, Equation 5 should equal to 1.

$$\frac{V2}{V1} = \frac{1}{1.56} \times \frac{R4}{R3 + R4} \times \frac{R1 + R2}{R2} \tag{5}$$

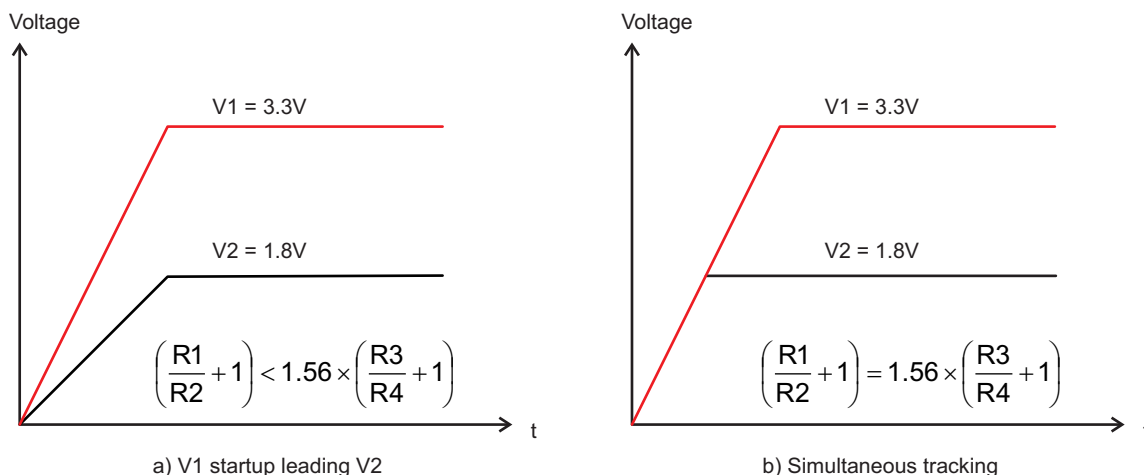


Figure 6. Voltage Tracking Applications

Device Functional Modes (continued)

7.4.3 Short Circuit Protection (Hiccup-Mode)

The device is protected against hard short circuits to GND and over-current events. This is implemented by a two level short circuit protection. During start-up and when the output is shorted to GND, the switch current limit is reduced to 1/3 of its typical current limit of 5.5A. Once the output voltage exceeds typically 0.6V the current limit is released to its nominal value. The full current limit is implemented as a hiccup current limit. Once the internal current limit is triggered 32 times, the device stops switching and starts a new start-up sequence after a typical delay time of 66 μ S passed by. The device repeats these cycles until the high current condition is released.

7.4.4 Output Discharge Function

To make sure the device starts up under defined conditions, the output gets discharged via the VOS pin with a typical discharge resistor of 200 Ω whenever the device shuts down. This happens when the device is disabled or if thermal shutdown, undervoltage lockout or short circuit hiccup-mode is triggered.

7.4.5 Power Good Output

The power good output is low when the output voltage is below its nominal value. The power good becomes high impedance once the output is within 5% of regulation. The PG pin is an open drain output and is specified to sink up to 1mA. This output requires a pull-up resistor to be monitored properly. The pull-up resistor cannot be connected to any voltage higher than the input voltage of the device.

7.4.6 Undervoltage Lockout

To avoid mis-operation of the device at low input voltages, an undervoltage lockout is included. UVLO shuts down the device at input voltages lower than typically 2.2V with a 200mV hysteresis.

7.4.7 Thermal Shutdown

The device goes into thermal shutdown once the junction temperature exceeds typically 150°C with a 20°C hysteresis.

8 Application and Implementation

8.1 Application Information

The TPS62095 is a synchronous step down converter based on DCS-Control™ topology whose output voltage can be adjusted by component selection. The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

8.2 Typical Applications

8.2.1 2.5V to 5.5V Input, 1.8V Output Converter

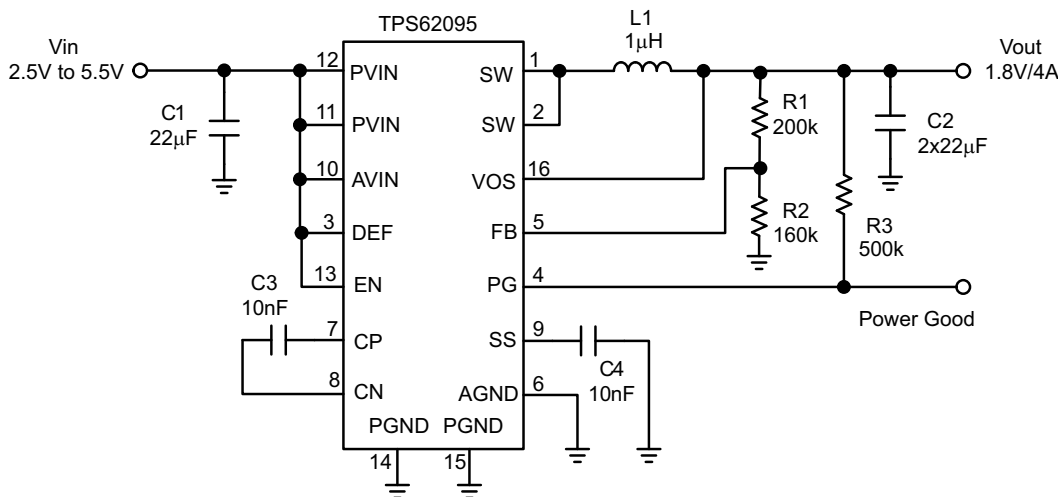


Figure 7. 1.8-V Output Application

8.2.1.1 Design Requirements

For this design example, use the following as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.5V to 5.5V
Output voltage	1.8V
Output ripple voltage	<20mV
Output current rating	4A

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Output Filter

The first step is the selection of the output filter components. To simplify this process, [Table 2](#) outlines possible inductor and capacitor value combinations.

Table 2. Output Filter Selection

INDUCTOR VALUE [μH] ⁽¹⁾	OUTPUT CAPACITOR VALUE [μF] ⁽²⁾				
	10	22	2 x 22	100	150
0.47			√	√	√
1.0			√ ⁽³⁾	√	√
2.2					

- (1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and –30%.
 (2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by +20% and –50%.
 (3) Typical application configuration. Other check mark indicates alternative filter combinations

8.2.1.2.2 Inductor Selection

The inductor selection is affected by several parameters like inductor ripple current, output voltage ripple, transition point into Power Save Mode, and efficiency. See [Table 3](#) for typical inductors.

Table 3. Inductor Selection⁽¹⁾

INDUCTOR VALUE	COMPONENT SUPPLIER	SIZE (LxWxH mm)	Isat / DCR
1 μH	Coilcraft XAL4020-102	4.0 x 4.0 x 2.1	8.75A / 13.2 m Ω
0.47 μH	TOKO DFE322512C	3.2 x 2.5 x 1.2	5.9A / 21 m Ω

(1) See [Third-Party Products Disclaimer](#).

In addition, the inductor has to be rated for the appropriate saturation current and DC resistance (DCR). The inductor needs to be rated for a saturation current as high as the typical switch current limit of 5.5A or according to [Equation 6](#) and [Equation 7](#). [Equation 6](#) and [Equation 7](#) calculate the maximum inductor current under static load conditions. The formula takes the converter efficiency into account. The converter efficiency can be taken from the data sheet graphs or 80% can be used as a conservative approach. The calculation must be done for the maximum input voltage where the peak switch current is highest.

$$I_L = I_{\text{OUT}} + \frac{\Delta I_L}{2} \quad (6)$$

$$I_L = I_{\text{OUT}} + \frac{\frac{V_{\text{OUT}}}{\eta} \times \left(1 - \frac{V_{\text{OUT}}}{V_{\text{IN}} \times \eta}\right)}{2 \times f \times L} \quad (7)$$

where

f = Converter switching frequency (typically 1.4MHz)

L = Inductor value

η = Estimated converter efficiency (use the number from the efficiency curves or 0.80 as a conservative assumption)

Note: The calculation must be done for the maximum input voltage of the application

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current. A margin of 20% should be added to cover for load transients during operation.

8.2.1.2.3 Input and Output Capacitor Selection

For best output and input voltage filtering, low ESR ceramic capacitors are recommended. The input capacitor minimizes input voltage ripple, suppresses input voltage spikes and provides a stable system rail for the device. A 22 μ F or larger input capacitor is required. The output capacitor value can range from 2x22 μ F up to 150 μ F. The recommended typical output capacitor value is 2x22 μ F and can vary over a wide range as outline in the output filter selection table.

8.2.1.2.4 Setting the Output Voltage

The output voltage is set by an external resistor divider according to the following equations:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2} \right) = 0.8 \text{ V} \times \left(1 + \frac{R1}{R2} \right) \quad (8)$$

$$R2 = \frac{V_{FB}}{I_{FB}} = \frac{0.8 \text{ V}}{5 \mu\text{A}} \approx 160 \text{ k}\Omega \quad (9)$$

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) = R2 \times \left(\frac{V_{OUT}}{0.8\text{V}} - 1 \right) \quad (10)$$

When sizing R2, in order to achieve low quiescent current and acceptable noise sensitivity, use a minimum of 5 μ A for the feedback current I_{FB} . Larger currents through R2 improve noise sensitivity and output voltage accuracy.

8.2.1.3 Application Performance Curves

$T_A = 25^\circ\text{C}$, $V_{IN} = 3.6\text{V}$, $V_{OUT} = 1.8\text{V}$, $L1 = 1\mu\text{H}$ (XAL4020-102), $C2 = 2 \times 22\mu\text{F}$, unless otherwise noted.

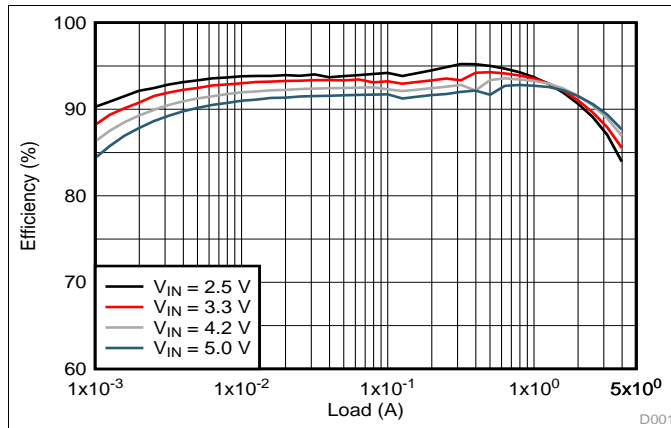


Figure 8. Efficiency, $V_{OUT} = 1.8\text{V}$

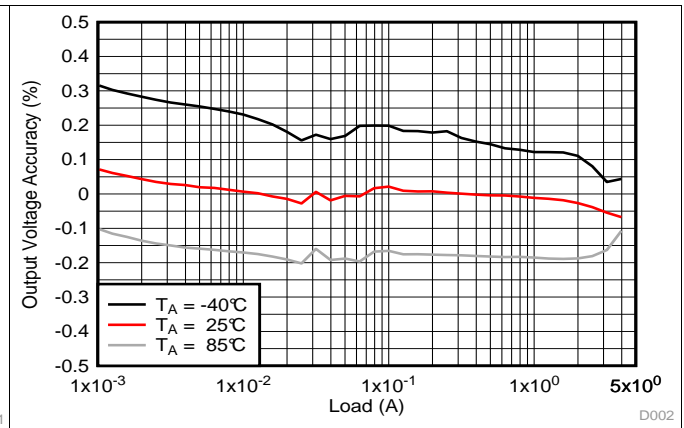


Figure 9. Load Regulation, $V_{OUT} = 1.8\text{V}$, $V_{IN} = 3.3\text{V}$

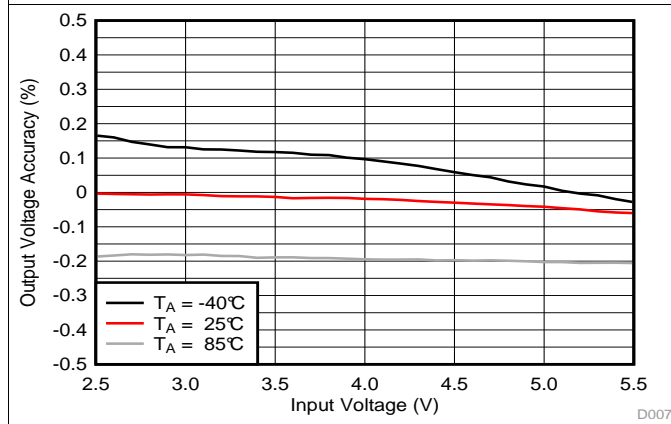


Figure 10. Line Regulation, $V_{OUT} = 1.8\text{V}$, $I_{OUT} = 1.0\text{A}$

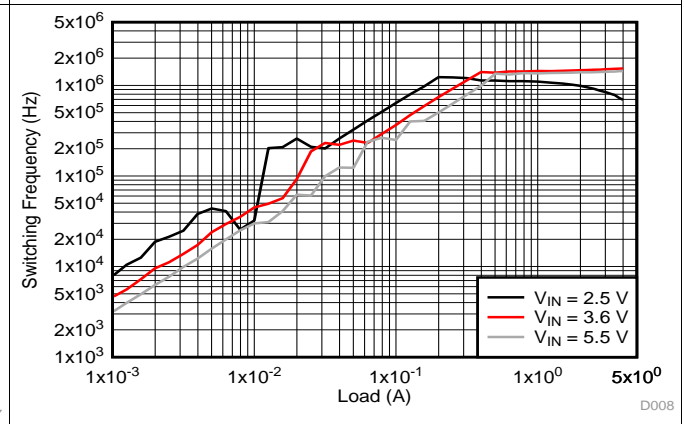


Figure 11. Switching Frequency, $V_{OUT} = 1.8\text{V}$

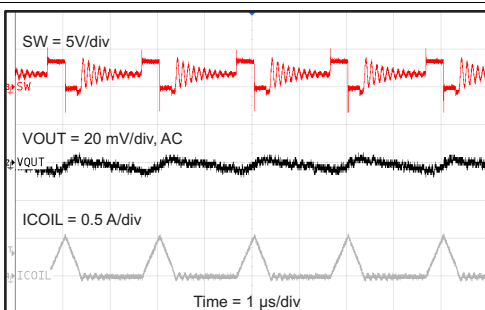


Figure 12. Output Ripple, $V_{OUT} = 1.8\text{V}$, $I_{OUT} = 100\text{mA}$

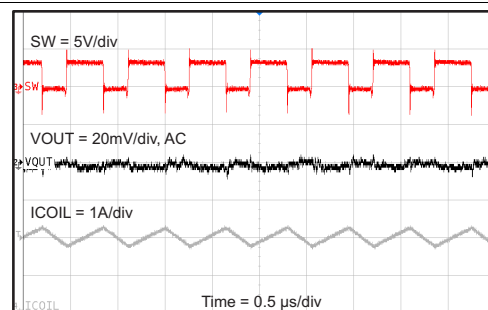


Figure 13. Output Ripple, $V_{OUT} = 1.8\text{V}$, $I_{OUT} = 3.5\text{A}$

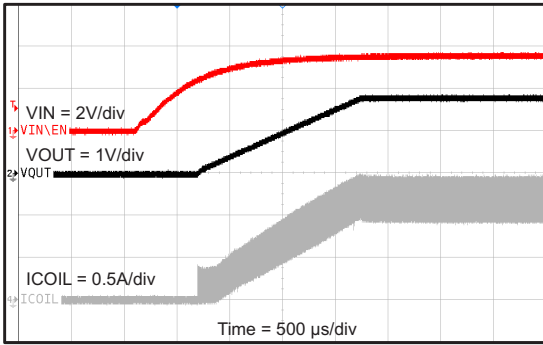


Figure 14. Startup, Relative to V_{IN} , $R_{LOAD} = 1.5\Omega$

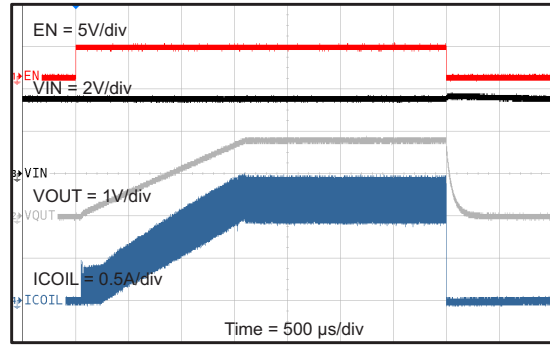


Figure 15. Startup, Relative to EN, $R_{LOAD} = 1.5\Omega$

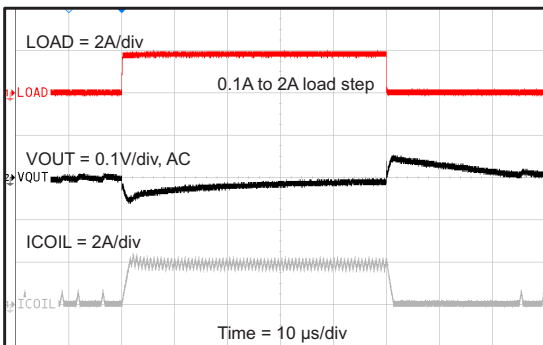


Figure 16. Load Transient, $V_{OUT} = 1.8V$

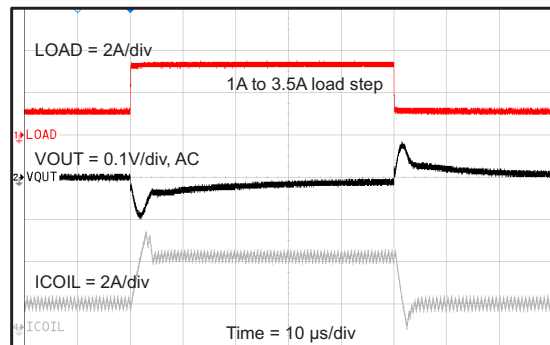


Figure 17. Load Transient, $V_{OUT} = 1.8V$

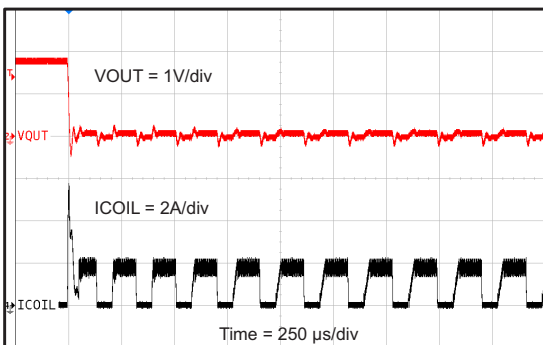


Figure 18. Short Circuit, HICCUP Protection Entry

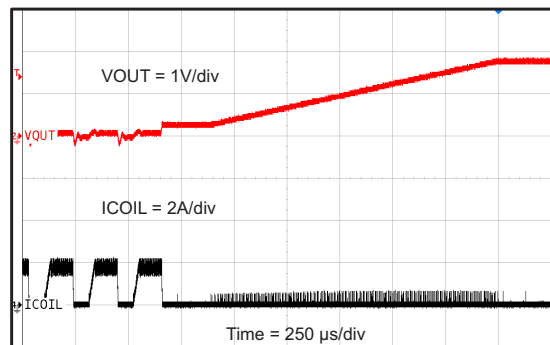
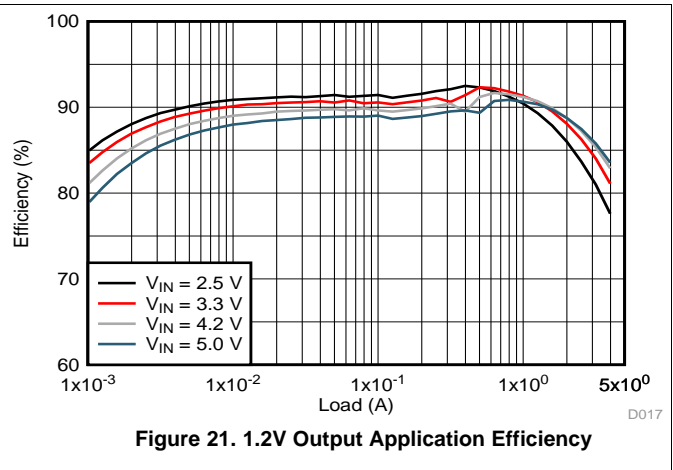
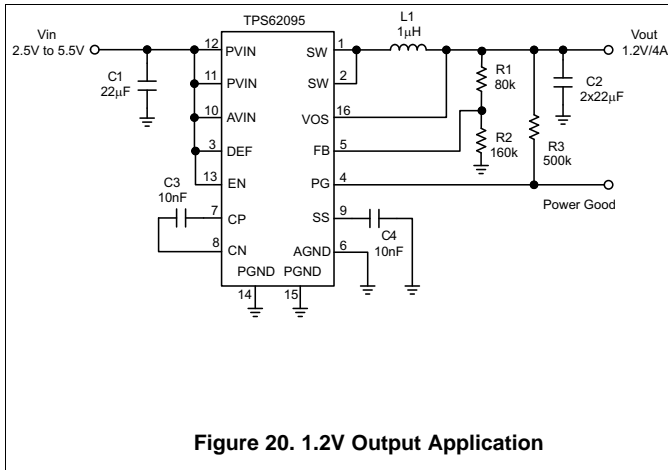
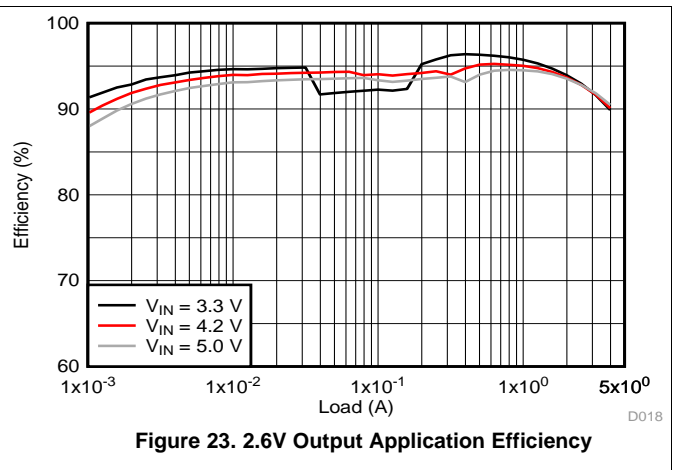
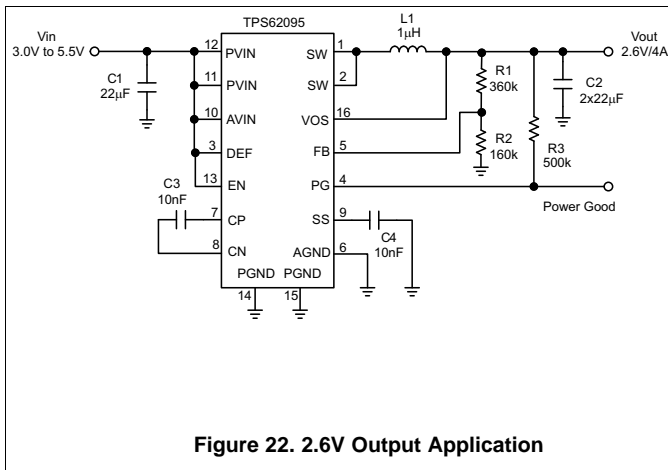


Figure 19. Short Circuit, HICCUP Protection Exit

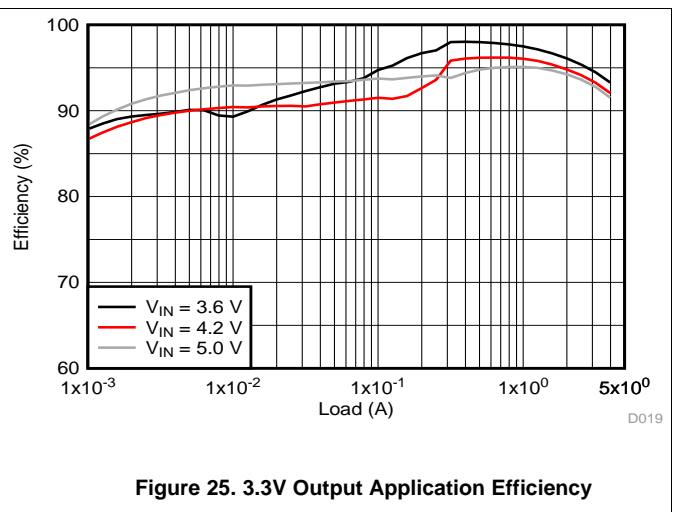
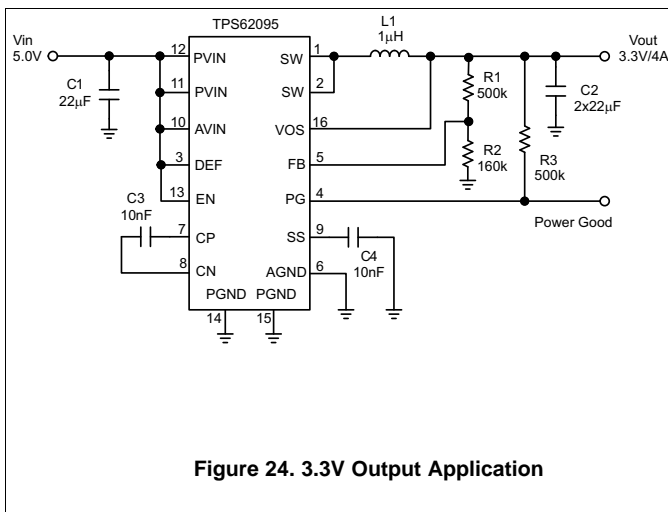
8.2.2 2.5V to 5.5V Input, 1.2V Output Converter



8.2.3 3.0V to 5.5V Input, 2.6V Output Converter



8.2.4 5V Input, 3.3V Output Converter



PRODUCT PREVIEW

9 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 2.5V and 5.5V. If the input supply is located more than a few inches from the device, an additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47μF is a typical choice.

The average input current of the TPS62095 is calculated as:

$$I_{IN} = \frac{1}{\eta} \times \frac{V_{OUT} \times I_{OUT}}{V_{IN}} \quad (11)$$

10 Layout

10.1 Layout Guidelines

- It is recommended to place all components as close as possible to the IC. Specially, the input capacitor placement is closest to the PVIN and PGND pins of the device.
- Use wide and short traces for the main current paths to reduce the parasitic inductance and resistance, like the SW node.
- The VOS pin is noise sensitive and needs to be routed as short and directly to the output pin of the inductor and the output capacitor. This minimizes switch node jitter.
- The exposed thermal pad of the package, the AGND and the PGND should have a single joint connection at the exposed thermal pad of the package. To enhance heat dissipation of the device, the exposed thermal pad should be connected to bottom or internal layer ground planes using vias.
- The charge pump capacitor connected to CP and CN should be placed close to the IC to minimize coupling of switching waveforms into other traces and circuits.
- The capacitor on the SS pin and the FB resistors divider network should be placed close to the IC and connected directly to those pins and the AGND pin.
- Refer to [Figure 26](#) for an example of component placement, routing and thermal design.

10.2 Layout Example

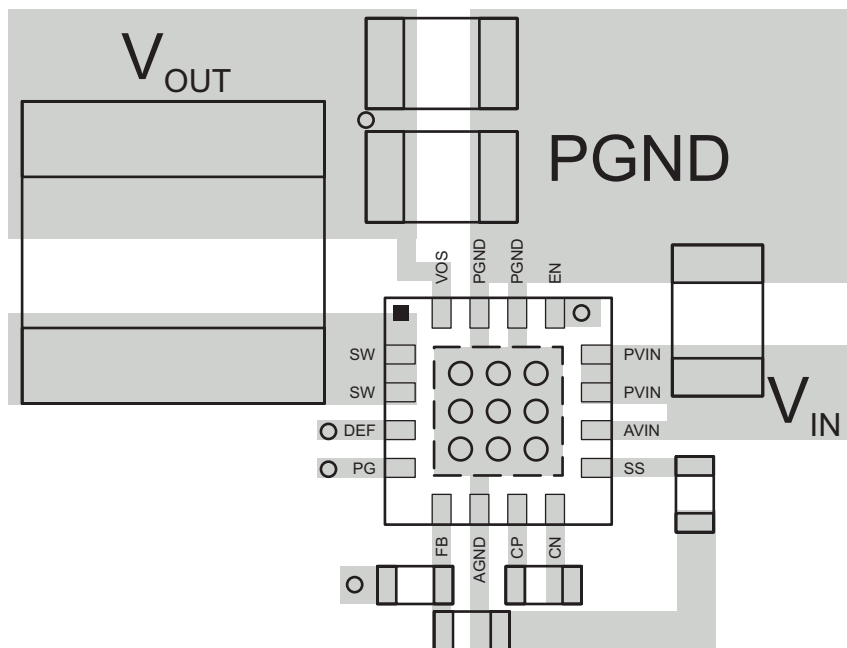


Figure 26. TPS62095 PCB Layout

10.3 Thermal Consideration

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component. The Thermal Information table provides the thermal metric of the device and its package based on JEDEC standard. For more details on how to use the thermal parameters in real applications, see the application notes: [SZZA017](#) and [SPRA953](#).

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Trademarks

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11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62095RGTR	PREVIEW	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85		
TPS62095RGTT	PREVIEW	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

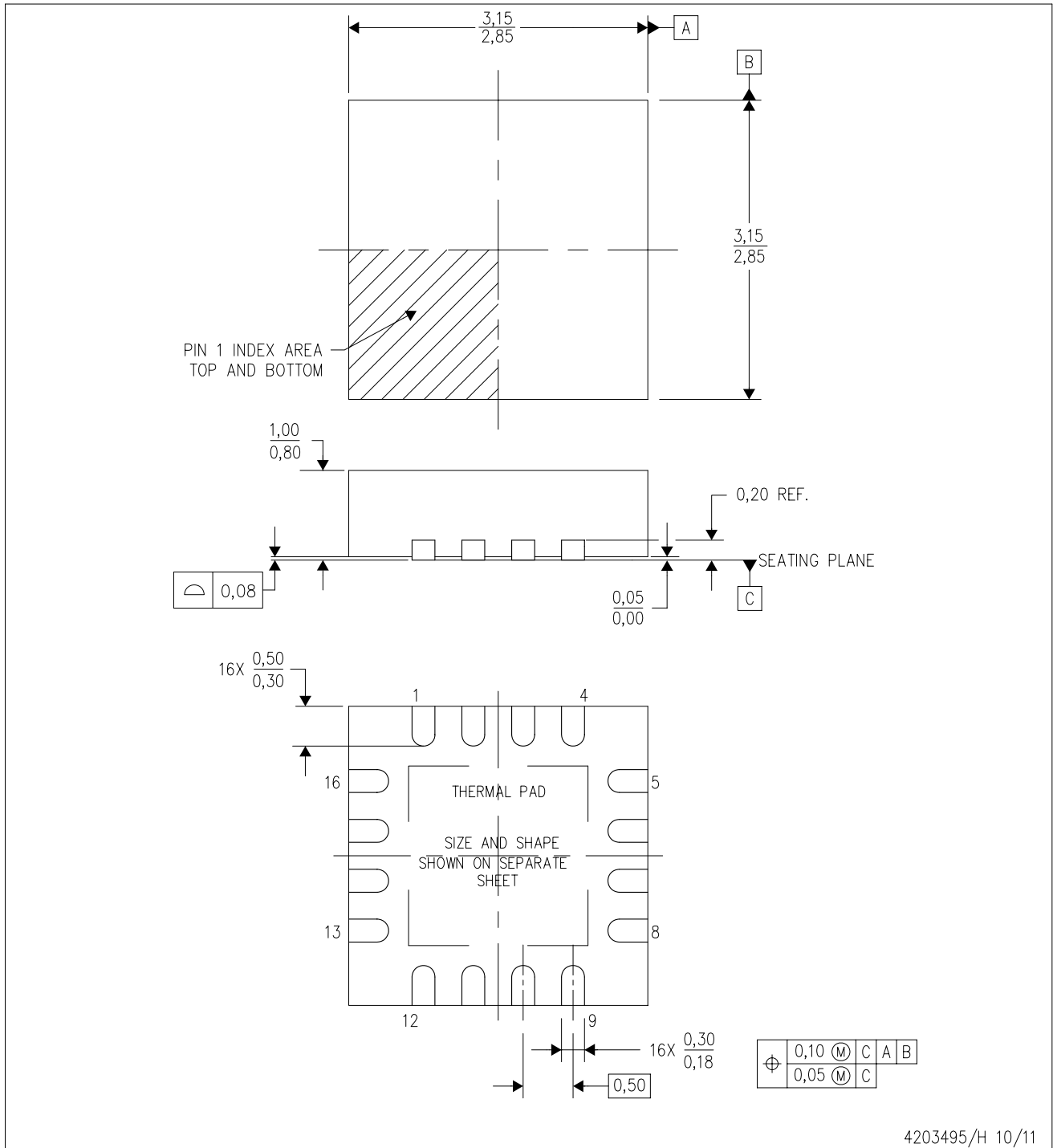
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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RGT (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203495/H 10/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Quad Flatpack, No-leads (QFN) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-220.

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