

## 3.3-V/5-V Input, 6-A, D-CAP+™ Mode Synchronous Step-Down Integrated FETs Converter

 Check for Samples: [TPS53317](#)

### FEATURES

- TI proprietary Integrated MOSFET and Packaging Technology
- External Tracking
- Minimum External Components Count
- 1-V to 6-V Conversion Voltage
- D-CAP+™ Mode Architecture
- Supports All MLCC Output Capacitors and SP/POSCAP
- Selectable SKIP Mode or Forced CCM
- Optimized Efficiency at Light and Heavy Loads
- Selectable 600-kHz or 1-MHz Switching Frequency
- Selectable Overcurrent Limit (OCL)
- Overvoltage Protection
- Hiccup Undervoltage Protection
- Thermal Shutdown
- Adjustable Output Voltage Ranging Between 0.6 V and 2 V
- 3.5 mm × 4 mm, 20-Pin QFN Package

### APPLICATIONS

- VTT Termination
- Low-Voltage Applications for 1-V to 6-V Input Rails

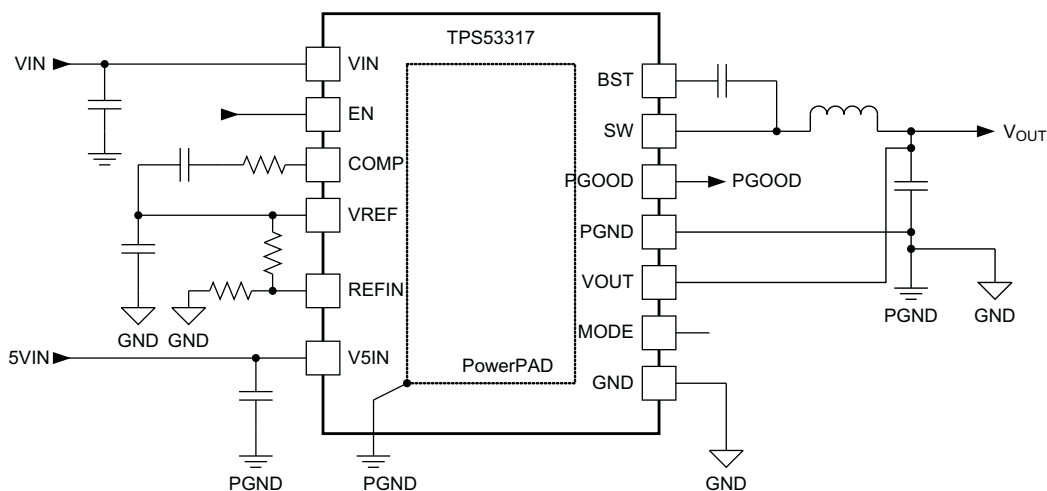
### DESCRIPTION

The TPS53317 is a fully-integrated, synchronous buck regulator employing D-CAP+™ technology. It is used for 1-V to 6-V input rails where space is a consideration, and an optimized component count is required.

The TPS53317 features two switching frequency settings (600 kHz and 1 MHz), synchronous operation in skip mode, integrated droop support, external tracking support, pre-bias startup, output soft discharge, integrated bootstrap switch, power good function, EN/Input UVLO protection, and both output ceramic and SP/POS/AL capacitor support. It supports supply and conversion voltages up to 6.0 V, and output voltages adjustable from 0.6 V to 2.0 V. It also provides external tracking support.

The TPS53317 is available in the 3.5 mm by 4 mm, 20-pin QFN package (Green RoHs compliant and Pb free) with TI proprietary Integrated MOSFET and packaging technology and is specified from -40°C to 85°C.

### Simplified Application



UDG-11105



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

D-CAP+ is a trademark of Texas Instruments.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### ORDERING INFORMATION<sup>(1)</sup>

T <sub>A</sub>	PACKAGE <sup>(2)</sup>	ORDERING NUMBER	PINS	OUTPUT SUPPLY	MINIMUM QUANTITY	ECO PLAN
-40°C to 85°C	Plastic QFN (RGB)	TPS53317RGBR	20	Tape and reel	3000	Green (RoHS and no Pb/Br)
		TPS53317RGBT	20	Mini reel	250	

- (1) For the most current package and ordering information, see the *Package Option Addendum* at the end of this document, or visit the TI website at [www.ti.com](http://www.ti.com).  
 (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

### THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		TPS53317	UNITS
		RGB	
		20 PINS	
$\theta_{JA}$	Junction-to-ambient thermal resistance <sup>(2)</sup>	35.5	°C/W
$\theta_{JcTop}$	Junction-to-case (top) thermal resistance <sup>(3)</sup>	39.6	
$\theta_{JB}$	Junction-to-board thermal resistance <sup>(4)</sup>	12.4	
$\psi_{JT}$	Junction-to-top characterization parameter <sup>(5)</sup>	0.5	
$\psi_{JB}$	Junction-to-board characterization parameter <sup>(6)</sup>	12.5	
$\theta_{JcBot}$	Junction-to-case (bottom) thermal resistance <sup>(7)</sup>	3.7	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](http://SPRA953).  
 (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.  
 (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.  
 (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.  
 (5) The junction-to-top characterization parameter,  $\psi_{JT}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).  
 (6) The junction-to-board characterization parameter,  $\psi_{JB}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).  
 (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Input voltage range	VIN, V5IN, BST (with respect to SW)	-0.3	7.0	V
	BST	-0.3	14.0	
	SW	-2	7	
	EN	-0.3	7	
	MODE, REFIN	-0.3	3.6	
	VOUT	-1	3.6	
Output voltage range	COMP, VREF	-0.3	3.6	V
	PGOOD	-0.3	7.0	
	PGND	-0.3	0.3	
Junction temperature	T <sub>J</sub>	-40	150	
Storage temperature	T <sub>stg</sub>	-55	150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			300	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS**

		VALUE			UNIT
		MIN	TYP	MAX	
Input voltage range	VIN, EN, BST (with respect fo SW)	-0.1		6.5	V
	V5IN	4.5		6.5	
	BST	-0.1		13.5	
	SW	-1.0		6.5	
	VOUT, MODE, REFIN	-0.1		3.5	
Output voltage range	COMP, VREF	-0.1		3.5	V
	PGOOD	-0.1		6.5	
	PGND	-0.1		0.1	
Operating temperature range, T <sub>A</sub>		-40		85	°C

## ELECTRICAL CHARACTERISTICS

over recommended free-air temperature range,  $V_{V5IN} = 5.0\text{ V}$ , PGND = GND (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY: VOLTAGE, CURRENTS AND 5 V UVLO</b>						
$I_{VINSD}$	VIN shutdown current	EN = 'LO'		0.02	5	$\mu\text{A}$
$V_{5VIN}$	5VIN supply voltage	V5IN voltage range	4.5	5.0	6.5	V
$I_{5VIN}$	5VIN supply current	EN = 'HI', V5IN supply current		1.1	2	mA
$I_{5VINSD}$	5VIN shutdown current	EN = 'LO', V5IN shutdown current		0.2	7.0	$\mu\text{A}$
$V_{V5UVLO}$	V5IN UVLO	Ramp up; EN = 'HI'	4.20	4.37	4.50	V
$V_{V5UVHYS}$	V5IN UVLO hysteresis	Falling hysteresis		440		mV
$V_{VREFUVLO}$	REF UVLO <sup>(1)</sup>	Rising edge of VREF, EN = 'HI'		1.8		V
$V_{VREFUVHYS}$	REF UVLO hysteresis <sup>(1)</sup>			100		mV
$V_{POR5VFILT}$	Reset	OVP latch is reset by V5IN falling below the reset threshold	1.5	2.3	3.1	V
<b>VOLTAGE FEEDBACK LOOP: VREF, VOUT, AND VOLTAGE GM AMPLIFIER</b>						
$V_{OUTTOL}$	VOUT accuracy	$V_{REFIN} = 1\text{ V}$ , No droop	-1%	0%	1%	
$V_{VREF}$	VREF	$I_{VREF} = 0\ \mu\text{A}$	1.98	2.00	2.02	V
		$I_{VREF} = 50\ \mu\text{A}$	1.975	2.000	2.025	
$I_{REFSNK}$	VREF sink current	$V_{VREF} = 2.05\text{ V}$		2.5		mA
$G_M$	Transconductance			1.00		mS
$V_{CM}$	Common mode input voltage range <sup>(1)</sup>		0		2	V
$V_{DM}$	Differential mode input voltage		0		80	mV
$I_{COMPSNK}$	COMP pin maximum sinking current	$V_{COMP} = 2\text{ V}$ , $(V_{REFIN} - V_{OUT}) = 80\text{ mV}$		80		$\mu\text{A}$
$I_{COMPSRC}$	COMP pin maximum sourcing current	$V_{COMP} = 2\text{ V}$		-80		$\mu\text{A}$
$V_{OFFSET}$	Input offset voltage	$T_A = 25^\circ\text{C}$		0		mV
$R_{DSCH}$	Output voltage discharge resistance			42		$\Omega$
$f_{-3dBVL}$	-3dB Frequency <sup>(1)</sup>		4.5	6.0	7.5	MHz
<b>CURRENT SENSE: CURRENT SENSE AMPLIFIER, OVERCURRENT AND ZERO CROSSING</b>						
$A_{CSINT}$	Internal current sense gain	Gain from the current of the low-side FET to PWM comparator when PWM = "OFF"	43	53	57	mV/A
$I_{OCL}$	Positive overcurrent limit (valley)			7.6		A
$I_{OCL(neg)}$	Negative overcurrent limit (valley)			-9.3		A
$V_{ZXOFF}$	Zero crossing comp internal offset			0		mV
<b>PROTECTION: OVP, UVP, PGOOD, and THERMAL SHUTDOWN</b>						
$V_{PGDLL}$	PGOOD deassert to lower (PGOOD $\rightarrow$ Low)	Measured at the VOUT pin wrt/ $V_{REFIN}$		84%		
$V_{PGHSHL}$	PGOOD high hysteresis			8%		
$V_{PGDLH}$	PGOOD de-assert to higher (PGOOD $\rightarrow$ Low)	Measured at the VOUT pin wrt/ $V_{REFIN}$		116%		
$V_{PGHSHH}$	PGOOD high hysteresis			-8%		
$V_{INMINPG}$	Minimum VIN voltage for valid PGOOD	Measured at the VIN pin with a 2-mA sink current on PGOOD pin	0.9	1.3	1.5	V
$V_{OVP}$	OVP threshold	Measured at the VOUT pin wrt/ $V_{REFIN}$	117%	120%	123%	
$V_{UVP}$	UVP threshold	Measured at the VOUT pin wrt/ $V_{REFIN}$ , device latches OFF, begins soft-stop	65%	68%	71%	
$TH_{SD}$	Thermal shutdown <sup>(1)</sup>	Latch off controller, attempt soft-stop.		145		$^\circ\text{C}$
$TH_{SD(hys)}$	Thermal Shutdown hysteresis <sup>(1)</sup>	Controller re-starts after temperature has dropped		10		$^\circ\text{C}$

(1) Ensured by design, not production tested.

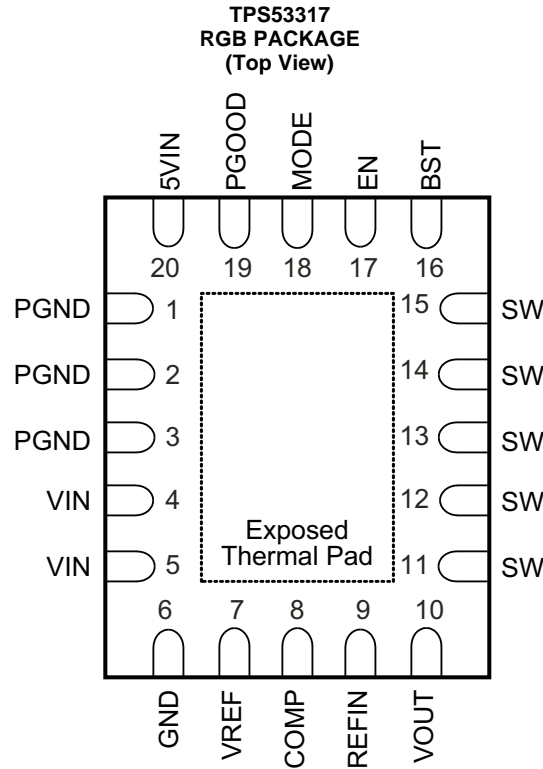
**ELECTRICAL CHARACTERISTICS (continued)**

over recommended free-air temperature range,  $V_{V5IN} = 5.0\text{ V}$ ,  $PGND = GND$  (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
<b>DRIVERS: BOOT STRAP SWITCH</b>						
$R_{DS(on)BST}$	Internal BST switch on-resistance	$I_{BST} = 10\text{ mA}$ , $T_A = 25^\circ\text{C}$			10	$\Omega$
$I_{BSTLK}$	Internal BST switch leakage current	$V_{BST} = 14\text{ V}$ , $V_{SW} = 7\text{ V}$			1	$\mu\text{A}$
<b>TIMERS: ON-TIME, MINIMUM OFF-TIME, SS, AND I/O TIMINGS</b>						
$t_{ONESHOTC}$	PWM one-shot <sup>(2)</sup>	$V_{VIN} = 5\text{ V}$ , $V_{VOUT} = 1.05\text{ V}$ , $f_{SW} = 1\text{ MHz}$		210		ns
		$V_{VIN} = 5\text{ V}$ , $V_{VOUT} = 1.05\text{ V}$ , $f_{SW} = 600\text{ kHz}$		310		
$t_{MIN(off)}$	Minimum OFF time	$V_{VIN} = 5\text{ V}$ , $V_{VOUT} = 1.05\text{ V}$ , $f_{SW} = 1\text{ MHz}$ , DRVL on, SW = PGND, $V_{VOUT} < V_{REFIN}$		270		ns
$t_{INT(SS)}$	Soft-start time	From EN = HI to VOUT =95%, default setting		1.6		ms
$t_{INT(SSDLY)}$	Internal soft-start delay time	From EN = HI to VOUT ramp starts		260		$\mu\text{s}$
$t_{PGDLY}$	PGOOD startup delay time	External tracking		8		ms
$t_{PGDPDLYH}$	PGOOD high propagation delay time	50 mV over drive, rising edge	0.8	1	1.2	ms
$t_{PGDPDLYL}$	PGOOD low propagation delay time	50 mV over drive, falling edge		10		$\mu\text{s}$
$t_{OVPDLY}$	OVP delay time	Time from the VOUT pin out of +20% of REFIN to OVP fault		10		$\mu\text{s}$
$t_{UVLDYEN}$	Undervoltage fault enable delay	Time from EN_INT going high to undervoltage fault is ready		2		ms
		External tracking from VOUT ramp starts		8		
$t_{UVPDLY}$	UVP delay time	Time from the VOUT pin out of -30% of REFIN to UVP fault		256		$\mu\text{s}$
<b>LOGIC PINS: I/O VOLTAGE AND CURRENT</b>						
$V_{PGDPD}$	PGOOD pull-down voltage	PGOOD low impedance, $I_{SINK} = 4\text{ mA}$ , $V_{V5IN} = 4.5\text{ V}$			0.3	V
$I_{PGDLKG}$	PGOOD leakage current	PGOOD high impedance, forced to 5.5 V	-1	0	1	$\mu\text{A}$
$V_{ENH}$	EN logic high	EN, VCCP logic	2			V
$V_{ENL}$	EN logic low	EN, VCCP logic			0.5	V
$I_{EN}$	EN input current				1	$\mu\text{A}$
$V_{MODETH}$	MODE threshold voltage <sup>(3)</sup>	Threshold 1	80	130	180	mV
		Threshold 2	200	250	300	
		Threshold 3	370	420	470	
		Threshold 4	1.765	1.800	1.850	
$I_{MODE}$	MODE current			15		$\mu\text{A}$

(2) Ensured by design, not production tested.

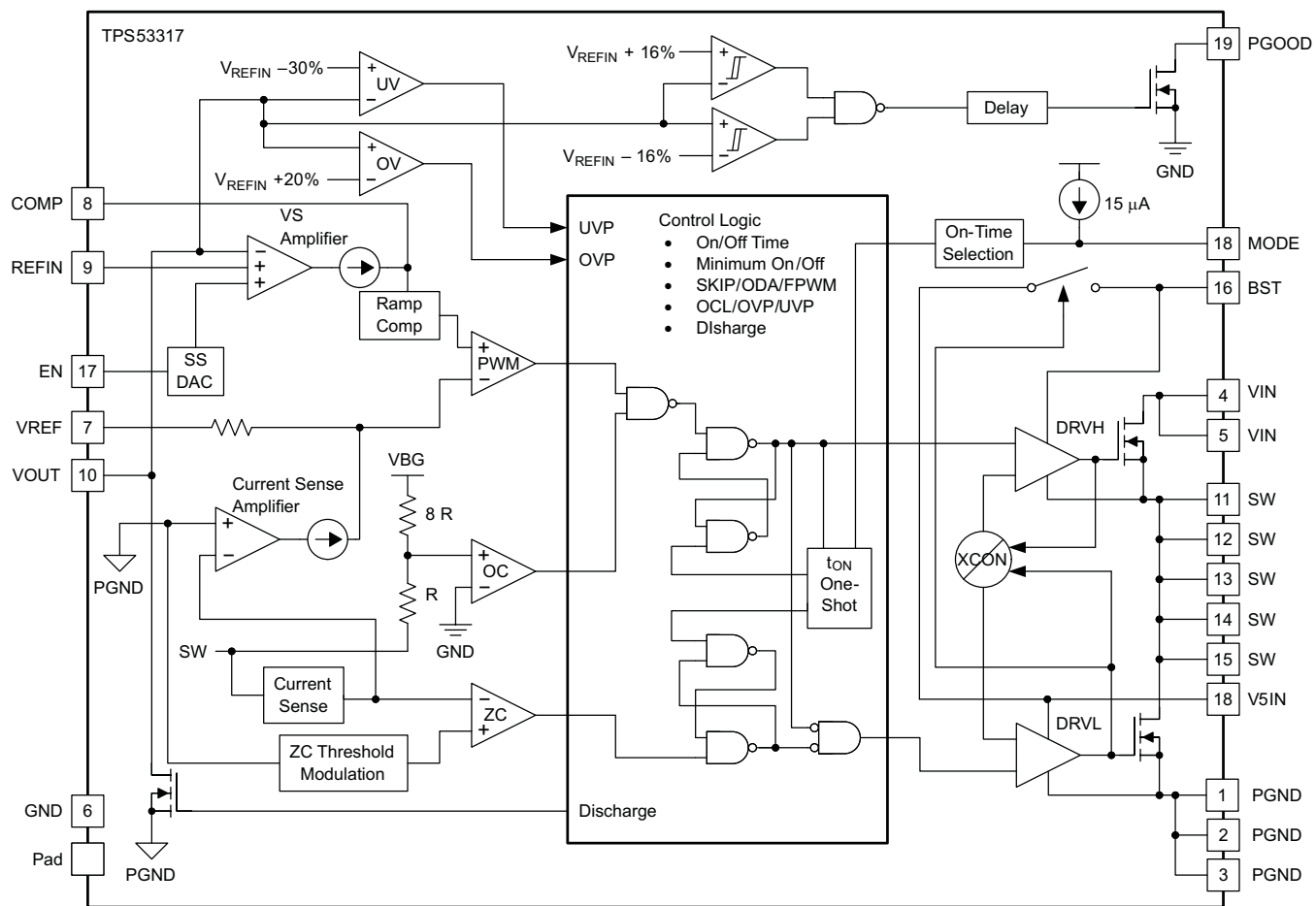
(3) See [Table 2](#) for descriptions of MODE parameters.



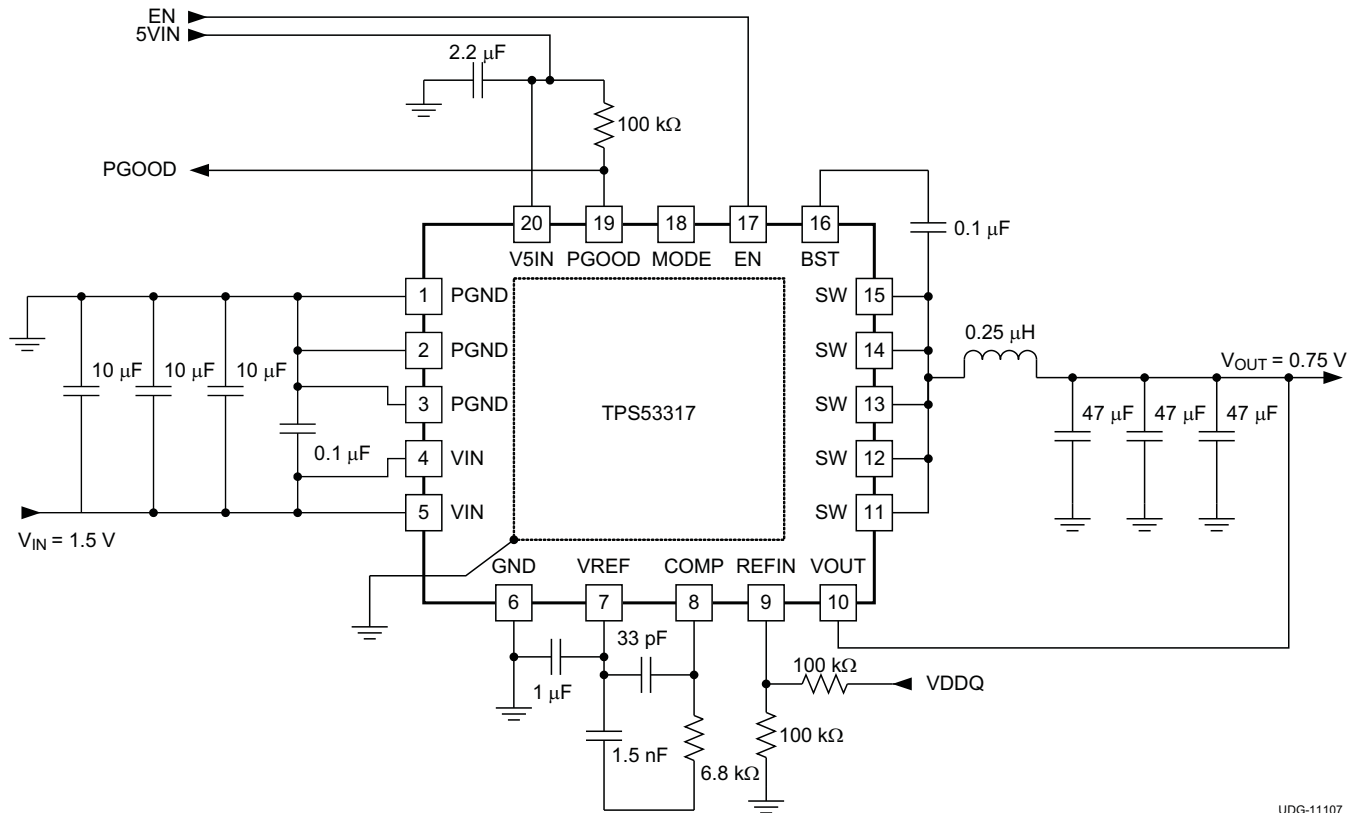
**Table 1. PIN FUNCTIONS**

PIN		I/O	DESCRIPTION
NO.	NAME		
16	BST	I	Power supply for internal high-side gate driver. Connect a 0.1- $\mu$ F bootstrap capacitor between this pin and the SW pin.
8	COMP	O	Connect series R-C filter between this pin and VREF for loop compensation.
17	EN	I	Enable of the SMPS (3.3-V logic compatible).
6	GND	–	Signal ground.
18	MODE	I	Allows selection of switching frequencies light-load modes. (See <a href="#">Table 2</a> )
1	PGND	I	Power ground. Source terminal of the rectifying low-side power FET. Positive input for current sensing.
2			
3			
19	PGOOD	O	Power good output. Connect pull-up resistor.
9	REFIN		Target output voltageinput pin. Apply voltage between 0.6 V to 2.0 V.
11	SW	I/O	Switching node output. Connect to the external inductor. Also serve as current-sensing negative input.
12			
13			
14			
15			
20	V5IN	I	5-V power supply for analog circuits and gate drive.
4	VIN	I	Power supply input pin. Drain terminal of the switching high-side power FET.
5			
10	VOUT	I	Output voltage monitor input pin.
7	VREF	O	2.0-V reference output. Connect a 0.22- $\mu$ F ceramic capacitor to GND.

**BLOCK DIAGRAM**

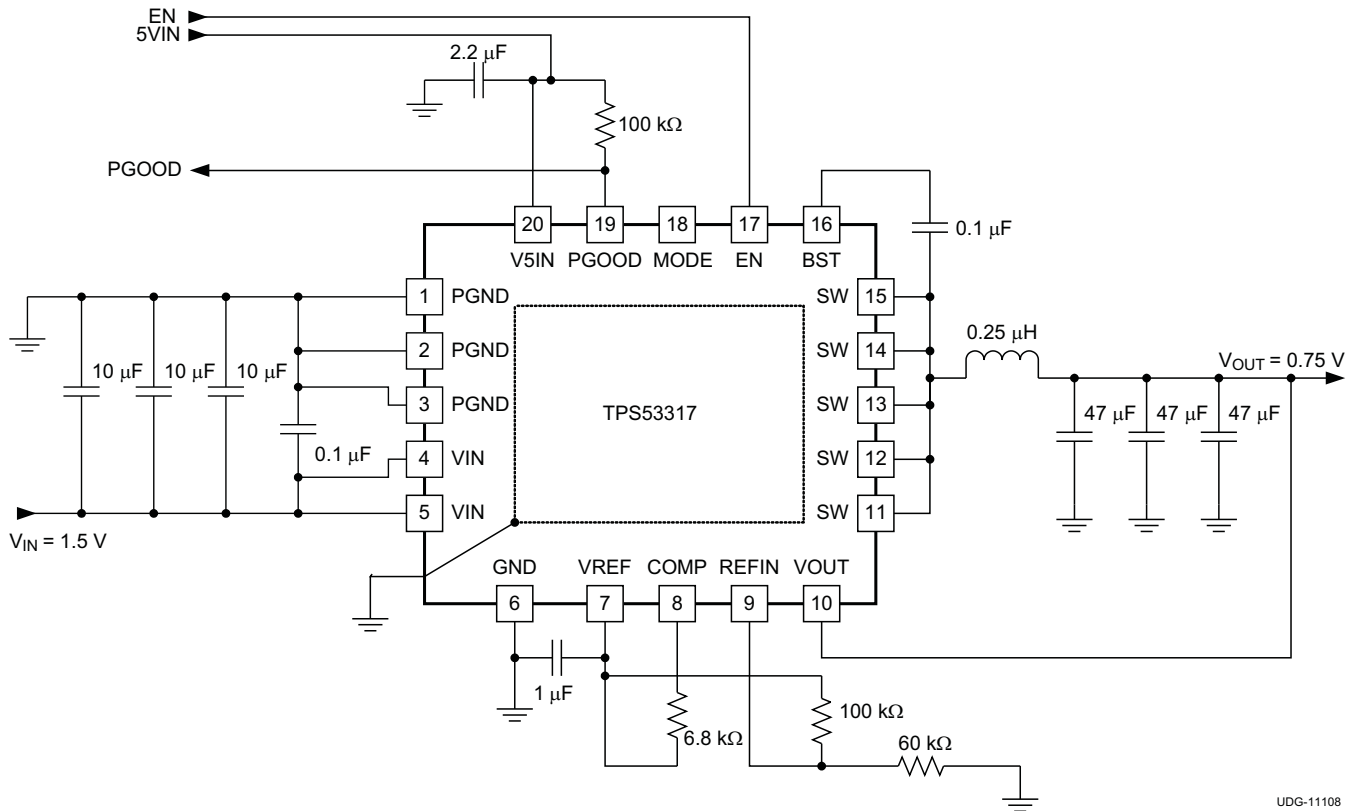


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Figure 1. VTT Application (Non-Droop Configuration)



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Figure 2. Application Using Droop Configuration

## APPLICATION INFORMATION

### Functional Overview

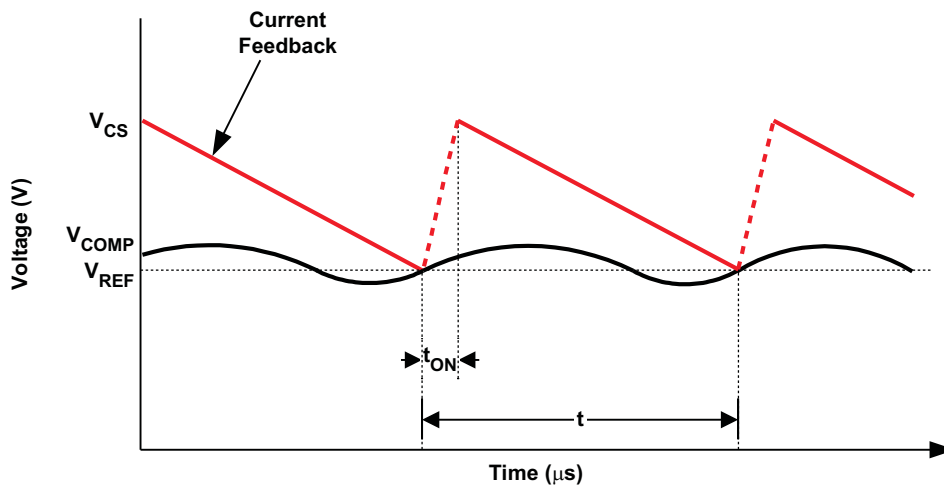
The TPS53317 is a D-CAP+™ mode adaptive on-time converter. Integrated high-side and low-side FET supports a maximum of 6-A DC output current. The converter automatically runs in discontinuous conduction mode (DCM) to optimize light-load efficiency. Multiple switching frequencies are provided to enable optimization of the power chain for the cost, size and efficiency requirements of the design (see [Table 2](#)).

In adaptive on-time converters, the controller varies the on-time as a function of input and output voltage to maintain a nearly constant frequency during steady-state conditions. In conventional constant on-time converters, each cycle begins when the output voltage crosses to a fixed reference level. However, in the TPS53317, the cycle begins when the current feedback reaches an error voltage level which is the amplified difference between the reference voltage and the feedback voltage.

### PWM Operation

Referring to [Figure 3](#), in steady state, continuous conduction mode, the converter operates in the following way.

Starting with the condition that the top FET is off and the bottom FET is on, the current feedback ( $V_{CS}$ ) is higher than the error amplifier output ( $V_{COMP}$ ).  $V_{CS}$  falls until it hits  $V_{COMP}$ , which contains a component of the output ripple voltage.  $V_{CS}$  is not directly accessible by measuring signals on pins of TPS53317. The PWM comparator senses where the two waveforms cross and triggers the on-time generator.



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**Figure 3. D-CAP+™ Mode Basic Waveforms**

The current feedback is an amplified and filtered version of the voltage between PGND and SW during low-side FET on-time. The TPS53317 also provides a single-ended differential voltage ( $V_{OUT}$ ) feedback to increase the system accuracy and reduce the dependence of circuit performance on layout.

## PWM Frequency and Adaptive on Time Control

In general, the on-time (at the SW node) can be estimated by [Equation 1](#).

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}}$$

where

- $f_{SW}$  is the frequency selected by the connection of the MODE pin (1)

The on-time pulse is sent to the top FET. The inductor current and the current feedback rises to peak value. Each ON pulse is latched to prevent double pulsing. Switching frequency settings are shown in [Table 2](#).

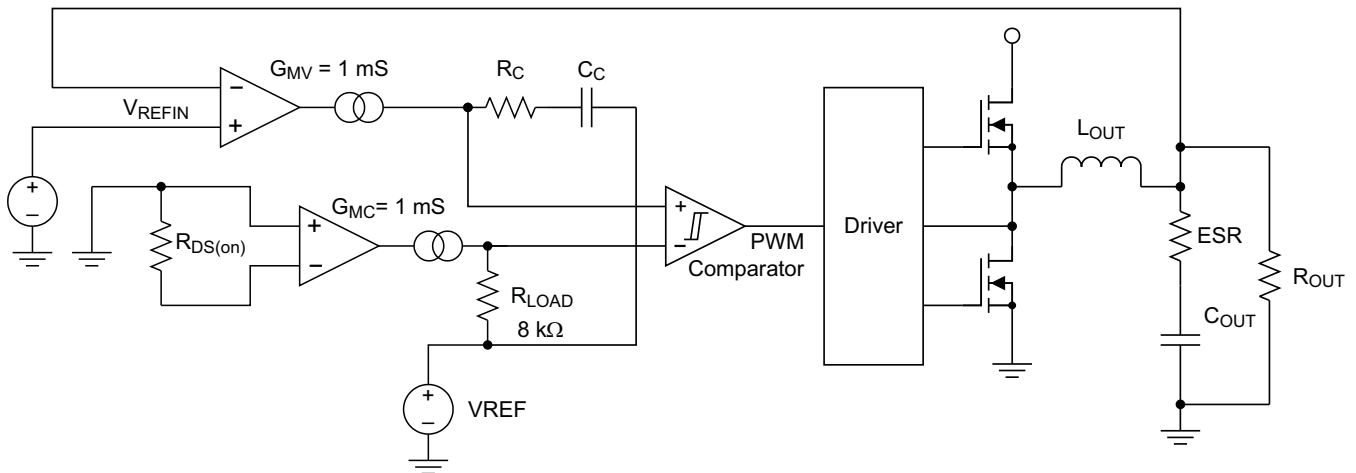
## Non-Droop Configuration

The TPS53317 can be configured as a non-droop solution. The benefit of a non-droop approach is that load regulation is flat, therefore, in a system where tight DC tolerance is desired, the non-droop approach is recommended. For the Intel system agent application, non-droop is recommended as the standard configuration.

The non-droop approach can be implemented by connecting a resistor and a capacitor between the COMP and the VREF pins. The purpose of the type II compensation is to obtain high DC feedback gain while minimizing the phase delay at unity gain cross over frequency of the converter.

The value of the resistor ( $R_C$ ) can be calculated using the desired unity gain bandwidth of the converter, and the value of the capacitor ( $C_C$ ) can be calculated by knowing where the zero location is desired.

[Figure 4](#) shows the basic implementation of the non-droop mode using the TPS53317.



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**Figure 4. Non-Droop Mode Basic Implementation**

Figure 5 shows shows the load regulation using non-droop configuration.

Figure 6 shows the transient response of TPS53317 using non-droop configuration, where  $C_{OUT} = 3 \times 47 \mu\text{F}$ . The applied step load is from 0 A to 2 A.

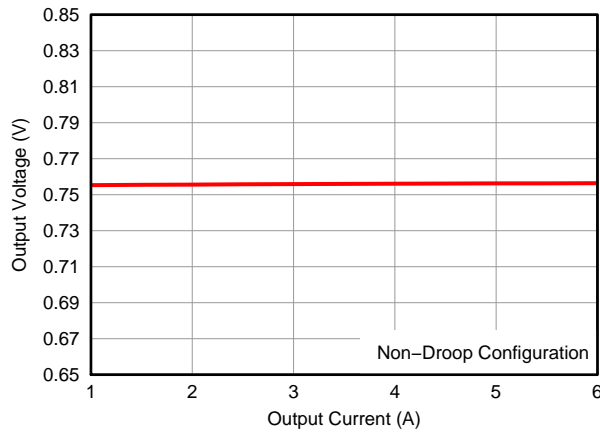


Figure 5. Load Regulation for 1.5-V Input and 0.75-V Output (Non-Droop Configuration)

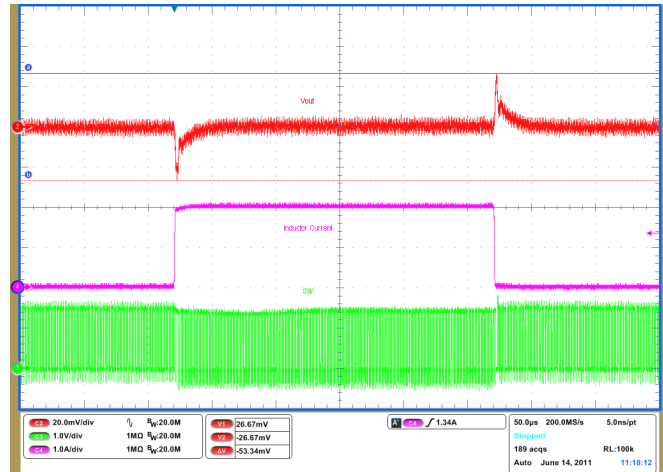


Figure 6. Non-Droop Configuration Transient Response  
 CH 2:  $V_{OUT}$  (20 mV/div)  
 CH 4:  $I_{LOAD}$  (1 A/div)  
 CH 3: SW (1 V/div)

### Droop Configuration

The terminology for droop is the same as *load line* or *voltage positioning* as defined in the Intel CPU  $V_{CORE}$  specification. Based on the actual tolerance requirement of the application, load-line set points can be defined to maximize either cost savings (by reducing output capacitors) or power reduction benefits.

Accurate droop voltage response is provided by the finite gain of the droop amplifier. The equation for droop voltage is shown in Equation 2.

$$V_{DROOP} = \frac{A_{CSINT} \times I(L)}{R_{DROOP} \times G_M}$$

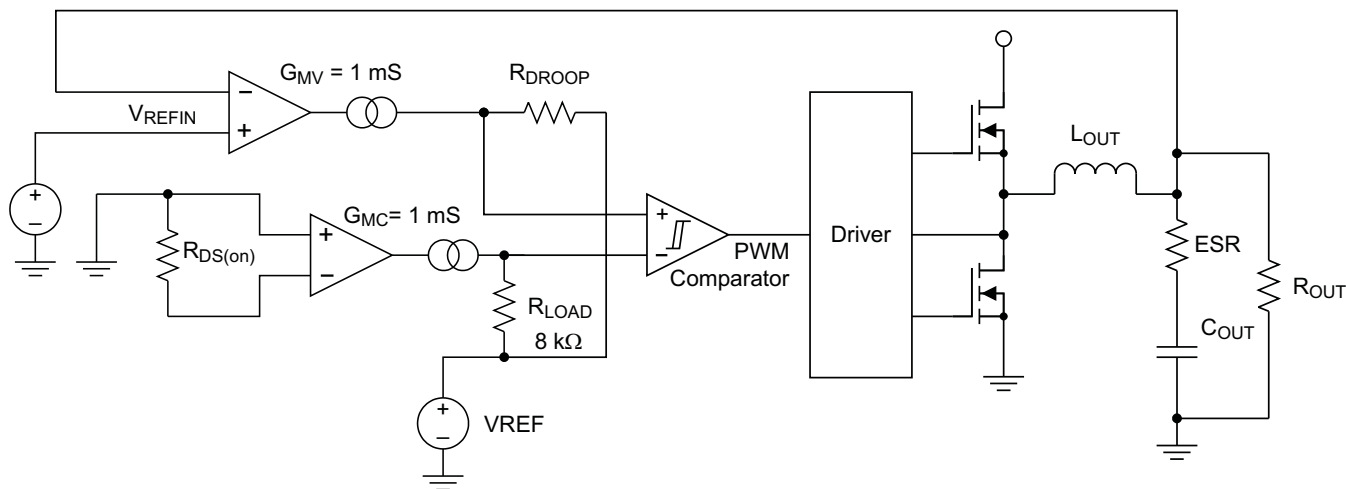
where

- low-side on-resistance is used as the current sensing element
- $A_{CSINT}$  is a constant, which nominally is 53 mV/A.
- $I(L)$  is the DC current of the inductor, or the load current
- $R_{DROOP}$  is the value of resistor from the COMP pin to the VREF pin
- $G_M$  is the transconductance of the droop amplifier with nominal value of 1 mS

Equation 3 can be used to easily derive  $R_{DROOP}$  for any load line slope/droop design target.

$$R_{LOAD\_LINE} = \frac{V_{DROOP}}{I(L)} = \frac{A_{CSINT}}{R_{DROOP} \times G_M} \therefore R_{DROOP} = \frac{A_{CSINT}}{R_{LOAD\_LINE} \times G_M}$$

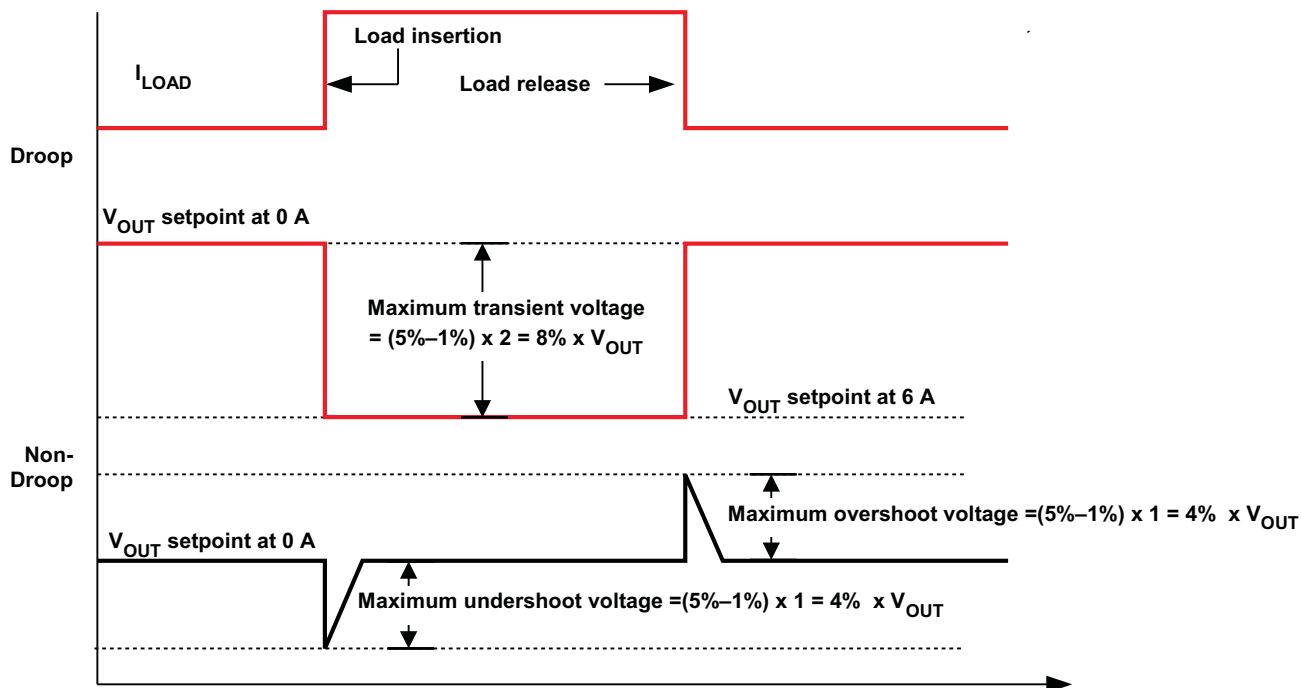
Figure 7 shows the basic implementation of the droop mode using the TPS53317.



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Figure 7. DROOP Mode Basic Implementation

The droop (voltage positioning) method was originally recommended to reduce the number of external output capacitors required. The effective transient voltage range is increased because of the active voltage positioning (see Figure 8).



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Figure 8. DROOP vs Non-DROOP in Transient Voltage Window

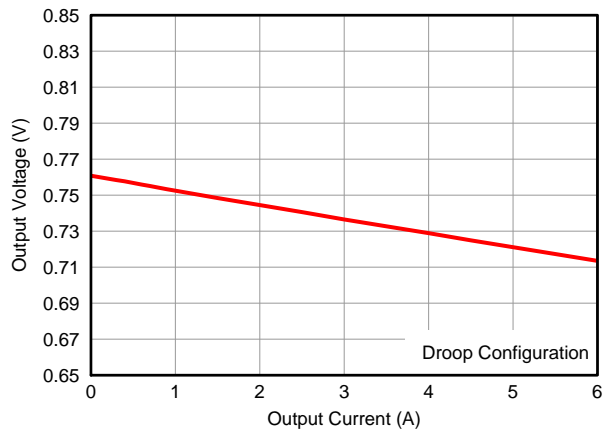
In applications where the DC and the AC tolerances are not separated, which means there is not a strict DC tolerance requirement, the droop method can be used.

**Table 2. Mode Definitions**

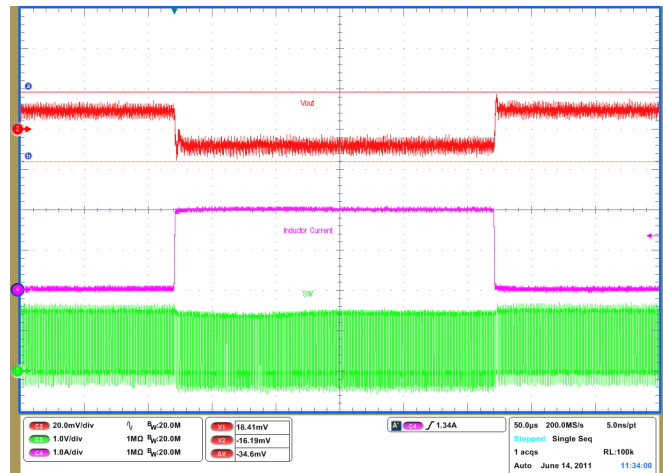
MODE	MODE RESISTANCE (kΩ)	LIGHT-LOAD POWER SAVING MODE	SWITCHING FREQUENCY (f <sub>sw</sub> )	OVERCURRENT LIMIT (OCL) VALLEY (A)
1	0	SKIP	600 kHz	6
2	12		600 kHz	4
3	22		1 MHz	4
4	33		1 MHz	6
5	47	PWM	600 kHz	6
6	68		600 kHz	4
7	100		1 MHz	4
8	OPEN		1 MHz	6

Figure 9 shows the load regulation of the 1.5-V rail using an R<sub>DRPOOP</sub> value of 6.8 kΩ.

Figure 10 shows the transient response of the TPS53317 using droop configuration and C<sub>OUT</sub> = 3 × 47 μF. The applied step load is from 0 A to 2 A.



**Figure 9. Load Regulation for 1.5-V Input and 0.75-V Output (Droop Configuration)**



**Figure 10. Droop Configuration Transient Response**  
 CH 2: V<sub>OUT</sub> (20 mV/div)  
 CH 4: I<sub>LOAD</sub> (1 A/div)  
 CH 3: SW (1 V/div)

## Light-Load Power Saving Features

The TPS53317 has an automatic pulse-skipping mode to provide excellent efficiency over a wide load range. The converter senses inductor current and prevents negative flow by shutting off the low-side gate driver. This saves power by eliminating re-circulation of the inductor current. Further, when the bottom FET shuts off, the converter enters discontinuous mode, and the switching frequency decreases, thus reducing switching losses as well.

TPS53317 also provides a special light-load power saving feature, called ripple reduction. Essentially, it reduces the on-time in SKIP mode to effectively reduce the output voltage ripple associated with using an all MLCC capacitor output power stage design.

## Power Sequences

### Non-Tracking Startup

The TPS53317 can be configured for non-tracking application. When non-tracking is configured, output voltage is regulated to the REFIN voltage which taps off the voltage dividers from the 2VREF. Either the EN pin or the V5IN pin can be used to start up the device. The TPS53317 uses internal voltage servo DAC to provide a precise 1.6-ms soft-start time during soft-start initialization. (See [Figure 11](#))

### Tracking Startup

TPS53317 can also be configured for tracking application. When tracking configuration is desired, output voltage is also regulated to the REFIN voltage which comes from external power source. In order for TPS53317 to differentiate between a non-tracking configuration or a tracking configuration, there is a minimum delay time of 260  $\mu$ s required between the time when the EN pin or the 5VIN pin is validated to the time when the REFIN pin voltage can be applied, in order for the TPS53317 to track properly (see [Figure 12](#)). The valid REFIN voltage range is between 0.6 V to 2 V.

## Protection Features

The TPS53317 offers many features to protect the converter power chain as well as the system electronics.

### 5-V Undervoltage Protection (UVLO)

The TPS53317 continuously monitors the voltage on the V5IN pin to ensure that the voltage level is high enough to bias the device properly and to provide sufficient gate drive potential to maintain high efficiency. The converter starts with approximately 4.3 V and has a nominal of 440 mV of hysteresis. If the 5-V UVLO limit is reached, the converter transitions the phase node into a off function. And the converter remains in the off state until the device is reset by cycling 5 V until the 5-V POR is reached (2.3-V nominal). The power input does not have a UVLO function.

### Power Good Signals

The TPS53317 has one open-drain *power good* (PGOOD) pin. During startup, there is a 1-ms power good high propagation delay. The PGOOD pin de-asserts as soon as the EN pin is pulled low or an undervoltage condition on V5IN or any other fault is detected.

### Output Overvoltage Protection (OVP)

In addition to the power good function described above, the TPS53317 has additional OVP and UVP thresholds and protection circuits.

An OVP condition is detected when the output voltage is approximately  $120\% \times V_{REFIN}$ . In this case, the converter de-asserts the PGOOD signals and performs the overvoltage protection function. During OVP, the low-side FET is always on before triggering a negative overcurrent. When a negative OC is also tripped, the low-side FET is no longer continuously on, and pulsed signals are generated to limit the negative inductor current. When the VOUT pin voltage drops below 400 mV, the low-side FET is turned off (non-latch) until the VOUT pin voltage exceeds 400 mV again.

## Output Undervoltage Protection (UVP)

Output undervoltage protection works in conjunction with the current protection described in the [Overcurrent Protection](#) and [Overcurrent Limit](#) sections. If the output voltage drops below 70% of  $V_{REFIN}$ , after approximately a 250  $\mu$ s delay, the device stops switching and enters hiccup mode. After a hiccup waiting time, a re-start is attempted. If the fault condition is not cleared, hiccup mode operation may continue indefinitely.

## Overcurrent Protection

Both positive and negative overcurrent protection are provided in the TPS53317:

- Overcurrent Limit (OCL)
- Negative OCL (level same as positive OCL)

### Overcurrent Limit

If the sensed current value is above the OCL setting, the converter delays the next ON pulse until the current drops below the OCL limit. Current limiting occurs on a pulse-by-pulse basis. The TPS53317 uses a valley current limiting scheme where the DC OCL trip point is the OCL limit plus half of the inductor ripple current. The minimum valley OCL is 6 A or 4 A (depending on mode selection) over process and temperature.

During the overcurrent protection event, the output voltage likely droops until the UVP limit is reached. Then, the converter de-asserts the PGOOD pin, and then enters hiccup mode after an 250- $\mu$ s delay. The converter remains in hiccup mode until the fault is cleared..

$$I_{OCL(dc)} = I_{OCL(valley)} + \frac{1}{2} \times I_{P-P} \quad (4)$$

### Negative OCL

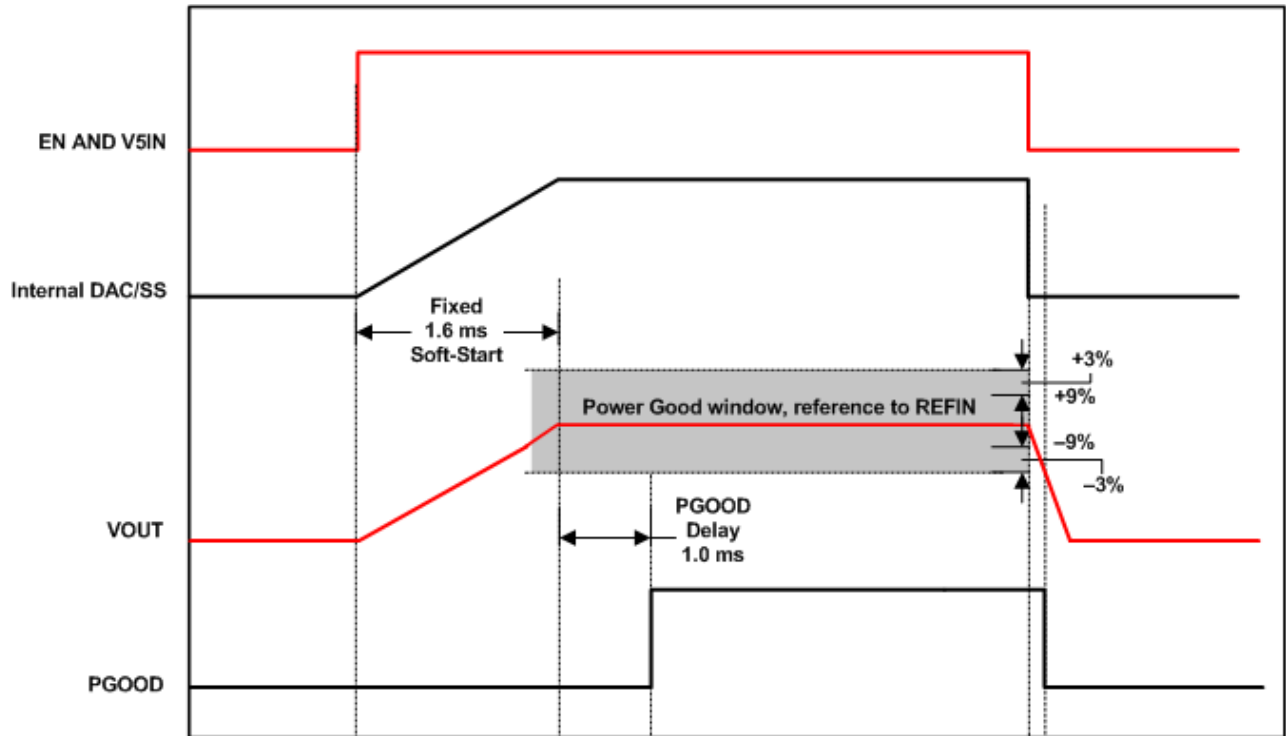
The negative OCL circuit acts when the converter is sinking current from the output capacitor(s). The converter continues to act in a *valley* mode, the absolute value of the negative OCL set point is typically -6.5 A or -4.5 A (depending on mode selection) .

## Thermal Protection

### Thermal Shutdown

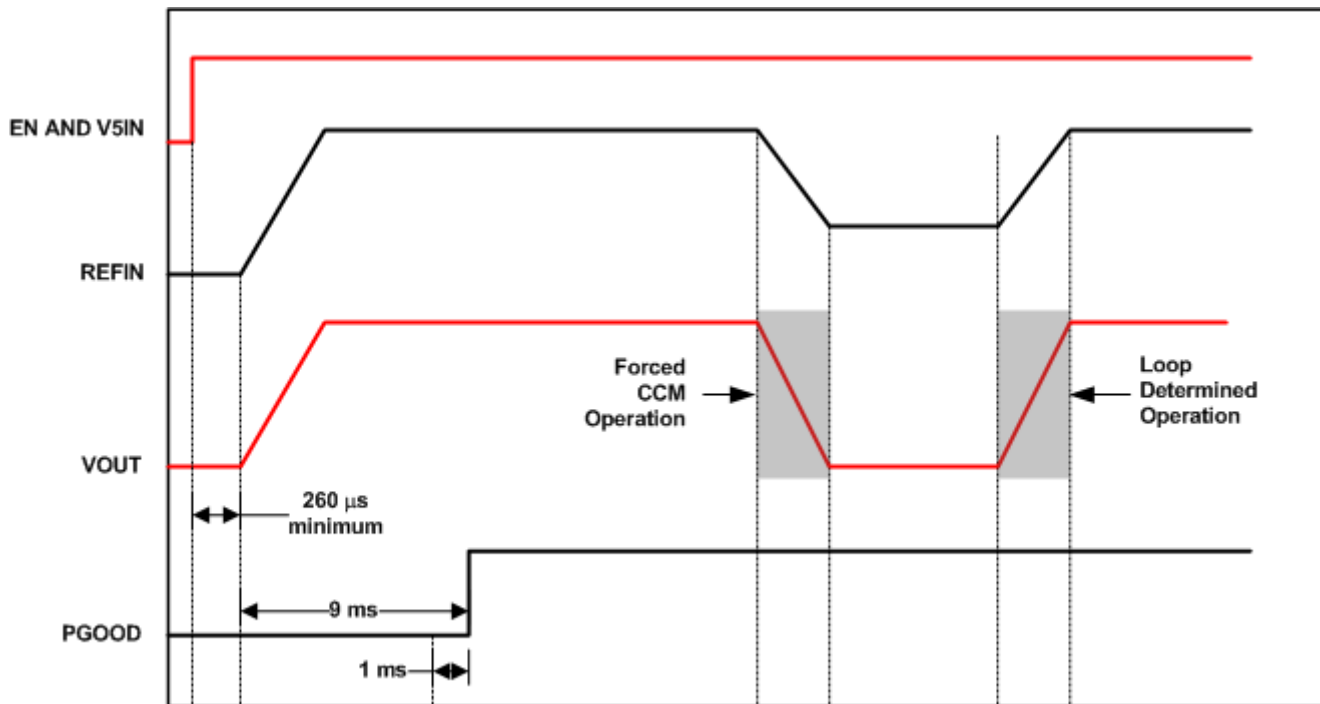
The TPS53317 has an internal temperature sensor. When the temperature reaches a nominal 145°C, the device shuts down until the temperature cools by approximately 10°C. Then the converter restarts.

Startup Timing Diagrams



UDG-11061

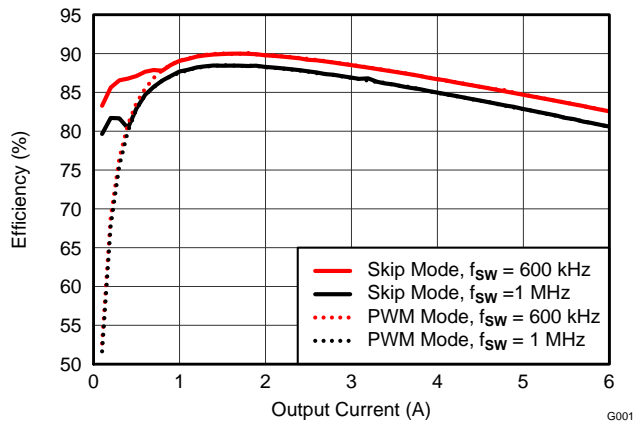
Figure 11. Non-Tracking Start-Up



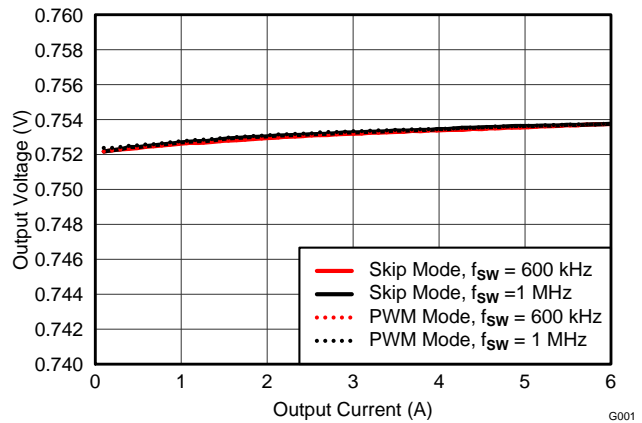
UDG-11079

Figure 12. Tracking Start-Up

**TYPICAL CHARACTERISTICS**



**Figure 13. Efficiency vs Output Current (1.5-V Input and 0.75-V Output)**



**Figure 14. Output Voltage vs Output Current (1.5-V Input and 0.75-V Output)**

**LAYOUT CONSIDERATIONS**

Good layout is essential for stable power supply operation. Follow these guidelines for an efficient PCB layout.

- Connect PGND pins (or at least one of the pins) to the thermal PAD underneath the device. Also connect GND pin to the thermal PAD underneath the device. Use four vias to connect the thermal pad to internal ground planes.
- Place VIN, V5IN and VREF decoupling capacitors as close to the device as possible.
- Use wide traces for the VIN, VOUT, PGND and SW pins. These nodes carry high current and also serve as heat sinks.
- Place feedback and compensation components as close to the device as possible.
- Place COMP analog signal away from noisy signals (SW, BST).

**Changes from Original (JUNE 2011) to Revision A**
**Page**

• Changed from "SKIP and Forced CCM" to "SKIP or Forced CCM" in FEATURES .....	1
• Changed from "600-kHz and 1-MHz Switching" to "600-kHz or 1-MHz Switching" in FEATURES .....	1
• Added clarity to Simplified Application drawing .....	1
• Changed from " $f_{SW} = 600 \text{ kHz}$ " to " $f_{SW} = 1 \text{ MHz}$ " for $t_{ON(min)}$ in EC table .....	5
• Added clarity to BLOCK DIAGRAM .....	7

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**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
TPS53317RGBR	ACTIVE	VQFN	RGB	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS53317RGBT	ACTIVE	VQFN	RGB	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

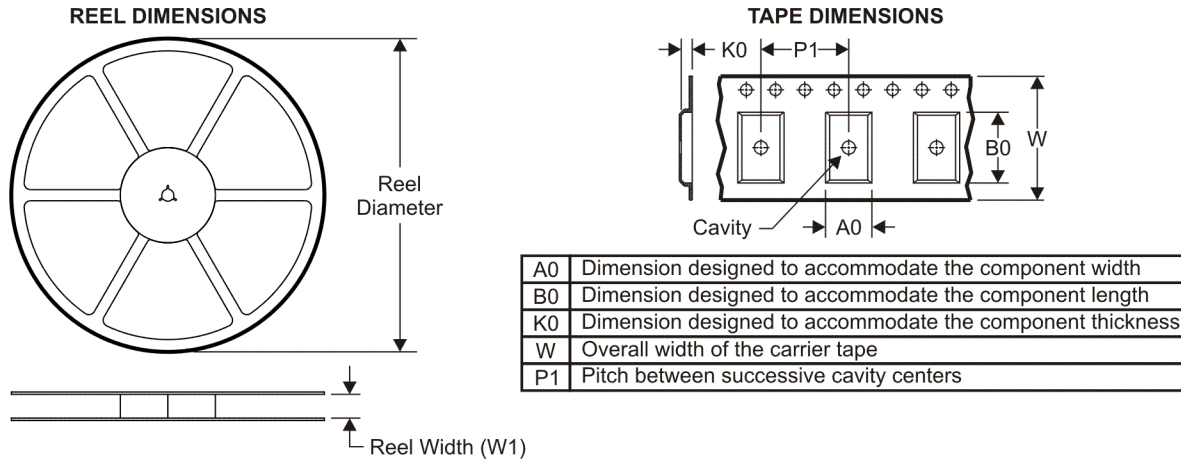
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53317RGBR	VQFN	RGB	20	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
TPS53317RGBT	VQFN	RGB	20	250	180.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

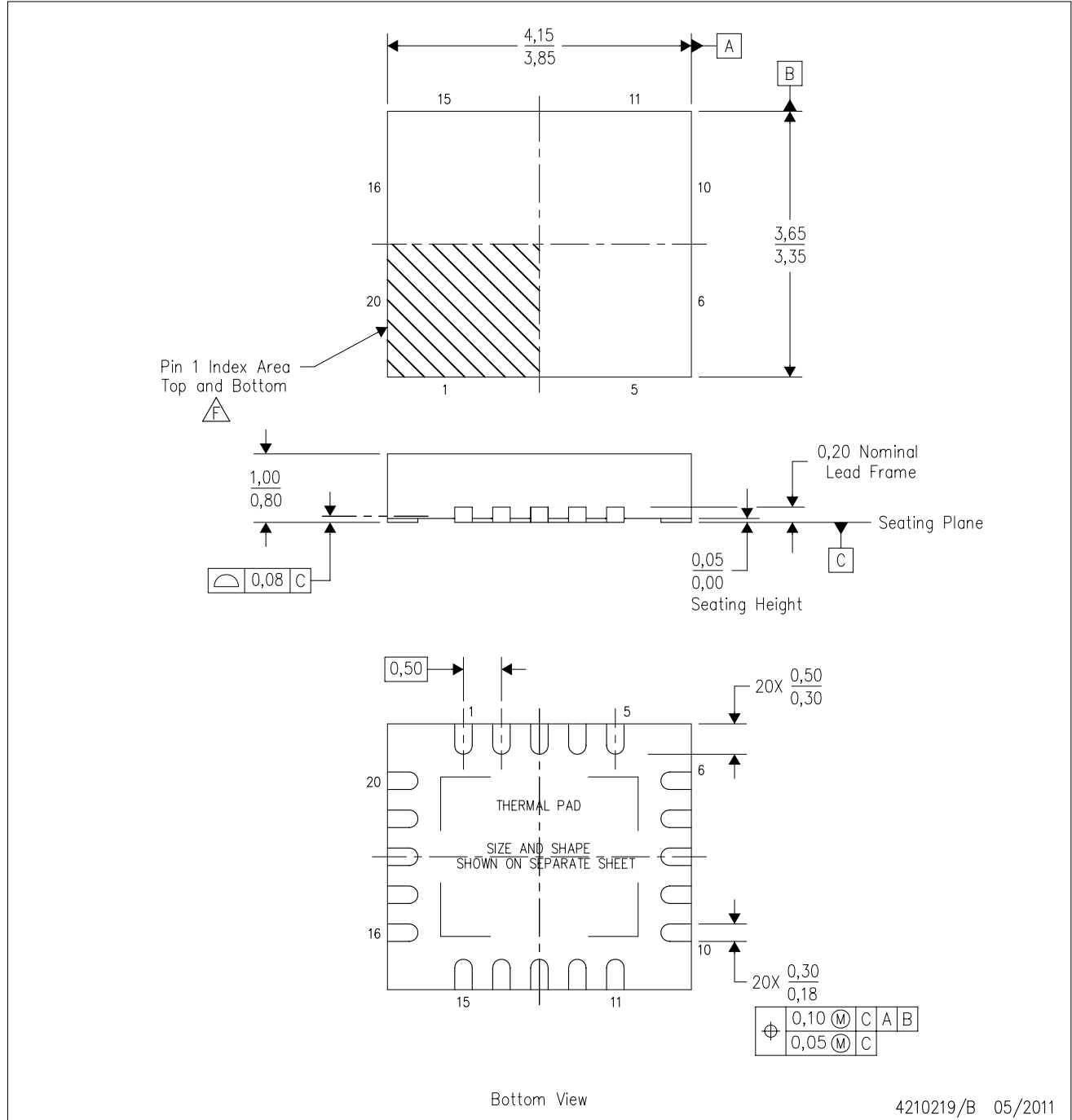
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53317RGBR	VQFN	RGB	20	3000	346.0	346.0	29.0
TPS53317RGBT	VQFN	RGB	20	250	190.5	212.7	31.8

RGB (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



4210219/B 05/2011

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F** Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

## THERMAL PAD MECHANICAL DATA

RGB (R-PVQFN-N20)

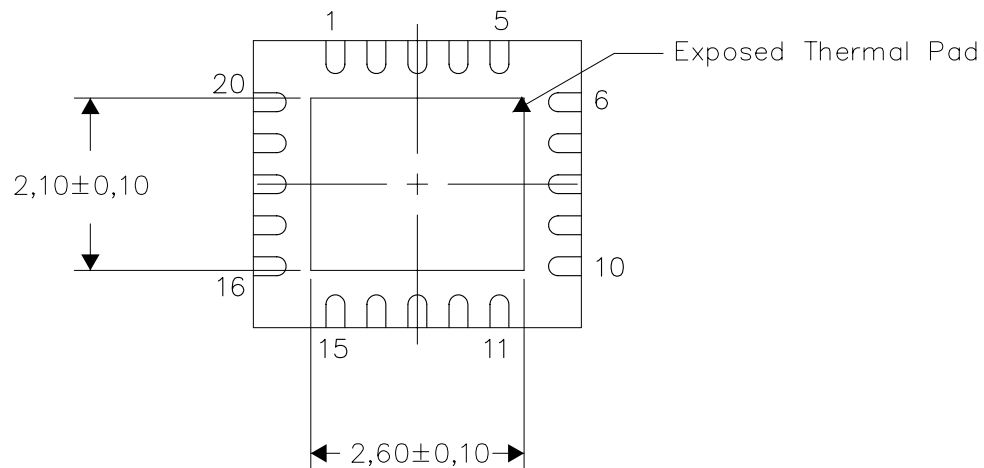
PLASTIC QUAD FLATPACK NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

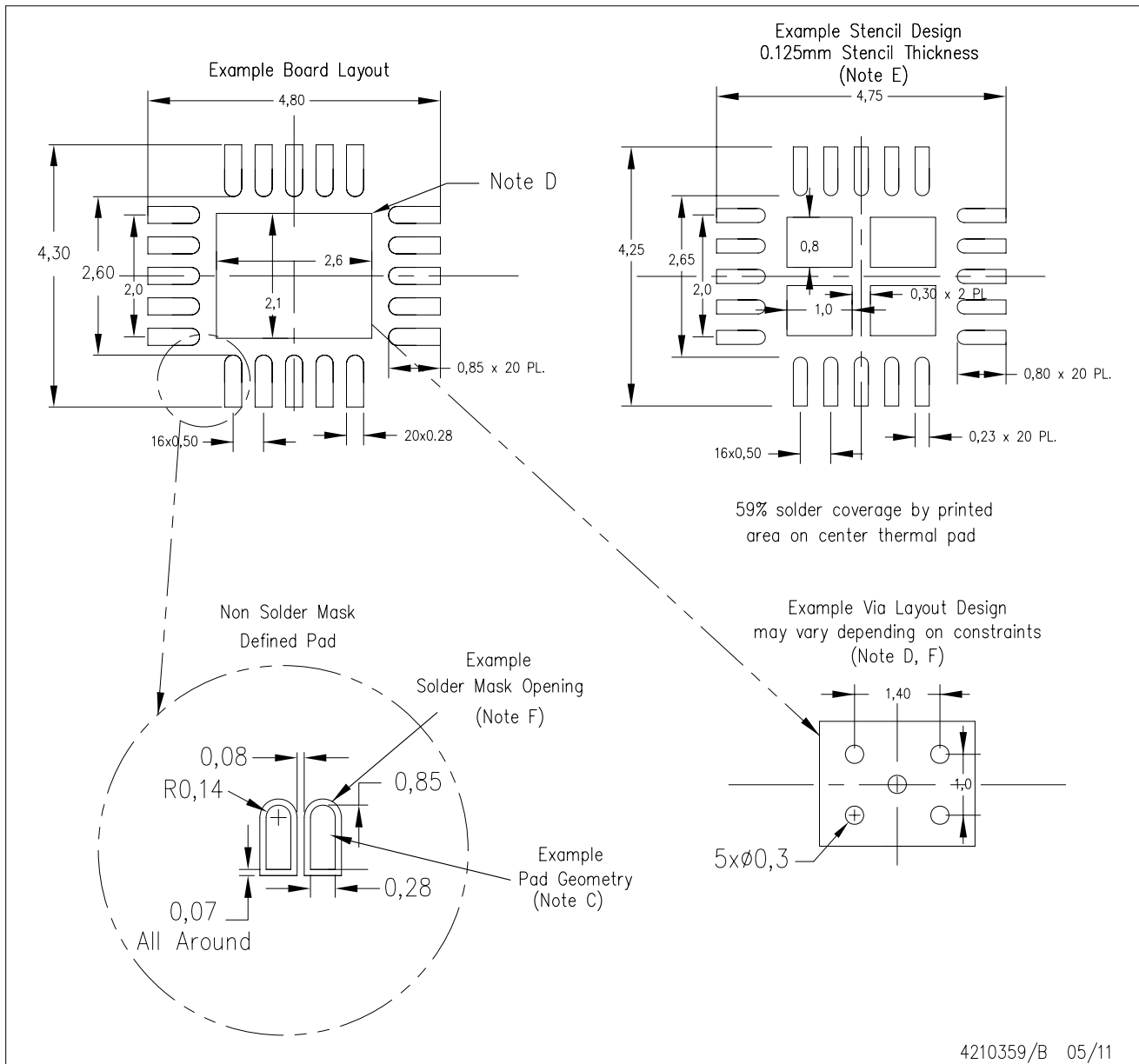
Exposed Thermal Pad Dimensions

4210242/B 05/11

NOTE: All linear dimensions are in millimeters

RGB (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



4210359/B 05/11

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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