



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾⁽²⁾

| T _A | PACKAGE | ORDERABLE DEVICE NUMBER | PINS | OUTPUT SUPPLY | MINIMUM QUANTITY | ECO PLAN |
|-------------------|---------------|-------------------------|------|---------------|------------------|---------------------------|
| Plastic QFN (RGT) | –40°C to 85°C | TPS53316RGTR | 16 | Tape and reel | 3000 | Green (RoHS and no Pb/Br) |
| | | TPS53316RGTT | 16 | Mini reel | 250 | |

- (1) For the most current package and ordering information, see the *Package Option Addendum* at the end of this document, or visit the TI website at www.ti.com.
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating free air-temperature range (unless otherwise noted)

| | | VALUE | UNIT | |
|--|--------------------------|---------------------|-------------|---|
| Input voltage range | VIN | –0.3 to 7 | V | |
| | VBST | –0.3 to 17 | | |
| | VBST(with respect to LL) | –0.3 to 7 | | |
| | EN | –0.3 to 7 | | |
| | FB, PS, RF/OC | –0.3 to 3.7 | | |
| Output voltage range | SW | DC | –1 to 7 | V |
| | | Pulse < 20ns, E=5μJ | ≥ –5 or <10 | |
| | PGD | –0.3 to 7 | | |
| | COMP, VREG3 | –0.3 to 3.7 | | |
| | PGND | –0.3 to 0.3 | | |
| Operating free-air temperature, T _A | | –40 to 85 | °C | |
| Storage temperature range, T _{stg} | | –55 to 150 | °C | |
| Junction temperature range, T _J | | –40 to 150 | °C | |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | | 300 | C | |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

| | | VALUE | | UNIT |
|--|--------------------------|-------|------|------|
| | | MIN | MAX | |
| Input voltage range | VIN (main supply) | 2.9 | 6 | V |
| | VBST | -0.1 | 13.5 | |
| | VBST(with respect to SW) | -0.1 | 6 | |
| | EN, | -0.1 | 6 | |
| | FB, PS, RF/OC | -0.1 | 3.5 | |
| Output voltage range | SW | -1 | 6.5 | V |
| | PGD | -0.1 | 6 | |
| | COMP, VREG3 | -0.1 | 3.5 | |
| | PGND | -0.1 | 0.1 | |
| Junction temperature range, T _J | | -40 | 125 | °C |

THERMAL INFORMATION

| THERMAL METRIC ⁽¹⁾ | | TPS53316 | UNITS |
|-------------------------------|--|---------------|-------|
| | | RGT (16) PINS | |
| θ_{JA} | Junction-to-ambient thermal resistance | 45.9 | °C/W |
| θ_{JCTop} | Junction-to-case (top) thermal resistance | 54.3 | |
| θ_{JB} | Junction-to-board thermal resistance | 18.3 | |
| ψ_{JT} | Junction-to-top characterization parameter | 1.1 | |
| ψ_{JB} | Junction-to-board characterization parameter | 18.3 | |
| θ_{JCbott} | Junction-to-case (bottom) thermal resistance | 5.3 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

ELECTRICAL CHARACTERISTICS

 over operating free-air temperature range, $V_{IN} = 3.3V$, $PGND = GND$ (unless otherwise noted)

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|--|--------|------|-------|-------------|
| SUPPLY: VOLTAGE, CURRENTS, AND UVLO | | | | | | |
| V_{VIN} | VIN supply voltage | Nominal input voltage range | 2.9 | | 6.0 | V |
| $I_{VIN(sdn)}$ | VIN shutdown current | EN = LO | | | 15 | μA |
| I_{VIN} | VIN supply current | EN = HI, $V_{FB} = 0.63V$, No load | | 2.0 | 3.5 | mA |
| V_{UVLO} | VIN UVLO threshold | Ramp up; EN = HI | | 2.8 | | V |
| $V_{UVLO(hys)}$ | VIN UVLO hysteresis | VIN UVLO hysteresis | | 120 | | mV |
| V_{REG3} | LDO output | $V_{VIN} = 5V$, $0 \leq I_{DD} \leq 5mA$ | 3.135 | 3.3 | 3.465 | V |
| VOLTAGE FEEDBACK LOOP: VREF AND ERROR AMPLIFIER | | | | | | |
| V_{VREF} | VREF | Internal precision reference voltage | | 0.6 | | V |
| TOL_{VREF} | VREF tolerance | $0^{\circ}C \leq T_A \leq 85^{\circ}C$ | -1% | | 1% | |
| | | $-40^{\circ}C \leq T_A \leq 85^{\circ}C$ | -1.25% | | 1.25% | |
| $UGBW^{(1)}$ | Unity gain bandwidth | | 14 | | | MHz |
| $A_{OL}^{(1)}$ | Open loop gain | | 80 | | | dB |
| I_{FBINT} | FB input leakage current | Sourced from FB pin | | | 30 | nA |
| $I_{EA(max)}^{(1)}$ | Output sinking and sourcing current | $C_{COMP} = 20pF$ | | 5 | | mA |
| $SR^{(1)}$ | Slew rate | | | 5 | | V/ μs |
| OCP: OVERCURRENT AND ZERO CROSSING | | | | | | |
| $I_{OCP13A}^{(2)}$ | Overcurrent limit on high-side FET | 4.5-A setting, when I_{OUT} exceeds this threshold for 4 consecutive cycles, $V_{VIN} = 3.3V$, $V_{OUT} = 1.5V$ with 1- μH inductor, $f_{SW} = 1.1MHz$, $T_A = 25^{\circ}C$ | 4.05 | 4.5 | 4.95 | A |
| $I_{OCPH3A}^{(2)}$ | One-time overcurrent latch off on the low-side FET | 4.5-A setting, immediate shut down when sensed current reach this value $V_{VIN} = 3.3V$, $V_{OUT} = 0.6V$ with 1- μH inductor, $f_{SW} = 1.1MHz$, $T_A = 25^{\circ}C$ | 4.49 | 5.1 | 5.61 | A |
| $I_{OCP15A}^{(2)}$ | Overcurrent limit on high-side FET | 6.5-A setting, when I_{OUT} exceeds this threshold for 4 consecutive cycles, $V_{VIN} = 3.3V$, $V_{OUT} = 1.5V$ with 1- μH inductor, $f_{SW} = 1.1MHz$, $T_A = 25^{\circ}C$ | 6.1 | 6.8 | 7.5 | A |
| $I_{OCPH5A}^{(2)}$ | One time overcurrent latch off on the low-side FET | 6.5-A setting, immediate shut down when sensed current reach this value $V_{VIN} = 3.3V$, $V_{OUT} = 0.6V$ with 1- μH inductor, $f_{SW} = 1.1MHz$, $T_A = 25^{\circ}C$ | 6.75 | 7.50 | 8.30 | A |
| t_{hiccup} | Hiccup time interval | $f_{SW} = 1.1MHz$ | | 14.5 | | ms |
| $V_{ZXOFF}^{(1)}$ | Zero crossing comparator internal offset | PGND – SW, SKIP mode | -4.5 | -3.0 | -1.5 | mV |
| PROTECTION: OVP, UVP, PGD, AND INTERNAL THERMAL SHUTDOWN | | | | | | |
| V_{OVP} | Overvoltage protection threshold voltage | Measured at the FB w/r/t VREF | 114% | 117% | 120% | |
| V_{UVP} | Undervoltage protection Threshold voltage | Measured at the FB w/r/t VREF | 80% | 83% | 86% | |
| V_{PGDL} | PGD low threshold | Measured at the FB w/r/t VREF | 80% | 83% | 86% | |
| V_{PGDU} | PGD upper threshold | Measured at the FB w/r/t VREF | 114% | 117% | 120% | |
| $V_{INMINPG}$ | Minimum input voltage for valid PGD at start-up | Measured at VIN with 1-mA sink current on PGD pin at start up | | 1 | | V |
| $THSD^{(1)}$ | Thermal shutdown | | 130 | 140 | 150 | $^{\circ}C$ |
| $THSD_{HYS}^{(1)}$ | Thermal shutdown hysteresis | Controller start again after temperature has dropped | | 40 | | $^{\circ}C$ |

(1) Ensured by design. Not production tested.

(2) See Figure 5 and Figure 6 on OCP level for other operating conditions.

ELECTRICAL CHARACTERISTICS (continued)

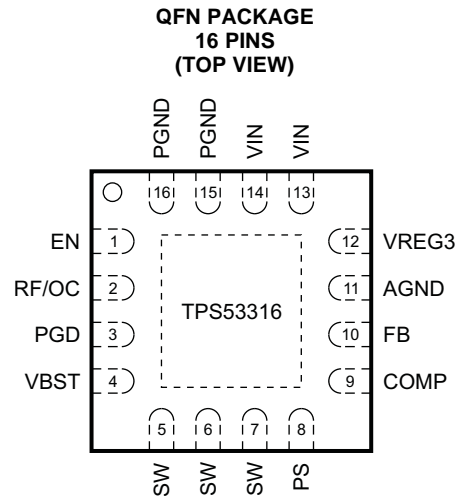
over operating free-air temperature range, $V_{IN} = 3.3V$, $PGND = GND$ (unless otherwise noted)

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--------------------------------------|---|-------|-------------|-------|------------|
| LOGIC PINS: I/O VOLTAGE AND CURRENT | | | | | | |
| V_{PGPD} | PGD pull down voltage | Pull down voltage with 4mA sink current | | 0.1 | 0.3 | V |
| I_{PGLK} | PGD leakage current | Hi-Z leakage current, Apply 3.3V in off state | -2 | 0 | 2 | μA |
| R_{ENPU} | Enable pull-up resistor | | | 2.25 | | M Ω |
| V_{ENH} | EN logic high | $V_{VIN} = 3.3 V$ | 0.82 | 0.97 | 1.10 | V |
| | | $V_{VIN} = 5 V$ | 0.95 | 1.10 | 1.25 | V |
| V_{ENHYS} | EN hysteresis | $V_{VIN} = 3.3 V$ | | 0.16 | 0.24 | V |
| | | $V_{VIN} = 5 V$ | | 0.2 | 0.275 | V |
| PS_{THS} | PS mode threshold voltage | Level 1 to Level 2 ⁽³⁾ | | 0.12 | | V |
| | | Level 2 to Level 3 | | 0.4 | | |
| | | Level 3 to Level 4 | | 0.8 | | |
| | | Level 4 to Level 5 | | 1.4 | | |
| | | Level 5 to Level 6 | | 2.2 | | |
| I_{PS} | PS source | 10- μA pull-up current when enabled | 8 | 10 | 12 | μA |
| RF/OC_{THS} | RF/OC pin threshold voltage | Level 1 to Level 2 ⁽⁴⁾ | | 0.12 | | V |
| | | Level 2 to Level 3 | | 0.4 | | |
| | | Level 3 to Level 4 | | 0.8 | | |
| | | Level 4 to Level 5 | | 1.4 | | |
| | | Level 5 to Level 6 | | 2.2 | | |
| $I_{RF/OC}$ | RF/OC source current | 10- μA pull-up current when enabled | 8 | 10 | 12 | μA |
| BOOT STRAP: VOLTAGE AND LEAKAGE CURRENT | | | | | | |
| I_{VBSTLK} | VBST leakage current | $V_{VIN} = 3.3 V$, $V_{VBST} = 6.6 V$, $T_A = 25^\circ C$ | | | 1 | μA |
| TIMERS: SS, FREQUENCY, RAMP, ON-TIME AND I/O TIMING | | | | | | |
| t_{SS_1} | Delay after EN Asserting | EN = 'HI' | | 0.2 | | ms |
| t_{SS_2} | Soft start ramp_up time | $0 V \leq V_{SS} \leq 0.6 V$ | | 0.4 | | ms |
| | | $0 V \leq V_{SS} \leq 0.6 V$, 4 x SS time(option2) | | 1.6 | | |
| $t_{PGDENDLY}$ | PGD startup delay time | $V_{SS} = 0.6 V$ to PGD (SSOK) going high | | 0.3 | | ms |
| | | $V_{SS} = 0.6 V$ to PGD (SSOK), option 2 | | 1.2 | | |
| t_{OVDPDY} | OVP delay time | Time from FB out of +20% of VREF to OVP fault | 1.0 | 1.7 | 2.5 | μs |
| t_{UVDPDY} | UVP delay time | Time from FB out of -20% of VREF to UVP fault | | 10 | | μs |
| f_{SW} | Switching frequency | All modes, $f_{SET} = 0.75 MHz$ | 0.653 | 0.725 | 0.798 | MHz |
| | | All modes, $f_{SET} = 1.1 MHz$ | 0.99 | 1.10 | 1.21 | |
| | | FCCM and DE mode, $f_{SET} = 2 MHz$ | 1.71 | 1.90 | 2.09 | |
| | | HEF mode, $f_{SET} = 2 MHz$ | 1.566 | 1.800 | 2.034 | |
| | Ramp amplitude ⁽⁵⁾ | $2.9 V \leq V_{VIN} \leq 6.0 V$ | | $V_{VIN}/4$ | | V |
| $t_{MIN(off)}$ | Minimum OFF time, FCCM and DE | All frequencies | | 90 | 130 | ns |
| | Minimum OFF time, HEF | $f_{SW} = 1.1 MHz$ | | 160 | 240 | ns |
| D_{MAX} | Maximum duty cycle, FCCM and DE | $f_{SW} = 1.1 MHz$ | 84% | 89% | | |
| D_{MAX} | Maximum duty cycle, HEF | All frequencies | 75% | 81% | | |
| R_{SFTSTP} | Soft-discharge transistor resistance | EN = LO, $V_{VIN} = 3.3 V$, $V_{OUT} = 0.5 V$ | | 60 | | Ω |

(3) See PS pin description for levels.

(4) See RF/OC pin description for levels.

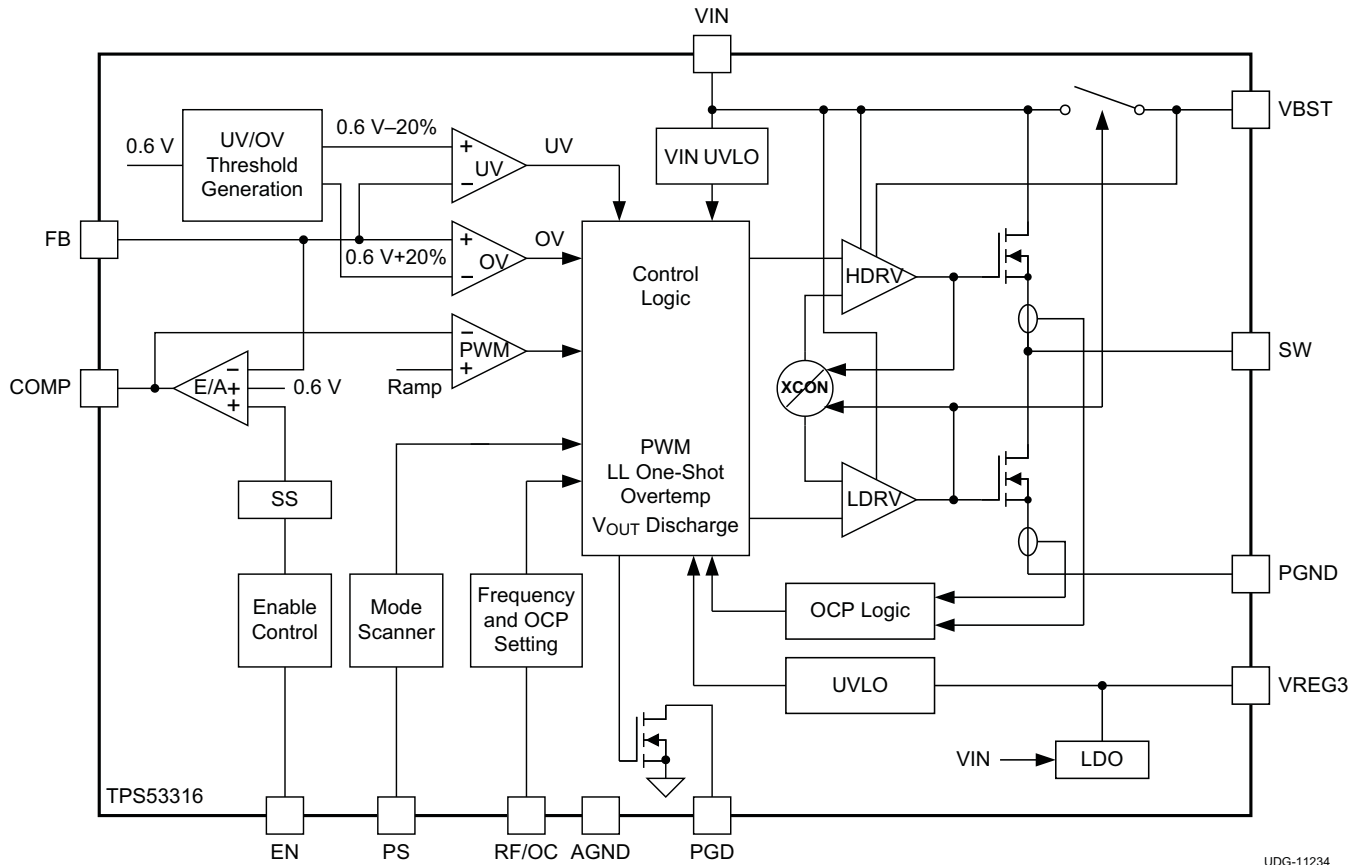
(5) Ensured by design. Not production tested.

DEVICE INFORMATION

PIN DESCRIPTIONS

| PIN | | I/O ⁽¹⁾ | DESCRIPTION |
|----------|-------------|--------------------|--|
| NAME | NO. | | |
| AGND | 11 | G | Device analog ground terminal |
| COMP | 9 | O | Error amplifier compensation terminal. Type III compensation method is generally recommended for stability. |
| EN | 1 | I | Enable pin. Internally pulled-up to the VIN pin through a 2-M Ω resistor. The EN voltage needs to be less than ($V_{IN} + 0.5$ V) |
| FB | 10 | I | Voltage feedback pin. Use for OVP, UVP and PGD determination |
| PGD | 3 | O | Power good output flag. Open drain output. Pull up to an external rail via a resistor |
| PGND | 15 16 | P | Device power ground terminal |
| PS | 8 | I | Mode configuration pin (with 10 μ A current): Connecting to ground: Forced CCM with 4 x soft-start time Pulled high or floating (internal pulled high): Forced CCM master Connect with 24.3 k Ω to GND: HEF mode with 4 x soft-start time, Connect with 57.6 k Ω to GND: HEFF mode Connect with 105 k Ω to GND : DE mode Connect with 174 k Ω to GND: DE Mode with 4 x soft-start time |
| RF/OC | 2 | I | Switching frequency and OC level configuration pin: Connecting to ground: 1.1 MHz, 6.5 A OCP Pulled high or floating (internal pulled high): 1.1 MHz, 4.5 A OCP Connect with 24.3 k Ω to GND: 750 kHz, 4.5 A OCP Connect with 57.6 k Ω to GND: 750 kHz, 6.5 A OCP Connect with 105 k Ω to GND : 2 MHz, 4.5 A OCP Connect with 174 k Ω to GND: 2MHz, 6. 5A OCP |
| SW | 5 6 7 | B | Output inductor connection to integrated power devices |
| VBST | 4 | P | Supply input for high-side MOSFET (bootstrap terminal). Connect capacitor from this pin to SW terminal |
| VREG3 | 12 | O | 3.3V LDO output, serves as supply voltage for internal analog circuitry. The EN pin controls the turn-on function of the LDO. |
| VIN | 13 14 | P | Gate driver supply and power conversion input voltage. The input range is from 2.9 V to 6 V. |
| PowerPad | – | – | Thermal pad of the device. use 4 or 5 vias to connect to GND plane for heat dissipation. |

(1) I – Input; B – Bidirectional; O – Output; G – Ground; P – Supply (or Ground)

FUNCTIONAL BLOCK DIAGRAM



UDG-11234

TYPICAL CHARACTERISTICS

Inductor used: PCMC065T-1R0, 1 μ H, 5.6 m Ω

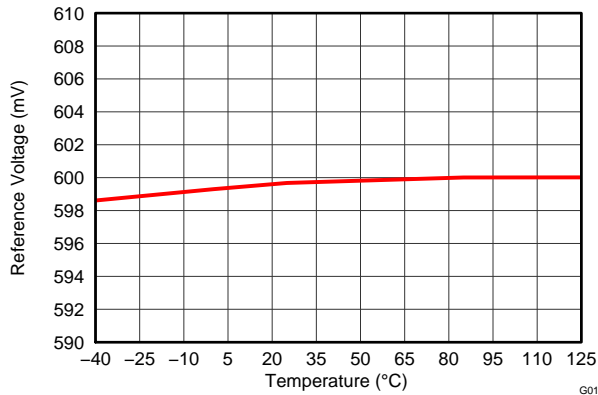


Figure 1. Reference Voltage vs. Temperature

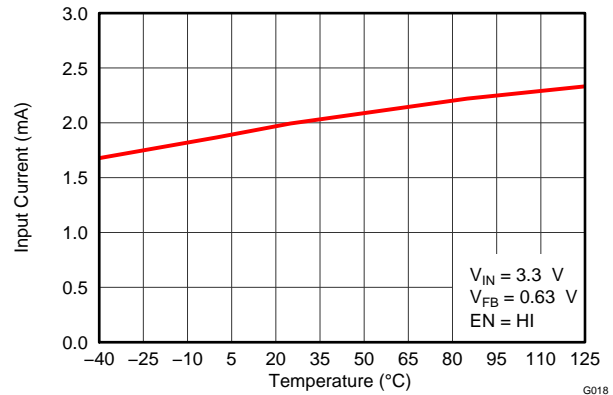


Figure 2. Input Current vs. Temperature

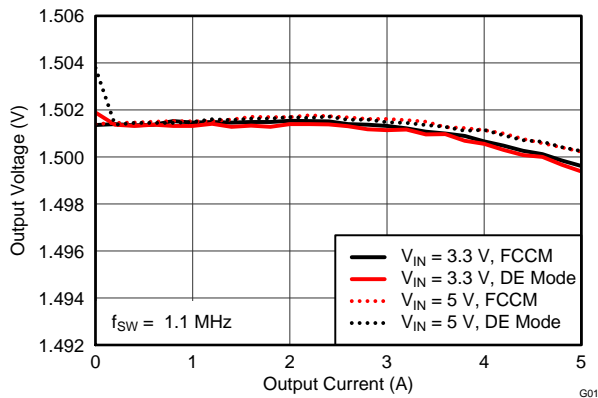


Figure 3. Output Voltage vs. Output Current

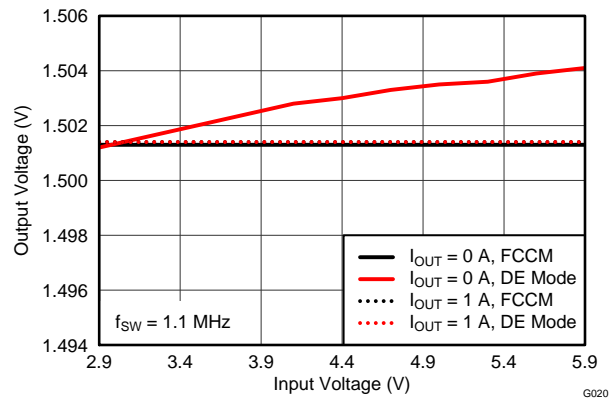


Figure 4. Output Voltage vs. Input Voltage

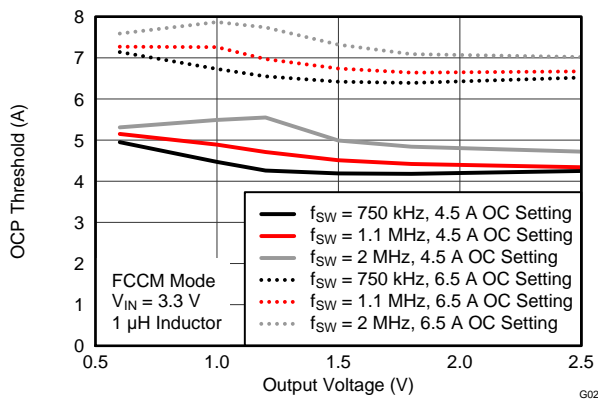


Figure 5. OCP Threshold vs. Output Voltage

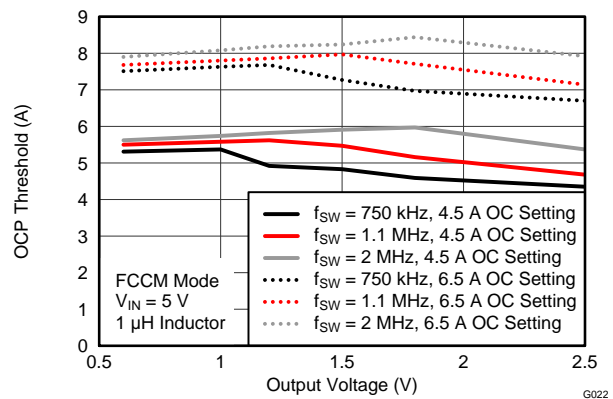


Figure 6. OCP Threshold vs. Output Voltage

TYPICAL CHARACTERISTICS (continued)

Inductor used: PCMC065T-1R0, 1 μ H, 5.6 m Ω

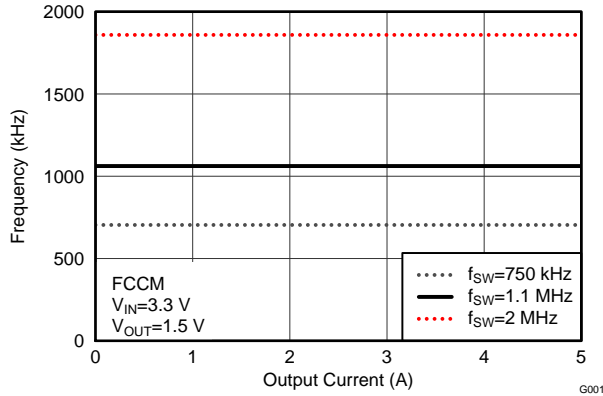


Figure 7. Frequency vs. Output Current, FCCM

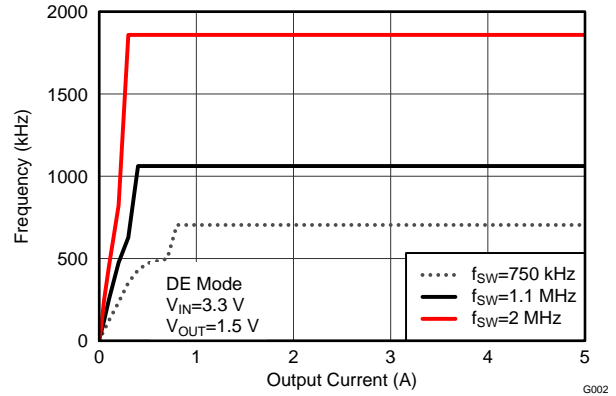


Figure 8. Frequency vs. Output Current, DE Mode

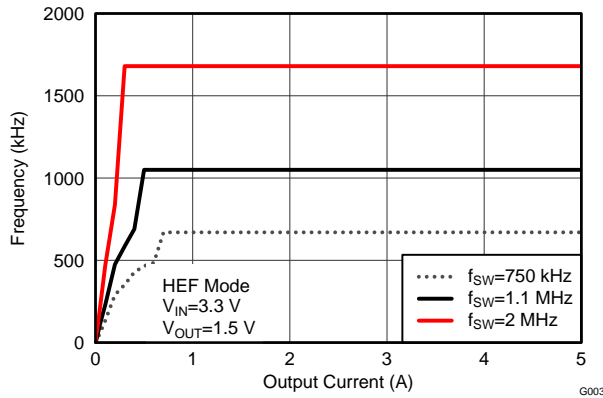


Figure 9. Frequency vs. Output Current, HEF Mode

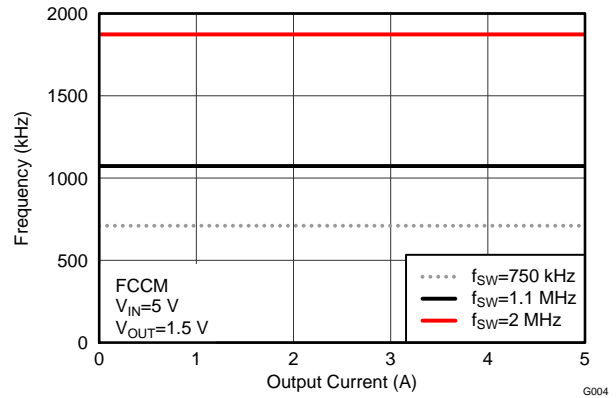


Figure 10. Frequency vs. Output Current, FCCM

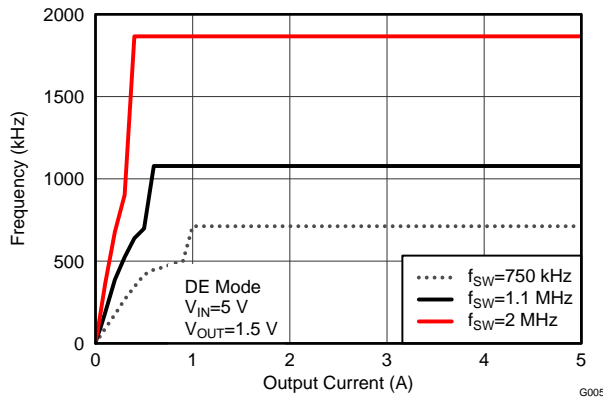


Figure 11. Frequency vs. Output Current, DE Mode

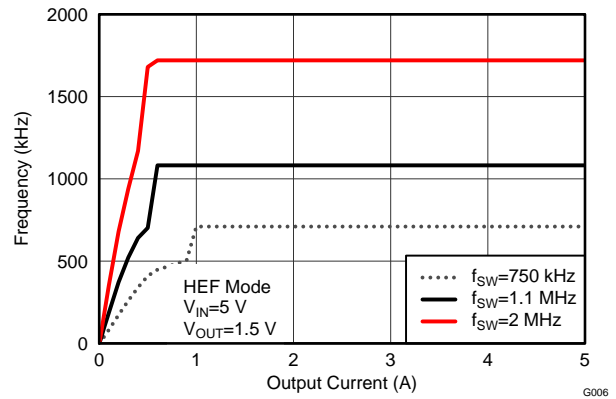


Figure 12. Frequency vs. Output Current, HEF Mode

TYPICAL CHARACTERISTICS (continued)

Inductor used: PCMC065T-1R0, 1 μ H, 5.6 m Ω

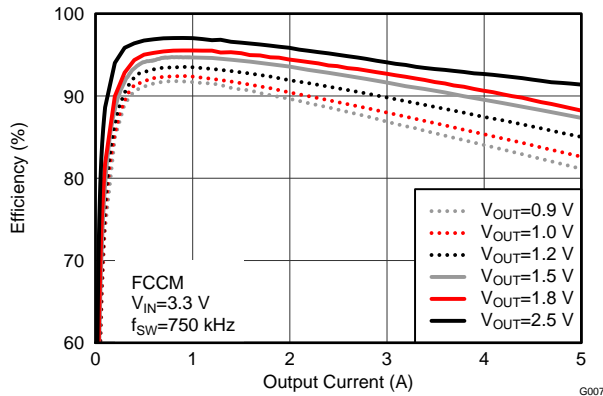


Figure 13. Efficiency vs. Output Current, FCCM

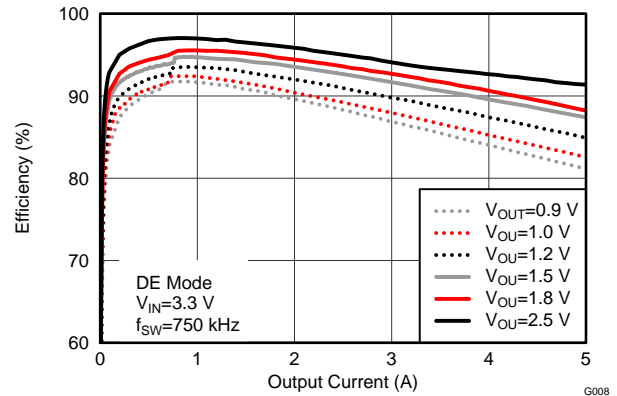


Figure 14. Efficiency vs. Output Current, DE Mode

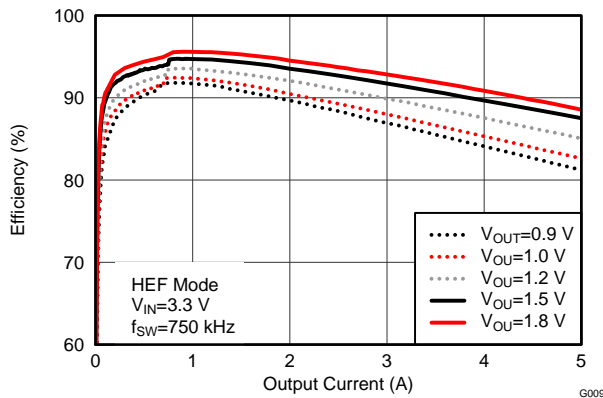


Figure 15. Efficiency vs. Output Current, HEF Mode

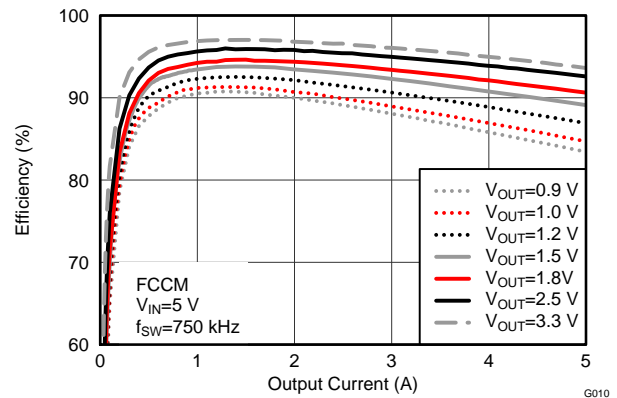


Figure 16. Efficiency vs. Output Current, FCCM

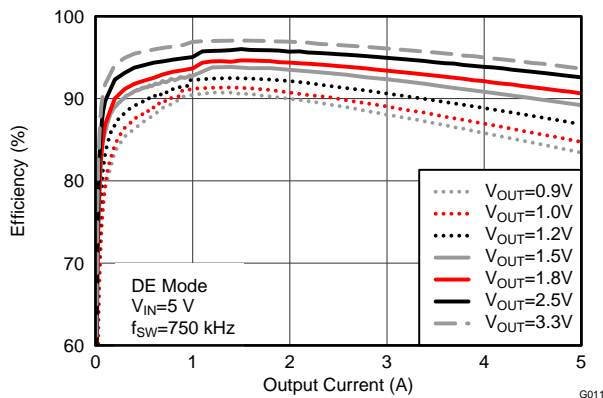


Figure 17. Efficiency vs. Output Current, DE Mode

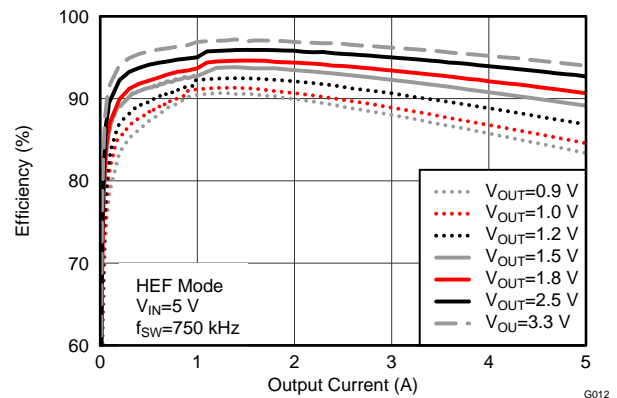


Figure 18. Efficiency vs. Output Current, HEF Mode

TYPICAL CHARACTERISTICS (continued)

Inductor used: PCMC065T-1R0, 1 μ H, 5.6 m Ω

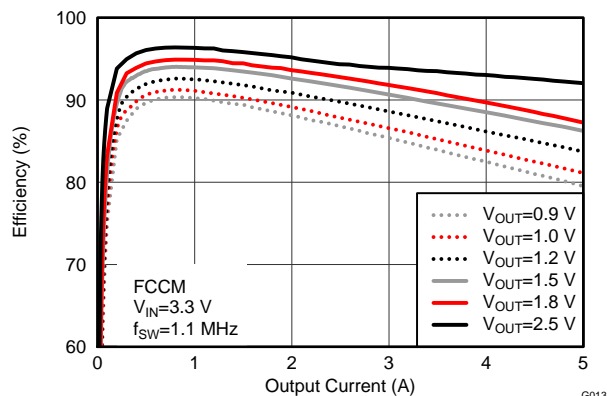


Figure 19. Efficiency vs. Output Current, FCCM

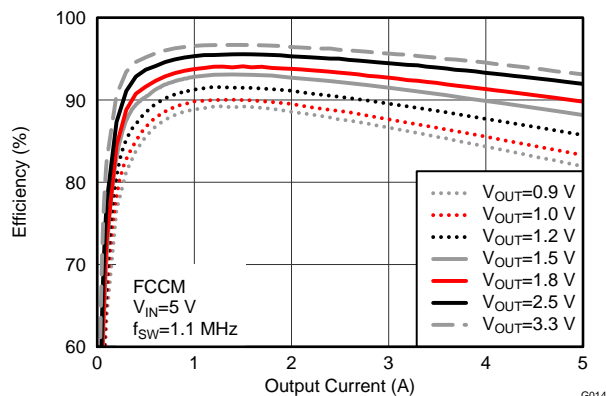


Figure 20. Efficiency vs. Output Current, FCCM

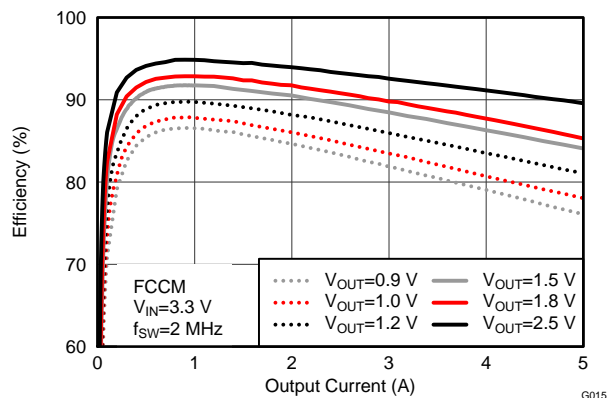


Figure 21. Efficiency vs. Output Current, FCCM

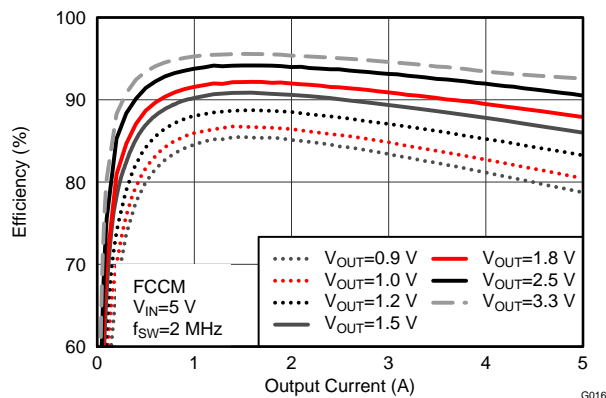


Figure 22. Efficiency vs. Output Current, FCCM

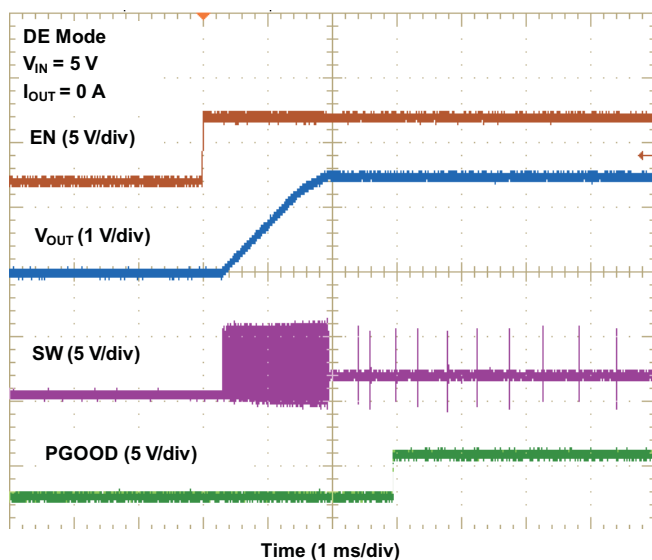


Figure 23. Normal Startup

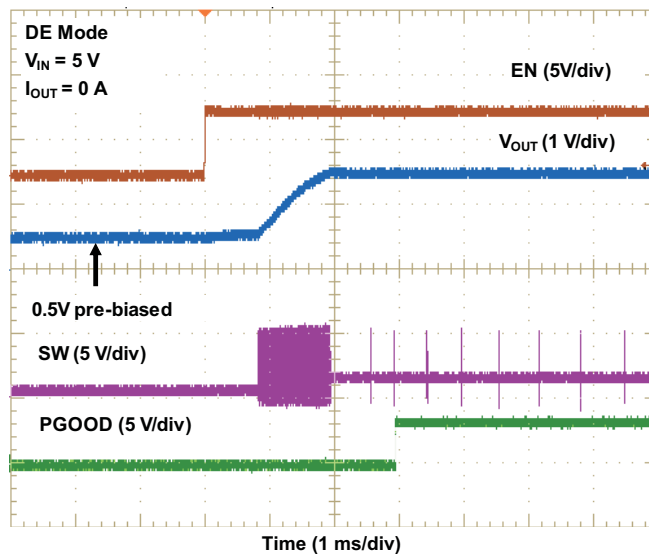


Figure 24. Pre-Biased Startup

TYPICAL CHARACTERISTICS (continued)

Inductor used: PCMC065T-1R0, 1 μ H, 5.6 m Ω

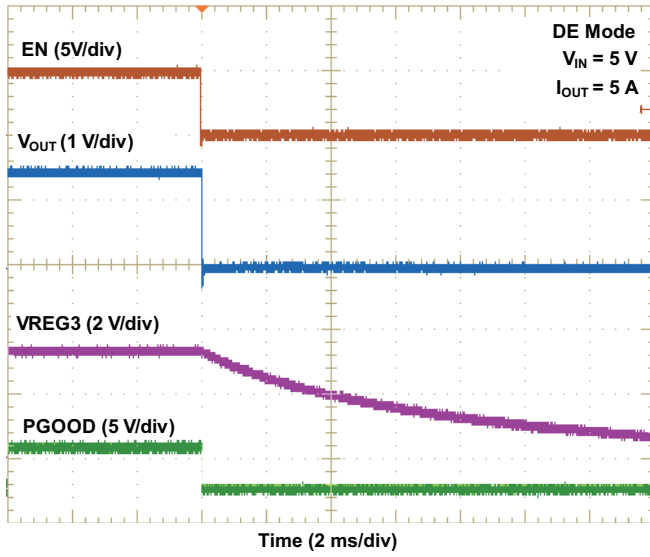


Figure 25. Turn-Off Enable

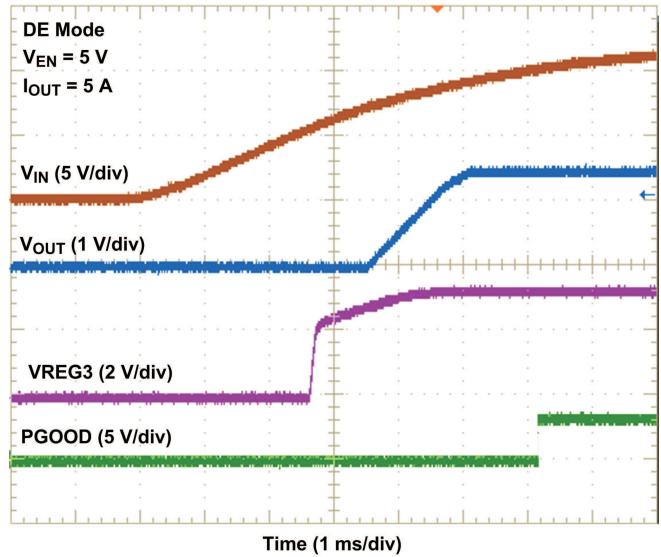


Figure 26. UVLO Start-Up Waveform

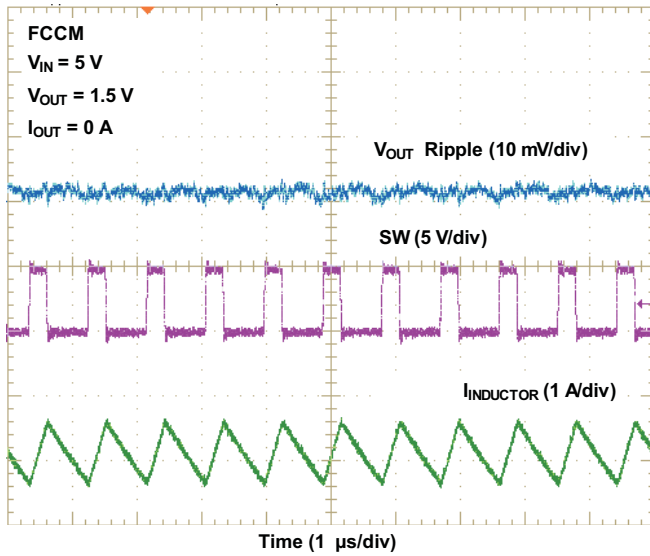


Figure 27. Output Voltage Ripple – FCCM

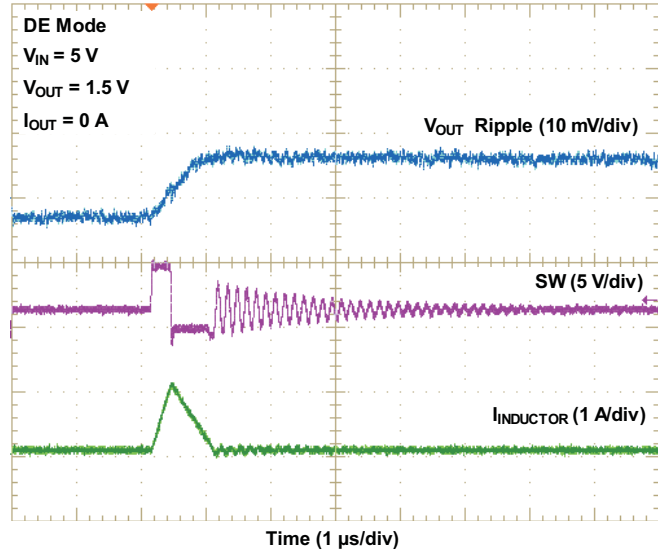


Figure 28. Output Voltage Ripple – DE Mode

TYPICAL CHARACTERISTICS (continued)

Inductor used: PCMC065T-1R0, 1 μ H, 5.6 m Ω

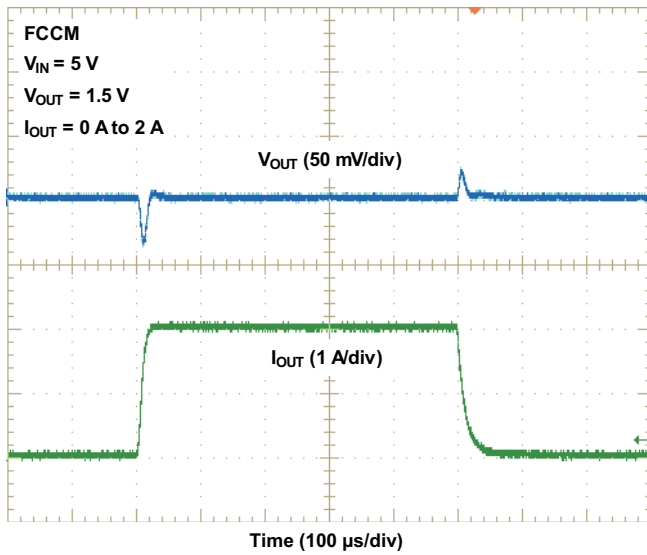


Figure 29. Load Transient – FCCM

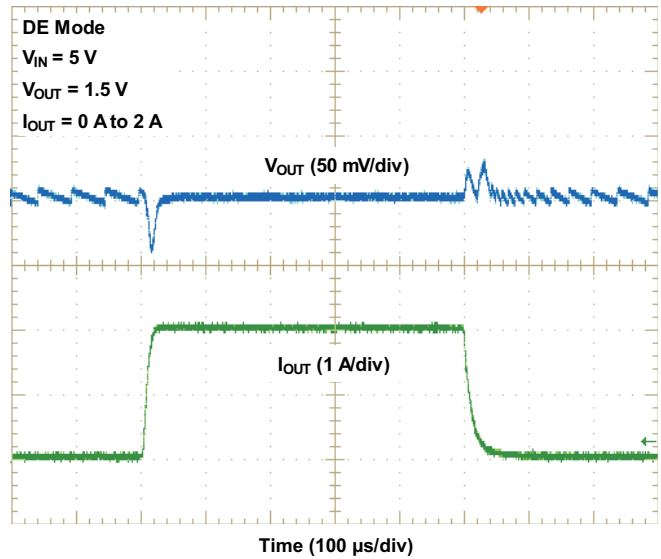


Figure 30. Load Transient – DE Mode

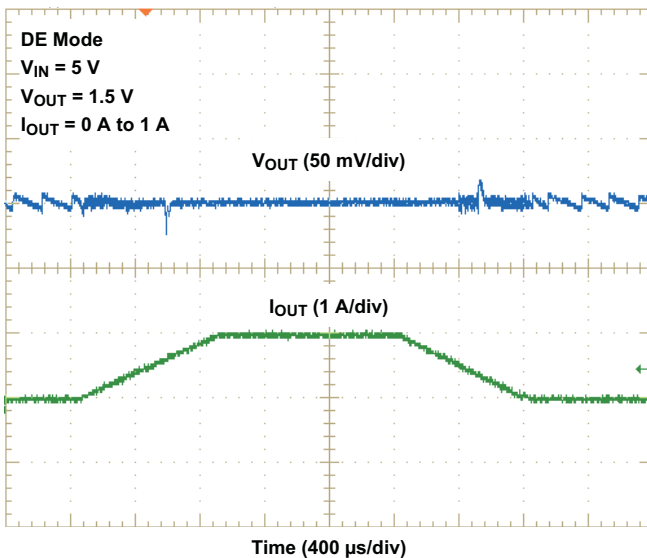


Figure 31. DE Mode DCM and CCM Transition

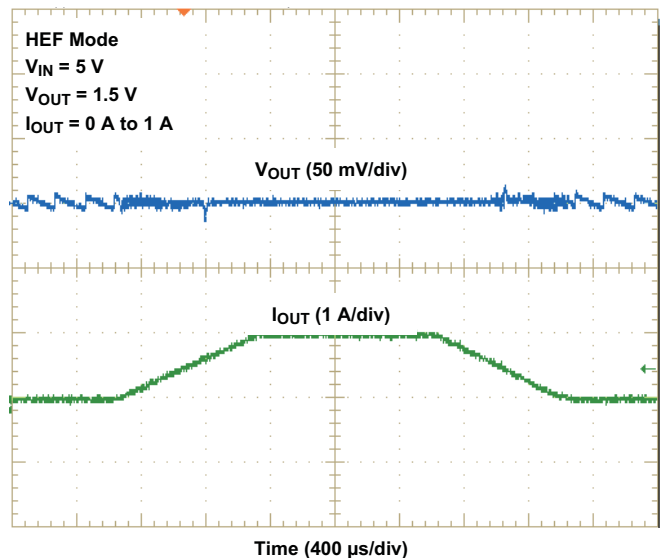


Figure 32. HEF Mode DCM and CCM Transition

TYPICAL CHARACTERISTICS (continued)

Inductor used: PCMC065T-1R0, 1 μ H, 5.6 m Ω

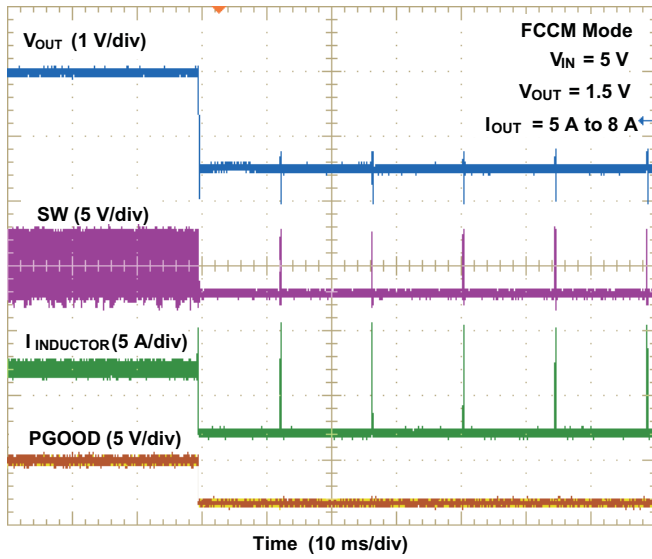


Figure 33. Overcurrent Protection

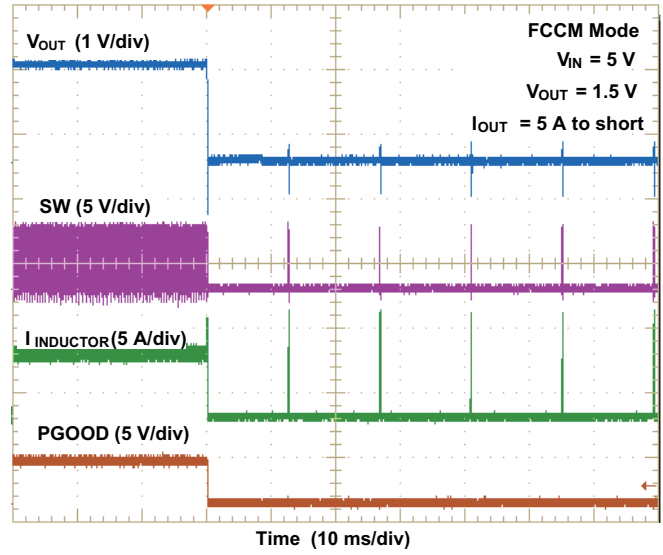


Figure 34. Short Circuit Protection

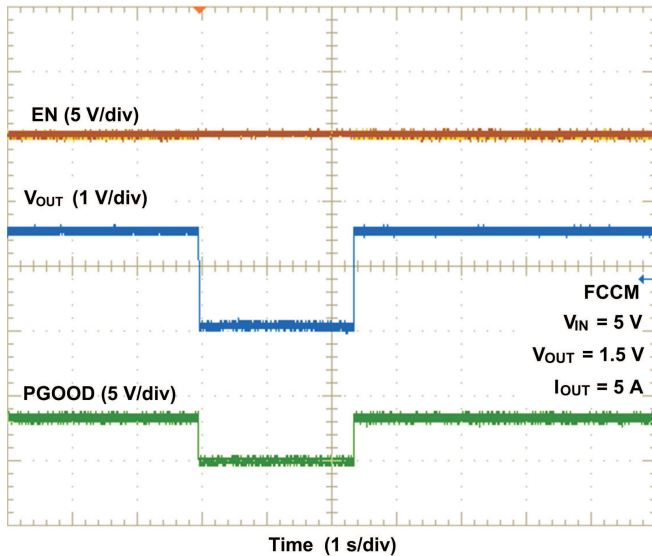


Figure 35. Over Temperature Protection

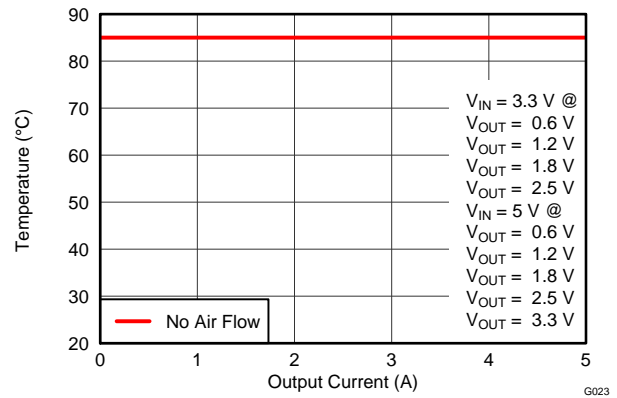


Figure 36. Safe Operating Area

APPLICATION INFORMATION

APPLICATION CIRCUIT DIAGRAM

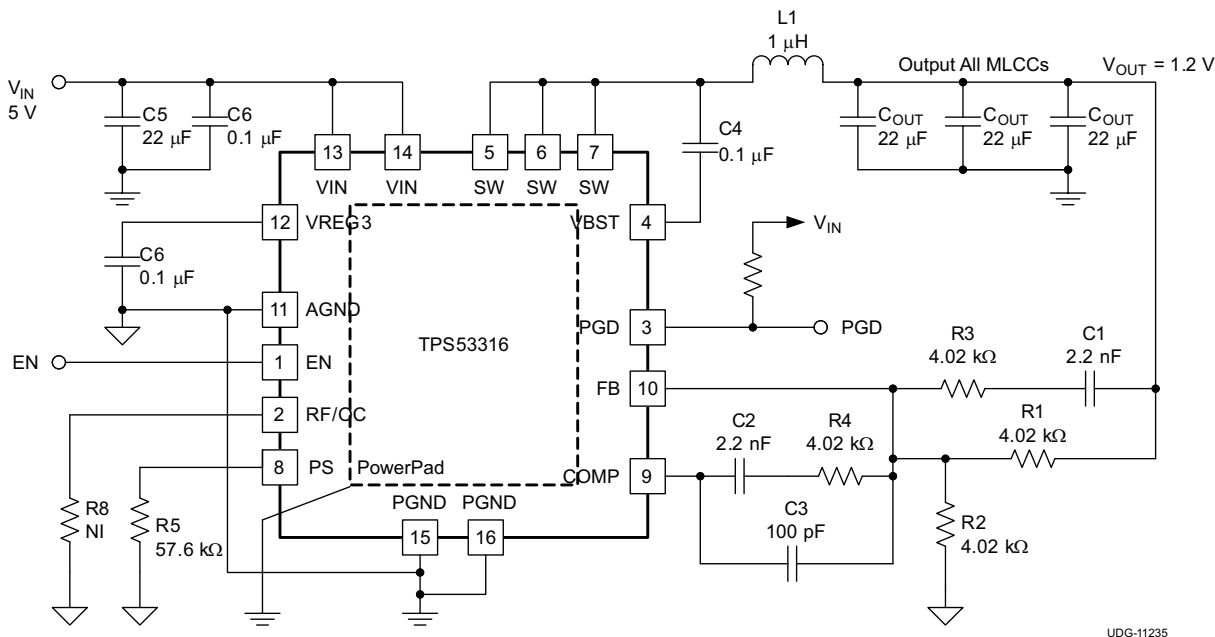


Figure 37. Typical 3.3V input Application Circuit Diagram

OVERVIEW

The TPS53316 is a high-efficiency switching regulator with two integrated N-channel MOSFETs and is capable of delivering up to 5 A of load current. The TPS53316 provides output voltage from 0.6 V up to 0.8 x VIN from 2.9V to 6.0V wide input voltage range.

This device employs 3 operation modes to fit into various application needs. The skip mode operation provides reduced power loss and increases the efficiency at light load. The unique, patented PWM modulator enables smooth light load to heavy load transition while maintaining fast load transient.

OVERCURRENT AND FREQUENCY SETTING

The Overcurrent and frequency setting are determined by RF/OC pin connection as shown in Table 1. At start up, the RF/OC pin sources 10 µA current and then sense the voltage on this pin to determine the switching frequency and OCP threshold.

Table 1. Overcurrent and Frequency Setting

| RF/OC PIN CONNECTION | FREQUENCY (kHz) | OVERCURRENT THRESHOLD (A) |
|-----------------------------|-----------------|---------------------------|
| GND | 1100 | 6.5 |
| 24.3 kΩ to GND | 750 | 4.5 |
| 57.6 kΩ to GND | 750 | 6.5 |
| 105 kΩ to GND | 2000 | 4.5 |
| 174 kΩ to GND | 2000 | 6.5 |
| Floating or pulled to VREG3 | 1100 | 4.5 |

OPERATION MODE

The TPS53316 has 3 operation modes determined by PS connection as listed in [Table 2](#). Each mode has two soft-start and power good delay options (1× and 4×). At start-up, the PS pin sources 10 μA of current and then sense the voltage on this pin to determine the operation mode and soft-start time.

Table 2. Operation Mode Selection

| PS PIN CONNECTION | OPERATION MODE | AUTO-SKIP AT LIGHT LOAD | SOFT-START TIME |
|-----------------------------|----------------|-------------------------|-----------------|
| GND | FCCM | No | 4 x |
| 24.3 kΩ to GND | HEF Mode | Yes | 4 x |
| 57.6 kΩ to GND | HEF Mode | Yes | 1 x |
| 105 kΩ to GND | DE Mode | Yes | 1 x |
| 174 kΩ to GND | DE Mode | Yes | 4 x |
| Floating or pulled to VREG3 | FCCM | No | 1 x |

In forced continuous conduction mode (FCCM), the high-side FET is ON during the on-time and low-side FET is ON during the off-time. The switching is synchronized to the internal clock thus the switching frequency is fixed.

In diode emulation mode (DE), the high-side FET is ON during the on-time and low-side FET is ON during the off-time until the inductor current reaches zero. An internal zero-crossing comparator detects the zero crossing of inductor current from positive to negative. When the inductor current reaches zero, the comparator sends a signal to the logic control and turns off the low-side FET.

When the load is increased, the inductor current is always positive and the zero-crossing comparator does not send a zero-crossing signal. The converter enters into continuous conduction mode (CCM) when no zero-crossing is detected for two consecutive PWM pulses. The switching is synchronized to the internal clock and the switching frequency is fixed.

In high-efficiency mode (HEF), the converter does not synchronize to internal clock during CCM. Instead, the PWM modulator determines the switching frequency. The operation in discontinuous conduction mode (DCM) is the same as DE mode.

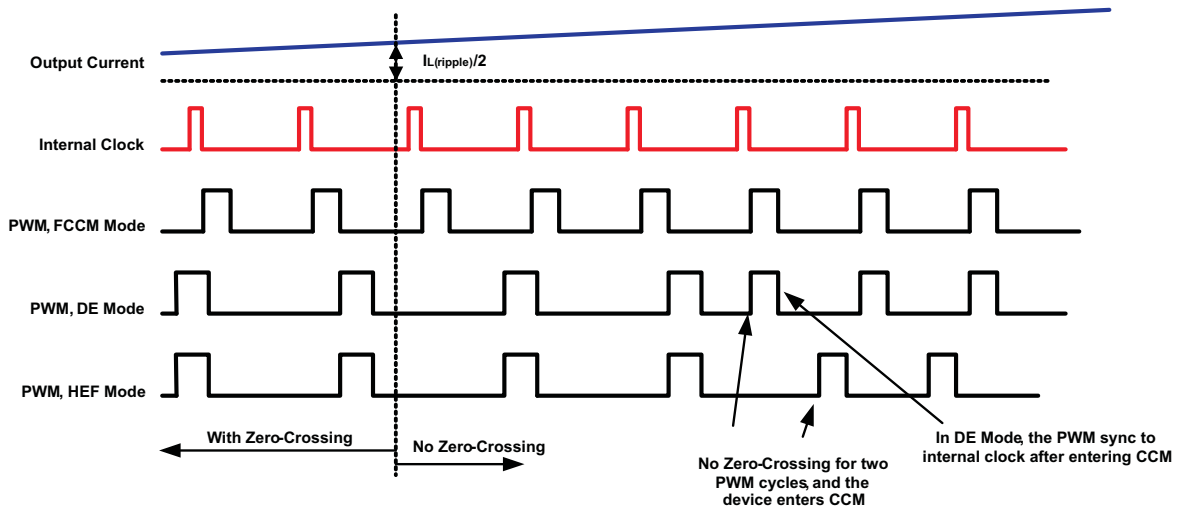
In both DE and HEF modes, the device operates under CCM with fixed SW frequency if the load current is higher than half of the inductor ripple current. When the load current is decreased and seven consecutive zero-crossing events are detected, the device enters DCM and light load control is enabled. The on-pulse in DCM is designed to be 25% higher than CCM to provide hysteresis to avoid chattering between CCM and DCM.

The PS pins also set the soft-start time and power good start-up delay of the device. The nominal sort-start time is 400 μs from the time $V_{OUT} = 0$ V to when $V_{OUT} = 100\%$, and the nominal power good delay is 300 μs from the time $V_{OUT} = 100\%$ to when power good is asserted. When the PS pin is connected to GND directly or with a resistor with a value of 24.3 kΩ or 174 kΩ, the soft-start time and power good delay is 4 times the nominal (1.6 ms for soft-start time and 1.2 ms for power good delay).

LIGHT LOAD OPERATION

In skip modes (DE and HEF), when the load current is less than half of inductor ripple current, the inductor current reaches zero by the end of OFF-Time. The light load control scheme then turns off the low-side MOSFET when inductor current reaches zero. Since there is no negative inductor current, the energy delivered to the load per switching cycle is increased compared to the normal PWM mode operation. The controller then reduces the switching frequency to maintain the output voltage regulation. The switching loss is reduced and thus efficiency is improved.

In both DE and HEF mode, when the load current decreases, the switching frequency also decreases continuously in discontinuous conduction mode (DCM). When the load current is 0 A, the minimum switching frequency is reached. It is also required that the difference between V_{VBST} and V_{SW} to be higher than 2.4 V to ensure the supply for high-side gate driver.



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Figure 38. TPS53316 Operation Modes in Light and Heavy Load Conditions

FORCED CONTINUOUS CONDUCTION MODE

When the PS pin is grounded or greater than 2.2 V, the TPS53316 is operating in continuous conduction mode in both light and heavy load condition. In this mode, the switching frequency remains constant over the entire load range which is suitable for applications need tight control of switching frequency at a cost of lower efficiency at light load.

SOFT-START OPERATION

The soft-start operation reduces the inrush current during the start-up time. A slow rising reference is generated by the soft-start circuitry and send to the input of the error amplifier. When the soft-start ramp voltage is less than 600 mV, the error amplifier uses this ramp voltage as the reference. When the ramp voltage reaches 600 mV, the error amplifier switch to a fixed 600 mV reference. The typical soft-start time is 400 μ s for 1 \times soft-start time setting and 1.6 ms for 4 \times the soft-start time setting.

POWER GOOD

The TPS53316 monitors the voltage on the FB pin. If the FB voltage is within 117% and 83% of the reference voltage, the power good signal remains high. If FB voltage is out of this window, power good pin is pulled low by the internal open drain output.

During start-up operation, the input voltage must be higher than 1 V in order to have valid power good logic, and the power good signal has 300 μ s (1.2 ms with 4x setting) delay after FB falling into the power good window. There is also 10- μ s delay during shut down after FB falling out of the power good window.

UVLO FUNCTION

The TPS53316 provides UVLO protection for input voltage. If the input voltage is higher than UVLO threshold voltage, the device starts up. When the voltage becomes lower than the threshold voltage minus the hysteresis, the device shuts off. The typical UVLO rising threshold is 2.8 V and the hysteresis is 130 mV.

A similar UVLO function is provided to the VREG3 pin. The typical UVLO rising threshold is 2.8V and the hysteresis is 75 mV for VREG3.

OVERCURRENT PROTECTION

The TPS53316 continuously monitors the current flowing through high-side and low-side MOSFETs. If the current through the high-side FET exceeds 6.8 A (or 4.5 A with 4.5 A setting), the high-side FET turns off and the low-side FET turns on. An OC counter starts to increment to count the occurrence of the overcurrent events. The converter shuts down immediately when the OC counter reaches 4. The OC counter resets if the detected current is less 6.8 A after an OC event.

Another set of overcurrent circuitry monitors the current through low-side FET. If the current through the low-side FET exceeds 7.5 A (or 5.1 A with 4.5 A setting), the overcurrent protection is engaged and turns off both high-side and low-side FETs immediately. The device is fully protected against overcurrent during both on-time and off-time.

After an OCP event, the device will attempt to restart after a hiccup delay (14.5 ms typical). If the OC condition clears before restart, the device starts up normally. Otherwise the hiccup process repeats.

OVERVOLTAGE PROTECTION

The TPS53316 monitors the voltage divided feedback voltage to detect the overvoltage and undervoltage conditions. When the feedback voltage is greater than 117% of the reference, the high-side MOSFET turns off and the low-side MOSFET turns on. Then the output voltage drops and reaches the undervoltage threshold. At that point the low-side MOSFET turns off and the device enters high-impedance state.

UNDERVOLTAGE PROTECTION

When the feedback voltage is lower than 83% of the reference voltage, the undervoltage protection counter starts. If the feedback voltage remains lower than the undervoltage threshold voltage after 10 μ s, the device turns off both high-side and low-side MOSFETs and enters high-impedance state. After a hiccup delay (14.5 ms typical), the device attempts to restart. If the UV condition clears before restart, the device starts up normally. Otherwise the hiccup process repeats.

OVERTEMPERATURE PROTECTION

The TPS53316 continuously monitors the die temperature. If the die temperature exceeds the threshold value (140°C typical), the device shuts off. When the device is cooled to 40°C below the overtemperature threshold, it restarts and returns to normal operation.

OUTPUT DISCHARGE

When the EN pin is low, the TPS53316 discharges the output capacitors through an internal MOSFET switch between SW and GND while the high-side and low-side MOSFETs remain OFF. The typical discharge switch on resistance is 60 Ω . This function is disabled when the input voltage is less than 1 V.

EXTERNAL COMPONENTS SELECTION

Step One: Determine the Value of R1 and R2

The output voltage is programmed by the voltage-divider resistor, R1 and R2 shown in [Figure 37](#). R1 is connected between VFB pin and the output, and R2 is connected between the VFB pin and GND. Recommended value for R1 is between 1 kΩ and 10 kΩ. Determine R2 using [Equation 1](#).

$$R2 = \frac{0.6}{V_{OUT} - 0.6} \times R1 \quad (1)$$

Step Two: Choose the Inductor

The inductance value should be determined to give the ripple current of approximately 20% to 40% of maximum output current. The inductor ripple current is determined by [Equation 2](#):

$$I_{L(\text{ripple})} = \frac{1}{L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (2)$$

The inductor also must have a low DCR to achieve good efficiency, as well as enough room above peak inductor current before saturation.

Step Three: Choose the Output Capacitor(s)

The output capacitor selection is determined by output ripple and transient requirement. When operating in CCM, the output ripple has three components. $V_{RIPPLE(C)}$ represents the ripple due to the output capacitance and is shown in [Equation 4](#).

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)} \quad (3)$$

$$V_{RIPPLE(C)} = \frac{I_{L(\text{ripple})}}{8 \times C_{OUT} \times f_{SW}} \quad (4)$$

$$V_{RIPPLE(ESR)} = I_{L(\text{ripple})} \times ESR \quad (5)$$

$$V_{RIPPLE(ESL)} = \frac{V_{IN} \times ESL}{L} \quad (6)$$

When ceramic output capacitor is chosen, the ESL component is usually negligible. In the case when multiple output capacitors are used, the total ESR and ESL should be the equivalent of the all output capacitors in parallel.

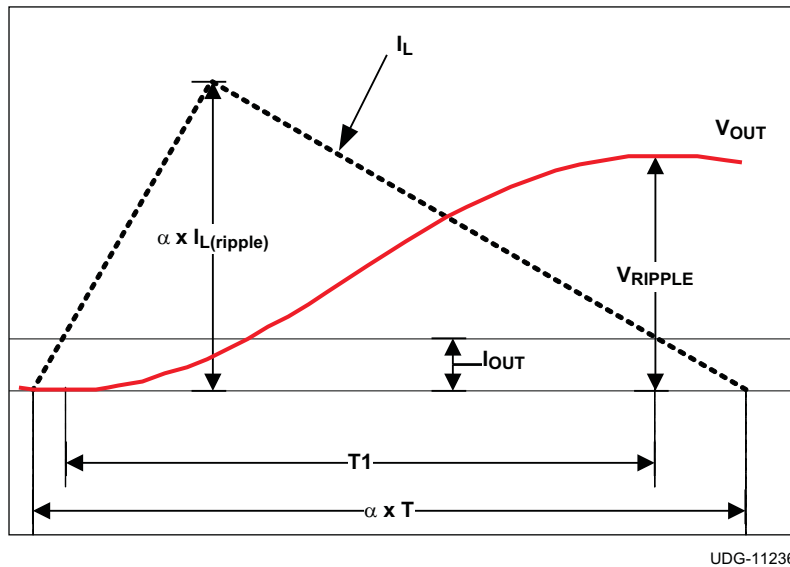
When operating in DCM, the output ripple is dominated by the component determined by capacitance. It also varies with load current and can be expressed as shown in [Equation 7](#).

$$V_{RIPPLE(DCM)} = \frac{(\alpha \times I_{L(\text{ripple})} - I_{OUT})^2}{2 \times f_{SW} \times C_{OUT} \times I_{L(\text{ripple})}}$$

where

- α is the DCM on-time coefficient (typical value is 1.25) and can be expressed as
$$\alpha = \frac{t_{ON(DCM)}}{t_{ON(CCM)}} \quad (7)$$

[Figure 39](#) illustrates the DCM output voltage ripple.


Figure 39. Discontinuous Mode Output Voltage Ripple

Step Four: Choose the Input Capacitors

The selection of input capacitor should be determined by the ripple current requirement. The ripple current generated by the converter needs to be absorbed by the input capacitors as well as the input source. The RMS ripple current from the converter can be expressed as shown in [Equation 8](#).

$$I_{IN(ripple)} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

where

$$D = \frac{V_{OUT}}{V_{IN}} \quad (8)$$

- D is the duty cycle and can be expressed as

To minimize the ripple current drawn from the input source, sufficient input decoupling capacitors should be placed close to the device. The ceramic capacitor is recommended due to the low ESR and low ESL. The input voltage ripple can be calculated as below when the total input capacitance is determined:

$$V_{IN(ripple)} = \frac{I_{OUT} \times D}{f_{SW} \times C_{IN}} \quad (9)$$

Compensation Design

The TPS53316 employs voltage mode control. To effectively compensation the power stage and ensures fast transient response, Type III compensation is typically used.

The control to output transfer function can be described in [Equation 10](#).

$$G_{CO} = 4 \times \frac{1 + s \times C_{OUT} \times ESR}{1 + s \times \left(\frac{L}{DCR + R_{LOAD}} + C_{OUT} \times (ESR + DCR) \right) + s^2 \times L \times C_{OUT}} \quad (10)$$

The output LC filter introduces a double pole which can be calculated in [Equation 11](#).

$$f_{DP} = \frac{1}{2 \times \pi \times \sqrt{L \times C_{OUT}}} \quad (11)$$

The ESR zero of can be calculated in [Equation 12](#).

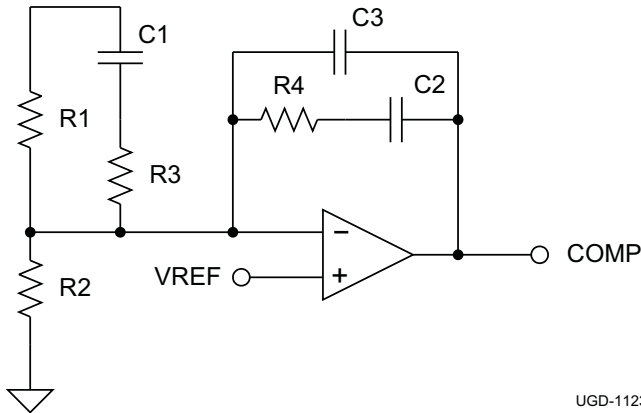
$$f_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}} \quad (12)$$

Figure 40 shows the configuration of Type III compensation and typical pole and zero locations. The following equations describe the compensator transfer function and poles and zeros of the Type III network.

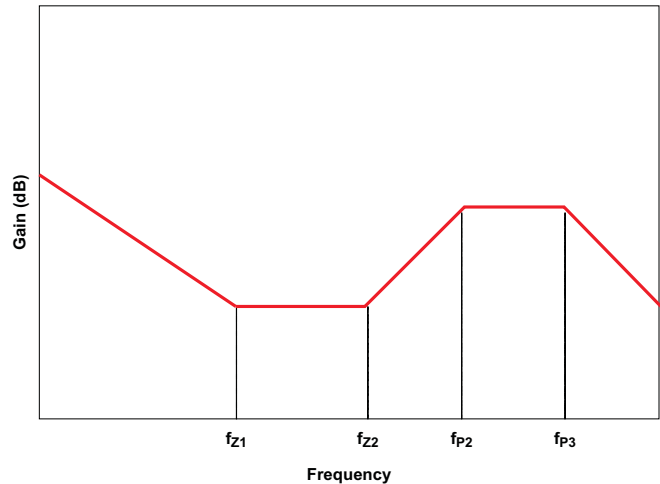
$$G_{EA} = \frac{(1 + s \times C1 \times (R1 + R3))(1 + s \times R4 \times C2)}{(s \times R1 \times (C2 + C3)) \times (1 + s \times C1 \times R3) \times \left(1 + s \times R4 \times \frac{C2 \times C3}{C2 + C3}\right)} \quad (13)$$

$$f_{Z1} = \frac{1}{2 \times \pi \times R4 \times C2} \quad (14)$$

$$f_{Z2} = \frac{1}{2 \times \pi \times (R1 + R3) \times C1} \cong \frac{1}{2 \times \pi \times R1 \times C1} \quad (15)$$



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Figure 40. Type III Compensation Network Schematic

Figure 41. Type III Compensation Network Waveform

$$f_{P1} = 0 \quad (16)$$

$$f_{P2} = \frac{1}{2 \times \pi \times R3 \times C1} \quad (17)$$

$$f_{P3} = \frac{1}{2 \times \pi \times R4 \times \left(\frac{C2 \times C3}{C2 + C3}\right)} \cong \frac{1}{2 \times \pi \times R4 \times C3} \quad (18)$$

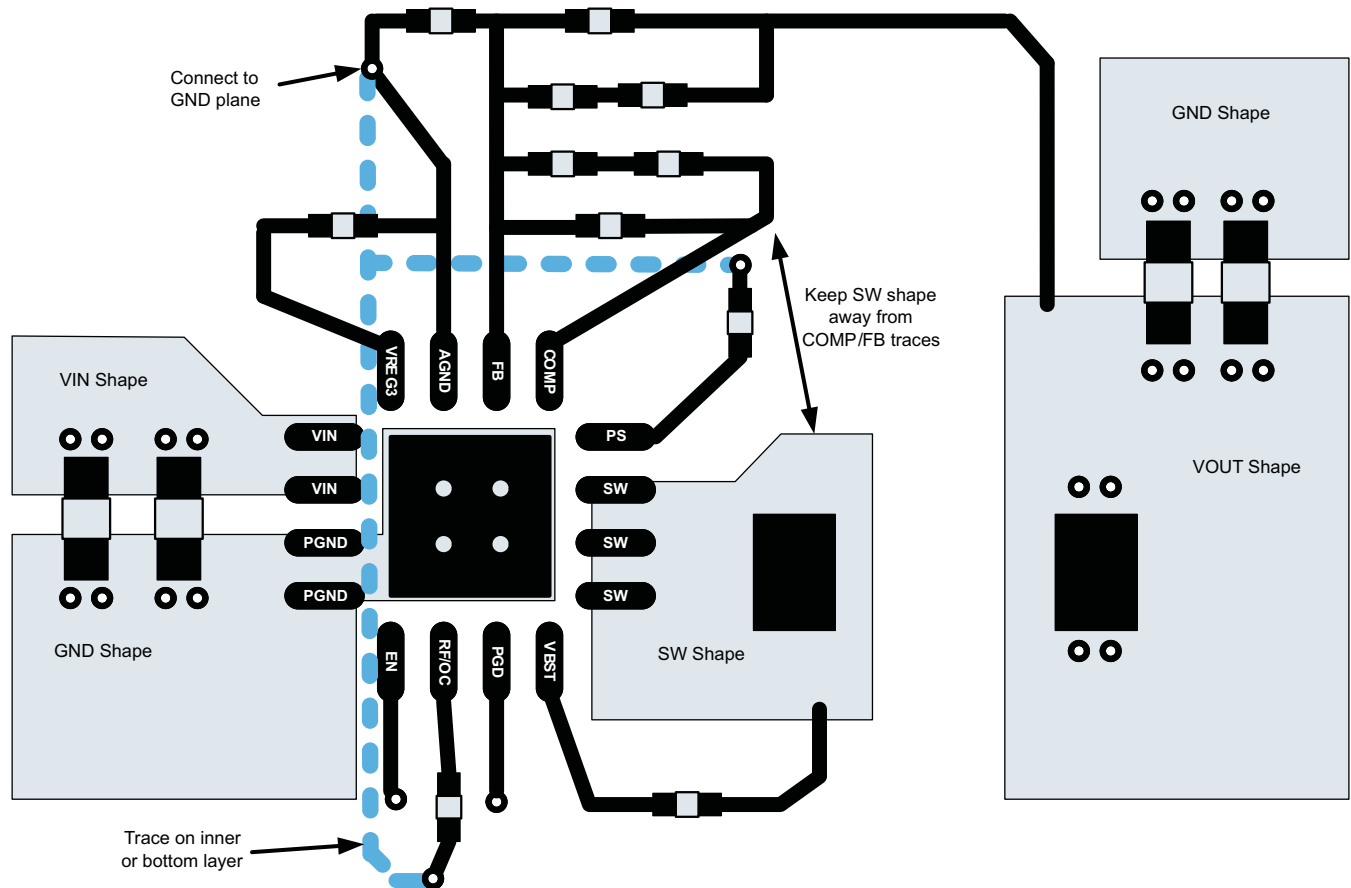
The two zeros can be placed near the double pole frequency to cancel the response from the double pole. One pole can be used to cancel ESR zero, and the other non-zero pole can be placed at half switching frequency to attenuate the high frequency noise and switching ripple. Suitable values can be selected to achieve a compromise between high phase margin and fast response. A phase margin higher than 45° is required for stable operation.

For DCM operation, a C3 capacitor value between 56 pF and 150 pF is recommended for output capacitance between 20 µF to 200 µF.

LAYOUT CONSIDERATIONS

Good layout is essential for stable power supply operation. Follow these guidelines for an efficient PCB layout:

- Separate the power ground and analog ground. Connect analog ground to GND plane with single via or a 0 Ω resistor at a quiet place.
- Use 4 vias to connect the thermal pad to power ground.
- Place VIN and VREG3 decoupling capacitors as close to the device as possible.
- Use wide traces for VIN, VOUT, PGND and SW. These nodes carry high-current and also serve as heat sinks.
- Place feedback and compensation components as close to the device as possible.
- Keep analog signals (FB, COMP) away from noisy signals (SW, VBST).
- Refer to TPS53316 evaluation kit for a layout example.



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Figure 42. Layout Guidelines

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| TPS53316RGTR | ACTIVE | QFN | RGT | 16 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 3316 | Samples |
| TPS53316RGTT | ACTIVE | QFN | RGT | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 3316 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS53316RGTR | QFN | RGT | 16 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS53316RGTT | QFN | RGT | 16 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

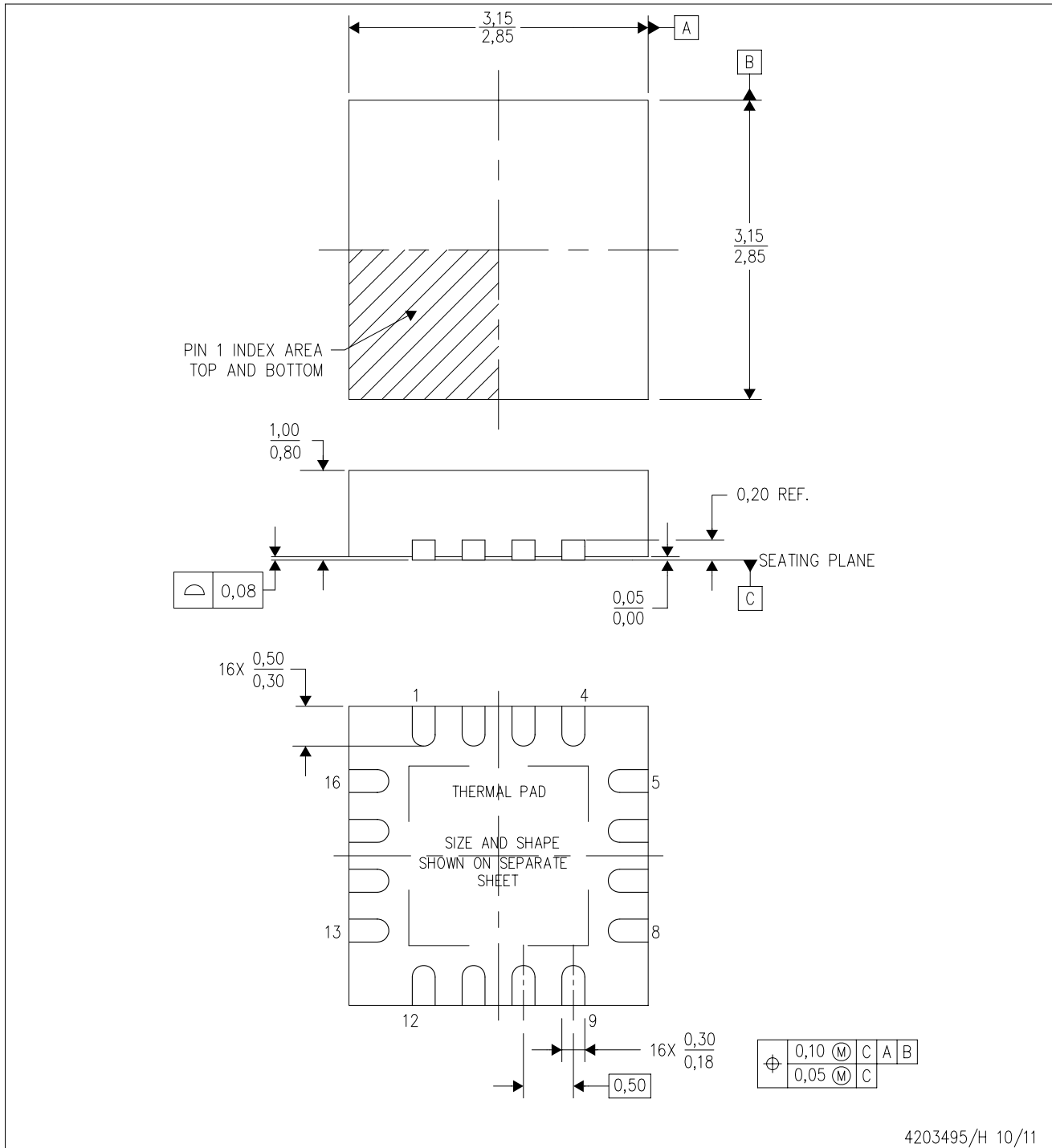
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS53316RGTR | QFN | RGT | 16 | 3000 | 367.0 | 367.0 | 35.0 |
| TPS53316RGTT | QFN | RGT | 16 | 250 | 210.0 | 185.0 | 35.0 |

RGT (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203495/H 10/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Quad Flatpack, No-leads (QFN) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-220.

THERMAL PAD MECHANICAL DATA

RGT (S-PVQFN-N16)

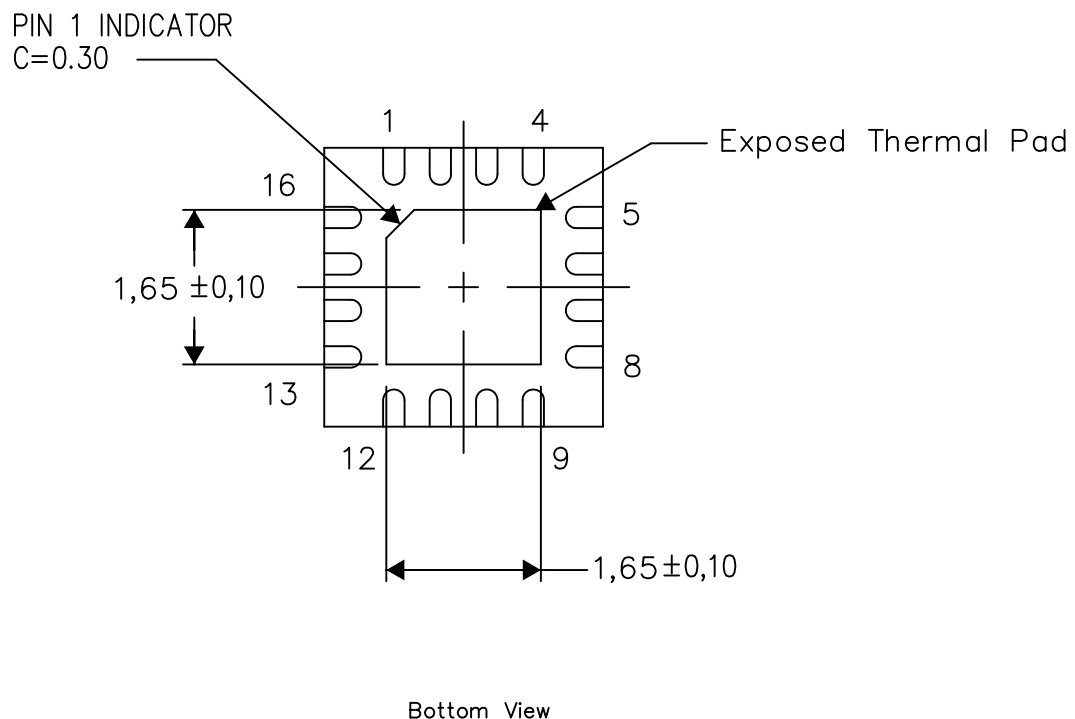
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



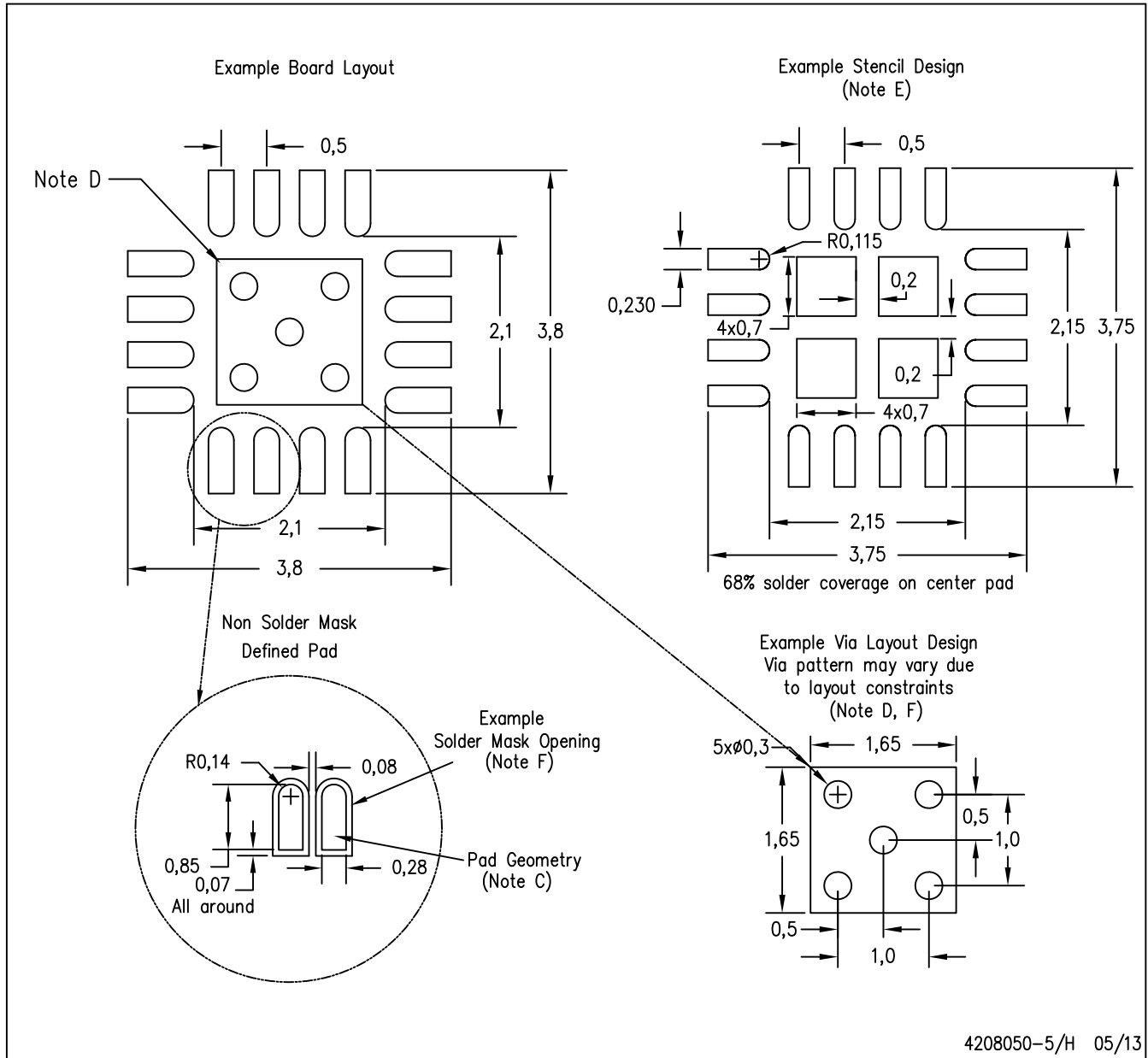
Exposed Thermal Pad Dimensions

4206349-7/S 04/13

NOTE: All linear dimensions are in millimeters

RGT (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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