

## Low Quiescent Current, Programmable-Delay Supervisory Circuit

### FEATURES

- Power-On Reset Generator with Adjustable Delay Time: 1.25ms to 10s
- Very Low Quiescent Current: 2.4µA typ
- High Threshold Accuracy: 0.5% typ
- Fixed Threshold Voltages for Standard Voltage Rails from 0.9V to 5V and Adjustable Voltage Down to 0.4V Are Available
- Manual Reset ( $\overline{\text{MR}}$ ) Input
- Open-Drain  $\overline{\text{RESET}}$  Output
- Temperature Range:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Small SOT23 and 2mm x 2mm QFN Packages

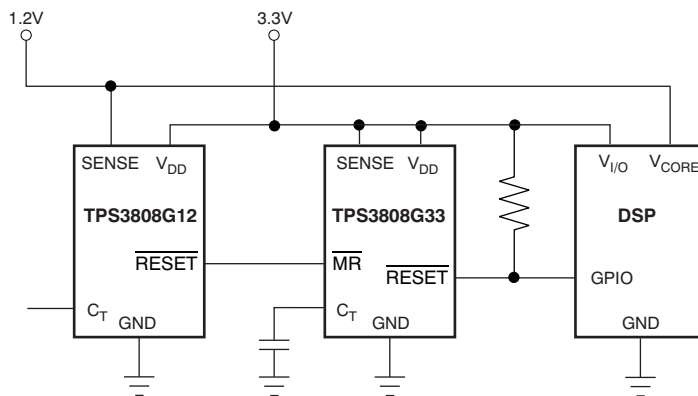
### APPLICATIONS

- DSP or Microcontroller Applications
- Notebook/Desktop Computers
- PDAs/Hand-Held Products
- Portable/Battery-Powered Products
- FPGA/ASIC Applications

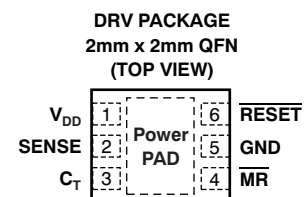
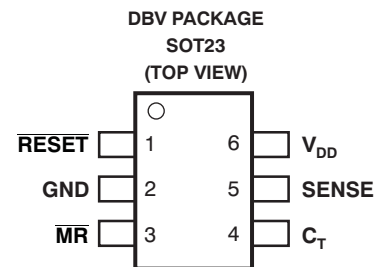
### DESCRIPTION

The TPS3808xxx family of microprocessor supervisory circuits monitor system voltages from 0.4V to 5.0V, asserting an open-drain  $\overline{\text{RESET}}$  signal when the SENSE voltage drops below a preset threshold or when the manual reset (MR) pin drops to a logic low. The  $\overline{\text{RESET}}$  output remains low for the user-adjustable delay time after the SENSE voltage and manual reset ( $\overline{\text{MR}}$ ) return above the respective thresholds.

The TPS3808 uses a precision reference to achieve 0.5% threshold accuracy for  $V_{\text{IT}} \leq 3.3\text{V}$ . The reset delay time can be set to 20ms by disconnecting the  $C_{\text{T}}$  pin, 300ms by connecting the  $C_{\text{T}}$  pin to  $V_{\text{DD}}$  using a resistor, or can be user-adjusted between 1.25ms and 10s by connecting the  $C_{\text{T}}$  pin to an external capacitor. The TPS3808 has a very low typical quiescent current of 2.4µA so it is well-suited to battery-powered applications. It is available in a small SOT23 and an ultra-small 2mm x 2mm QFN PowerPAD™ package, and is fully specified over a temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  ( $T_{\text{J}}$ ).



**Typical Application Circuit**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	NOMINAL SUPPLY VOLTAGE <sup>(2)</sup>	THRESHOLD VOLTAGE ( $V_{IT}$ )
TPS3808G01	Adjustable	0.405V
TPS3808G09	0.9V	0.84V
TPS3808G12	1.2V	1.12V
TPS3808G125	1.25V	1.16V
TPS3808G15	1.5V	1.40V
TPS3808G18	1.8V	1.67V
TPS3808G19	1.9V	1.77V
TPS3808G25	2.5V	2.33V
TPS3808G30	3.0V	2.79V
TPS3808G33	3.3V	3.07V
TPS3808G50	5.0V	4.65V

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).
- (2) Custom threshold voltages from 0.82V to 3.3V, 4.4V to 5.0V are available through the use of factory EEPROM programming. Minimum order quantities apply. Contact factory for details and availability.

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Over operating junction temperature range, unless otherwise noted.

	TPS3808	UNIT
Input voltage range, $V_{DD}$	–0.3 to 7.0	V
$C_T$ voltage range, $V_{CT}$	–0.3 to $V_{DD} + 0.3$	V
Other voltage ranges: $V_{RESET}$ , $V_{MR}$ , $V_{SENSE}$	–0.3 to 7	V
$\overline{RESET}$ pin current	5	mA
Operating junction temperature range, $T_J$ <sup>(2)</sup>	–40 to +150	°C
Storage temperature range, $T_{STG}$	–65 to +150	°C
ESD rating, HBM	2	kV
ESD rating, CDM	500	V

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the [Electrical Characteristics](#) is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
- (2) As a result of the low dissipated power in this device, it is assumed that  $T_J = T_A$ .

## ELECTRICAL CHARACTERISTICS

1.7V ≤ V<sub>DD</sub> ≤ 6.5V, R<sub>LRESET</sub> = 100kΩ, C<sub>LRESET</sub> = 50pF, over operating temperature range (T<sub>J</sub> = –40°C to +125°C), unless otherwise noted. Typical values are at T<sub>J</sub> = +25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
V <sub>DD</sub>	Input supply range	–40°C < T <sub>J</sub> < +125°C		1.7		6.5	V	
		0°C < T <sub>J</sub> < +85°C		1.65		6.5		
I <sub>DD</sub>	Supply current (current into V <sub>DD</sub> pin)	V <sub>DD</sub> = 3.3V, $\overline{\text{RESET}}$ not asserted MR, $\overline{\text{RESET}}$ , C <sub>T</sub> open			2.4	5.0	μA	
		V <sub>DD</sub> = 6.5V, $\overline{\text{RESET}}$ not asserted MR, $\overline{\text{RESET}}$ , C <sub>T</sub> open			2.7	6.0	μA	
V <sub>OL</sub>	Low-level output voltage	1.3V ≤ V <sub>DD</sub> < 1.8V, I <sub>OL</sub> = 0.4mA				0.3	V	
		1.8V ≤ V <sub>DD</sub> ≤ 6.5V, I <sub>OL</sub> = 1.0mA				0.4	V	
	Power-up reset voltage <sup>(1)</sup>	V <sub>OL</sub> (max) = 0.2V, I <sub>RESET</sub> = 15μA				0.8	V	
V <sub>IT</sub>	Negative-going input threshold accuracy	TPS3808G01		–2.0	±1.0	+2.0	%	
		V <sub>IT</sub> ≤ 3.3V		–1.5	±0.5	+1.5		
		3.3V < V <sub>IT</sub> ≤ 5.0V		–2.0	±1.0	+2.0		
		V <sub>IT</sub> ≤ 3.3V	–40°C < T <sub>J</sub> < +85°C	–1.25	±0.5	+1.25		
		3.3V < V <sub>IT</sub> ≤ 5.0V	–40°C < T <sub>J</sub> < +85°C	–1.5	±0.5	+1.5		
V <sub>HYS</sub>	Hysteresis on V <sub>IT</sub> pin	TPS3808G01			1.5	3.0	%V <sub>IT</sub>	
		Fixed versions	–40°C < T <sub>J</sub> < +85°C		1.0	2.0		
					1.0	2.5		
R <sub>MR</sub>	$\overline{\text{MR}}$ Internal pull-up resistance			70	90		kΩ	
I <sub>SENSE</sub>	Input current at SENSE pin	TPS3808G01	V <sub>SENSE</sub> = V <sub>IT</sub>	–25		25	nA	
		Fixed versions	V <sub>SENSE</sub> = 6.5V		1.7		μA	
I <sub>OH</sub>	$\overline{\text{RESET}}$ leakage current	V <sub>RESET</sub> = 6.5V, $\overline{\text{RESET}}$ not asserted				300	nA	
C <sub>IN</sub>	Input capacitance, any pin	C <sub>T</sub> pin	V <sub>IN</sub> = 0V to V <sub>DD</sub>		5		pF	
		Other pins	V <sub>IN</sub> = 0V to 6.5V		5			
V <sub>IL</sub>	$\overline{\text{MR}}$ logic low input			0		0.3 V <sub>DD</sub>	V	
V <sub>IH</sub>	$\overline{\text{MR}}$ logic high input			0.7 V <sub>DD</sub>		V <sub>DD</sub>		
t <sub>w</sub>	Input pulse width to $\overline{\text{RESET}}$	SENSE	V <sub>IH</sub> = 1.05V <sub>IT</sub> , V <sub>IL</sub> = 0.95V <sub>IT</sub>		20		μs	
		$\overline{\text{MR}}$	V <sub>IH</sub> = 0.7V <sub>DD</sub> , V <sub>IL</sub> = 0.3V <sub>DD</sub>		0.001			
t <sub>d</sub>	$\overline{\text{RESET}}$ delay time	C <sub>T</sub> = Open	See <a href="#">Timing Diagram</a>		12	20	28	ms
		C <sub>T</sub> = V <sub>DD</sub>			180	300	420	ms
		C <sub>T</sub> = 100pF			0.75	1.25	1.75	ms
		C <sub>T</sub> = 180nF			0.7	1.2	1.7	s
t <sub>pHL</sub>	Propagation delay	$\overline{\text{MR}}$ to $\overline{\text{RESET}}$	V <sub>IH</sub> = 0.7V <sub>DD</sub> , V <sub>IL</sub> = 0.3V <sub>DD</sub>		150		ns	
	High to low level $\overline{\text{RESET}}$ delay	SENSE to $\overline{\text{RESET}}$	V <sub>IH</sub> = 1.05V <sub>IT</sub> , V <sub>IL</sub> = 0.95V <sub>IT</sub>		20		μs	
θ <sub>JA</sub>	Thermal resistance, junction-to-ambient				290		°C/W	

(1) The lowest supply voltage (V<sub>DD</sub>) at which  $\overline{\text{RESET}}$  becomes active. T<sub>rise(VDD)</sub> ≥ 15μs/V.

FUNCTIONAL BLOCK DIAGRAMS

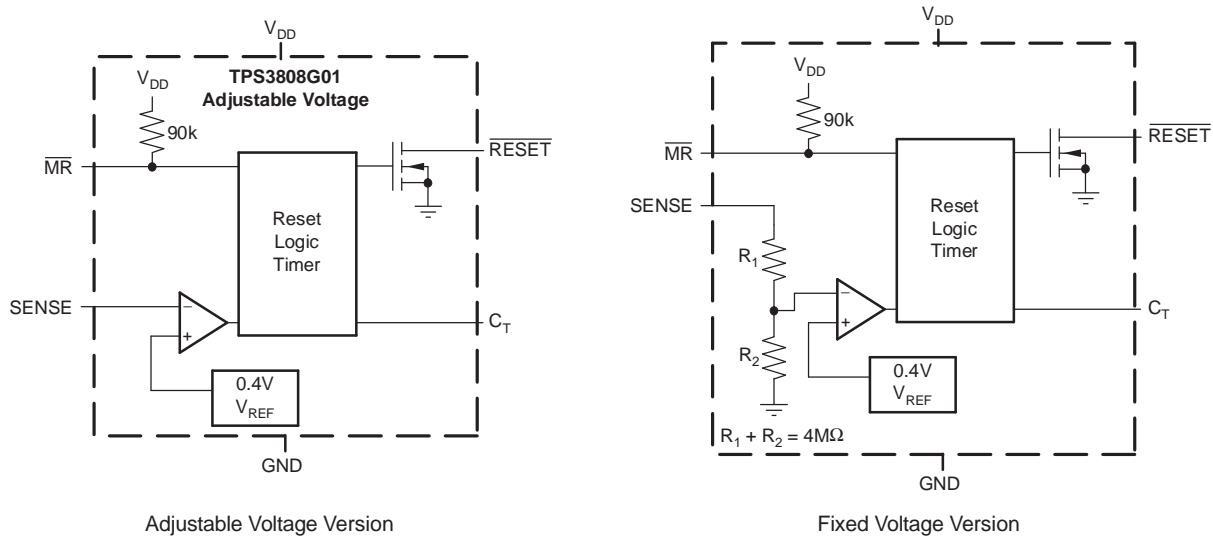


Figure 1. Adjustable and Fixed Voltage Versions

PIN ASSIGNMENTS

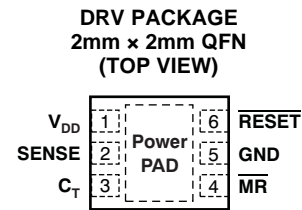
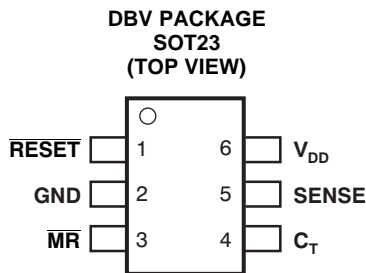
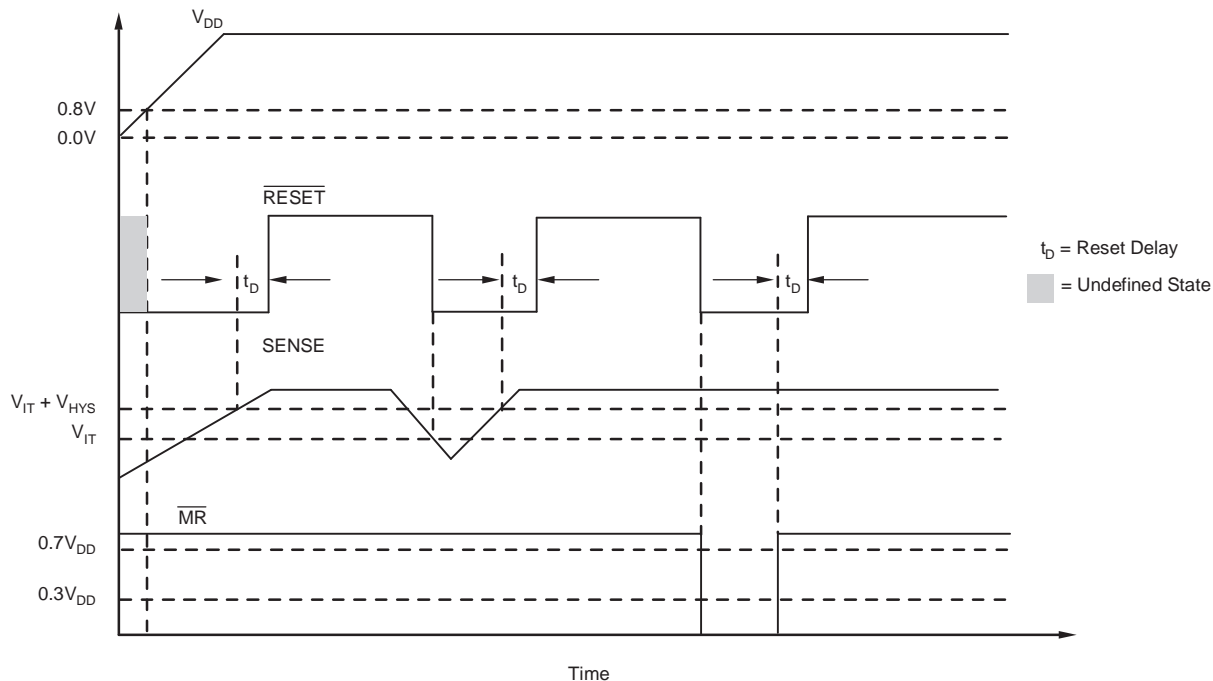


Table 1. TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	SOT23 (DBV) PIN NO.	
RESET	1	RESET is an open-drain output that is driven to a low impedance state when RESET is asserted (either the SENSE input is lower than the threshold voltage (V <sub>IT</sub> ) or the MR pin is set to a logic low). RESET will remain low (asserted) for the reset period after both SENSE is above V <sub>IT</sub> and MR is set to a logic high. A pull-up resistor from 10kΩ to 1MΩ should be used on this pin, and allows the reset pin to attain voltages higher than V <sub>DD</sub> .
GND	2	Ground
MR	3	Driving the manual reset pin (MR) low asserts RESET. MR is internally tied to V <sub>DD</sub> by a 90kΩ pull-up resistor.
C <sub>T</sub>	4	Reset period programming pin. Connecting this pin to V <sub>DD</sub> through a 40kΩ to 200kΩ resistor or leaving it open results in fixed delay times (see <a href="#">Electrical Characteristics</a> ). Connecting this pin to a ground referenced capacitor ≥ 100pF gives a user-programmable delay time. See the <a href="#">Selecting the Reset Delay Time</a> section for more information.
SENSE	5	This pin is connected to the voltage to be monitored. If the voltage at this terminal drops below the threshold voltage V <sub>IT</sub> , then RESET is asserted.
V <sub>DD</sub>	6	Supply voltage. It is good analog design practice to place a 0.1μF ceramic capacitor close to this pin.
PowerPAD		PowerPAD. Connect to ground plane to enhance thermal performance of package.

**TIMING DIAGRAM**



**Figure 2. TPS3808 Timing Diagram Showing  $\overline{MR}$  and SENSE Reset Timing**

**TRUTH TABLE**

$\overline{MR}$	SENSE > $V_{IT}$	$\overline{RESET}$
L	0	L
L	1	L
H	0	L
H	1	H

**TYPICAL CHARACTERISTICS**

At  $T_J = +25^\circ\text{C}$ ,  $V_{DD} = 3.3\text{V}$ ,  $R_{L\text{RESET}} = 100\text{k}\Omega$ , and  $C_{L\text{RESET}} = 50\text{pF}$ , unless otherwise noted.

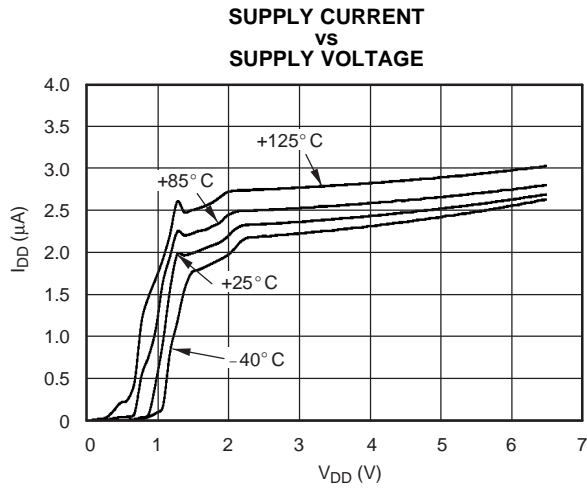


Figure 3.

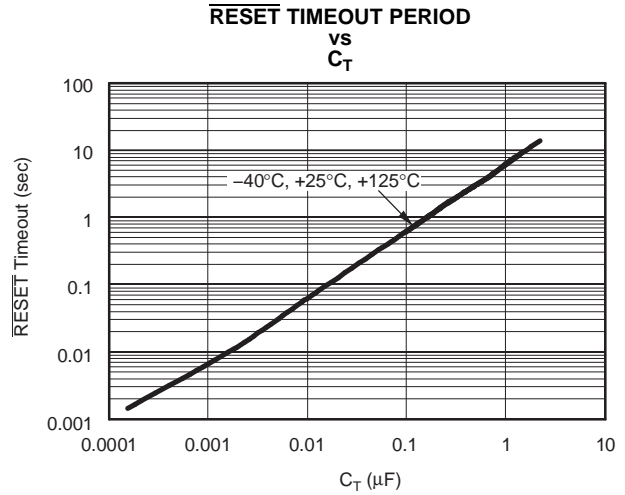


Figure 4.

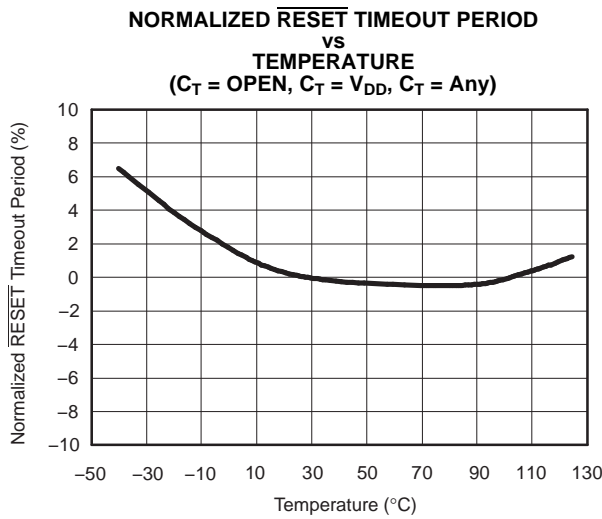


Figure 5.

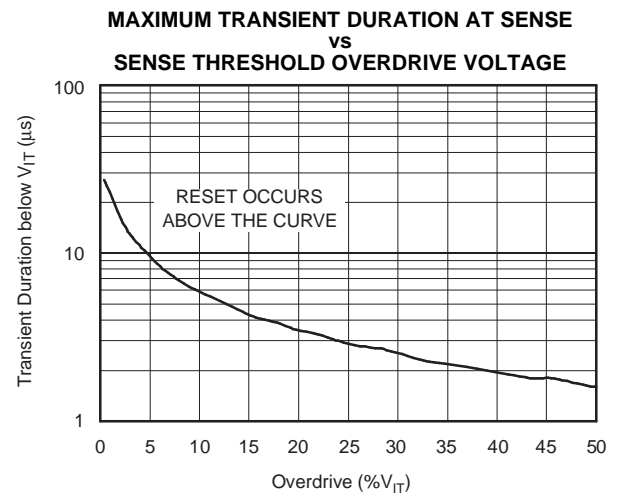


Figure 6.

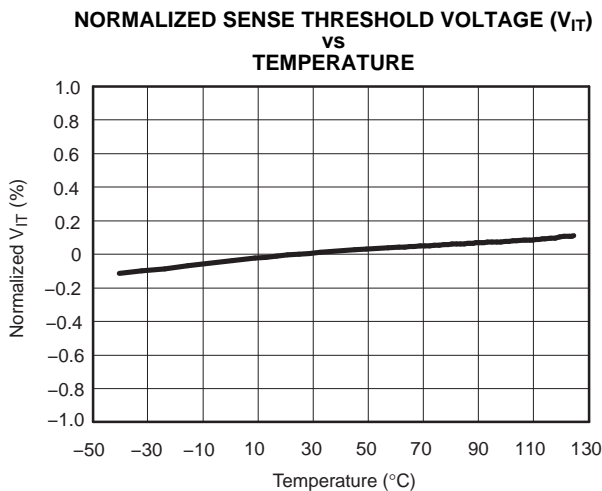


Figure 7.

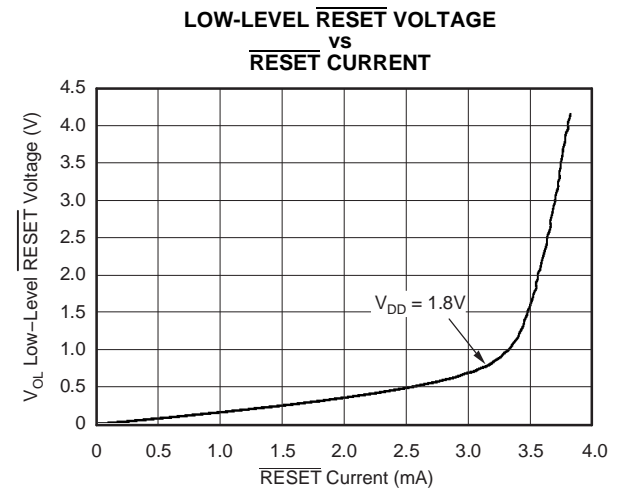
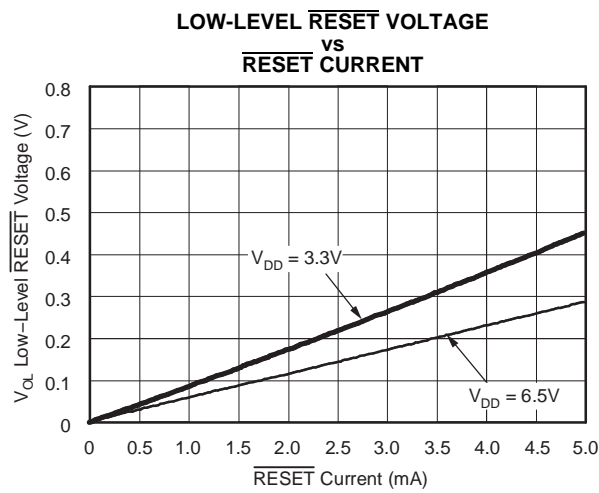


Figure 8.

**TYPICAL CHARACTERISTICS (continued)**

At  $T_J = +25^\circ\text{C}$ ,  $V_{DD} = 3.3\text{V}$ ,  $R_{LRESET} = 100\text{k}\Omega$ , and  $C_{LRESET} = 50\text{pF}$ , unless otherwise noted.



**Figure 9.**

## DEVICE OPERATION

The TPS3808 microprocessor supervisory product family is designed to assert a  $\overline{\text{RESET}}$  signal when either the SENSE pin voltage drops below  $V_{IT}$  or the manual reset (MR) is driven low. The RESET output remains asserted for a user-adjustable time after both the manual reset ( $\overline{\text{MR}}$ ) and SENSE voltages return above the respective thresholds. A broad range of voltage threshold and reset delay time adjustments are available, allowing these devices to be used in a wide array of applications. Reset threshold voltages can be factory-set from 0.82V to 3.3V or from 4.4V to 5.0V, while the TPS3808G01 can be set to any voltage above 0.405V using an external resistor divider. Two preset delay times are also user-selectable: connecting the  $C_T$  pin to  $V_{DD}$  results in a 300ms reset delay, while leaving the  $C_T$  pin open yields a 20ms reset delay. In addition, connecting a capacitor between  $C_T$  and GND allows the designer to select any reset delay period from 1.25ms to 10s.

### RESET OUTPUT

A typical application of the TPS3808G25 used with the OMAP1510 processor is shown in Figure 10. The open-drain RESET output is typically connected to the  $\overline{\text{RESET}}$  input of a microprocessor. A pull-up resistor must be used to hold this line high when  $\overline{\text{RESET}}$  is not asserted. The RESET output is undefined for voltage below 0.8V, but this is normally not a problem since most microprocessors do not function below this voltage. RESET remains high (unasserted) as long as SENSE is above its threshold ( $V_{IT}$ ) and the manual reset ( $\overline{\text{MR}}$ ) is logic high. If either SENSE falls below  $V_{IT}$  or  $\overline{\text{MR}}$  is driven low,  $\overline{\text{RESET}}$  is asserted, driving the  $\overline{\text{RESET}}$  pin to a low impedance.

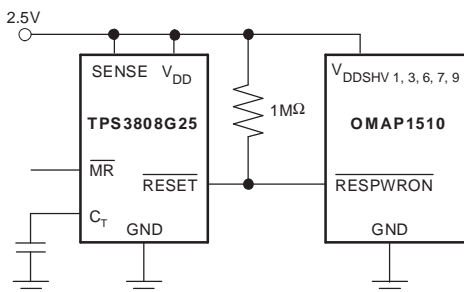


Figure 10. Typical Application of the TPS3808 with an OMAP Processor

Once  $\overline{\text{MR}}$  is again logic high and SENSE is above  $V_{IT} + V_{HYS}$  (the threshold hysteresis), a delay circuit is enabled which holds  $\overline{\text{RESET}}$  low for a specified reset delay period. Once the reset delay has expired, the RESET pin goes to a high impedance state. The pull-up resistor from the open-drain RESET to the

supply line can be used to allow the reset signal for the microprocessor to have a voltage higher than  $V_{DD}$  (up to 6.5V). The pull-up resistor should be no smaller than 10kΩ as a result of the finite impedance of the RESET line.

### SENSE INPUT

The SENSE input provides a terminal at which any system voltage can be monitored. If the voltage on this pin drops below  $V_{IT}$ , then  $\overline{\text{RESET}}$  is asserted. The comparator has a built-in hysteresis to ensure smooth RESET assertions and de-assertions. It is good analog design practice to put a 1nF to 10nF bypass capacitor on the SENSE input to reduce sensitivity to transients and layout parasitics.

The TPS3808G01 can be used to monitor any voltage rail down to 0.405V using the circuit shown in Figure 11.

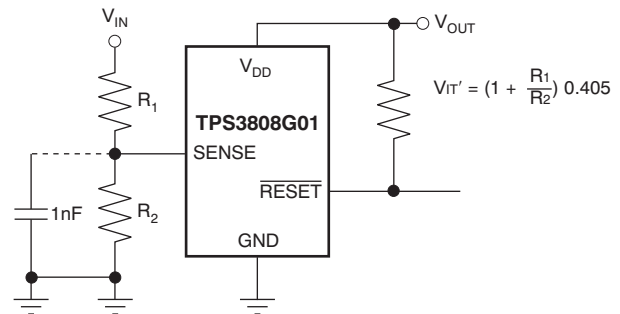


Figure 11. Using the TPS3808G01 to Monitor a User-Defined Threshold Voltage

### MANUAL RESET ( $\overline{\text{MR}}$ ) INPUT

The manual reset ( $\overline{\text{MR}}$ ) input allows a processor or other logic circuits to initiate a reset. A logic low ( $0.3V_{DD}$ ) on MR causes RESET to assert. After MR returns to a logic high and SENSE is above its reset threshold,  $\overline{\text{RESET}}$  is de-asserted after the user defined reset delay expires. Note that  $\overline{\text{MR}}$  is internally tied to  $V_{DD}$  using a 90kΩ resistor so this pin can be left unconnected if  $\overline{\text{MR}}$  will not be used.

See Figure 12 for how  $\overline{\text{MR}}$  can be used to monitor multiple system voltages. Note that if the logic signal driving  $\overline{\text{MR}}$  does not go fully to  $V_{DD}$ , there will be some additional current draw into  $V_{DD}$  as a result of the internal pull-up resistor on MR. To minimize current draw, a logic-level FET can be used as illustrated in Figure 13.

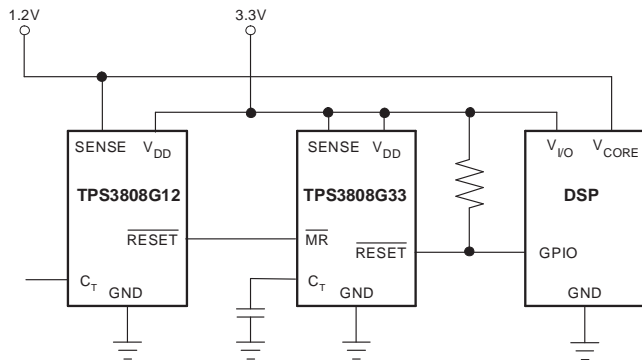


Figure 12. Using MR to Monitor Multiple System Voltages

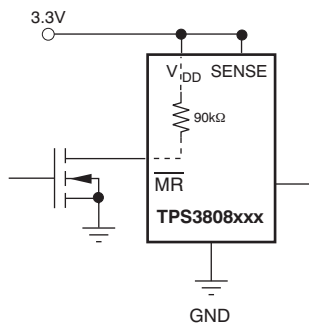


Figure 13. Using an External MOSFET to Minimize I<sub>DD</sub> When MR Signal Does Not Go to V<sub>DD</sub>

### SELECTING THE RESET DELAY TIME

The TPS3808 has three options for setting the RESET delay time as shown in Figure 14. Figure 14a shows the configuration for a fixed 300ms typical delay time by tying C<sub>T</sub> to V<sub>DD</sub>; a resistor from 40kΩ to 200kΩ must be used. Supply current is not affected

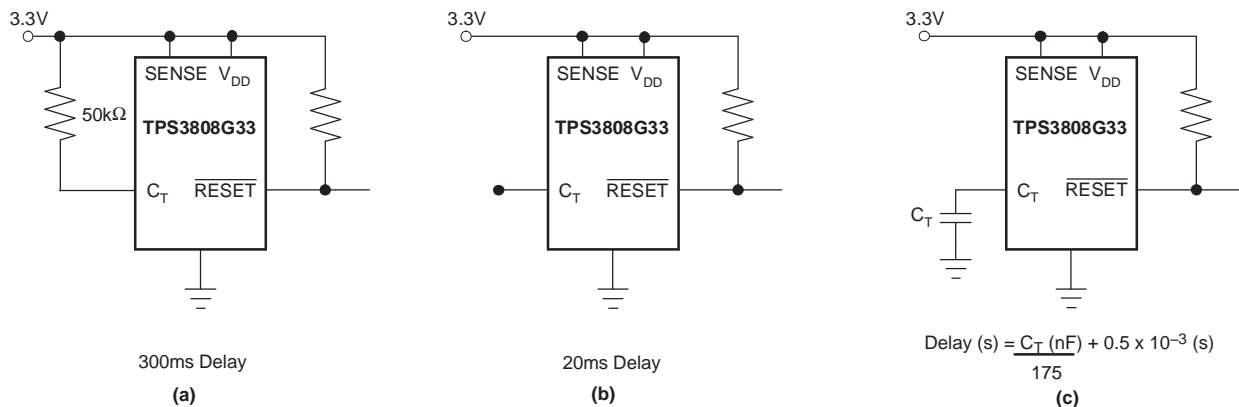


Figure 14. Configuration Used to Set the RESET Delay Time

by the choice of resistor. Figure 14b shows a fixed 20ms delay time by leaving the C<sub>T</sub> pin open. Figure 14c shows a ground referenced capacitor connected to C<sub>T</sub> for a user-defined program time between 1.25ms and 10s.

The capacitor C<sub>T</sub> should be ≥ 100pF nominal value in order for the TPS3808xxx to recognize that the capacitor is present. The capacitor value for a given delay time can be calculated using the following equation:

$$C_T \text{ (nF)} = [t_D \text{ (s)} - 0.5 \times 10^{-3} \text{ (s)}] \times 175 \quad (1)$$

The reset delay time is determined by the time it takes an on-chip precision 220nA current source to charge the external capacitor to 1.23V. When a RESET is asserted the capacitor is discharged. When the RESET conditions are cleared, the internal current source is enabled and begins to charge the external capacitor. When the voltage on this capacitor reaches 1.23V, RESET is de-asserted. Note that a low leakage type capacitor such as a ceramic should be used, and that stray capacitance around this pin may cause errors in the reset delay time.

### IMMUNITY TO SENSE PIN VOLTAGE TRANSIENTS

The TPS3808 is relatively immune to short negative transients on the SENSE pin. Sensitivity to transients is dependent on threshold overdrive, as shown in the Maximum Transient Duration at Sense vs Sense Threshold Overdrive Voltage graph (Figure 6) in the Typical Characteristics section.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TPS3808G01DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G01DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G01DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G01DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G01DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G01DRVRG4	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G01DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G01DRVTG4	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G09DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G09DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G09DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G09DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G125DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G125DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G125DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G125DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G12DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G12DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G12DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G12DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G12DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G12DRVRG4	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G12DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G12DRVTG4	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G15DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TPS3808G15DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G15DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G15DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G15DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G15DRVRG4	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G15DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G15DRVTG4	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G18DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G18DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G18DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G18DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G18DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G18DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G19DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G19DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G19DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G19DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G25DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G25DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G25DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G25DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G25DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G25DRVRG4	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G25DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G25DRVTG4	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G30DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TPS3808G30DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G30DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G30DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G30DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G30DRVRG4	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G30DRVVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G30DRVVTG4	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G33DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G33DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G33DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G33DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G50DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G50DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G50DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3808G50DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is

provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS3808G01, TPS3808G12, TPS3808G30, TPS3808G33, TPS3808G50 :**

- Automotive: [TPS3808G01-Q1](#), [TPS3808G12-Q1](#), [TPS3808G30-Q1](#), [TPS3808G33-Q1](#), [TPS3808G50-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

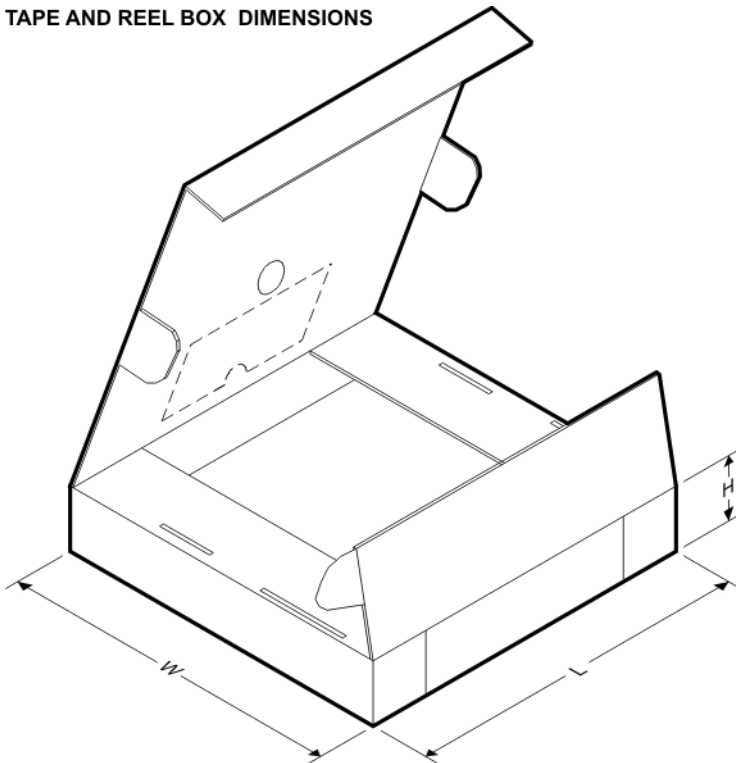


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3808G01DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G01DBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G01DRVR	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G01DRVT	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G09DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G09DBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G125DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G125DBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G12DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G12DBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G12DRVR	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G12DRVT	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G15DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G15DBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G15DRVR	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G15DRVT	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G18DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G18DBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3808G18DRVR	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G18DRVT	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G19DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G19DBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G25DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G25DBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G25DRVR	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G25DRVT	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G30DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G30DBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G30DRVR	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G30DRVT	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS3808G33DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G33DBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G50DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G50DBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**



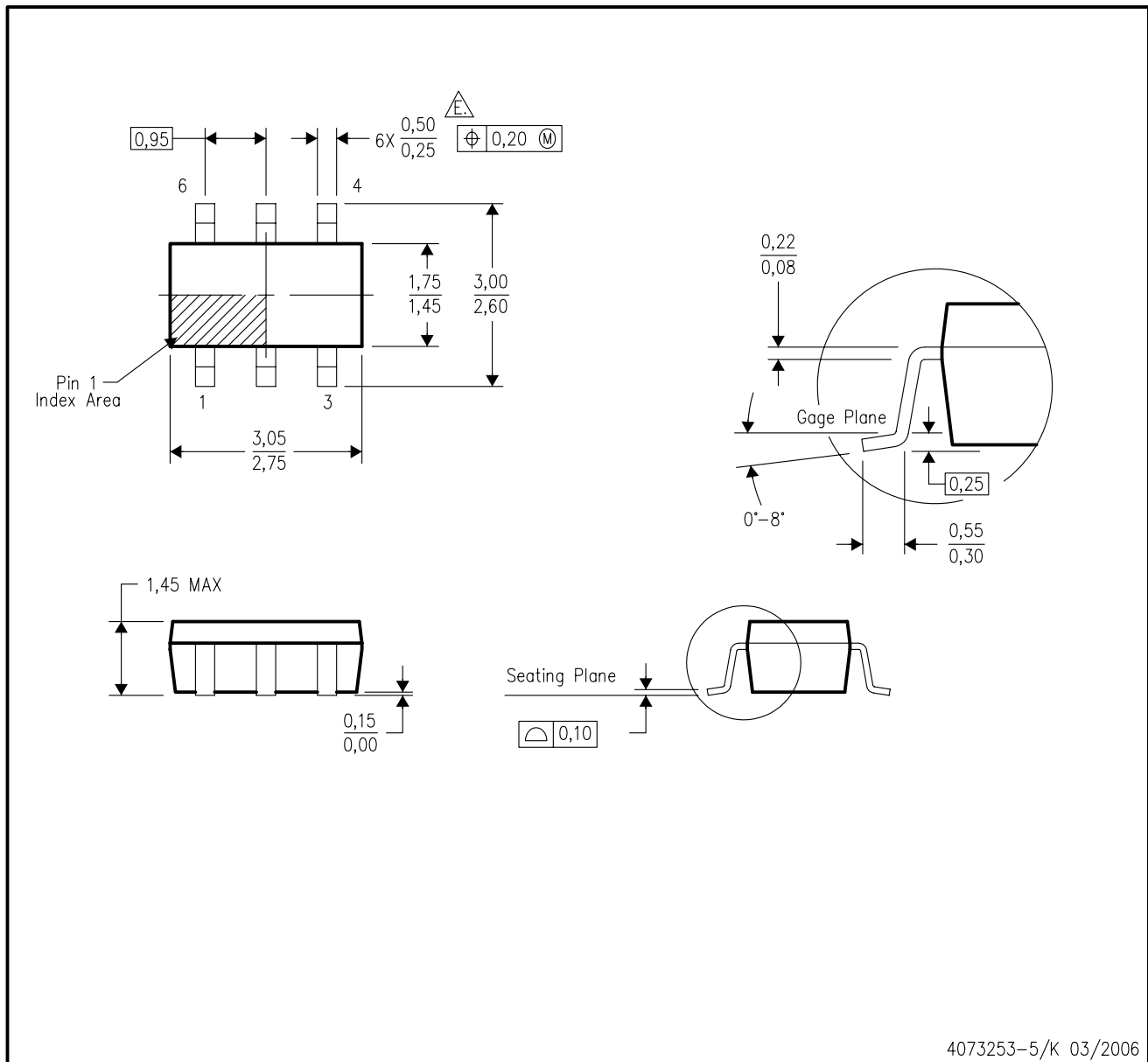
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3808G01DBVR	SOT-23	DBV	6	3000	195.0	200.0	45.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3808G01DBVT	SOT-23	DBV	6	250	195.0	200.0	45.0
TPS3808G01DRVR	SON	DRV	6	3000	195.0	200.0	45.0
TPS3808G01DRVT	SON	DRV	6	250	195.0	200.0	45.0
TPS3808G09DBVR	SOT-23	DBV	6	3000	195.0	200.0	45.0
TPS3808G09DBVT	SOT-23	DBV	6	250	195.0	200.0	45.0
TPS3808G125DBVR	SOT-23	DBV	6	3000	195.0	200.0	45.0
TPS3808G125DBVT	SOT-23	DBV	6	250	195.0	200.0	45.0
TPS3808G12DBVR	SOT-23	DBV	6	3000	195.0	200.0	45.0
TPS3808G12DBVT	SOT-23	DBV	6	250	195.0	200.0	45.0
TPS3808G12DRVR	SON	DRV	6	3000	195.0	200.0	45.0
TPS3808G12DRVT	SON	DRV	6	250	195.0	200.0	45.0
TPS3808G15DBVR	SOT-23	DBV	6	3000	195.0	200.0	45.0
TPS3808G15DBVT	SOT-23	DBV	6	250	195.0	200.0	45.0
TPS3808G15DRVR	SON	DRV	6	3000	195.0	200.0	45.0
TPS3808G15DRVT	SON	DRV	6	250	195.0	200.0	45.0
TPS3808G18DBVR	SOT-23	DBV	6	3000	195.0	200.0	45.0
TPS3808G18DBVT	SOT-23	DBV	6	250	195.0	200.0	45.0
TPS3808G18DRVR	SON	DRV	6	3000	195.0	200.0	45.0
TPS3808G18DRVT	SON	DRV	6	250	195.0	200.0	45.0
TPS3808G19DBVR	SOT-23	DBV	6	3000	195.0	200.0	45.0
TPS3808G19DBVT	SOT-23	DBV	6	250	195.0	200.0	45.0
TPS3808G25DBVR	SOT-23	DBV	6	3000	195.0	200.0	45.0
TPS3808G25DBVT	SOT-23	DBV	6	250	195.0	200.0	45.0
TPS3808G25DRVR	SON	DRV	6	3000	195.0	200.0	45.0
TPS3808G25DRVT	SON	DRV	6	250	195.0	200.0	45.0
TPS3808G30DBVR	SOT-23	DBV	6	3000	195.0	200.0	45.0
TPS3808G30DBVT	SOT-23	DBV	6	250	195.0	200.0	45.0
TPS3808G30DRVR	SON	DRV	6	3000	195.0	200.0	45.0
TPS3808G30DRVT	SON	DRV	6	250	195.0	200.0	45.0
TPS3808G33DBVR	SOT-23	DBV	6	3000	195.0	200.0	45.0
TPS3808G33DBVT	SOT-23	DBV	6	250	195.0	200.0	45.0
TPS3808G50DBVR	SOT-23	DBV	6	3000	195.0	200.0	45.0
TPS3808G50DBVT	SOT-23	DBV	6	250	195.0	200.0	45.0

DBV (R-PDSO-G6)

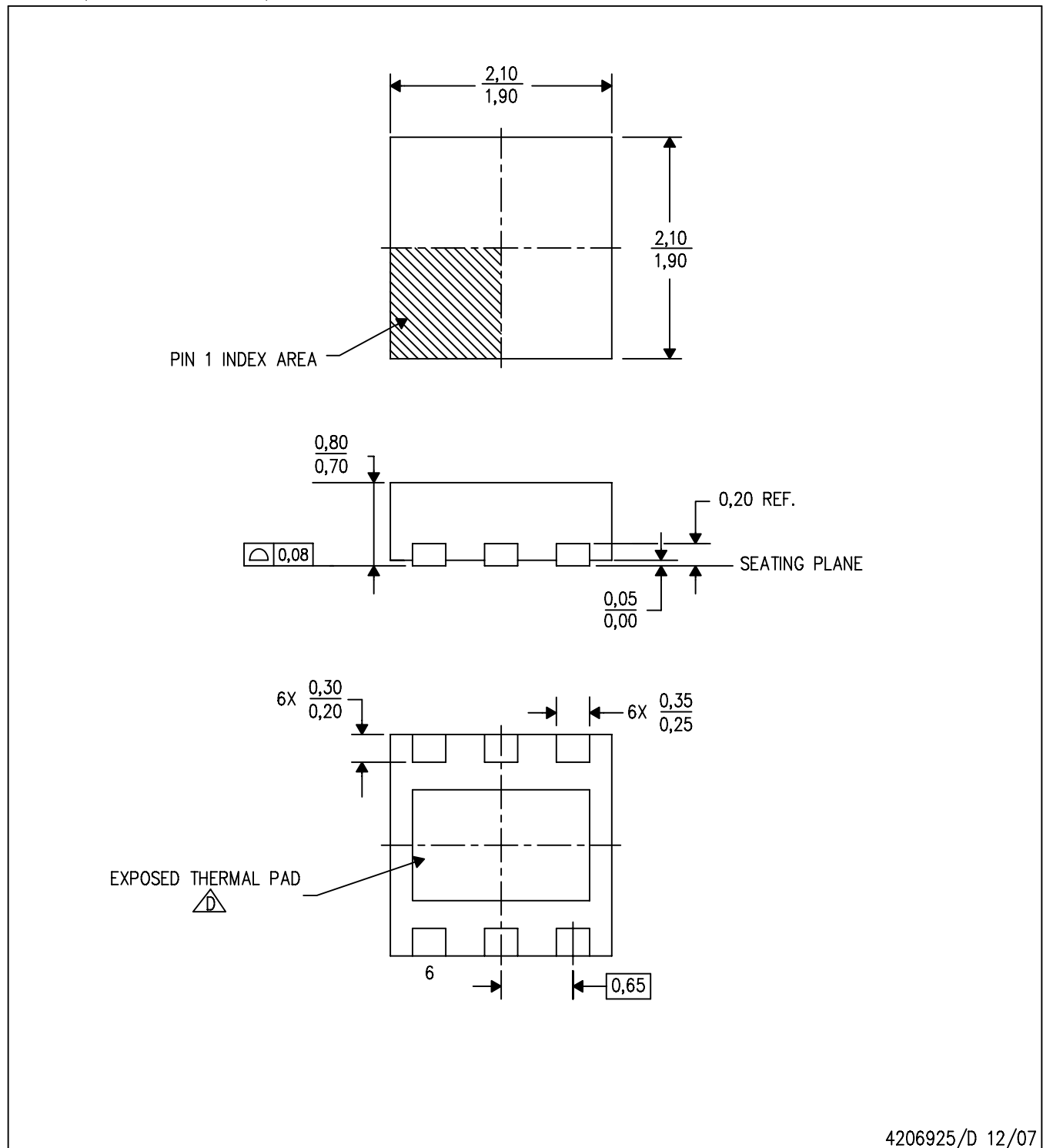
PLASTIC SMALL-OUTLINE PACKAGE




- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- $\triangle E$  Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DRV (S-PDSO-N6)

PLASTIC SMALL OUTLINE



4206925/D 12/07

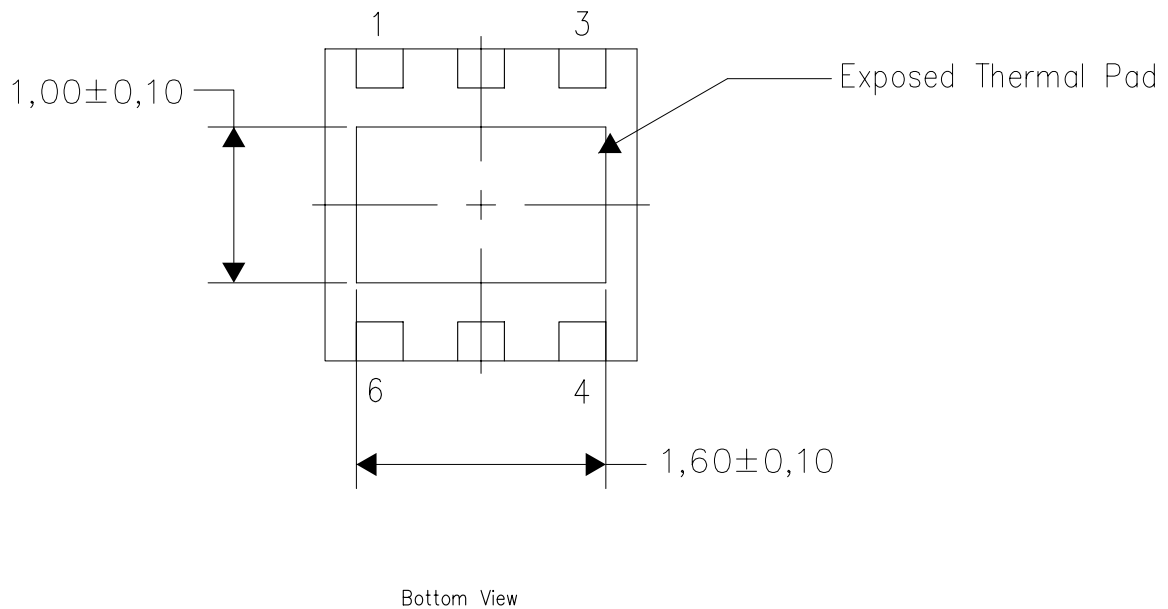
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Small Outline No-Lead (SON) package configuration.
-  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at [www.ti.com](http://www.ti.com).

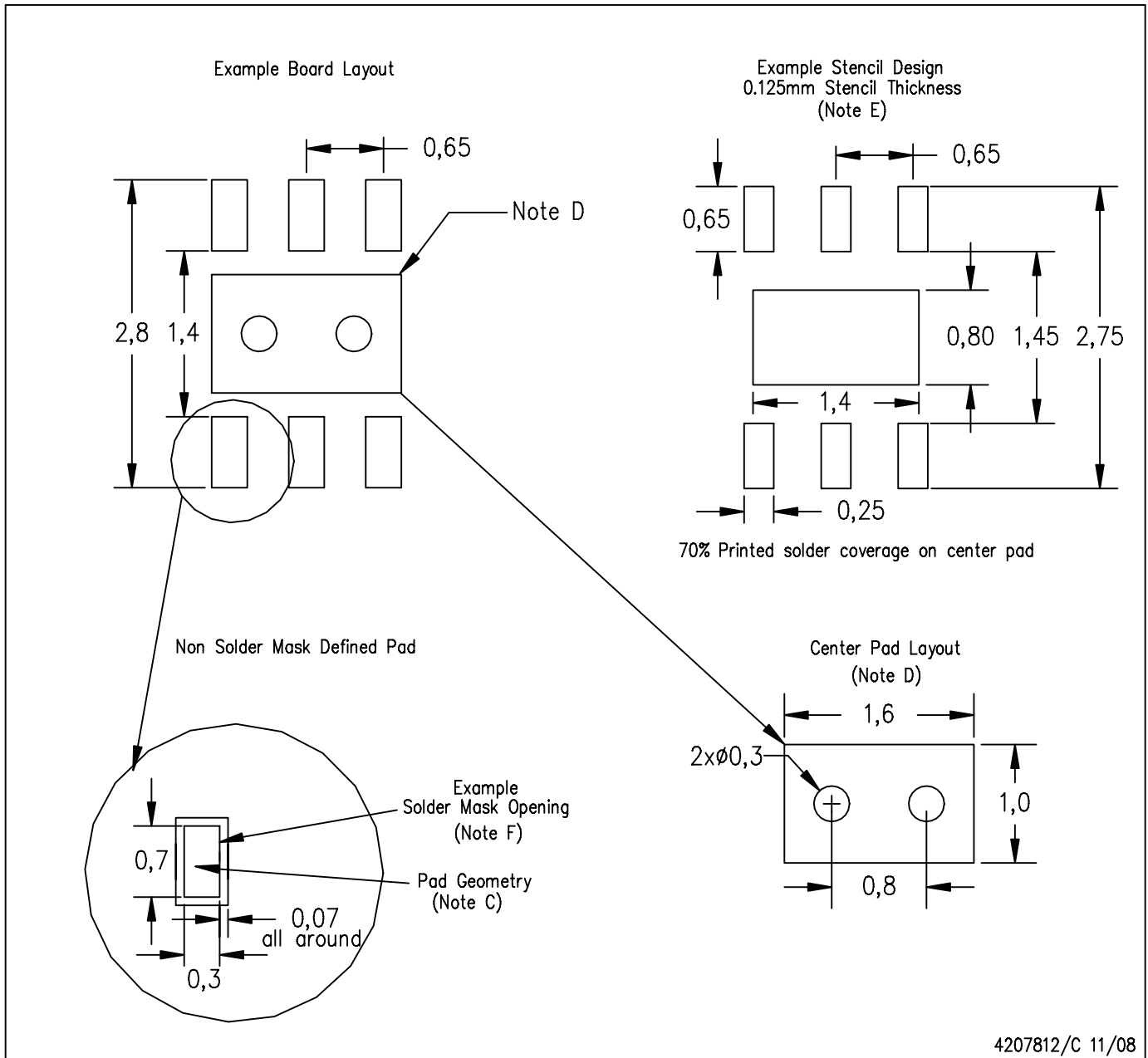
The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

## DRV (S-PDSO-N6)



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for solder mask tolerances.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

### Products

Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>

### Applications

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2009, Texas Instruments Incorporated