

TPS3700 用于过压和欠压检测功能且具有内部基准电压的窗口比较器

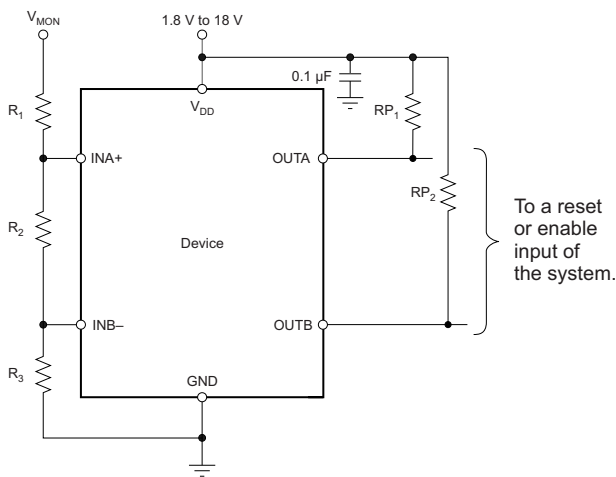
1 特性

- 宽电源电压范围：1.8V 至 18V
- 可调节阀值：低至 400mV
- 高阈值精度：
 - 在温度范围内为 1.0%
 - 0.25%（典型值）
- 低静态电流：5.5 μ A（典型值）
- 针对过压和欠压检测的开漏输出
- 内部滞后：5.5mV（典型值）
- 温度范围：-40°C 至 125°C
- 封装：
 - 小外形尺寸晶体管 (SOT)-6 封装
 - 1.5mm x 1.5mm 晶圆级小外形无引线 (WSON)-6 封装

2 应用

- 工业控制系统
- 车载系统
- 嵌入式计算模块
- 数字信号处理器 (DSP)，微控制器，或者微处理器应用
- 笔记本和台式计算机
- 便携式和电池供电类产品
- 现场可编程门阵列 (FPGA) 和专用集成电路 (ASIC) 应用

4 简化电路原理图



3 说明

TPS3700 宽电源电压窗口比较器在 1.8V 至 18V 的电压范围内运行。此器件具有两个带有一个内部 400mV 基准的高精度比较器和两个用于过压和欠压检测的额定值为 18V 的开漏输出。TPS3700 可被用作一个窗口比较器或者两个独立电压监视器；使用外部电阻器可对监视电压进行设定。

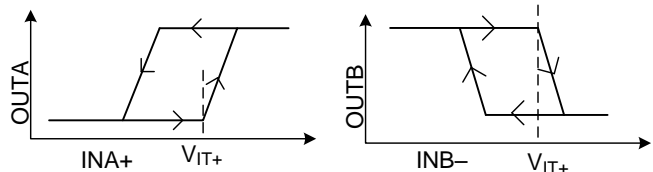
当 INA+ 上的电压下降至低于 ($V_{ITP} - V_{HYS}$) 时，OUTA 被驱动至低电平，当电压返回到相应阈值 (V_{ITP}) 之上时，OUTA 变为高电平。当 INB- 上的电压上升至高于 V_{ITP} 时，OUTB 被驱动至低电平，当电压下降至低于各自的阈值 ($V_{ITP} - V_{HYS}$) 时，OUTB 变为高电平。TPS3700 中的两个比较器包括用于滤波的内置滞后来抑制短时毛刺脉冲，从而确保无故障触发的稳定输出运行。

TPS3700 可采用 SOT-6 和 1.5mm x 1.5mm WSON-6 封装，额定工作结温范围为 -40°C 至 125°C。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
TPS3700	SOT (6)	2.90mm x 1.60mm
	WSON (6)	1.50mm x 1.50mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。



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5 修订历史记录

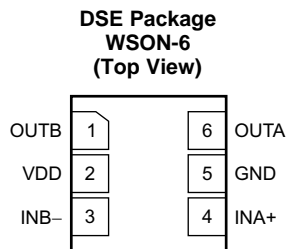
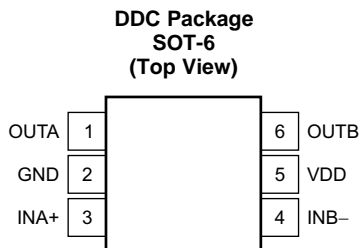
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (May 2013) to Revision D	Page
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	4
• Changed HBM maximum specification from 2 kV to 2.5 kV in <i>ESD Ratings</i>	4
• Changed <i>Functional Block Diagram</i> ; added hysteresis symbol	9

Changes from Revision B (April 2012) to Revision C	Page
• 已更改 特性中的“封装”项	1
• 已添加 SON-6 封装选项到“说明”部分	1
• 已添加 DSE 引脚分配图到标题页	1
• Added DSE pin out graphic	3
• Added DSE package to Thermal Information table	4

Changes from Revision A (February 2012) to Revision B	Page
• 移动到生产数据	1

6 Pin Configuration and Functions



Pin Functions

NAME	PIN		I/O	DESCRIPTION
	DDC	DSE		
GND	2	5	—	Ground
INA+	3	4	I	This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this terminal drops below the threshold voltage ($V_{ITP} - V_{HYS}$), OUTA is driven low.
INB-	4	3	I	This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this terminal exceeds the threshold voltage (V_{ITP}), OUTB is driven low.
OUTA	1	6	O	INA+ comparator open-drain output. OUTA is driven low when the voltage at this comparator is below ($V_{ITP} - V_{HYS}$). The output goes high when the sense voltage returns above the respective threshold (V_{ITP}).
OUTB	6	1	O	INB- comparator open-drain output. OUTB is driven low when the voltage at this comparator exceeds V_{ITP} . The output goes high when the sense voltage returns below the respective threshold ($V_{ITP} - V_{HYS}$).
VDD	5	2	I	Supply voltage input. Connect a 1.8-V to 18-V supply to VDD to power the device. Good analog design practice is to place a 0.1- μ F ceramic capacitor close to this pin.

7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage ⁽²⁾	V _{DD}	-0.3	20	V
	OUTA, OUTB	-0.3	20	V
	INA+, INB-	-0.3	7	V
Current	Output terminal current		40	mA
Operating junction temperature, T _J		-40	125	°C
Storage temperature, T _{stg}		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network ground terminal.

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge		
	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2500	V
Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1000		

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{DD}	Supply voltage	1.8		18	V
V _I	Input voltage	0		6.5	V
V _O	Output voltage	0		18	V

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS3700		UNIT
		DDC (SOT)	DSE (WSON)	
		6 PINS	6 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	204.6	194.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	50.5	128.9	
R _{θJB}	Junction-to-board thermal resistance	54.3	153.8	
ψ _{JT}	Junction-to-top characterization parameter	0.8	11.9	
ψ _{JB}	Junction-to-board characterization parameter	52.8	157.4	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

Over the operating temperature range of $T_J = -40^{\circ}\text{C}$ to 125°C , and $1.8\text{ V} < V_{DD} < 18\text{ V}$, unless otherwise noted.

Typical values are at $T_J = 25^{\circ}\text{C}$ and $V_{DD} = 5\text{ V}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage range		1.8		18	V
$V_{(POR)}$	Power-on reset voltage ⁽¹⁾	$V_{OLmax} = 0.2\text{ V}$, $I_{(OUTA/B)} = 15\text{ }\mu\text{A}$			0.8	V
V_{IT+}	Positive-going input threshold voltage	$V_{DD} = 1.8\text{ V}$	396	400	404	mV
		$V_{DD} = 18\text{ V}$	396	400	404	
V_{IT-}	Negative-going input threshold voltage	$V_{DD} = 1.8\text{ V}$	387	394.5	400	mV
		$V_{DD} = 18\text{ V}$	387	394.5	400	
V_{hys}	Hysteresis voltage ($hys = V_{IT+} - V_{IT-}$)			5.5	12	
$I_{(INA+)}$	Input current (at the INA+ terminal)	$V_{DD} = 1.8\text{ V}$ and 18 V , $V_I = 6.5\text{ V}$	-25	1	25	nA
$I_{(INB-)}$	Input current (at the INB- terminal)	$V_{DD} = 1.8\text{ V}$ and 18 V , $V_I = 0.1\text{ V}$	-15	1	15	nA
V_{OL}	Low-level output voltage	$V_{DD} = 1.3\text{ V}$, $I_O = 0.4\text{ mA}$			250	mV
		$V_{DD} = 1.8\text{ V}$, $I_O = 3\text{ mA}$			250	
		$V_{DD} = 5\text{ V}$, $I_O = 5\text{ mA}$			250	
$I_{(kg)(OD)}$	Open-drain output leakage-current	$V_{DD} = 1.8\text{ V}$ and 18 V , $V_O = V_{DD}$			300	nA
		$V_{DD} = 1.8\text{ V}$, $V_O = 18\text{ V}$			300	
I_{DD}	Supply current	$V_{DD} = 1.8\text{ V}$, no load		5.5	11	μA
		$V_{DD} = 5\text{ V}$		6	13	
		$V_{DD} = 12\text{ V}$		6	13	
		$V_{DD} = 18\text{ V}$		7	13	
	Start-up delay ⁽²⁾			150		μs
UVLO	Undervoltage lockout ⁽³⁾	V_{DD} falling	1.3		1.7	V

(1) The lowest supply voltage (V_{DD}) at which output is active; $t_{r(VDD)} > 15\text{ }\mu\text{s/V}$. Below $V_{(POR)}$, the output cannot be determined.

(2) During power on, V_{DD} must exceed 1.8 V for at least $150\text{ }\mu\text{s}$ before the output is in a correct state.

(3) When V_{DD} falls below UVLO, OUTA is driven low and OUTB goes to high impedance. The outputs cannot be determined below $V_{(POR)}$.

7.6 Timing Requirements

Over operating temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
t_{PHL}	High-to-low propagation delay ⁽¹⁾		18		μs
t_{PLH}	Low-to-high propagation delay ⁽¹⁾		29		μs

(1) High-to-low and low-to-high refers to the transition at the input terminals (INA+ and INB-).

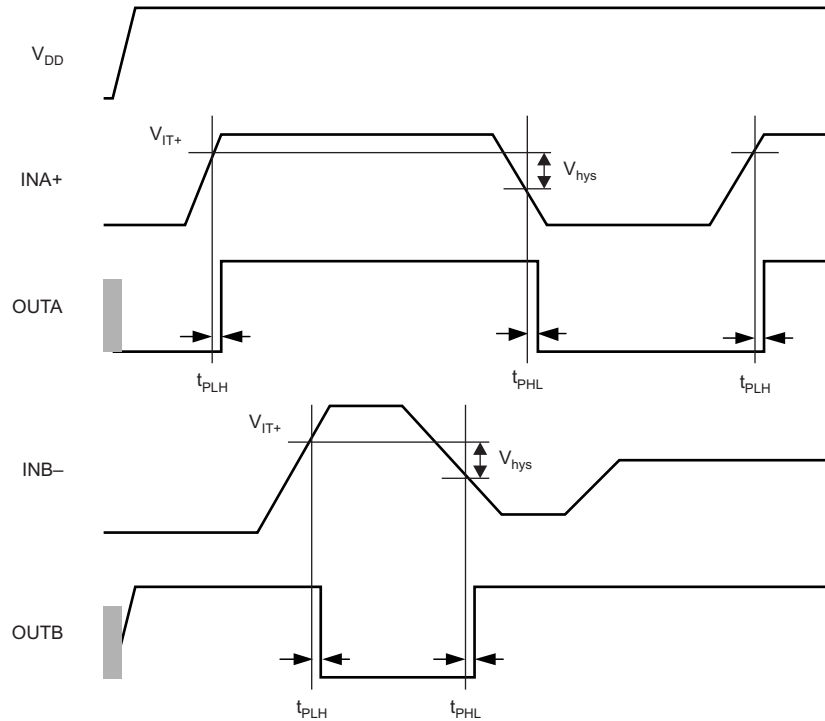


Figure 1. Timing Diagram

7.7 Switching Characteristics

Over operating temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output rise time $V_{DD} = 5\text{ V}$, 10-mV input overdrive, $R_P = 10\text{ k}\Omega$, $V_O = (0.1\text{ to }0.9) \times V_{DD}$		2.2		μs
t_f	Output fall time $V_{DD} = 5\text{ V}$, 10-mV input overdrive, $R_P = 10\text{ k}\Omega$, $V_O = (0.1\text{ to }0.9) \times V_{DD}$		0.22		μs

7.8 Typical Characteristics

At $T_J = 25^\circ\text{C}$ and $V_{DD} = 5\text{ V}$, unless otherwise noted.

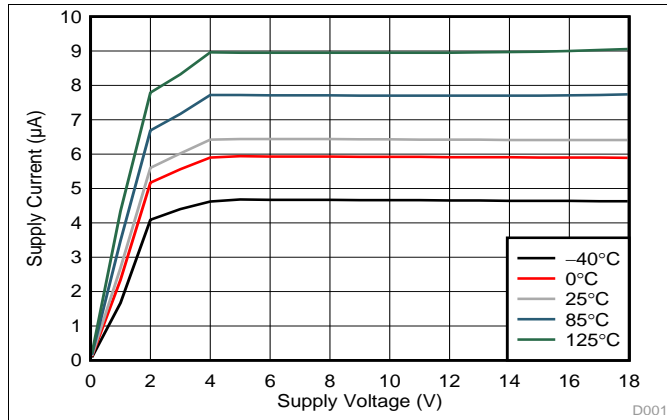


Figure 2. Supply Current (I_{DD}) vs Supply Voltage (V_{DD})

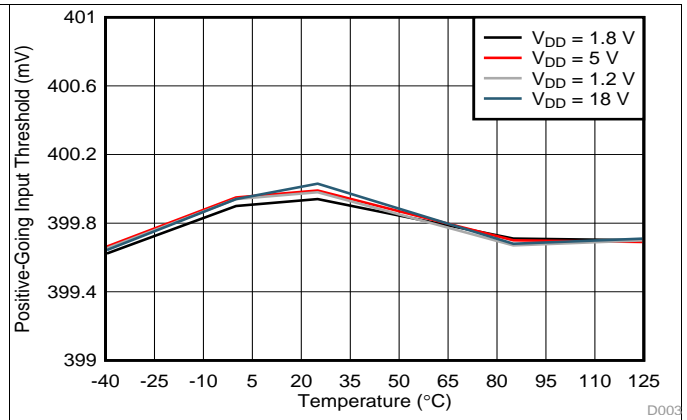


Figure 3. Rising Input Threshold Voltage (V_{IT+}) vs Temperature

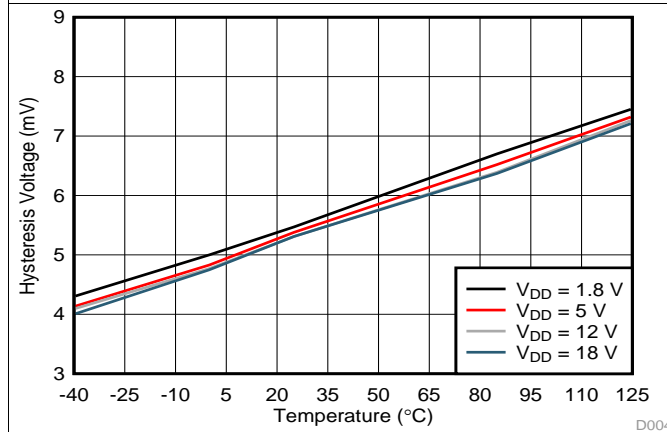


Figure 4. Hysteresis (V_{hys}) vs Temperature

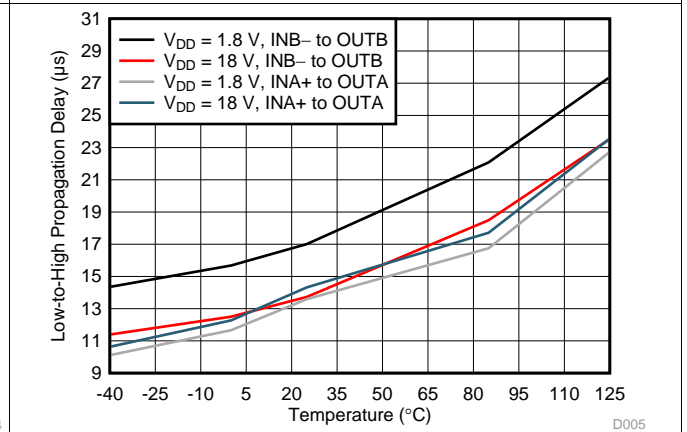


Figure 5. Propagation Delay vs Temperature (High-to-Low Transition at the Inputs)

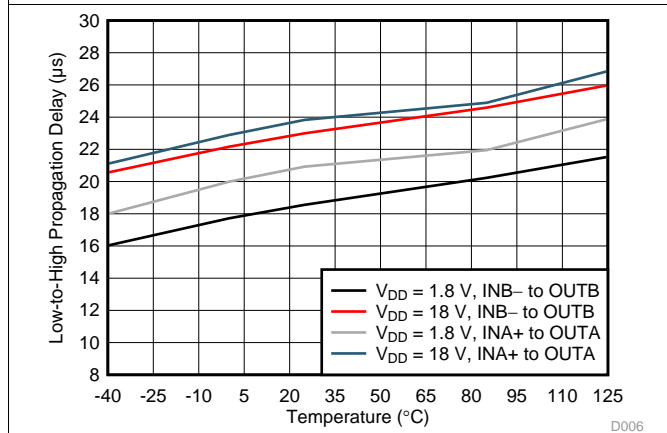
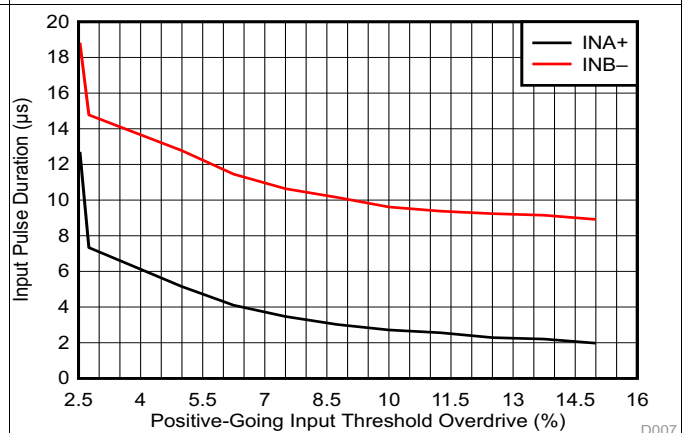


Figure 6. Propagation Delay vs Temperature (Low-to-High Transition at the Inputs)



INA+ = negative spike below V_{IT-}
 INB- = positive spike above V_{IT+}

Figure 7. Minimum Pulse Width vs Threshold Overdrive Voltage

Typical Characteristics (continued)

At $T_J = 25^\circ\text{C}$ and $V_{DD} = 5\text{ V}$, unless otherwise noted.

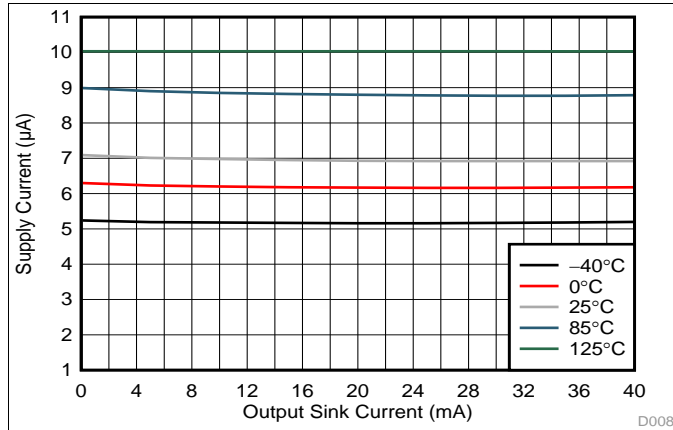


Figure 8. Supply Current (I_{DD}) vs Output Sink Current

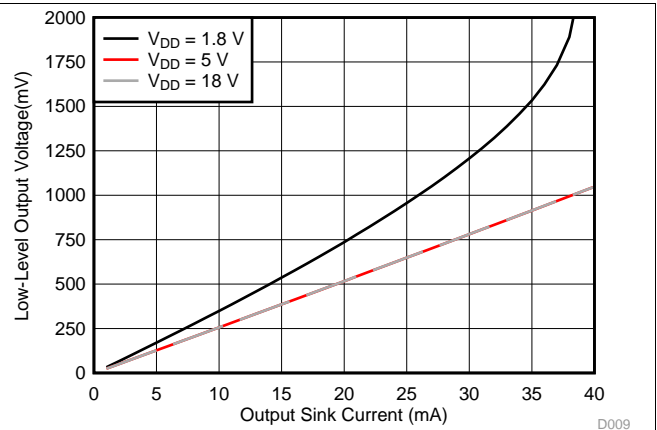


Figure 9. Output Voltage Low (V_{OL}) vs Output Sink Current (-40°C)

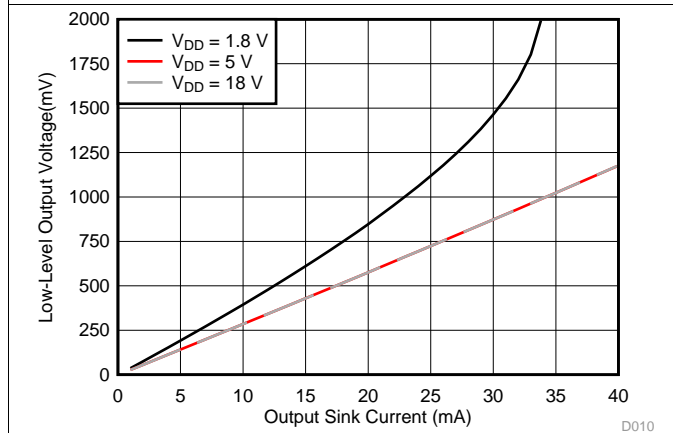


Figure 10. Output Voltage Low (V_{OL}) vs Output Sink Current (0°C)

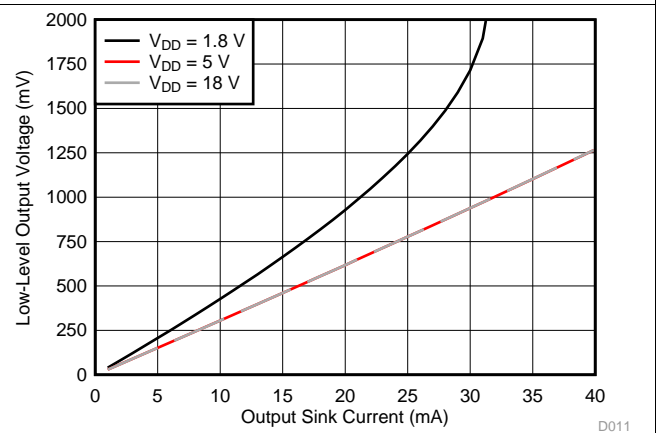


Figure 11. Output Voltage Low (V_{OL}) vs Output Sink Current (25°C)

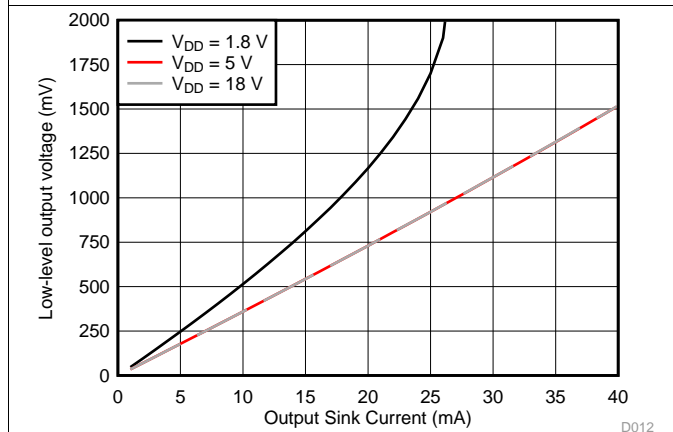


Figure 12. Output Voltage Low (V_{OL}) vs Output Sink Current (85°C)

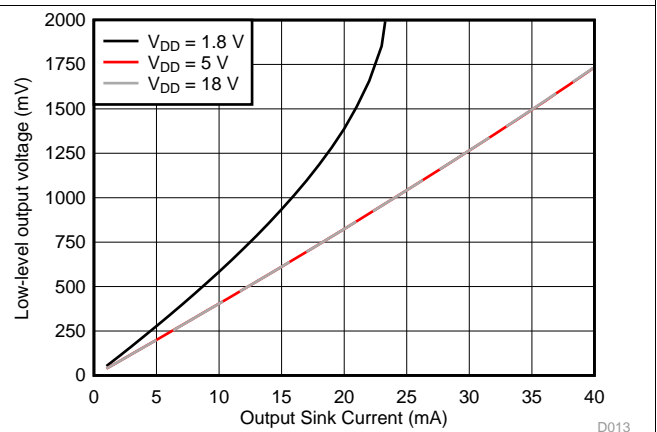


Figure 13. Output Voltage Low (V_{OL}) vs Output Sink Current (125°C)

8 Detailed Description

8.1 Overview

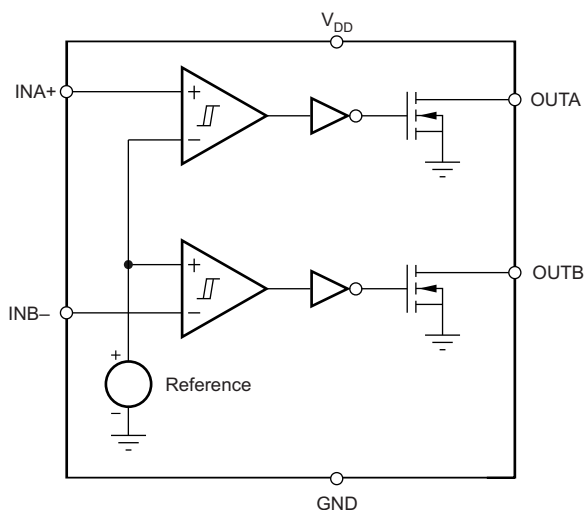
The TPS3700 device combines two comparators for overvoltage and undervoltage detection. The TPS3700 device is a wide-supply voltage range (1.8 V to 18 V) device with a high-accuracy rising input threshold of 400 mV (1% over temperature) and built-in hysteresis. The outputs are also rated to 18 V and can sink up to 40 mA.

The TPS3700 device is designed to assert the output signals, as shown in [Table 1](#). Each input terminal can be set to monitor any voltage above 0.4 V using an external resistor divider network. With the use of two input terminals of different polarities, the TPS3700 device forms a window comparator. Broad voltage thresholds can be supported that allow the device to be used in a wide array of applications.

Table 1. TPS3700 Truth Table

CONDITION	OUTPUT	STATUS
$INA+ > V_{IT+}$	OUTA high	Output A not asserted
$INA+ < V_{IT-}$	OUTA low	Output A asserted
$INB- > V_{IT+}$	OUTB low	Output B asserted
$INB- < V_{IT-}$	OUTB high	Output B not asserted

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Inputs (INA+, INB-)

The TPS3700 device combines two comparators. Each comparator has one external input (inverting and noninverting); the other input is connected to the internal reference. The comparator rising threshold is designed and trimmed to be equal to the reference voltage (400 mV). Both comparators also have a built-in falling hysteresis that makes the device less sensitive to supply rail noise and ensures stable operation.

The comparator inputs can swing from ground to 6.5 V, regardless of the device supply voltage used. Although not required in most cases, good analog design practice is to place a 1-nF to 10-nF bypass capacitor at the comparator input for extremely noisy applications to reduce sensitivity to transients and layout parasitics.

For comparator A, the corresponding output (OUTA) is driven to logic low when the input INA+ voltage drops below $(V_{IT+} - V_{hys})$. When the voltage exceeds V_{IT+} , the output (OUTA) goes to a high-impedance state; see [Figure 1](#).

Feature Description (continued)

For comparator B, the corresponding output (OUTB) is driven to logic low when the voltage at input INB– exceeds V_{IT+} . When the voltage drops below $V_{IT+} - V_{hys}$ the output (OUTB) goes to a high-impedance state; see [Figure 1](#). Together, these comparators form a window-detection function as discussed in [Window Comparator](#).

8.3.2 Outputs (OUTA, OUTB)

In a typical TPS3700 application, the outputs are connected to a reset or enable input of the processor (such as a digital signal processor [DSP], central processing unit [CPU], field-programmable gate array [FPGA], or application-specific integrated circuit [ASIC]) or the outputs are connected to the enable input of a voltage regulator (such as a DC-DC or low-dropout regulator [LDO]).

The TPS3700 device provides two open-drain outputs (OUTA and OUTB). Pullup resistors must be used to hold these lines high when the output goes to high impedance (not asserted). By connecting pullup resistors to the proper voltage rails, the outputs can be connected to other devices at the correct interface-voltage levels. The TPS3700 outputs can be pulled up to 18 V, independent of the device supply voltage. By using wired-OR logic, OUTA and OUTB can merge into one logic signal that goes low if either outputs are asserted because of a fault condition.

[Table 1](#) and [Inputs \(INA+, INB–\)](#) describe how the outputs are asserted or deasserted. See [Figure 1](#) for a timing diagram that describes the relationship between threshold voltages and the respective output.

8.3.3 Window Comparator

The inverting and noninverting configuration of the comparators forms a window-comparator detection circuit using a resistor divider network, as shown in [Figure 14](#) and [Figure 15](#). The input terminals can monitor any system voltage above 400 mV with the use of a resistor divider network. The INA+ and INB– terminals monitor for undervoltage and overvoltage conditions, respectively.

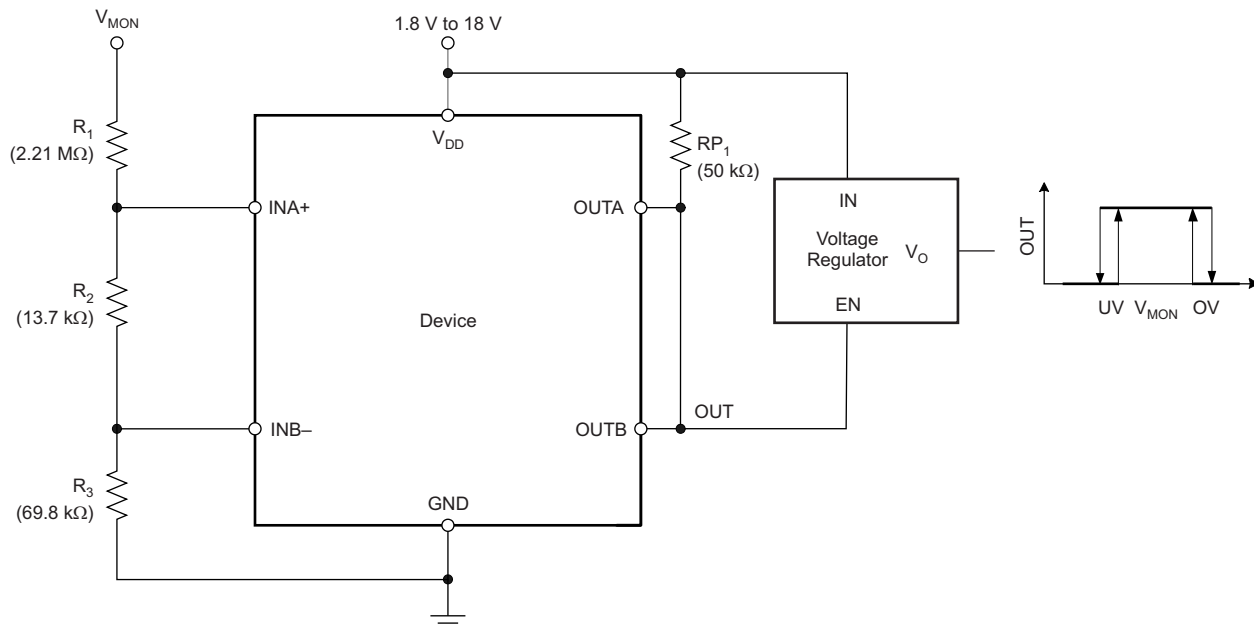


Figure 14. Window Comparator Block Diagram

Feature Description (continued)

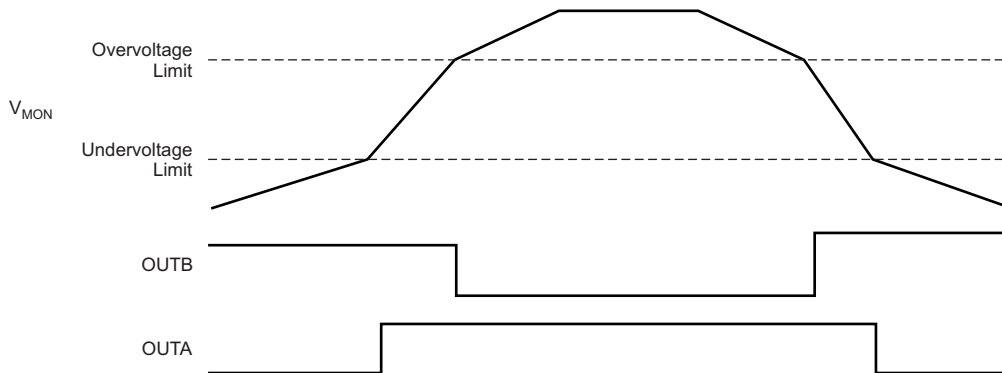


Figure 15. Window Comparator Timing Diagram

8.3.4 Immunity to Input Terminal Voltage Transients

The TPS3700 device is relatively immune to short voltage transient spikes on the input terminals. Sensitivity to transients depends on both transient duration and amplitude; see the *Minimum Pulse Width vs Threshold Overdrive Voltage* curve (Figure 7) in *Typical Characteristics*.

8.4 Device Functional Modes

8.4.1 Normal Operation ($V_{DD} > UVLO$)

When the voltage on V_{DD} is greater than 1.8 V for at least 150 μ s, the OUTA and OUTB signals correspond to the voltage on INA+ and INB– as listed in Table 1.

8.4.2 Undervoltage Lockout ($V_{(POR)} < V_{DD} < UVLO$)

When the voltage on V_{DD} is less than the device UVLO voltage, and greater than the power-on reset voltage, $V_{(POR)}$, the OUTA and OUTB signals are asserted and high impedance, respectively, regardless of the voltage on INA+ and INB–.

8.4.3 Power-On Reset ($V_{DD} < V_{(POR)}$)

When the voltage on V_{DD} is lower than the required voltage to internally pull the asserted output to GND ($V_{(POR)}$), both outputs are in a high-impedance state.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS3700 device is a wide-supply voltage window comparator that operates over a V_{DD} range of 1.8 V to 18 V. The device has two high-accuracy comparators with an internal 400-mV reference and two open-drain outputs rated to 18 V for overvoltage and undervoltage detection. The device can be used either as a window comparator or as two independent voltage monitors. The monitored voltages are set with the use of external resistors.

9.1.1 V_{PULLUP} to a Voltage Other Than V_{DD}

The outputs are often tied to V_{DD} through a resistor. However, some applications may require the outputs to be pulled up to a higher or lower voltage than V_{DD} to correctly interface with the reset and enable terminals of other devices.

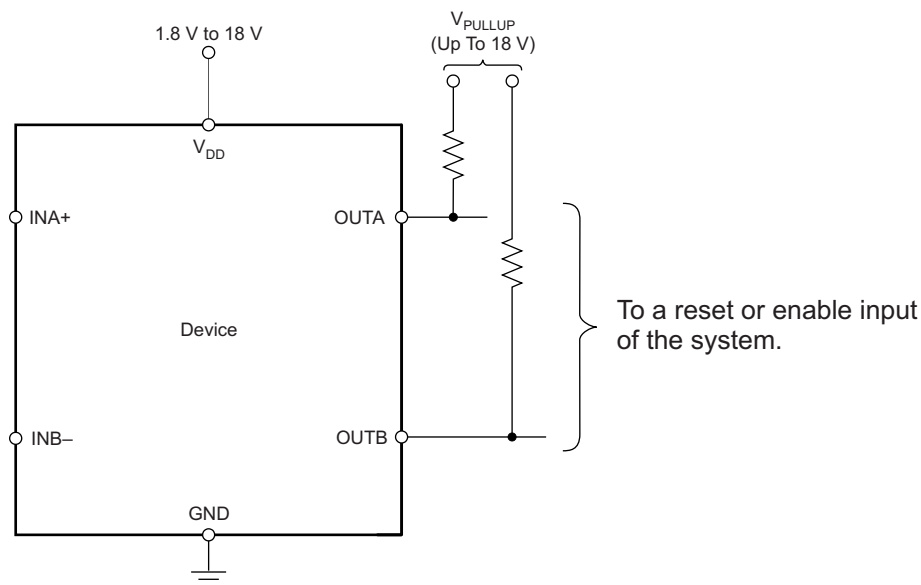


Figure 16. Interfacing to Voltages Other Than V_{DD}

Application Information (continued)

9.1.2 Monitoring V_{DD}

Many applications monitor the same rail that is powering V_{DD} . In these applications the resistor divider is simply connected to the V_{DD} rail.

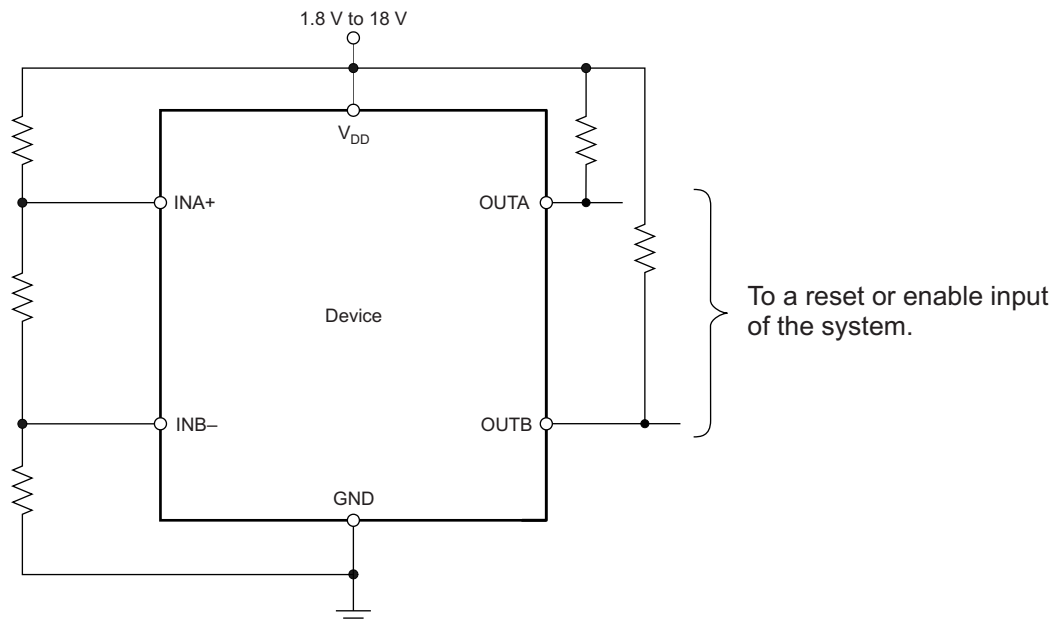
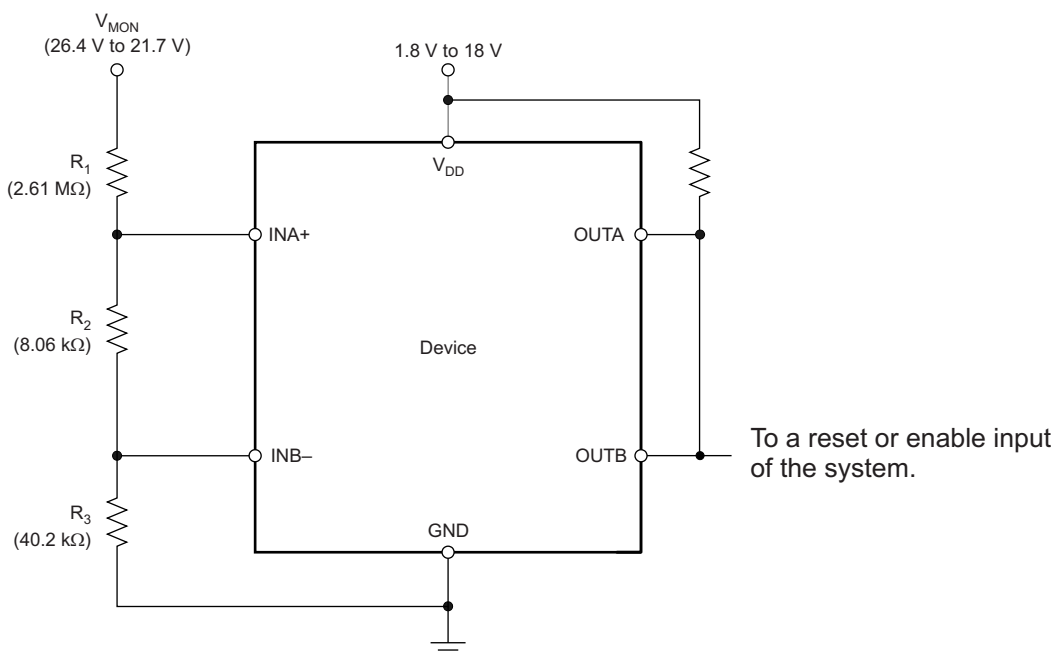


Figure 17. Monitoring the Same Voltage as V_{DD}

9.1.3 Monitoring a Voltage Other Than V_{DD}

Some applications monitor rails other than the one that is powering V_{DD} . In these types of applications the resistor divider used to set the desired thresholds is connected to the rail that is being monitored.

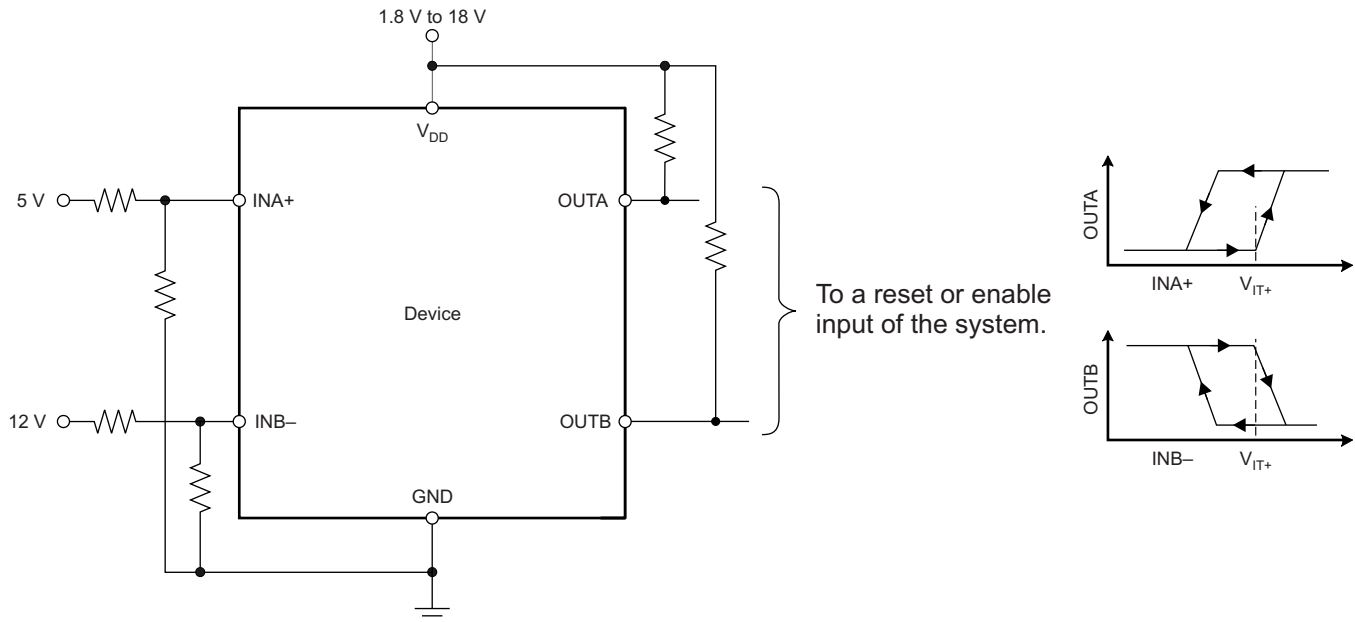


NOTE: The inputs can monitor a voltage higher than V_{DDmax} with the use of an external resistor divider network.

Figure 18. Monitoring a Voltage Other Than V_{DD}

Application Information (continued)
9.1.4 Monitoring Overvoltage and Undervoltage for Separate Rails

Some applications may want to monitor for overvoltage conditions on one rail while also monitoring for undervoltage conditions on a different rail. In these applications two independent resistor dividers must be used.



NOTE: In this case, OUTA is driven low when an undervoltage condition is detected at the 5-V rail and OUTB is driven low when an overvoltage condition is detected at the 12-V rail.

Figure 19. Monitoring Overvoltage for One Rail and Undervoltage for a Different Rail

9.2 Typical Application

The TPS3700 device is a wide-supply voltage window comparator that operates over a V_{DD} range of 1.8 to 18 V. The monitored voltages are set with the use of external resistors, so the device can be used either as a window comparator or as two independent overvoltage and undervoltage monitors.

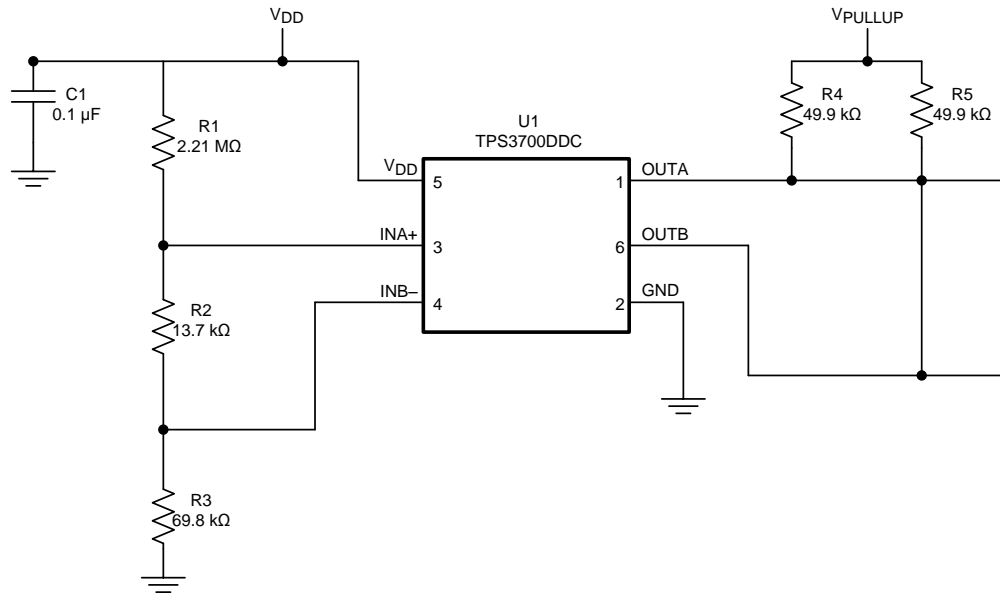


Figure 20. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the values summarized in [Table 2](#) as the input parameters.

Table 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Monitored voltage	12-V nominal rail with maximum rising and falling thresholds of $\pm 10\%$	$V_{MON(UV)} = 10.99 \text{ V (8.33\%)} \pm 2.94\%$, $V_{MON(OV)} = 13.14 \text{ V (8.33\%)} \pm 2.94\%$

9.2.2 Detailed Design Procedure

9.2.2.1 Resistor Divider Selection

Use [Equation 1](#) through [Equation 4](#) to calculate the resistor divider values and target threshold voltages.

$$R_T = R_1 + R_2 + R_3 \quad (1)$$

Select a value for R_T such that the current through the divider is approximately 100 times higher than the input current at the INA+ and INB- terminals. The resistors can have high values to minimize current consumption as a result of low-input bias current without adding significant error to the resistive divider. See the application note *Optimizing Resistor Dividers at a Comparator Input (SLVA450)* for details on sizing input resistors.

Use [Equation 2](#) to calculate the value of R_3 .

$$R_3 = \frac{R_T}{V_{MON(OV)}} \times V_{IT+}$$

where:

$$V_{MON(OV)} \text{ is the target voltage at which an overvoltage condition is detected} \quad (2)$$

Use Equation 3 or Equation 4 to calculate the value of R_2 .

$$R_2 = \left[\frac{R_T}{V_{\text{MON(no UV)}}} \times V_{\text{IT+}} \right] - R_3$$

where:

$V_{\text{MON(no UV)}}$ is the target voltage at which an undervoltage condition is removed as V_{MON} rises (3)

$$R_2 = \left[\frac{R_T}{V_{\text{MON(UV)}}} \times (V_{\text{IT+}} - V_{\text{hys}}) \right] - R_3$$

where:

$V_{\text{MON(UV)}}$ is the target voltage at which an undervoltage condition is detected (4)

The worst-case tolerance can be calculated by referring to Equation 13 in application report [SLVA450, Optimizing Resistor Dividers at a Comparator Input](#) (available for download at www.ti.com). An example of the rising threshold error, $V_{\text{MON(OV)}}$, is given in Equation 5.

$$\% \text{ ACC} = \% \text{ TOL}(V_{\text{IT+(INB)}}) + 2 \times \left[1 - \frac{V_{\text{IT+(INB)}}}{V_{\text{MON(OV)}}} \right] \times \% \text{ TOL}_R = 1\% + 2 \times \left[1 - \frac{0.4}{13.2} \right] \times 1\% = 2.94\% \quad (5)$$

9.2.2.2 Pullup Resistor Selection

To ensure proper voltage levels, the pullup resistor value is selected by ensuring that the pullup voltage divided by the resistor does not exceed the sink-current capability of the device. This confirmation is calculated by verifying that the pullup voltage minus the output-leakage current ($I_{\text{kg(OD)}}$) multiplied by the resistor is greater than the desired logic-high voltage. These values are specified in the [Electrical Characteristics](#).

Use Equation 6 to calculate the value of the pullup resistor.

$$\frac{(V_{\text{HI}} - V_{\text{PU}})}{I_{\text{kg(OD)}}} \geq R_{\text{PU}} \geq \frac{V_{\text{PU}}}{I_{\text{O}}} \quad (6)$$

9.2.2.3 Input Supply Capacitor

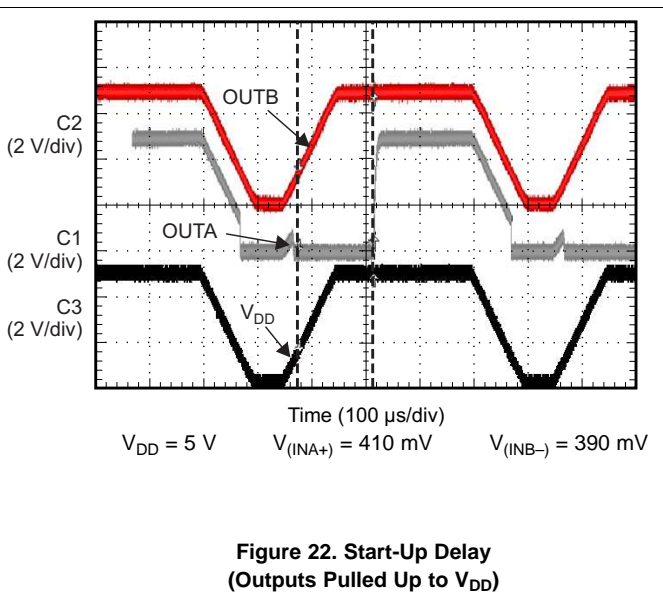
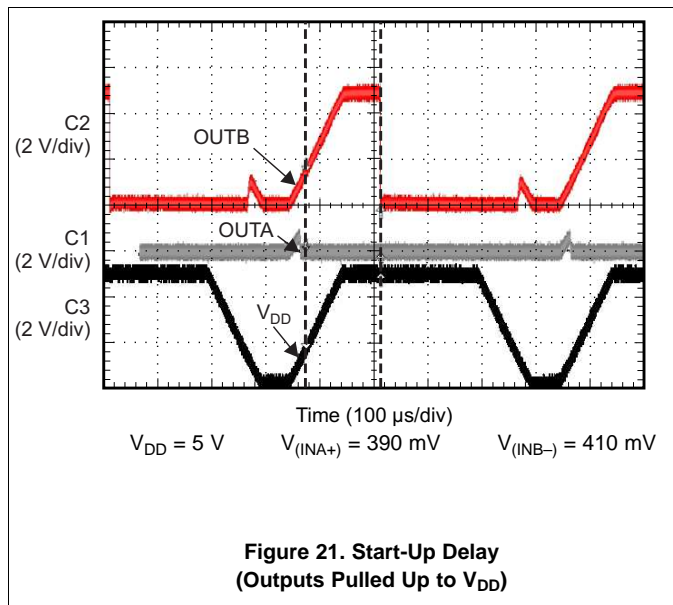
Although an input capacitor is not required for stability, connecting a 0.1- μF low equivalent series resistance (ESR) capacitor across the V_{DD} terminal and GND terminal is good analog design practice. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source.

9.2.2.4 Input Capacitors

Although not required in most cases, for extremely noisy applications, placing a 1-nF to 10-nF bypass capacitor from the comparator inputs (INA+, INB-) to the GND terminal is good analog design practice. This capacitor placement reduces device sensitivity to transients.

9.2.3 Application Curves

At $T_J = 25^\circ\text{C}$



9.3 Do's and Don'ts

It is good analog design practice to have a 0.1- μF decoupling capacitor from V_{DD} to GND.

If the monitored rail is noisy, connect decoupling capacitors from the comparator inputs to GND.

Do not use resistors for the voltage divider that cause the current through them to be less than 100 times the input current of the comparators without also accounting for the effect to the accuracy.

Do not use pullup resistors that are too small, because the larger current sunk by the output then exceeds the desired low-level output voltage (V_{OL}).

10 Power-Supply Recommendations

These devices are designed to operate from an input voltage supply range between 1.8 V and 18 V.

11 Layout

11.1 Layout Guidelines

Placing a 0.1- μ F capacitor close to the V_{DD} terminal to reduce the input impedance to the device is good analog design practice. The pullup resistors can be separated if separate logic functions are needed (see [Figure 23](#)) or both resistors can be tied to a single pullup resistor if a logical AND function is desired.

11.2 Layout Example

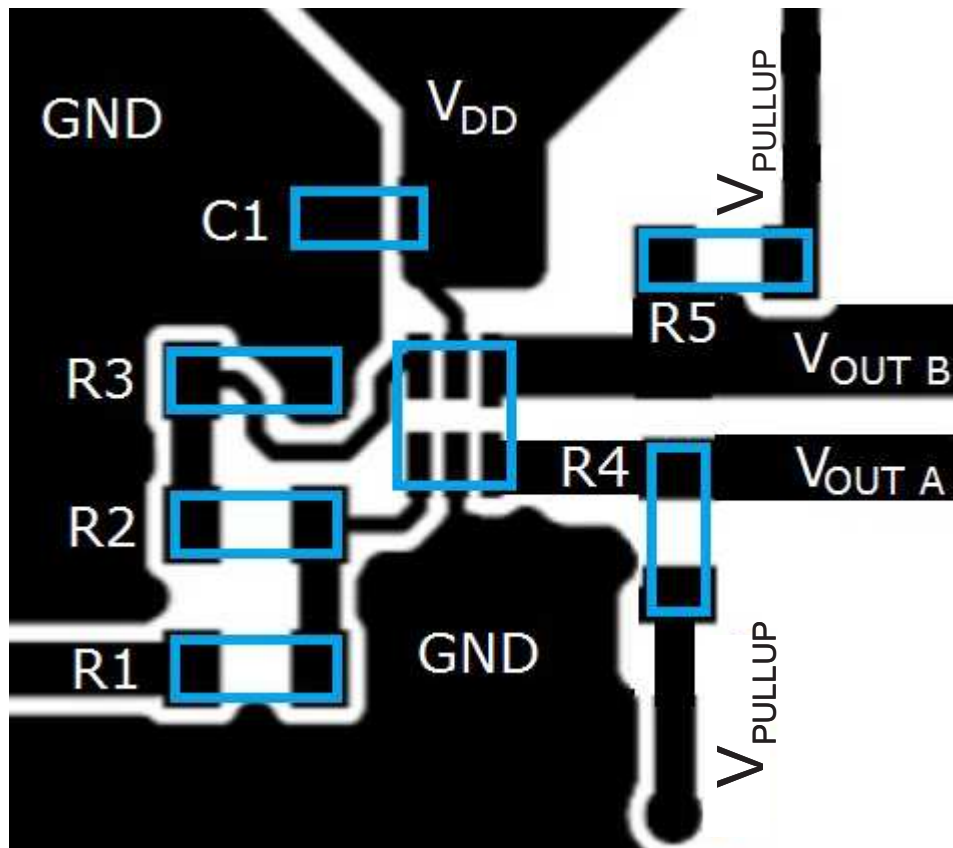


Figure 23. TPS3700 Layout Schematic

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

12.1.1.1 评估模块

有两个评估模块 (EVM) 可与 TPS3700 配套使用, 帮助评估初始电路性能。 [TPS3700EVM-114 评估模块](#)和 [TPS3700EVM-202 评估模块](#) (以及相关用户指南) 可在德州仪器 (TI) 网站上的 [TPS3700 产品文件夹](#) 中获取, 也可直接从 [TI 网上商店](#) 购买。

12.1.2 器件命名规则

表 3. 器件命名规则

产品	说明
TPS3700yyyz	yyy 为封装标识符 z 为封装数量

12.2 文档支持

12.2.1 相关文档

相关文档如下:

- 应用报告 《使用 TPS3700 作为负轨过压和欠压检测器》, [SLVA600](#)
- 应用报告 《优化比较器输入端的电阻分压器》, [SLVA450](#)
- 《TPS3700EVM-114 评估模块用户指南》, [SLVU683](#)
- 《TPS3700EVM-202 评估模块用户指南》, [SLVU950](#)

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ESD 的损坏小至导致微小的性能降级, 大至整个器件故障。精密的集成电路可能更容易受到损坏, 这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 术语表

[SLYZ022](#) — TI 术语表。

这份术语表列出并解释术语、首字母缩略词和定义。

13 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本, 请查阅左侧的导航栏。

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TPS3700DDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PXVQ	Samples
TPS3700DDCR2	ACTIVE	SOT-23-THIN	DDC	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PB4Q	Samples
TPS3700DDCT	ACTIVE	SOT-23-THIN	DDC	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PXVQ	Samples
TPS3700DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BE	Samples
TPS3700DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BE	Samples

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- Automotive: [TPS3700-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3700DDCR	SOT-23-THIN	DDC	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3700DDCR2	SOT-23-THIN	DDC	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q2
TPS3700DDCT	SOT-23-THIN	DDC	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3700DSER	WSO	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TPS3700DSET	WSO	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3700DDCR	SOT-23-THIN	DDC	6	3000	195.0	200.0	45.0
TPS3700DDCR2	SOT-23-THIN	DDC	6	3000	195.0	200.0	45.0
TPS3700DDCT	SOT-23-THIN	DDC	6	250	195.0	200.0	45.0
TPS3700DSE	WSON	DSE	6	3000	203.0	203.0	35.0
TPS3700DSET	WSON	DSE	6	250	203.0	203.0	35.0

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