

TPS2330, TPS2331 SINGLE HOT-SWAP POWER CONTROLLERS WITH CIRCUIT BREAKER AND POWER-GOOD REPORTING

SLVS277D – MARCH 2000 – REVISED SEPTEMBER 2001

features

- Single-Channel High-Side MOSFET Driver
- Input Voltage: 3 V to 13 V
- Inrush Current Limiting With dv/dt Control
- Circuit-Breaker Control With Programmable Current Limit and Transient Timer
- Power-Good Reporting With Transient Filter
- CMOS- and TTL-Compatible Enable Input
- Low 5- μ A Standby Supply Current . . . Max
- Available in 14-Pin SOIC and TSSOP Package
- -40°C to 85°C Ambient Temperature Range
- Electrostatic Discharge Protection

applications

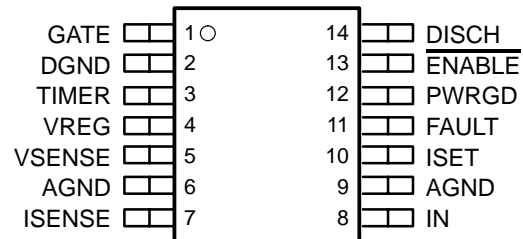
- Hot-Swap/Plug/Dock Power Management
- Hot-Plug PCI, Device Bay
- Electronic Circuit Breaker

description

The TPS2330 and TPS2331 are single-channel hot-swap controllers that use external N-channel MOSFETs as high-side switches in power applications. Features of these devices, such as overcurrent protection (OCP), inrush-current control, output-power status reporting, and separation of load transients from actual load increases, are critical requirements for hot-swap applications.

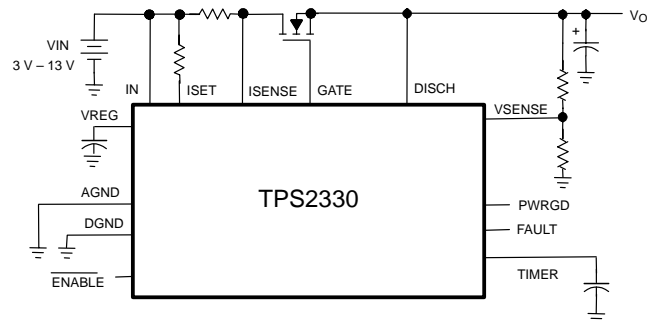
The TPS2330/31 devices incorporate undervoltage lockout (UVLO) and power-good (PG) reporting to ensure the device is off at start-up and confirm the status of the output voltage rails during operation. An internal charge pump, capable of driving multiple MOSFETs, provides enough gate-drive voltage to fully enhance the N-channel MOSFETs. The charge pump controls both the rise times and fall times (dv/dt) of the MOSFETs, reducing power transients during power up/down. The circuit-breaker functionality combines the ability to sense overcurrent conditions with a timer function; this allows designs such as DSPs, that may have high peak currents during power-state transitions, to disregard transients for a programmable period.

D OR PW PACKAGE
(TOP VIEW)



NOTE: Terminal 13 is active high on TPS2331.

typical application



AVAILABLE OPTIONS

TA	HOT-SWAP CONTROLLER DESCRIPTION	PIN COUNT	PACKAGES	
			ENABLE	ENABLE
-40°C to 85°C	Dual-channel with independent OCP and adjustable PG	20	TPS2300IPW	TPS2301IPW
	Dual-channel with interdependent OCP and adjustable PG	20	TPS2310IPW	TPS2311IPW
	Dual-channel with independent OCP	16	TPS2320ID TPS2320IPW	TPS2321ID TPS2321IPW
	Single-channel with OCP and adjustable PG	14	TPS2330ID TPS2330IPW	TPS2331ID TPS2331IPW

† The packages are available left-end taped and reeled (indicated by the R suffix on the device type; e.g., TPS2331IPWR).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

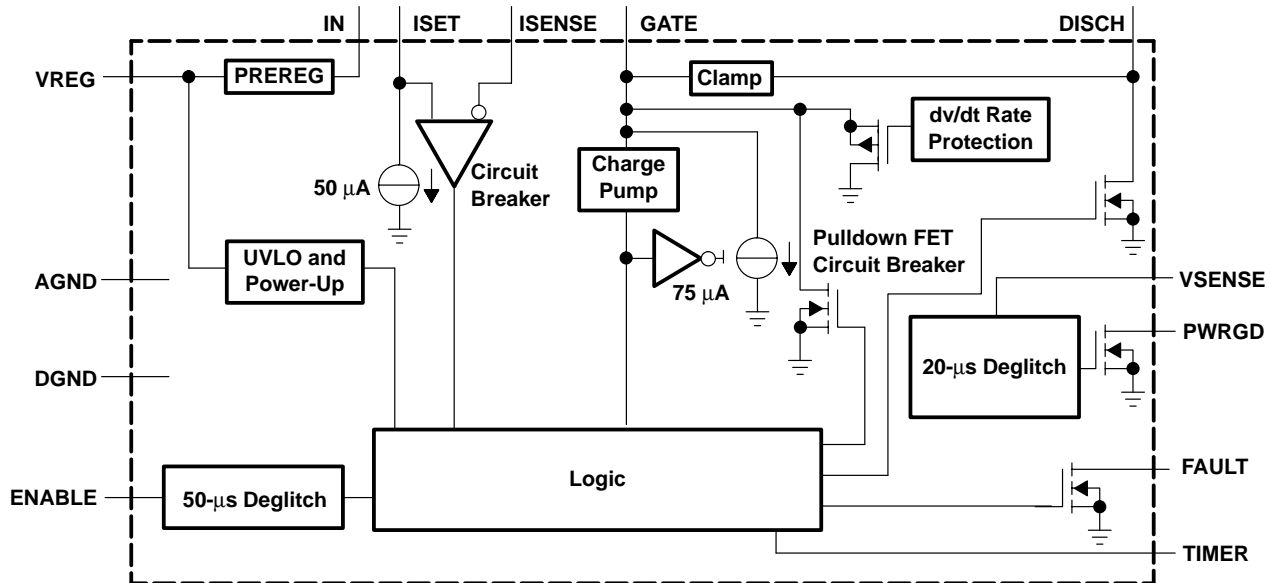
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functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AGND	6,9	I	Analog ground, connects to DGND as close as possible
DGND	2	I	Digital ground
DISCH	14	O	Discharge transistor
ENABLE/ ENABLE	13	I	Active low (TPS2330) or active high enable (TPS2331)
FAULT	11	O	Overcurrent fault, open-drain output
GATE	1	O	Connects to gate of high-side MOSFET
IN	8	I	Input voltage
ISENSE	7	I	Current-sense input
ISET	10	I	Adjusts circuit-breaker threshold with resistor connected to IN
PWRGD	12	O	Open-drain output, asserted low when VSENSE voltage is less than reference.
TIMER	3	O	Adjusts circuit-breaker deglitch time
VREG	4	O	Connects to bypass capacitor, for stable operation
VSENSE	5	I	Power-good sense input

detailed description

DISCH – DISCH should be connected to the source of the external N-channel MOSFET transistor connected to GATE. This pin discharges the load when the MOSFET transistor is disabled. They also serve as reference-voltage connection for internal gate-voltage-clamp circuitry.

ENABLE or ENABLER – $\overline{\text{ENABLE}}$ for TPS2330 is active low. ENABLE for TPS2331 is active high. When the controller is enabled, GATE voltage will power up to turn on the external MOSFETs. When the $\overline{\text{ENABLE}}$ pin is pulled high for TPS2330 or the ENABLE pin is pulled low for TPS2331 for more than 50 μs , the gate of the MOSFET is discharged at a controlled rate by a current source, and a transistor is enabled to discharge the output bulk capacitance. In addition, the device turns on the internal regulator PREREG (see VREG) when enabled and shuts down PREREG when disabled so that total supply current is much less than 5 μA .

FAULT – FAULT is an open-drain overcurrent flag output. When an overcurrent condition is sustained long enough to charge TIMER to 0.5 V, the device latches off and pulls FAULT low. In order to turn the device back on, either the enable pin has to be toggled or the input power has to be cycled.

GATE – GATE connects to the gate of the external N-channel MOSFET transistor. When the device is enabled, internal charge-pump circuitry pulls this pin up by sourcing approximately 15 μA . The turnon slew rates depend upon the capacitance present at the GATE terminal. If desired, the turnon slew rates can be further reduced by connecting capacitors between this pin and ground. These capacitors also reduce inrush current and protect the device from false overcurrent triggering during power up. The charge-pump circuitry generates gate-to-source voltages of 9 V–12 V across the external MOSFET transistor.

IN – IN should be connected to the power source driving the external N-channel MOSFET transistor connected to GATE. The TPS2330/31 draws its operating current from IN, and remains disabled until the IN power supply has been established. The device has been constructed to support 3-V, 5-V, or 12-V operation.

ISENSE, ISET – ISENSE in combination with ISET implements overcurrent sensing for GATE. ISET sets the magnitude of the current that generates an overcurrent fault, through a external resistor connected to ISET. An internal current source draws 50 μA from ISET. With a sense resistor from IN to ISENSE, which is also connected to the drain of the external MOSFET, the voltage on the sense resistor reflects the load current. An overcurrent condition is assumed to exist if ISENSE is pulled below ISET.

PWRGD – PWRGD signals the presence of undervoltage conditions on VSENSE. The pin is an open-drain output and is pulled low during an undervoltage condition. To minimize erroneous PWRGD responses from transients on the voltage rail, the voltage sense circuit incorporates a 20- μs deglitch filter. When VSENSE is lower than the reference voltage (about 1.23 V), PWRGD is active low to indicate an undervoltage condition on the power-rail voltage. PWRGD may not correctly report power conditions when the device is disabled because there is no gate drive power for the PWRGD output transistor in the disable mode, or, in other words, PWRGD is floating. Therefore, PWRGD is pulled up to its pull-up power supply rail in disable mode.

TIMER – A capacitor on TIMER sets the time during which the power switch can be in overcurrent before turning off. When the overcurrent protection circuits sense an excessive current, a current source is enabled which charges the capacitor on TIMER. Once the voltage on TIMER reaches approximately 0.5 V, the circuit-breaker latch is set and the power switch is latched off. Power must be recycled or the ENABLE pin must be toggled to restart the controller. In high-power or high-temperature applications, a minimum 50-pF capacitor is strongly recommended from TIMER to ground, to prevent any false triggering.

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detailed description (continued)

VREG – VREG is the output of an internal low-dropout voltage regulator, where IN1 is the input. The regulator is used to generate a regulated voltage source, less than 5.5 V, for the device. A 0.1- μ F ceramic capacitor should be connected between VREG and ground to aid in noise rejection. In this configuration, upon disabling the device, the internal low-dropout regulator will also be disabled, which removes power from the internal circuitry and allows the device to be placed in low-quiescent-current mode. In applications where IN1 is less than 5.5 V, VREG and IN1 may be connected together. However, under these conditions, disabling the device may not place the device in low-quiescent-current mode, because the internal low-dropout voltage regulator is being bypassed, thereby keeping internal circuitry operational. If VREG and IN1 are connected together, a 0.1- μ F ceramic capacitor between VREG and ground is not needed if IN1 already has a bypass capacitor of 1 μ F to 10 μ F.

VSENSE – VSENSE can be used to detect undervoltage conditions on external circuitry. If VSENSE senses a voltage below approximately 1.23 V, PWRGD is pulled low.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Input voltage range:	$V_{I(IN)}, V_{I(ISENSE)}, V_{I(VSENSE)}, V_{I(ISET)}, V_{I(ENABLE)}$	-0.3 V to 15 V
	$V_{I(VREG)}$	-0.3 V to 7 V
Output voltage range:	$V_{O(GATE)}$	-0.3 V to 30 V
	$V_{O(DISCH)}, V_{O(PWRGD)}, V_{O(FAULT)}, V_{O(TIMER)}$	-0.3 V to 15V
Sink current range:	$I_{(GATE)}, I_{(DISCH)}$	0 mA to 100 mA
	$I_{(PWRGD)}, I_{(TIMER)}, I_{(FAULT)}$	0 mA to 10 mA
Operating virtual junction temperature range, T_J		-40°C to 100°C
Storage temperature range, T_{stg}		-55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are respect to DGND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
PW-14	755 mW	10.07 mW/°C	302 mW	151 mW
D-14	613 mW	8.18 mW/°C	245 mW	123 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Input voltage, V_I	$V_{I(IN)}, V_{I(ISENSE)}, V_{I(VSENSE)}, V_{I(ISET)}$	3		13	V
	$V_{I(VREG)}$	3		5.5	
Operating virtual junction temperature, T_J		-40		100	°C



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**electrical characteristics over recommended operating temperature range ($-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$),
 $3\text{ V} \leq V_{I(IN)} \leq 13\text{ V}$ (unless otherwise noted)**

general

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{I(IN)}$	Input current, IN	$V_{I(ENABLE)} = 5\text{ V}$ (TPS2331), $V_{I(ENABLE)} = 0\text{ V}$ (TPS2330)		0.5	1	mA
$I_{I(stby)}$	Standby current (sum of currents into IN ISENSE and ISET)	$V_{I(ENABLE)} = 0\text{ V}$ (TPS2331), $V_{I(ENABLE)} = 5\text{ V}$ (TPS2330)			5	μA

GATE

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{G(GATE_3V)}$	Gate voltage	$I_{I(GATE)} = 500\text{ nA}$, DISCH open	$V_{I(IN)} = 3\text{ V}$	9	11.5	V
$V_{G(GATE_4.5V)}$			$V_{I(IN)} = 4.5\text{ V}$	10.5	14.5	
$V_{G(GATE_10.8V)}$			$V_{I(IN)} = 10.8\text{ V}$	16.8	21	
$V_{C(GATE)}$	Clamping voltage, GATE to DISCH		9	10	12	V
$I_{S(GATE)}$	Source current, GATE	$3\text{ V} \leq V_{I(IN)} \leq 13.2\text{ V}$, $3\text{ V} \leq V_{O(VREG)} \leq 5.5\text{ V}$, $V_{I(GATE)} = V_{I(IN)} + 6\text{ V}$	10	14	20	μA
	Sink current, GATE	$3\text{ V} \leq V_{I(IN)} \leq 13.2\text{ V}$, $3\text{ V} \leq V_{O(VREG)} \leq 5.5\text{ V}$, $V_{I(GATE)} = V_{I(IN)}$	50	75	100	μA
$t_r(GATE)$	Rise time, GATE	C_g to GND = 1 nF (see Note 2)	$V_{I(IN)} = 3\text{ V}$	0.5		ms
			$V_{I(IN)} = 4.5\text{ V}$	0.6		
			$V_{I(IN)} = 10.8\text{ V}$	1		
$t_f(GATE)$	Fall time, GATE	C_g to GND = 1 nF (see Note 2)	$V_{I(IN)} = 3\text{ V}$	0.1		ms
			$V_{I(IN)} = 4.5\text{ V}$	0.12		
			$V_{I(IN)} = 10.8\text{ V}$	0.2		

NOTE 2: Specified, but not production tested.

TIMER

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(TO_TIMER)}$	Threshold voltage, TIMER		0.4	0.5	0.6	V
	Charge current, TIMER	$V_{I(TIMER)} = 0\text{ V}$	35	50	65	μA
	Discharge current, TIMER	$V_{I(TIMER)} = 1\text{ V}$	1	2.5		mA

circuit breaker

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT(CB)}$	Undervoltage voltage, circuit breaker	$R_{ISET} = 1\text{ k}\Omega$	40	50	60	mV
$I_{(IB_SENSE)}$	Input bias current, ISENSE			0.1	5	μA
	Discharge current, GATE	$V_{O(GATE)} = 4\text{ V}$	400	800		mA
		$V_{O(GATE)} = 1\text{ V}$	25	150		
$t_{pd(CB)}$	Propagation (delay) time, comparator inputs to gate output	$C_g = 50\text{ pF}$, 10 mV overdrive, (50% to 10%) $C_{TIMER} = 50\text{ pF}$		1.3		μs

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 $3\text{ V} \leq V_{I(\text{IN})} \leq 13\text{ V}$ (unless otherwise noted) (continued)

ENABLE, active low (TPS2330)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$V_{IH(\overline{\text{ENABLE}})}$	High-level input voltage, $\overline{\text{ENABLE}}$	2			V	
$V_{IL(\overline{\text{ENABLE}})}$	Low-level input voltage, $\overline{\text{ENABLE}}$			0.8	V	
$R_{I(\overline{\text{ENABLE}})}$	Input pullup resistance, $\overline{\text{ENABLE}}$	See Note 3	100	200	300	k Ω
$t_{d(\text{off}_{\overline{\text{ENABLE}}})}$	Turnoff delay time, $\overline{\text{ENABLE}}$	$V_{I(\overline{\text{ENABLE}})}$ increasing above stop threshold; 100 ns rise time, 20 mV overdrive (see Note 2)		60	μs	
$t_{d(\text{on}_{\overline{\text{ENABLE}}})}$	Turnon delay time, $\overline{\text{ENABLE}}$	$V_{I(\overline{\text{ENABLE}})}$ decreasing below start threshold; 100 ns fall time, 20 mV overdrive (see Note 2)		125	μs	

NOTES: 2. Specified, but not production tested.

3. Test I_O of $\overline{\text{ENABLE}}$ at $V_{I(\overline{\text{ENABLE}})} = 1\text{ V}$ and 0 V , then $R_{I(\overline{\text{ENABLE}})} = \frac{1\text{ V}}{I_{O_{0V}} - I_{O_{1V}}}$

ENABLE, active high (TPS2331)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IH(\text{ENABLE})}$	High-level input voltage, ENABLE	2			V
$V_{IL(\text{ENABLE})}$	Low-level input voltage, ENABLE			0.7	V
$R_{I(\text{ENABLE})}$	Input pulldown resistance, ENABLE	100	150	300	k Ω
$t_{d(\text{on}_{\text{ENABLE}})}$	Turnon delay time, ENABLE	$V_{I(\text{ENABLE})}$ increasing above start threshold; 100 ns rise time, 20 mV overdrive (see Note 2)		85	μs
$t_{d(\text{off}_{\text{ENABLE}})}$	Turnoff delay time, ENABLE	$V_{I(\text{ENABLE})}$ decreasing below stop threshold; 100 ns fall time, 20 mV overdrive (see Note 2)		100	μs

NOTE 2: Specified, but not production tested.

PREREG

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$V_{(\text{VREG})}$	PREREG output voltage	$4.5 \leq V_{I(\text{IN})} \leq 13\text{ V}$	3.5	4.1	5.5	V
$V_{(\text{drop}_{\text{PREREG}})}$	PREREG dropout voltage	$V_{I(\text{IN})} = 3\text{ V}$		0.1		V

VREG UVLO

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(\text{TO}_{\text{UVLOstart}})}$	Output threshold voltage, start	2.75	2.85	2.95	V
$V_{(\text{TO}_{\text{UVLOstop}})}$	Output threshold voltage, stop	2.65	2.78		V
$V_{\text{hys}(\text{UVLO})}$	Hysteresis	50	75		mV
	UVLO sink current, GATE	$V_{I(\text{GATE})} = 2\text{ V}$		10	mA



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 $3\text{ V} \leq V_{I(IN1)} \leq 13\text{ V}$, $3\text{ V} \leq V_{I(IN2)} \leq 5.5\text{ V}$ (unless otherwise noted) (continued)**

PWRGD

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT(ISENSE)}$	Trip threshold, VSENSE	$V_{I(VSENSE)}$ decreasing	1.2	1.225	1.25	V
V_{hys}	Hysteresis voltage, power-good comparator		20	30	40	mV
$V_{O(sat_PWRGD)}$	Output saturation voltage, PWRGD	$I_O = 2\text{ mA}$		0.2	0.4	V
$V_{O(VREGmin)}$	Minimum $V_{O(VREG)}$ for valid power-good	$I_O = 100\ \mu\text{A}$, $V_{O(PWRGD)} = 1\text{ V}$			1	V
	Input bias current, power-good comparator	$V_{I(VSENSE)} = 5.5\text{ V}$			1	μA
$I_{lkg(PWRGD)}$	Leakage current, PWRGD	$V_{O(PWRGD)} = 13\text{ V}$			1	μA
t_{dr}	Delay time, rising edge, PWRGD	$V_{I(VSENSE)}$ increasing, Overdrive = 20 mV, $t_r = 100\text{ ns}$, See Note 2		25		μs
t_{df}	Delay time, falling edge, PWRGD	$V_{I(VSENSE)}$ decreasing, Overdrive = 20 mV, $t_f = 100\text{ ns}$, See Note 2		2		μs

NOTE 2: Specified, but not production tested.

FAULT output

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{O(sat_FAULT)}$	Output saturation voltage, FAULT	$I_O = 2\text{ mA}$			0.4	V
$I_{lkg(FAULT)}$	Leakage current, FAULT	$V_{O(FAULT)} = 13\text{ V}$			1	μA

DISCH

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(DISCH)}$	Discharge current, DISCH	$V_{I(DISCH)} = 1.5\text{ V}$, $V_{I(VIN)} = 5\text{ V}$	5	10		mA
$V_{IH(DISCH)}$	Discharge on high-level input voltage		2			V
$V_{IL(DISCH)}$	Discharge on low-level input voltage				1	V

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PARAMETER MEASUREMENT INFORMATION

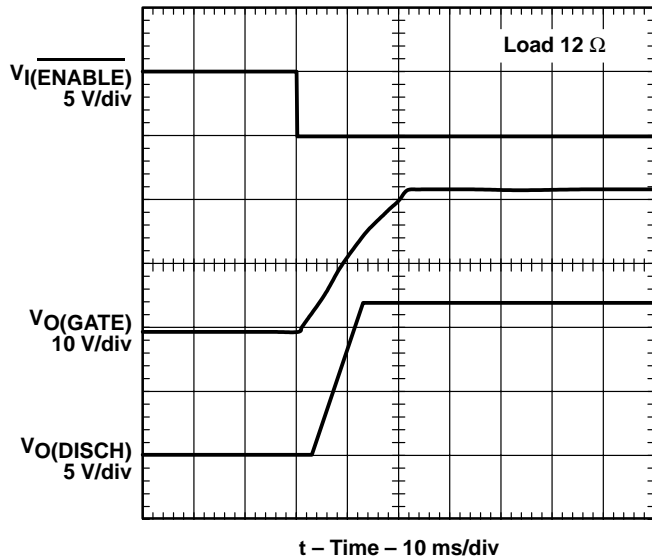


Figure 1. Turnon Voltage Transition

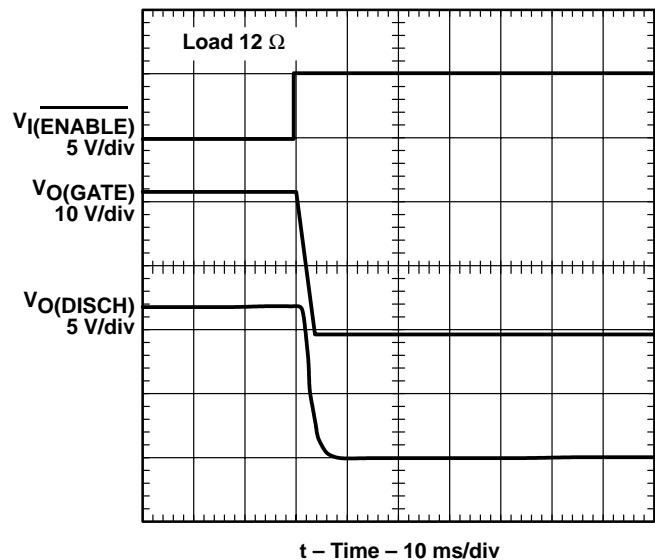


Figure 2. Turnoff Voltage Transition

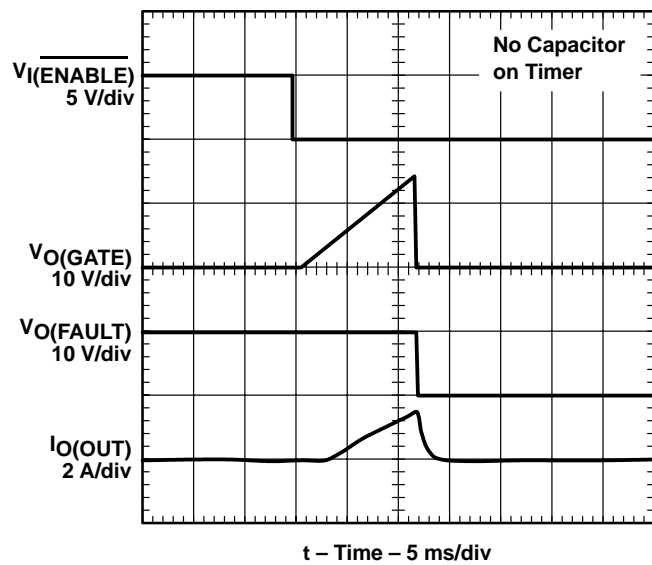


Figure 3. Overcurrent Response: Enabled Into Overcurrent Load

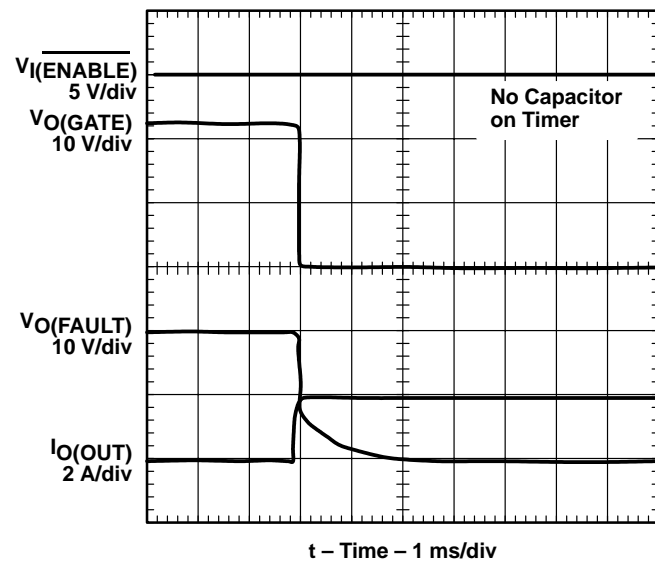


Figure 4. Overcurrent Response: an Overcurrent Load Plugged Into the Enabled Board

PARAMETER MEASUREMENT INFORMATION

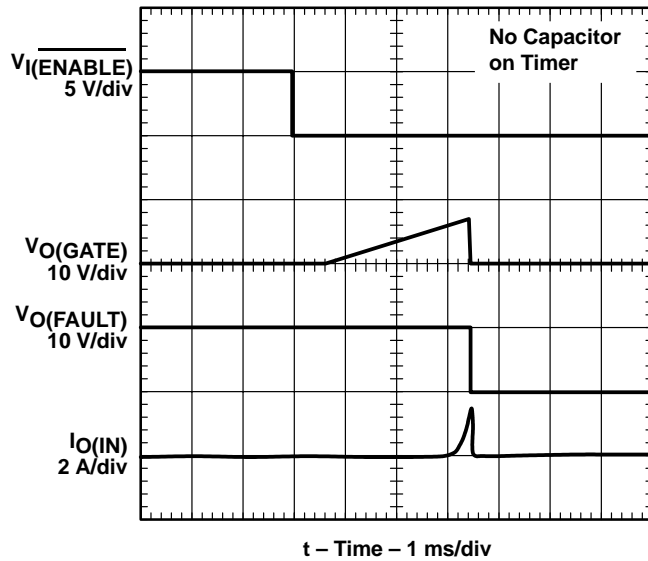


Figure 5. Enabled Into Short Circuit

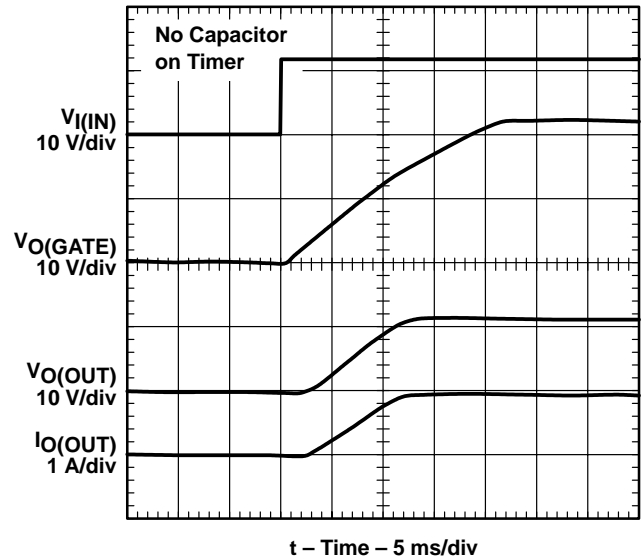


Figure 6. Hot Plug

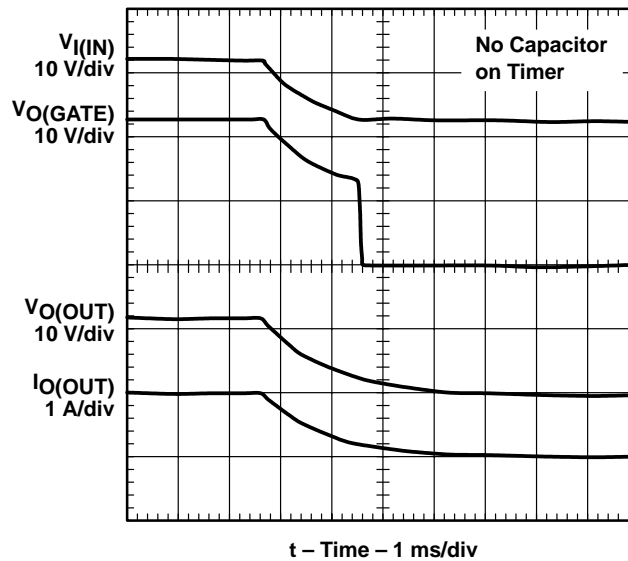


Figure 7. Hot Removal

TYPICAL CHARACTERISTICS

SUPPLY CURRENT (ENABLED)
 vs
 INPUT VOLTAGE

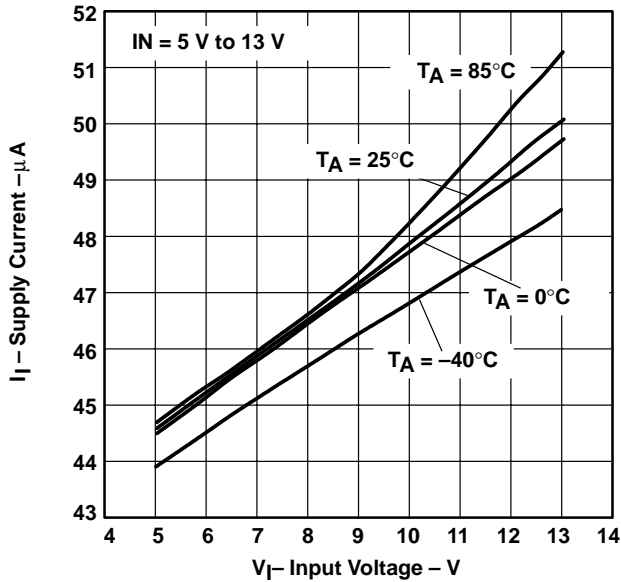


Figure 8

SUPPLY CURRENT (DISABLED)
 vs
 INPUT VOLTAGE

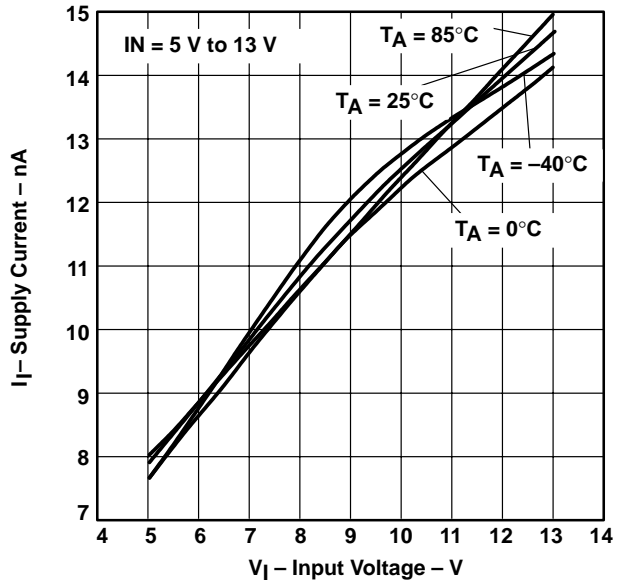


Figure 9

GATE OUTPUT VOLTAGE
 vs
 INPUT VOLTAGE

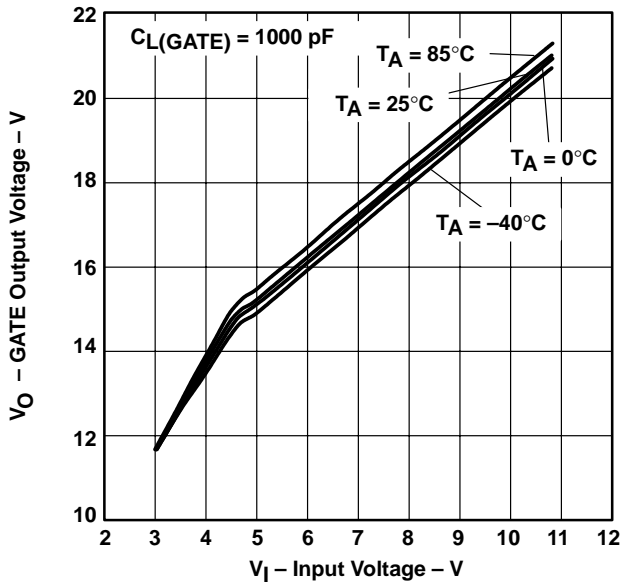


Figure 10

GATE VOLTAGE RISE TIME
 vs
 GATE LOAD CAPACITANCE

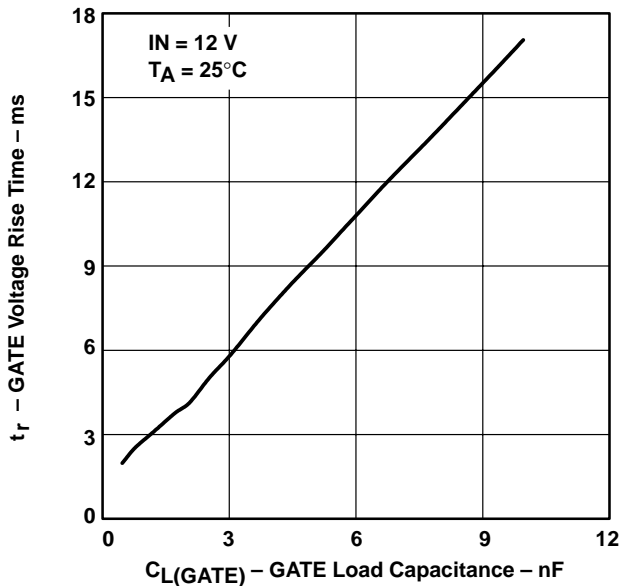


Figure 11

TYPICAL CHARACTERISTICS

GATE VOLTAGE FALL TIME
 VS
 GATE LOAD CAPACITANCE

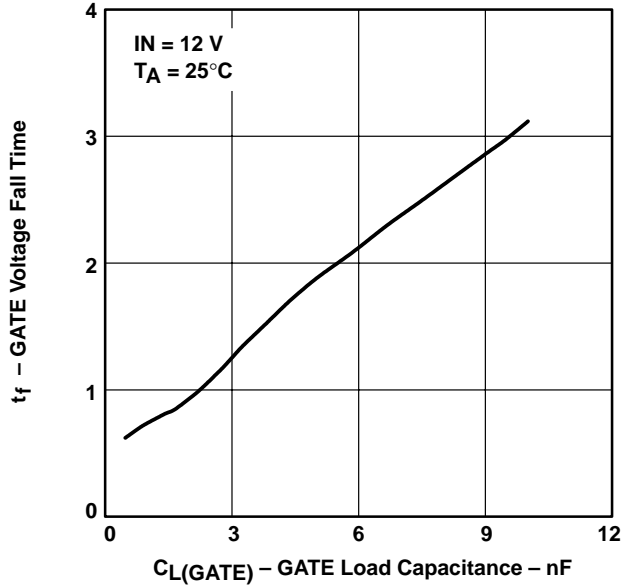


Figure 12

GATE OUTPUT CURRENT
 VS
 GATE VOLTAGE

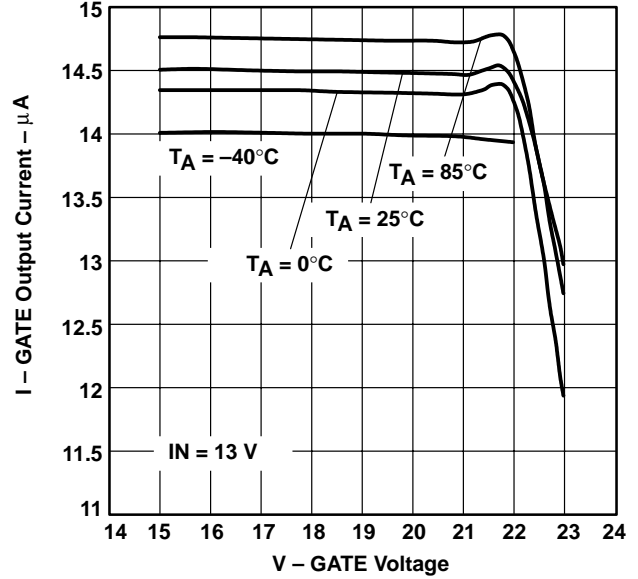


Figure 13

CIRCUIT-BREAKER RESPONSE TIME
 VS
 TIMER CAPACITANCE

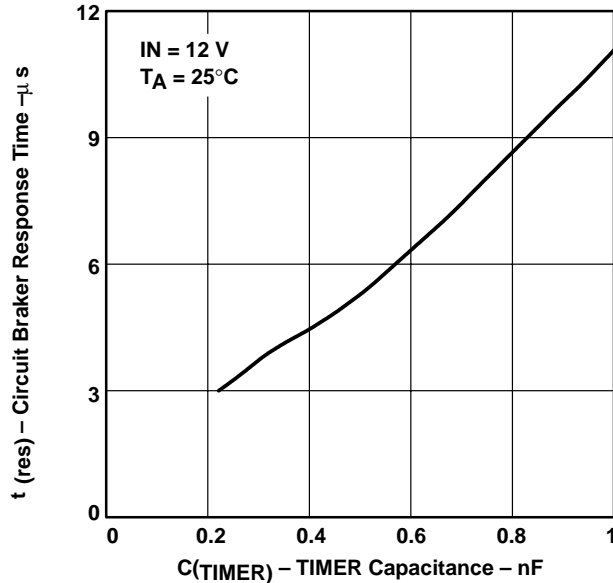


Figure 14

LOAD VOLTAGE DISCHARGE TIME
 VS
 LOAD CAPACITANCE

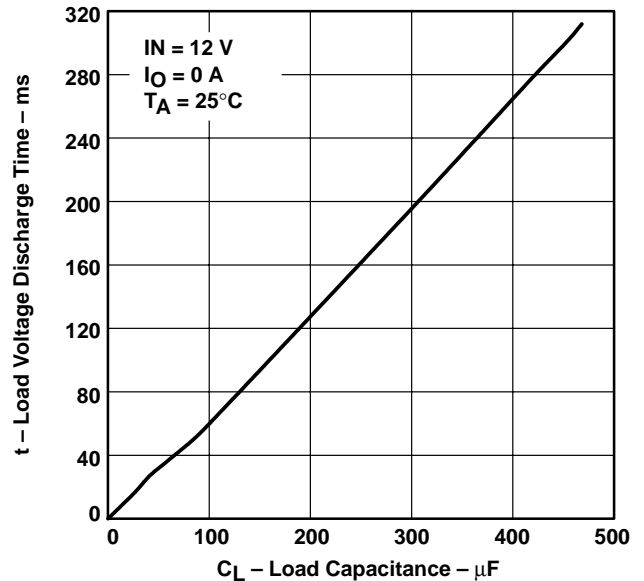


Figure 15

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TYPICAL CHARACTERISTICS

UVLO START AND STOP THRESHOLDS
VS
TEMPERATURE

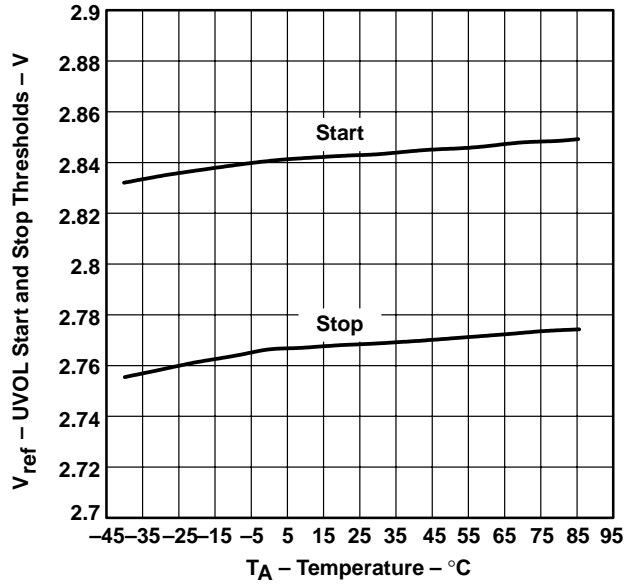


Figure 16

PWRGD INPUT THRESHOLD
VS
TEMPERATURE

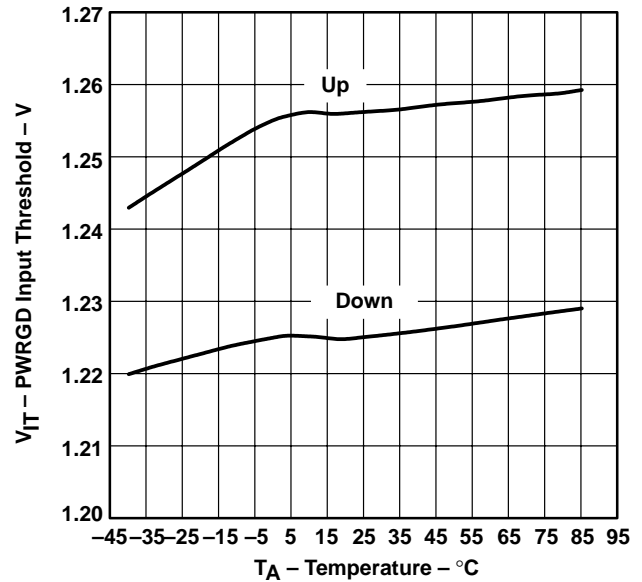


Figure 17



APPLICATION INFORMATION

typical application diagram

This diagram shows a typical dual hot-swap application. The pullup resistors at PWRGD and FAULT should be relatively large (e.g. 100 k Ω) to reduce power loss unless they are required to drive a large load.

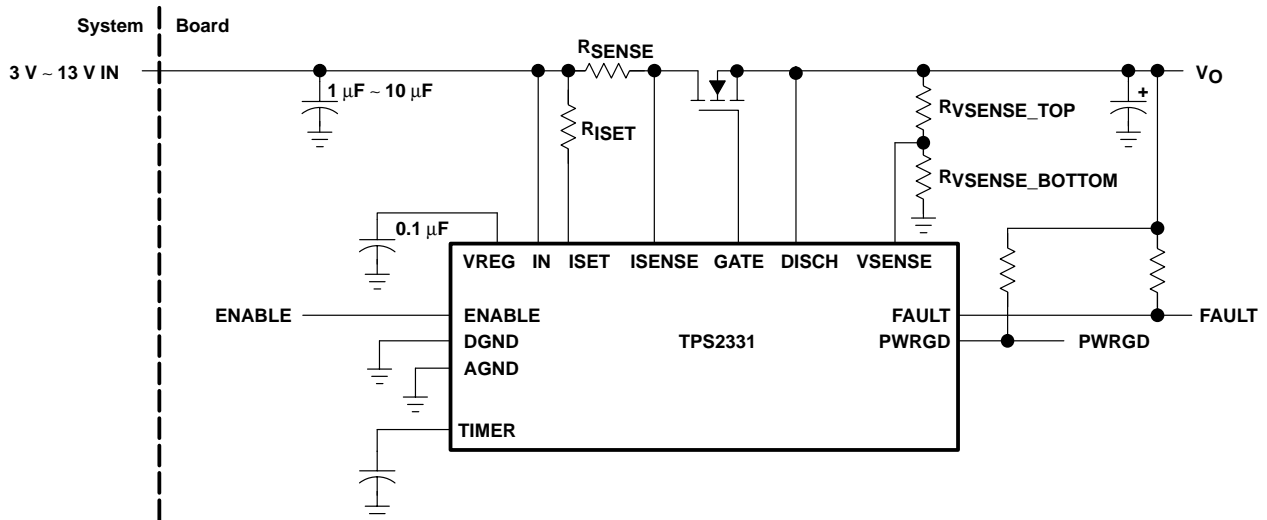


Figure 18. Typical Hot-Swap Application

input capacitor

A 0.1- μF ceramic capacitor in parallel with a 1- μF ceramic capacitor should be placed on the input power terminals near the connector on the hot-plug board to help stabilize the voltage rails on the cards. The TPS2330/31 does not need to be mounted near the connector or these input capacitors. For applications with more severe power environments, a 2.2- μF or higher ceramic capacitor is recommended near the input terminals of the hot-plug board. A bypass capacitor for IN should be placed close to the device.

output capacitor

A 0.1- μF ceramic capacitor is recommended per load on the TPS2330/31; these capacitors should be placed close to the external FETs and to TPS2330/31. A larger bulk capacitor on the load is also recommended. The value of the bulk capacitor should be selected based on the power requirements and the transients generated by the application.

external FET

To deliver power from the input sources to the loads, the controller needs an external N-channel MOSFET. A few widely used MOSFETs are shown in Table 1. But many other MOSFETs on the market can also be used with TPS23xx in hot-swap systems.

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APPLICATION INFORMATION

Table 1. Some Available N-Channel MOSFETs

CURRENT RANGE (A)	PART NUMBER	DESCRIPTION	MANUFACTURER
0 to 2	IRF7601	N-channel, $r_{DS(on)} = 0.035 \Omega$, 4.6 A, Micro-8	International Rectifier
	MTSF3N03HDR2	N-channel, $r_{DS(on)} = 0.040 \Omega$, 4.6 A, Micro-8	ON Semiconductor
	IRF7101	Dual N-channel, $r_{DS(on)} = 0.1 \Omega$, 2.3 A, SO-8	International Rectifier
	MMSF5N02HDR2	Dual N-channel, $r_{DS(on)} = 0.04 \Omega$, 5 A, SO-8	ON Semiconductor
2 to 5	IRF7401	N-channel, $r_{DS(on)} = 0.022 \Omega$, 7 A, SO-8	International Rectifier
	MMSF5N02HDR2	N-channel, $r_{DS(on)} = 0.025 \Omega$, 5 A, SO-8	ON Semiconductor
	IRF7313	Dual N-channel, $r_{DS(on)} = 0.029 \Omega$, 5.2 A, SO-8	International Rectifier
	SI4410	N-channel, $r_{DS(on)} = 0.020 \Omega$, 8 A, SO-8	Vishay Dale
5 to 10	IRLR3103	N-channel, $r_{DS(on)} = 0.019 \Omega$, 29 A, d-Pak	International Rectifier
	IRLR2703	N-channel, $r_{DS(on)} = 0.045 \Omega$, 14 A, d-Pak	International Rectifier

timer

For most applications, a minimum capacitance of 50 pF is recommended to prevent false triggering. This capacitor should be connected between TIMER and ground. The presence of an overcurrent condition on of the TPS2330/31 causes a 50- μ A current source to begin charging this capacitor. If the overcurrent condition persists until the capacitor has been charged to approximately 0.5 V, the TPS2330/31 latches off the transistor and will pull the FAULT pin low. The timer capacitor can be made as large as desired to provide additional time delay before registering a fault condition. The time delay is approximately: $dt = C_{(TIMER)} \times 10,000$.

output-voltage slew-rate control

When enabled, the TPS2330/TPS2331 controllers supply the gate of an external MOSFET transistor with a current of approximately 15 μ A. The slew rate of the MOSFET source voltage is thus limited by the gate-to-drain capacitance C_{gd} of the external MOSFET capacitor to a value approximating:

$$\frac{dvs}{dt} = \frac{15 \mu A}{C_{gd}}$$

If a slower slew rate is desired, an additional capacitance can be connected between the gate of the external MOSFET and ground.

VREG capacitor

The internal voltage regulator connected to VREG requires an external capacitor to ensure stability. A 0.1- μ F or 0.22- μ F ceramic capacitor is recommended.



APPLICATION INFORMATION

gate drive circuitry

The TPS2330/TPS2331 includes four separate features associated with each gate-drive terminal:

- A charging current of approximately 15 μA is applied to enable the external MOSFET transistor. This current is generated by an internal charge pump that can develop a gate-to-source potential (referenced to DISCH) of 9 V–12 V. DISCH must be connected to the external MOSFET source terminal to ensure proper operation of this circuitry.
- A discharge current of approximately 75 μA is applied to disable the external MOSFET transistor. Once the transistor gate voltage has dropped below approximately 1.5 V, this current is disabled and the UVLO discharge driver is enabled instead. This feature allows the part to enter a low-current shutdown mode while ensuring that the gate of the external MOSFET transistor remain at a low voltage.
- During a UVLO condition, the gate of the MOSFET transistor is pulled down by an internal PMOS transistor. This transistor continues to operate even if the voltage at IN is 0 V. This circuitry also helps hold the external MOSFET transistor off when power is suddenly applied to the system.
- During an overcurrent fault condition, the external MOSFET transistor that exhibited an over-current condition is rapidly turned off by an internal pulldown circuit capable of pulling in excess of 400 mA (at 4 V) from the pin. Once the gate has been pulled below approximately 1.5 V, this driver is disengaged and the UVLO driver is enabled instead.

setting the current-limit circuit-breaker threshold

The current sensing resistor R_{ISENSE} and the current limit setting resistor R_{ISET} determine the current limit of the channel, and can be calculated by the following equation:

$$I_{\text{LMT}} = \frac{R_{\text{ISET}} \times 50 \times 10^{-6}}{R_{\text{ISENSE}}}$$

Typically R_{ISENSE} is usually very small (0.001 Ω to 0.1 Ω). If the trace and solder-junction resistances between the junction of R_{ISENSE} and ISENSE and the junction of R_{ISENSE} and R_{ISET} are greater than 10% of the R_{ISENSE} value, then these resistance values should be added to the R_{ISENSE} value used in the calculation above.

Table 2 shows some of the current sense resistors available in the market.

Table 2. Some Current Sense Resistors

CURRENT RANGE (A)	PART NUMBER	DESCRIPTION	MANUFACTURER
0 to 1	WSL-1206, 0.05 1%	0.05 Ω , 0.25 W, 1% resistor	Vishay Dale
1 to 2	WSL-1206, 0.025 1%	0.025 Ω , 0.25 W, 1% resistor	
2 to 4	WSL-1206, 0.015 1%	0.015 Ω , 0.25 W, 1% resistor	
4 to 6	WSL-2010, 0.010 1%	0.010 Ω , 0.5 W, 1% resistor	
6 to 8	WSL-2010, 0.007 1%	0.007 Ω , 0.5 W, 1% resistor	
8 to 10	WSR-2, 0.005 1%	0.005 Ω , 0.5 W, 1% resistor	

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setting the power-good threshold voltage

The two feedback resistors R_{VSENSE_TOP} and R_{VSENSE_BOT} connected between V_O and ground form a resistor divider setting the voltage at the $VSENSE$ pins. $VSENSE$ voltage equals:

$$V_{I(SENSE)} = V_O \times R_{VSENSE_BOT} / (R_{VSENSE_TOP} + R_{VSENSE_BOT})$$

This voltage is compared to an internal voltage reference ($1.225\text{ V} \pm 2\%$) to determine whether the output voltage level is within a specified tolerance. For example, given a nominal output voltage at V_O , and defining V_{O_min} as the minimum required output voltage, then the feedback resistors are defined by:

$$R_{VSENSE_TOP} = \frac{V_{O_min} - 1.225}{1.225} \times R_{VSENSE_BOT}$$

Start the process by selecting a large standard resistor value for R_{VSENSE_BOT} to reduce power loss. Then R_{VSENSE_TOP} can be calculated by inserting all of the known values into the equation above. When V_O is lower than V_{O_min} , $PWRGD$ is low as long as the controller is enabled.

undervoltage lockout (UVLO)

The TPS2330/TPS2331 includes an undervoltage lockout (UVLO) feature that monitors the voltage present on the $VREG$ pin. This feature disables the external MOSFET if the voltage on $VREG$ drops below 2.78 V (nominal) and re-enables normal operation when it rises above 2.85 V (nominal). Since $VREG$ is fed from IN through a low-dropout voltage regulator, the voltage on $VREG$ tracks the voltage on IN within 50 mV. While the undervoltage lockout is engaged, $GATE$ is held low by an internal PMOS pulldown transistor, ensuring that the external MOSFET transistor remain off at the times, even if the power supply has fallen to 0 V.

power-up control

The TPS2330/TPS2331 includes a 500 μs (nominal) start up delay that ensures that internal circuitry has sufficient time to start before the device begins turning on the external MOSFETs. This delay is triggered only upon the rapid application of power to the circuit. If the power supply ramps up slowly, the undervoltage lockout circuitry provides adequate protection against undervoltage operation.

3-channel hot-swap application

Some applications require hot-swap control of up to three voltage rails, but may not explicitly require the sensing of the status of the output power on all three of the voltage rails. One such application is device bay, where dv/dt control of 3.3 V, 5 V, and 12 V is required. By using TPS2330/TPS2331 to drive all three power rails, as is shown below, TPS2330/31 can deliver three different voltages to three loads while monitoring the status of one of the loads.



APPLICATION INFORMATION

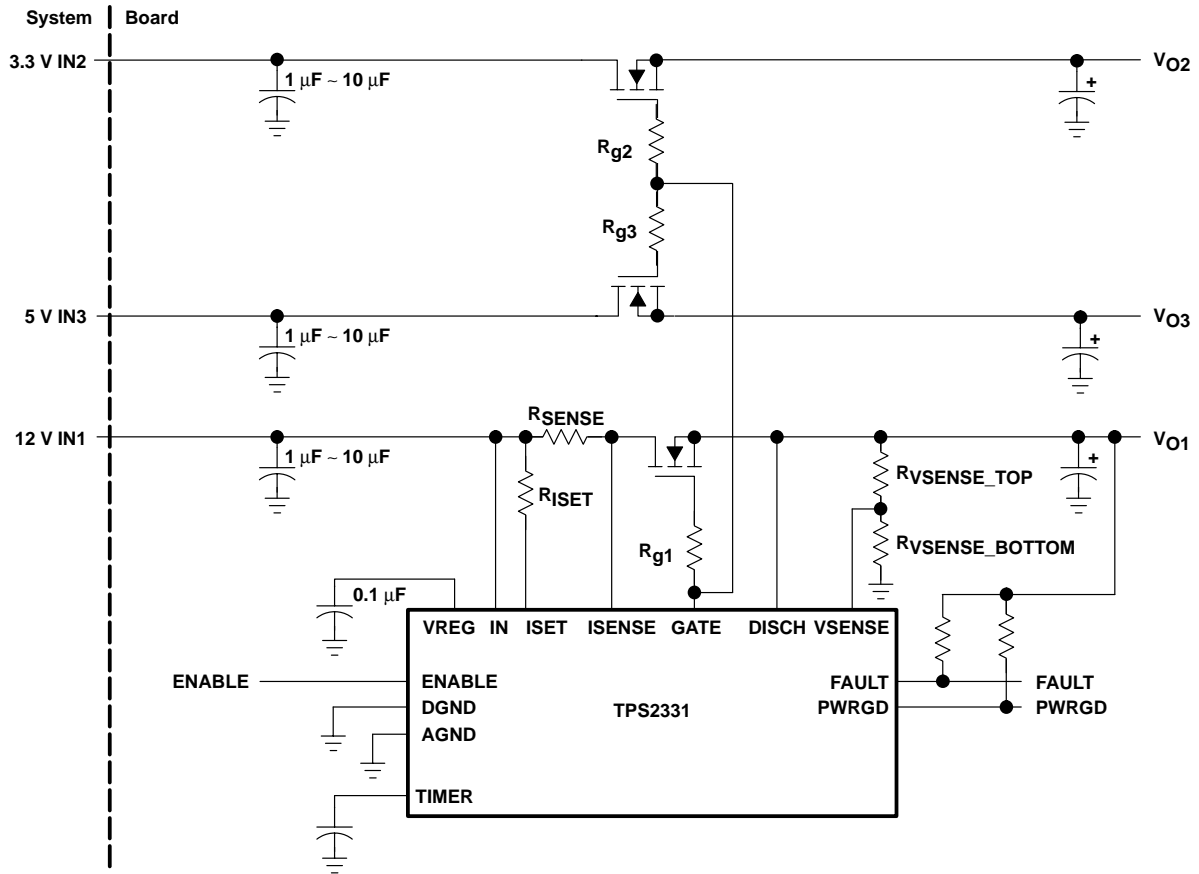


Figure 19. Three-Channel Application

Figure 29 shows ramp-up waveforms of the three output voltages.

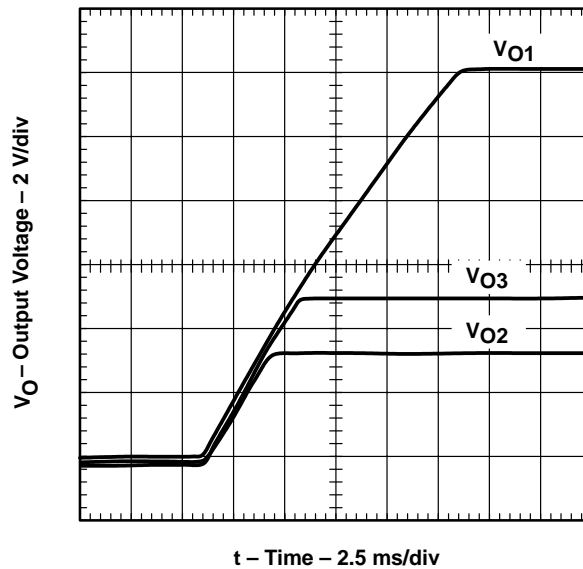


Figure 20

TPS2330, TPS2331
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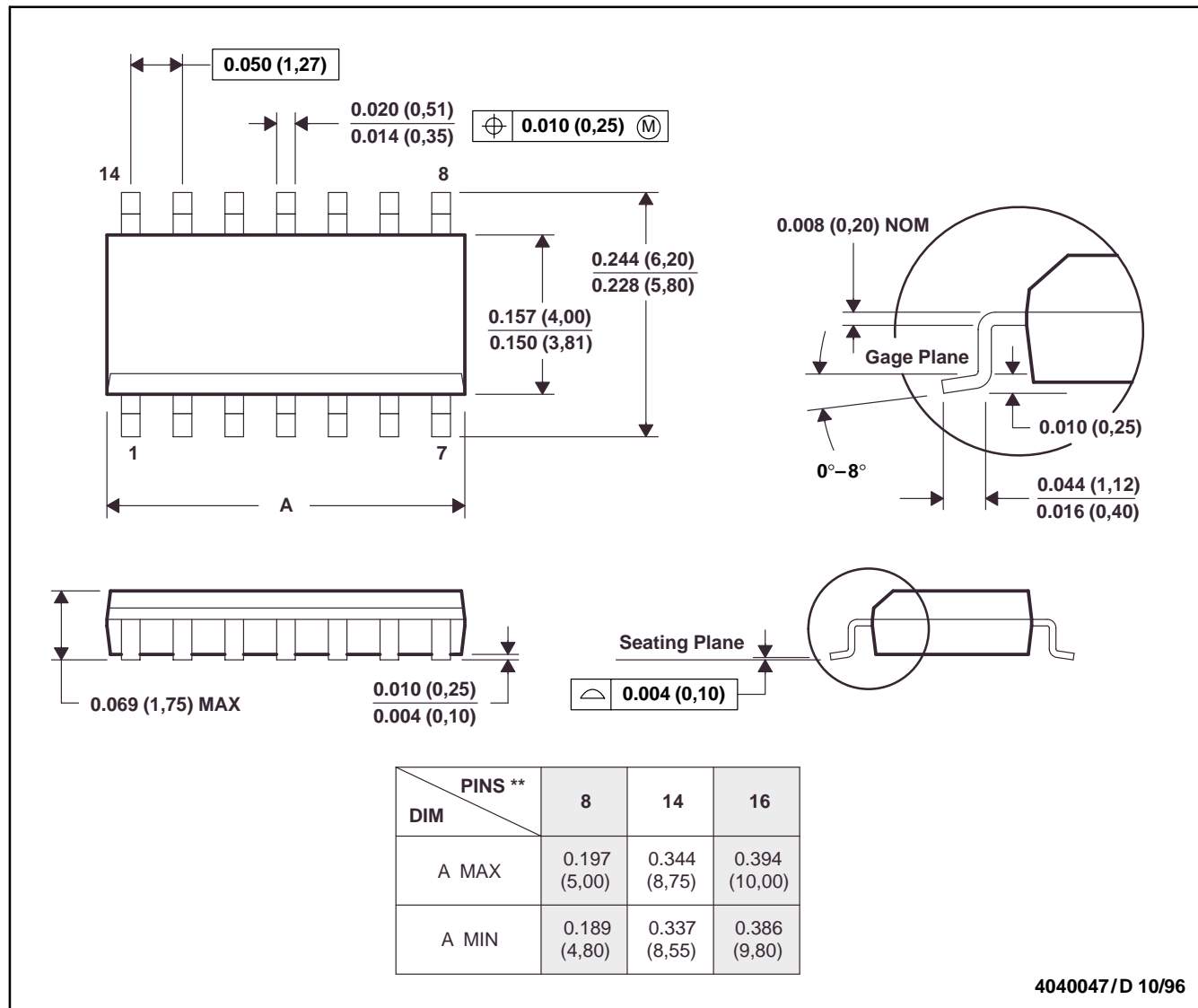
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MECHANICAL DATA

D (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

TPS2330, TPS2331
**SINGLE HOT-SWAP POWER CONTROLLERS WITH
 CIRCUIT BREAKER AND POWER-GOOD REPORTING**

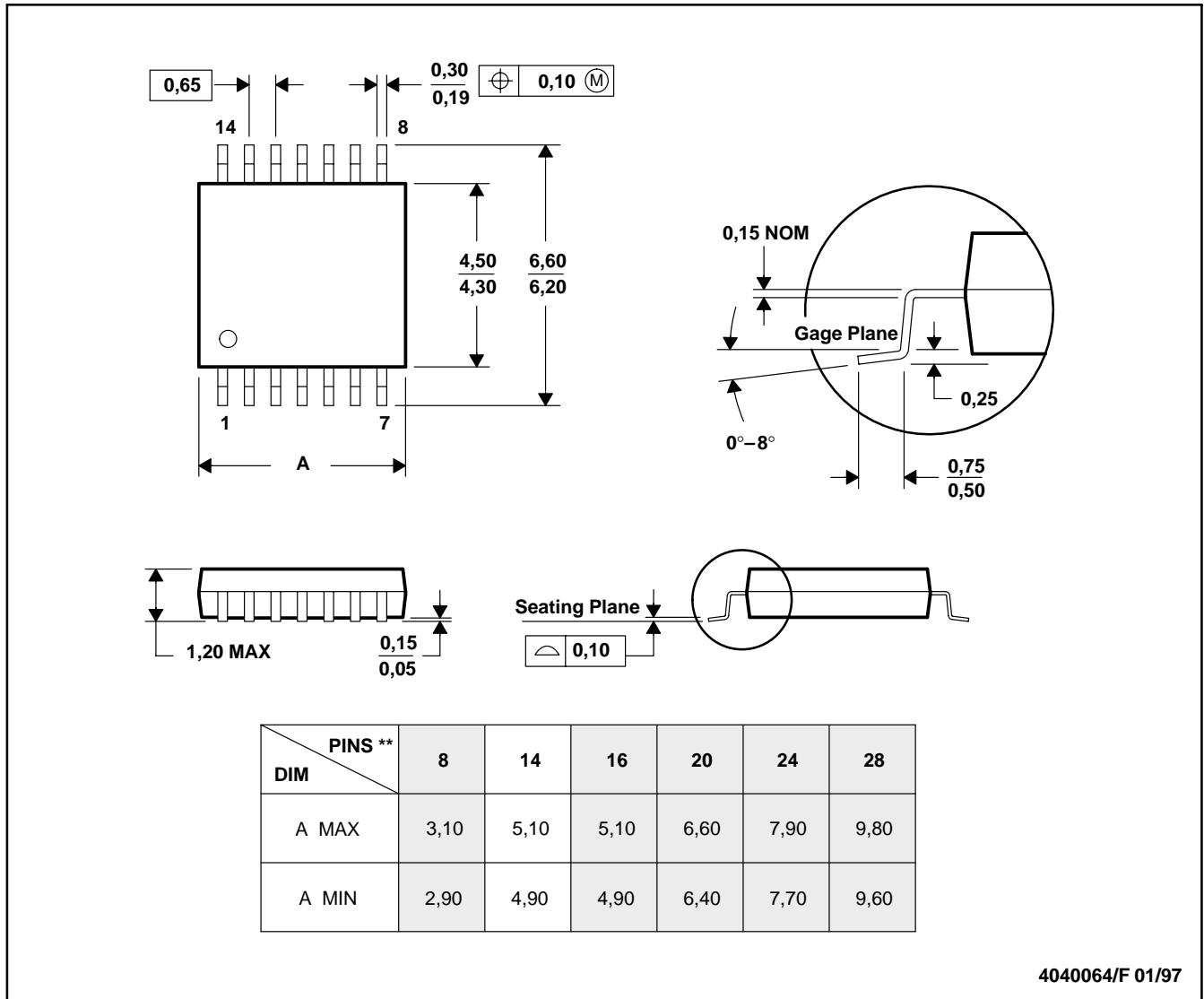
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MECHANICAL DATA

PW (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPS2330ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2330IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2330IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2330IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2330IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2330IPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2330IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2330IPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2331ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2331IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2331IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2331IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2331IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2331IPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2331IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2331IPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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