



TPS22965-Q1 5.5-V, 4-A, 16-mΩ On-Resistance Load Switch

1 Features

- Qualified for Automotive Applications
 - AEC-Q100 Qualified
 - Device Temperature Grade 2: -40°C to 105°C
 - Device HBM ESD Classification Level 3A
 - Device CDM ESD Classification Level C6
- Integrated Single Channel Load Switch
- Input Voltage Range: 0.8V to 5.5V
- Ultra-Low On Resistance (R_{ON})
 - $R_{\text{ON}} = 16\text{m}\Omega$ at $V_{\text{IN}} = 5\text{V}$ ($V_{\text{BIAS}} = 5\text{V}$)
 - $R_{\text{ON}} = 16\text{m}\Omega$ at $V_{\text{IN}} = 3.6\text{V}$ ($V_{\text{BIAS}} = 5\text{V}$)
 - $R_{\text{ON}} = 16\text{m}\Omega$ at $V_{\text{IN}} = 1.8\text{V}$ ($V_{\text{BIAS}} = 5\text{V}$)
- 4 A Maximum Continuous Switch Current
- Low Quiescent Current ($50\mu\text{A}$)
- Low Control Input Threshold Enables Use of 1.2-V, 1.8-V, 2.5-V and 3.3-V Logic
- Configurable Rise Time
- Quick Output Discharge (QOD)
- SON 8-terminal Package with Thermal Pad

2 Applications

- Automotive Electronics
- Infotainment
- ADAS (Advanced Driver Assistance Systems)

3 Description

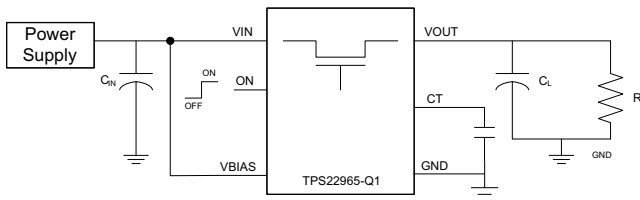
The TPS22965-Q1 is a small, ultra-low R_{ON} , single channel load switch with controlled turn on. The device contains an N-channel MOSFET that can operate over an input voltage range of 0.8-V to 5.5-V and can support a maximum continuous current of 4-A. The V_{OUT} rise time is configurable so that inrush current may be reduced. The TPS22965-Q1 includes a 225- Ω on-chip load resistor for quick output discharge when the switch is turned off.

The TPS22965-Q1 is available in a small, space-saving 2-mm x 2-mm 8-terminal SON package (DSG) with integrated thermal pad allowing for high power dissipation. The device is characterized for operation over the free-air temperature range of -40°C to 105°C .

Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
TPS22965-Q1DSG	SON (8)	2mm x 2mm

4 Simplified Schematic



R_{ON} vs V_{IN} ($V_{\text{BIAS}} = 5\text{V}$, $I_{\text{VOUT}} = -200\text{mA}$)

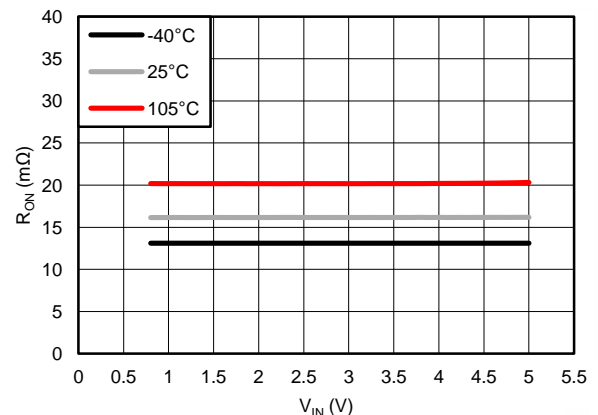


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5 Revision History

DATE	REVISION	NOTES
March 2014	*	Initial release.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

		MIN	MAX	UNIT ⁽²⁾
V _{IN}	Input voltage range	-0.3	6	V
V _{OUT}	Output voltage range	-0.3	6	V
V _{BIAS}	Bias voltage range	-0.3	6	V
V _{ON}	Input voltage range	-0.3	6	V
I _{MAX}	Maximum continuous switch current		4	A
I _{PLS}	Maximum pulsed switch current, pulse <300 μs, 2% duty cycle		6	A
T _A	Operating free-air temperature range ⁽³⁾	-40	105	°C
T _J	Maximum junction temperature		150	°C
T _{STG}	Storage temperature range	-65	150	°C
T _{LEAD}	Maximum lead temperature (10-s soldering time)		300	°C

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.
- (3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [T_{A(max)}] is dependent on the maximum operating junction temperature [T_{J(max)}], the maximum power dissipation of the device in the application [P_{D(max)}], and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: T_{A(max)} = T_{J(max)} - (θ_{JA} × P_{D(max)})

7.2 Handling Ratings

		MIN	MAX	UNIT
T _{stg}	Storage Temperature Range	-65	150	°C
V _{ESD} ⁽¹⁾	Human-Body Model (HBM) AEC-Q100 Classification Level 3A ⁽²⁾	All Terminals	4000	V
	Charged-Device Model (CDM) AEC-Q100 Classification Level C6 ⁽³⁾	All Terminals	1500	

- (1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
- (2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{IN}	Input voltage range		0.8	V _{BIAS}	V
V _{BIAS}	Bias voltage range		2.5	5.5	V
V _{ON}	ON voltage range		0	5.5	V
V _{OUT}	Output voltage range			V _{IN}	V
V _{IH}	High-level input voltage, ON	V _{BIAS} = 2.5 V to 5.5 V	1.2	5.5	V
V _{IL}	Low-level input voltage, ON	V _{BIAS} = 2.5 V to 5.5 V	0	0.5	V
C _{IN}	Input capacitor		1 ⁽¹⁾		μF

- (1) Refer to the [Application and Implementation](#) section.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS22965-Q1	UNIT
		DSG	
		8 TERMINALS	
R _{θJA}	Junction-to-ambient thermal resistance	63.0	°C/W
R _{θJctop}	Junction-to-case (top) thermal resistance	72.9	
R _{θJB}	Junction-to-board thermal resistance	34.2	
ψ _{JT}	Junction-to-top characterization parameter	1.9	
ψ _{JB}	Junction-to-board characterization parameter	34.8	
R _{θJcbot}	Junction-to-case (bottom) thermal resistance	11.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

Unless otherwise note, the specification in the following table applies over the operating ambient temperature $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ (Full) and $V_{\text{BIAS}} = 5.0\text{ V}$. Typical values are for $T_A = 25^{\circ}\text{C}$.

PARAMETER		TEST CONDITIONS	T _A	MIN	TYP	MAX	UNIT	
POWER SUPPLIES AND CURRENTS								
I _Q V _{BIAS}	V _{BIAS} quiescent current	I _{VOUT} = 0 mA, V _{IN} = V _{ON} = V _{BIAS} = 5.0 V	Full		50	75	μA	
I _{SD} V _{BIAS}	V _{BIAS} shutdown current	V _{ON} = GND, V _{OUT} = 0 V	Full			2	μA	
I _{SD} V _{IN}	V _{IN} off-state supply current	V _{ON} = GND, V _{OUT} = 0 V	Full	V _{IN} = 5.0 V		0.2	8	μA
				V _{IN} = 3.3 V		0.02	3	
				V _{IN} = 1.8 V		0.01	2	
				V _{IN} = 0.8 V		0.005	1	
I _{ON}	ON terminal input leakage current	V _{ON} = 5.5 V	Full			0.5	μA	
RESISTANCE CHARACTERISTICS								
R _{ON}	ON-state resistance	I _{VOUT} = -200 mA, V _{BIAS} = 5.0 V	V _{IN} = 5.0 V	25°C		16	23	mΩ
				Full			25	
			V _{IN} = 3.3 V	25°C		16	23	mΩ
				Full			25	
			V _{IN} = 1.8 V	25°C		16	23	mΩ
				Full			25	
			V _{IN} = 1.5 V	25°C		16	23	mΩ
				Full			25	
			V _{IN} = 1.2 V	25°C		16	23	mΩ
				Full			25	
			V _{IN} = 0.8 V	25°C		16	23	mΩ
				Full			25	
R _{PD}	Output pull-down resistance	V _{IN} = 5.0 V, V _{ON} = 0 V, I _{VOUT} = 1 mA	Full		225	300	Ω	

7.6 Electrical Characteristics

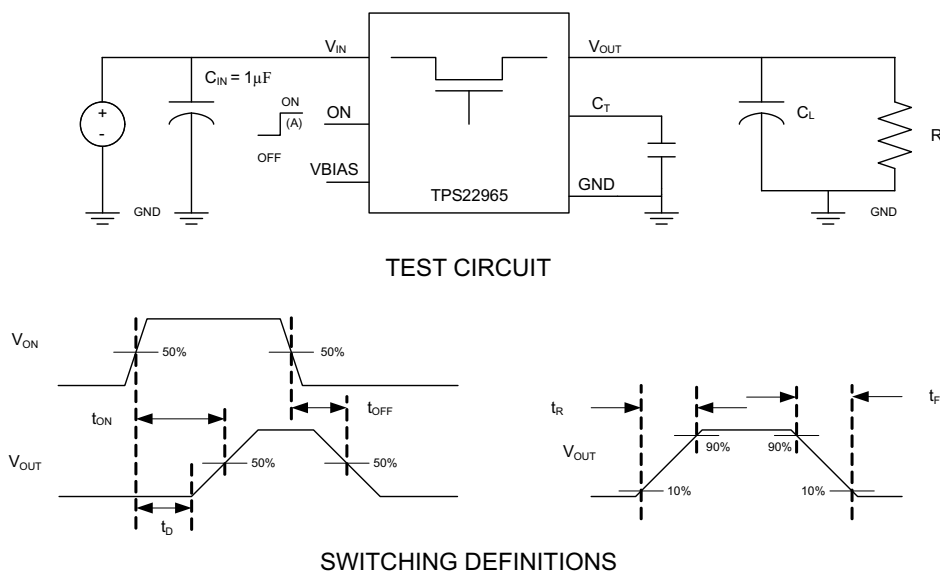
Unless otherwise noted, the specification in the following table applies over the operating ambient temperature $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ (Full) and $V_{\text{BIAS}} = 2.5\text{ V}$. Typical values are for $T_A = 25^{\circ}\text{C}$.

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT	
POWER SUPPLIES AND CURRENTS								
I_Q	V_{BIAS} quiescent current	$I_{\text{VOUT}} = 0\text{ mA}$, $V_{\text{IN}} = V_{\text{ON}} = V_{\text{BIAS}} = 2.5\text{ V}$	Full		20	30	μA	
I_{SD}	V_{BIAS} shutdown current	$V_{\text{ON}} = \text{GND}$, $V_{\text{OUT}} = 0\text{ V}$	Full			2	μA	
I_{SD}	V_{IN} off-state supply current	$V_{\text{ON}} = \text{GND}$, $V_{\text{OUT}} = 0\text{ V}$	Full		$V_{\text{IN}} = 2.5\text{ V}$	0.01	3	μA
					$V_{\text{IN}} = 1.8\text{ V}$	0.01	2	
					$V_{\text{IN}} = 1.2\text{ V}$	0.005	2	
					$V_{\text{IN}} = 0.8\text{ V}$	0.003	1	
I_{ON}	ON terminal input leakage current	$V_{\text{ON}} = 5.5\text{ V}$	Full			0.5	μA	
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	$I_{\text{VOUT}} = -200\text{ mA}$, $V_{\text{BIAS}} = 2.5\text{ V}$	$V_{\text{IN}} = 2.5\text{ V}$	25°C	20	26	$\text{m}\Omega$	
				Full		28		
			$V_{\text{IN}} = 1.8\text{ V}$	25°C	19	26	$\text{m}\Omega$	
				Full		28		
			$V_{\text{IN}} = 1.5\text{ V}$	25°C	18	25	$\text{m}\Omega$	
				Full		27		
			$V_{\text{IN}} = 1.2\text{ V}$	25°C	18	25	$\text{m}\Omega$	
				Full		27		
			$V_{\text{IN}} = 0.8\text{ V}$	25°C	17	25	$\text{m}\Omega$	
				Full		27		
R_{PD}	Output pull-down resistance	$V_{\text{IN}} = 2.5\text{ V}$, $V_{\text{ON}} = 0\text{ V}$, $I_{\text{VOUT}} = 1\text{ mA}$	Full		275	325	Ω	

7.7 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted). Switching characteristics shown below are only valid for the power-up sequence where VIN and VBIAS are already in steady state condition before the ON terminal is asserted high.

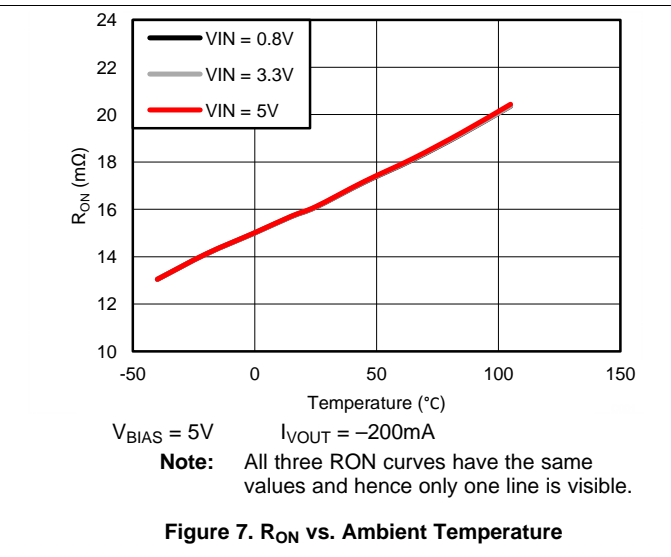
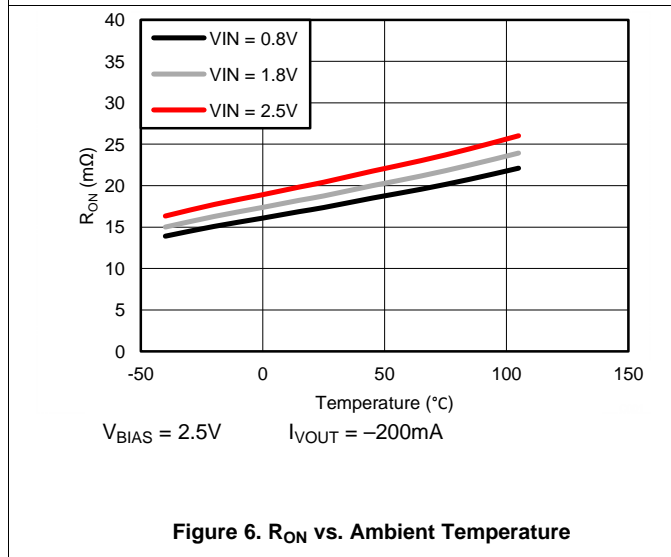
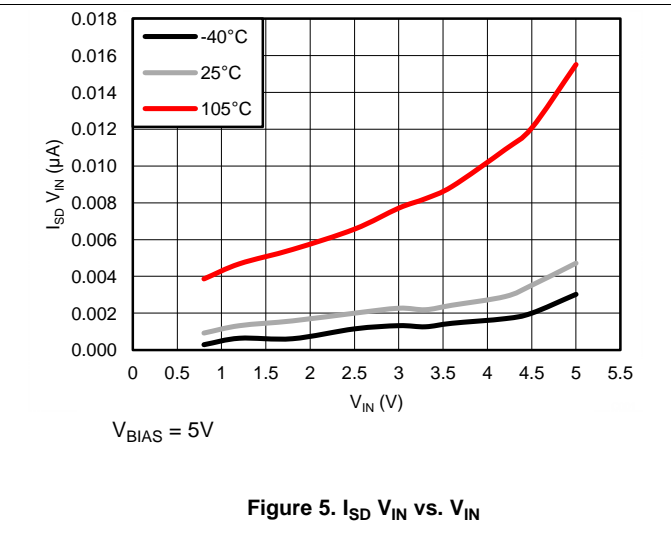
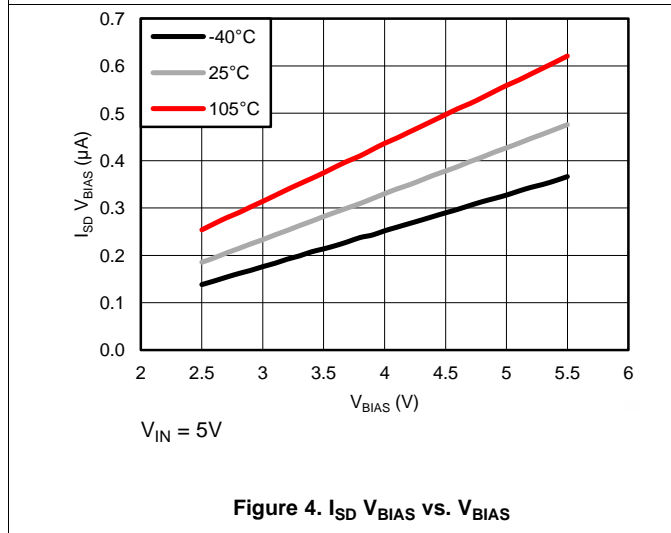
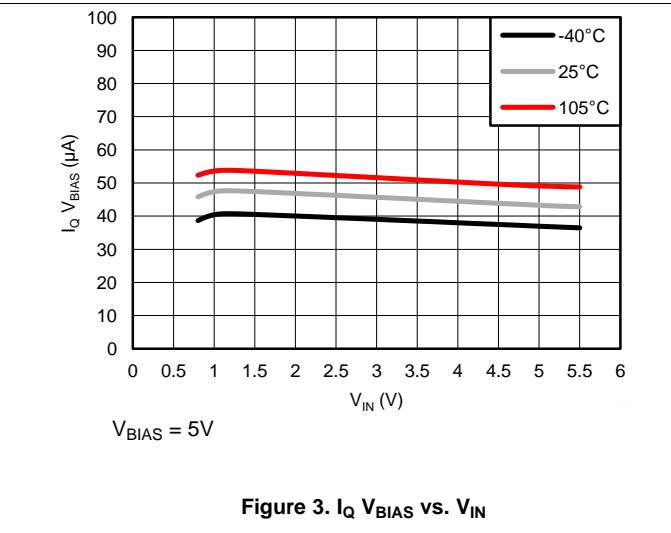
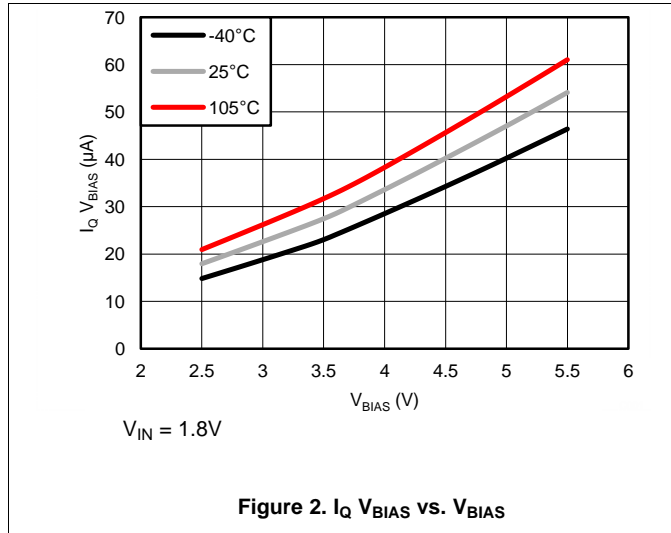
PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN} = V_{ON} = V_{BIAS} = 5 V, T_A = 25°C (unless otherwise noted)					
t _{ON} Turn-on time	R _L = 10 Ω, C _L = 0.1 μF, C _T = 1000 pF, C _{IN} = 1 μF		1323		μs
t _{OFF} Turn-off time			9		
t _R V _{OUT} rise time			1577		
t _F V _{OUT} fall time			3		
t _D ON delay time			575		
V_{IN} = 0.8 V, V_{ON} = V_{BIAS} = 5 V, T_A = 25°C (unless otherwise noted)					
t _{ON} Turn-on time	R _L = 10 Ω, C _L = 0.1 μF, C _T = 1000 pF, C _{IN} = 1 μF		638		μs
t _{OFF} Turn-off time			90		
t _R V _{OUT} rise time			296		
t _F V _{OUT} fall time			8		
t _D ON delay time			485		
V_{IN} = 2.5V, V_{ON} = 5 V, V_{BIAS} = 2.5 V, T_A = 25°C (unless otherwise noted)					
t _{ON} Turn-on time	R _L = 10 Ω, C _L = 0.1 μF, C _T = 1000 pF, C _{IN} = 1 μF		2010		μs
t _{OFF} Turn-off time			9		
t _R V _{OUT} rise time			1997		
t _F V _{OUT} fall time			4		
t _D ON delay time			1057		
V_{IN} = 0.8 V, V_{ON} = 5 V, V_{BIAS} = 2.5 V, T_A = 25°C (unless otherwise noted)					
t _{ON} Turn-on time	R _L = 10 Ω, C _L = 0.1 μF, C _T = 1000 pF, C _{IN} = 1 μF		1333		μs
t _{OFF} Turn-off time			69		
t _R V _{OUT} rise time			728		
t _F V _{OUT} fall time			8		
t _D ON delay time			954		



(A) Rise and fall times of the control signal is 100ns.

Figure 1. Test Circuit and Switching Definitions

7.8 Typical DC Characteristics



Typical DC Characteristics (continued)

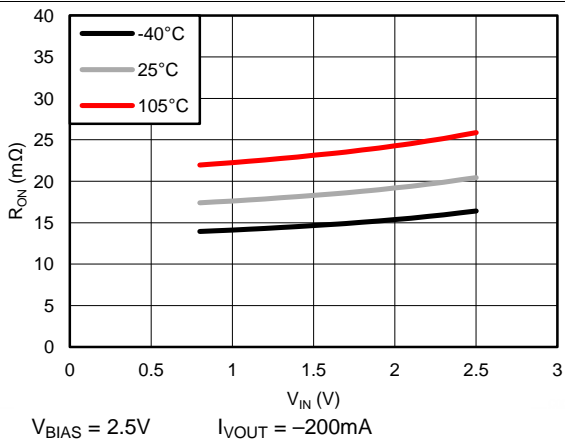


Figure 8. R_{ON} vs. V_{IN}

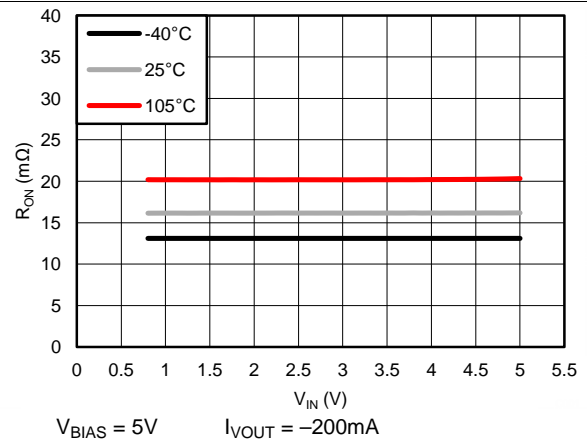


Figure 9. R_{ON} vs. V_{IN}

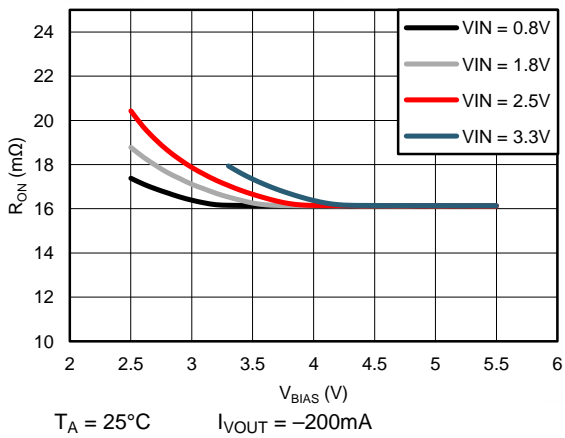


Figure 10. R_{ON} vs. V_{BIAS}

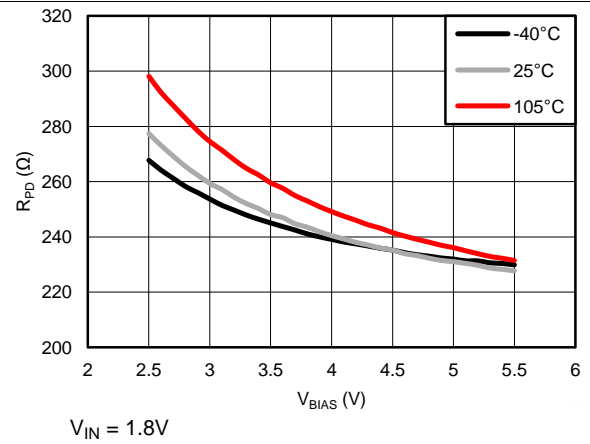


Figure 11. R_{PD} vs. V_{BIAS}

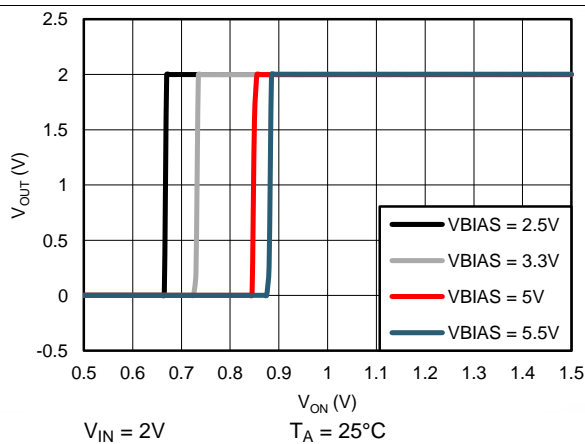


Figure 12. V_{OUT} vs V_{ON}

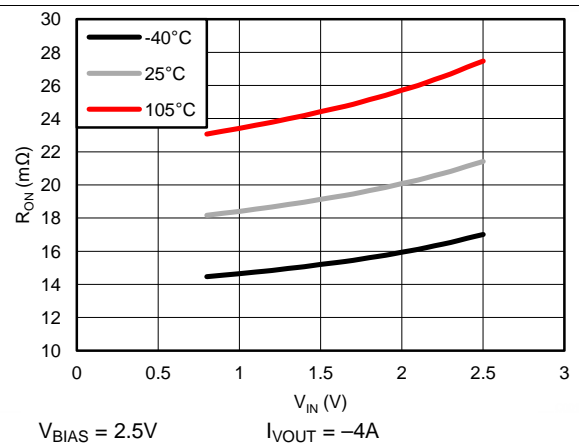


Figure 13. R_{ON} vs V_{IN}

Typical DC Characteristics (continued)

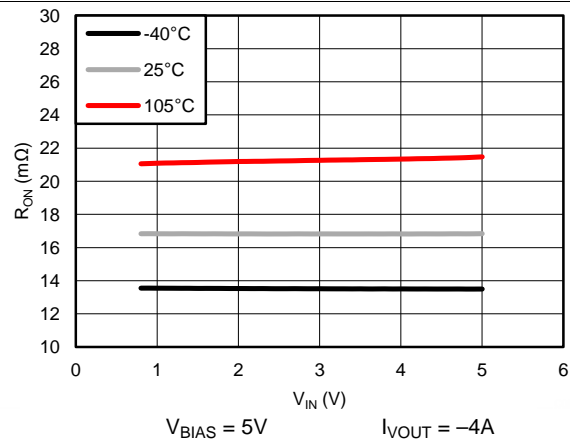


Figure 14. R_{ON} vs V_{IN}

7.9 Typical Switching Characteristics

$C_{IN} = 1\mu\text{F}$, $C_L = 0.1\mu\text{F}$, $R_L = 10\Omega$

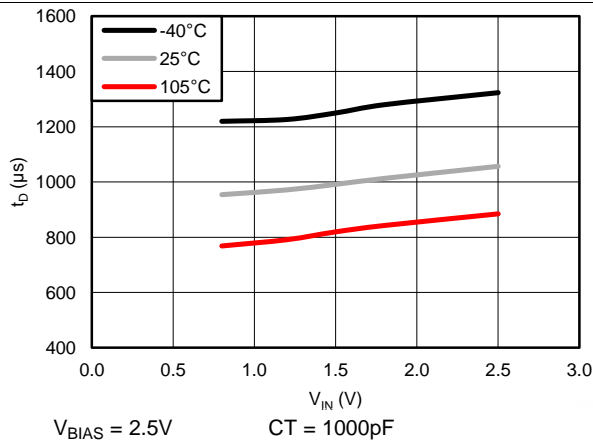


Figure 15. t_D vs. V_{IN}

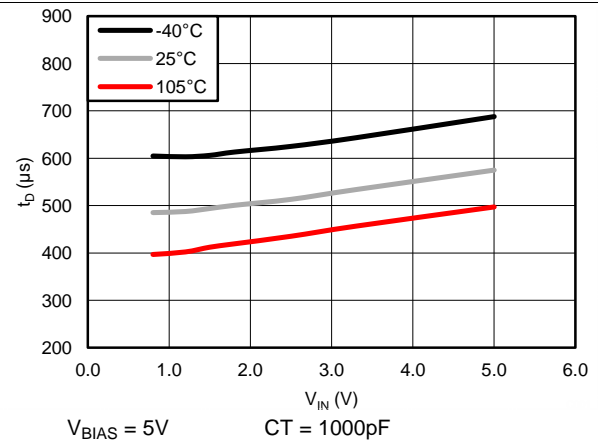


Figure 16. t_D vs. V_{IN}

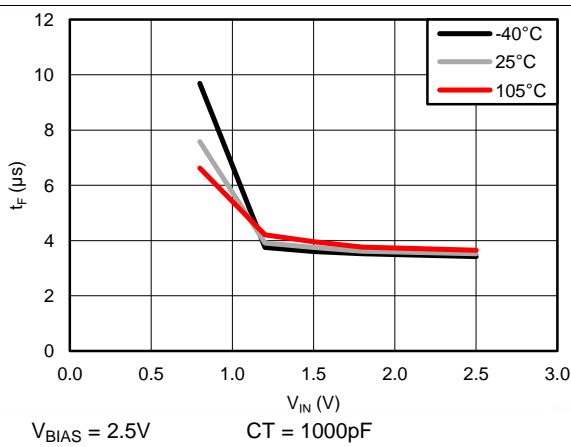


Figure 17. t_F vs. V_{IN}

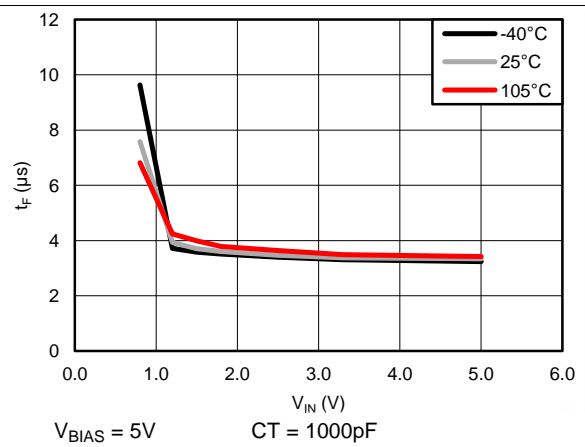


Figure 18. t_F vs. V_{IN}

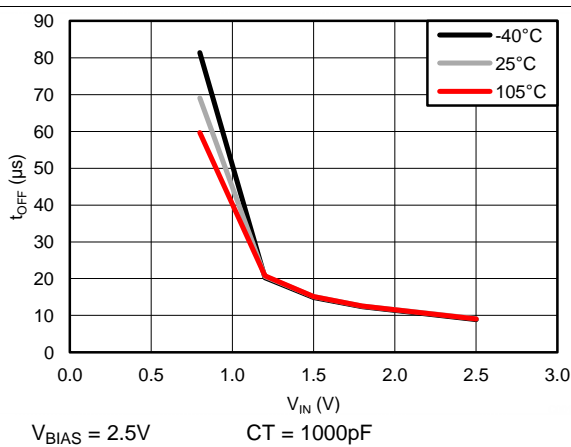


Figure 19. t_{OFF} vs. V_{IN}

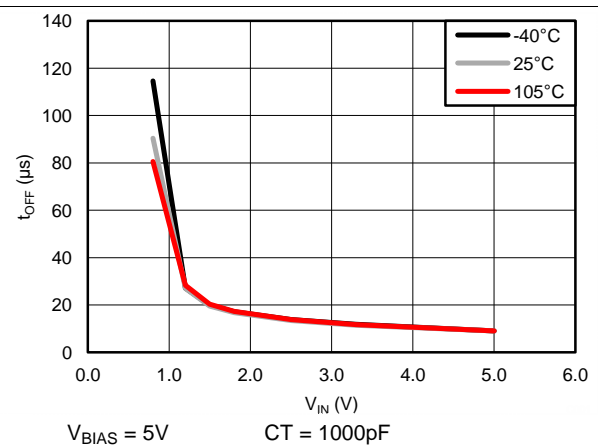


Figure 20. t_{OFF} vs. V_{IN}

Typical Switching Characteristics (continued)

$C_{IN} = 1\mu F$, $C_L = 0.1\mu F$, $R_L = 10\Omega$

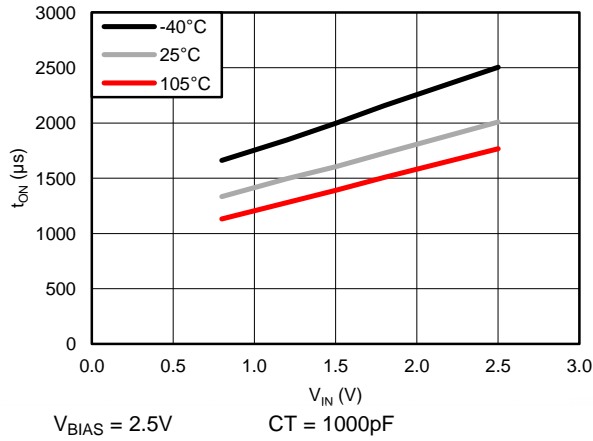


Figure 21. t_{ON} vs. V_{IN}

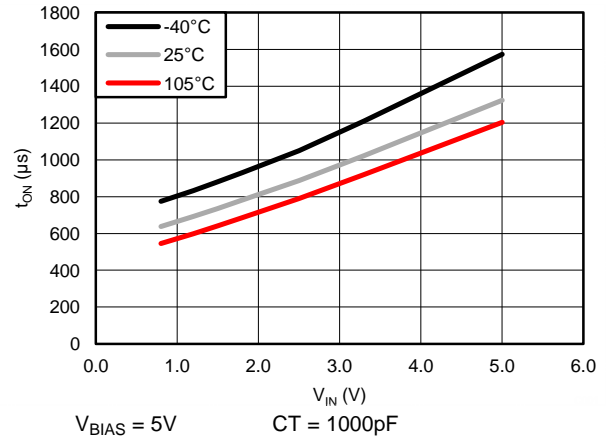


Figure 22. t_{ON} vs. V_{IN}

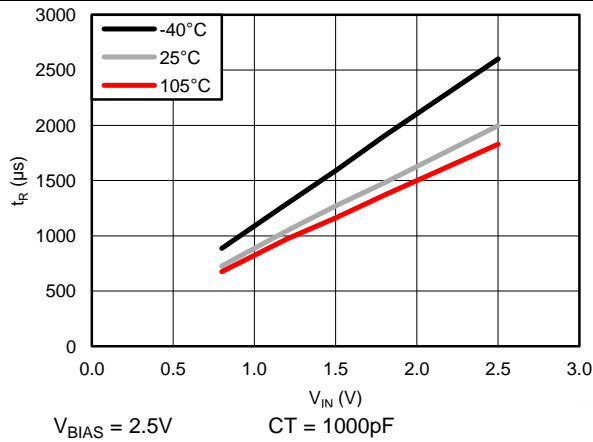


Figure 23. t_R vs. V_{IN}

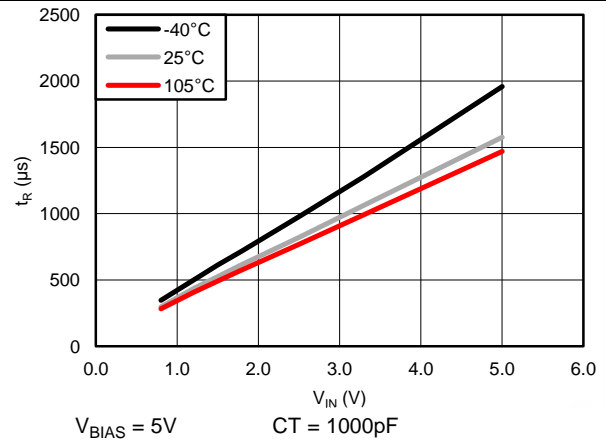


Figure 24. t_R vs. V_{IN}

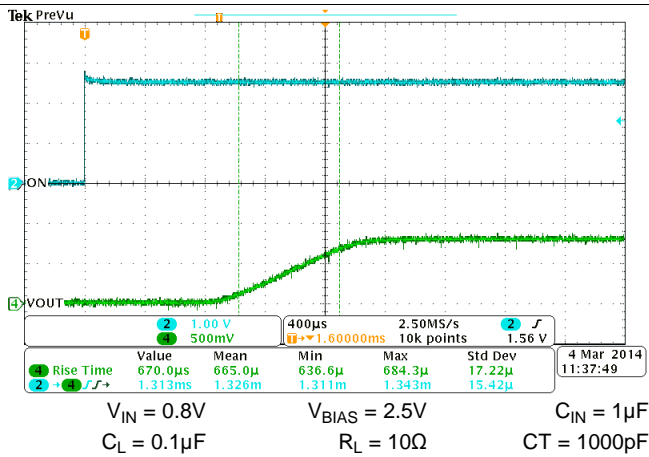


Figure 25. Turn-On Response Time

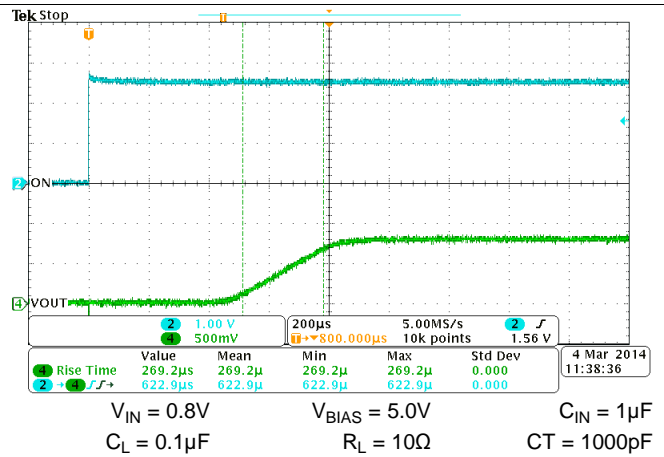


Figure 26. Turn-On Response Time

Typical Switching Characteristics (continued)

$C_{IN} = 1\mu F$, $C_L = 0.1\mu F$, $R_L = 10\Omega$

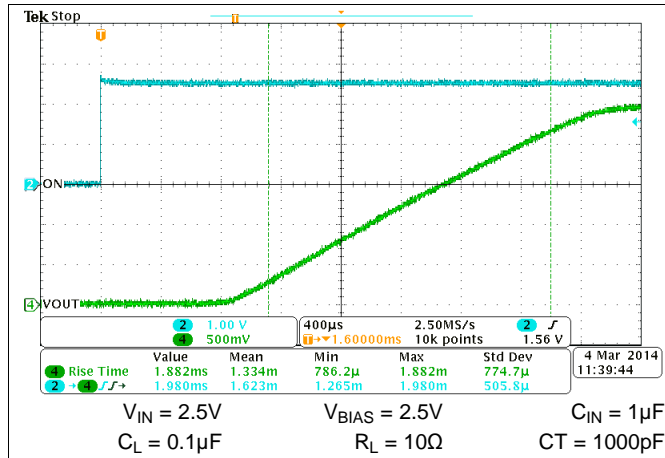


Figure 27. Turn-On Response Time

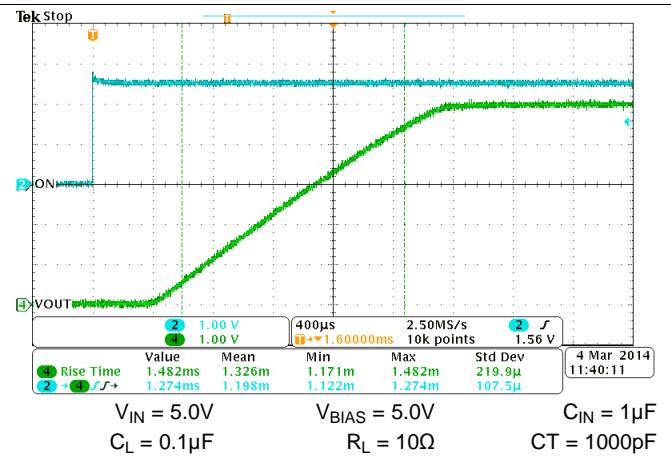


Figure 28. Turn-On Response Time

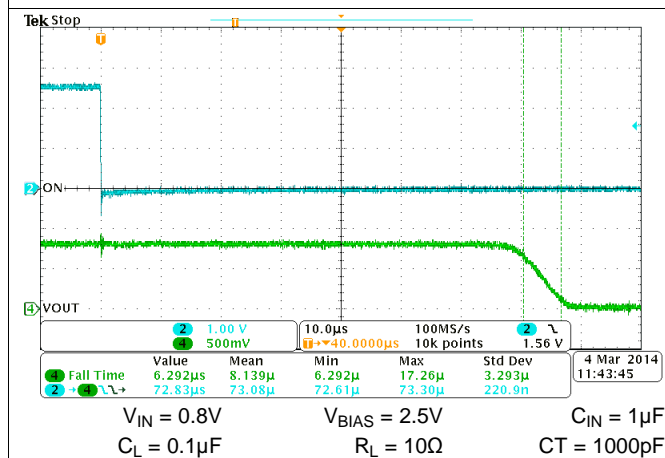


Figure 29. Turn-Off Response Time

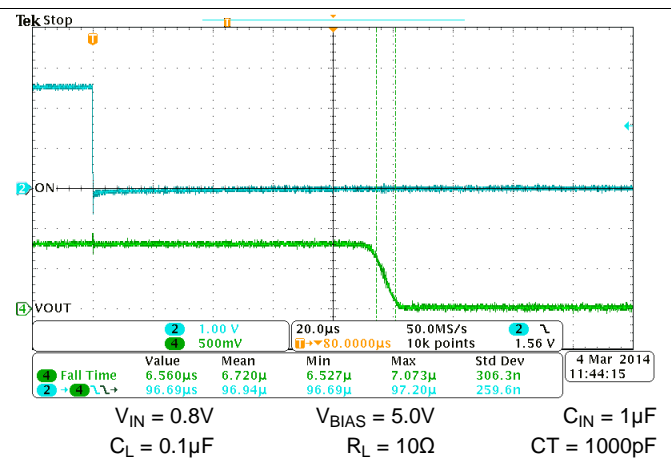


Figure 30. Turn-Off Response Time

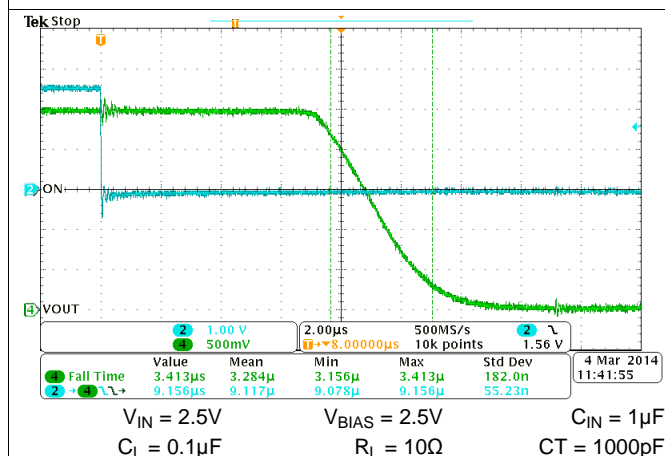


Figure 31. Turn-Off Response Time

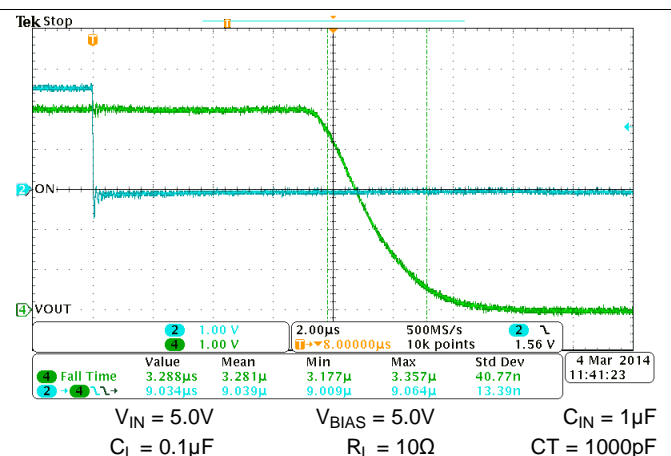


Figure 32. Turn-Off Response Time

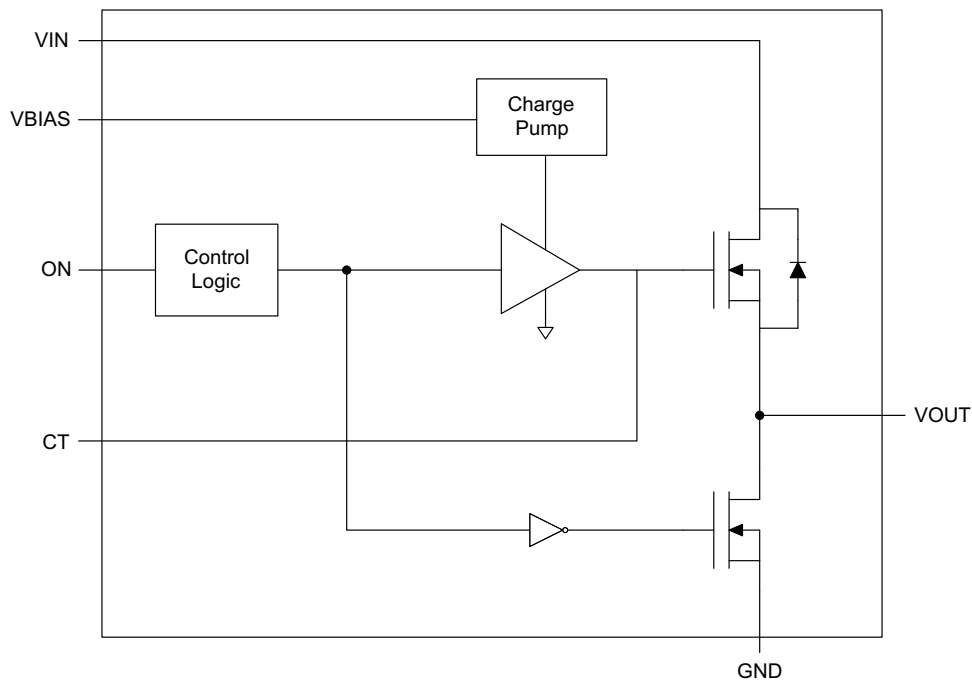
8 Detailed Description

8.1 Overview

The device is a single channel, 4-A load switch in an 8-terminal SON package. To reduce the voltage drop in high current rails, the device implements an ultra-low resistance N-channel MOSFET. The device has a programmable slew rate for applications that require specific rise-time.

The device has very low leakage current during off state. This prevents downstream circuits from pulling high standby current from the supply. Integrated control logic, driver, power supply, and output discharge FET eliminates the need for any external components, which reduces solution size and BOM count.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Adjustable Rise Time

A capacitor to GND on the CT terminal sets the slew rate. The voltage on the CT terminal can be as high as 12 V. Therefore, the minimum voltage rating for the CT cap should be 25 V for optimal performance. An approximate formula for the relationship between CT and slew rate when V_{BIAS} is set to 5 V is shown in Equation 1 below. This equation accounts for 10% to 90% measurement on V_{OUT} and does **NOT** apply for CT = 0 pF. Use table below to determine rise times for when CT = 0 pF.

$$SR = 0.39 \times CT + 13.4 \quad (1)$$

Where,

SR = slew rate (in $\mu\text{s}/\text{V}$)

CT = the capacitance value on the CT terminal (in pF)

The units for the constant 13.4 are $\mu\text{s}/\text{V}$. The units for the constant 0.39 are $\mu\text{s}/(\text{V} \cdot \text{pF})$.

Rise time can be calculated by multiplying the input voltage by the slew rate. The table below contains rise time values measured on a typical device. Rise times shown below are only valid for the power-up sequence where V_{IN} and V_{BIAS} are already in steady state condition before the ON terminal is asserted high.

CT (pF)	RISE TIME (μs) 10% - 90%, $C_L = 0.1 \mu\text{F}$, $C_{IN} = 1 \mu\text{F}$, $R_L = 10 \Omega$, $V_{BIAS} = 5 \text{ V}$ TYPICAL VALUES at 25°C with a 25V X7R 10% CERAMIC CAPACITOR on CT						
	VIN = 5 V	VIN = 3.3 V	VIN = 2.5 V	VIN = 1.8 V	VIN = 1.5 V	VIN = 1.2 V	VIN = 0.8 V
0	172	129	109	91	82	73	57
220	546	377	298	230	200	170	123
470	962	654	510	387	330	275	195
1000	1577	1063	821	617	525	434	296
2200	4177	2770	2140	1577	1343	1097	748
4700	8717	5783	4460	3313	2797	2297	1580
10000	18167	12000	9253	6823	5820	4760	3290

8.3.2 Quick Output Discharge

The TPS22965-Q1 includes a Quick Output Discharge (QOD) feature. When the switch is disabled, a discharge resistor is connected between VOUT and GND. This resistor has a typical value of 225- Ω and prevents the output from floating while the switch is disabled.

8.3.3 Low Power Consumption During Off State

The I_{SD} V_{IN} supply current is 0.01- μA typical at 1.8- V_{IN} . Typically, the downstream loads would have a significantly higher off-state leakage current. The load switch allows system standby power consumption to be reduced.

8.4 Device Functional Modes

Functional Table

ON	VIN to VOUT	VOUT to GND
L	Off	On
H	On	Off

9 Applications and Implementation

9.1 Application Information

This section will highlight some of the design considerations when implementing this device in various applications. A PSPICE model for this device is also available in the product page of this device on www.ti.com for further aid.

9.1.1 VIN to VOUT Voltage Drop

The VIN to VOUT voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the V_{IN} and V_{BIAS} conditions of the device. Refer to the R_{ON} specification of the device in the Electrical Characteristics table of this datasheet. Once the R_{ON} of the device is determined based upon the V_{IN} and V_{BIAS} conditions, use [Equation 2](#) to calculate the VIN to VOUT voltage drop:

$$\Delta V = I_{LOAD} \times R_{ON} \quad (2)$$

where

- ΔV = voltage drop from VIN to VOUT
- I_{LOAD} = load current
- R_{ON} = On-resistance of the device for a specific V_{IN} and V_{BIAS} combination

An appropriate I_{LOAD} must be chosen such that the I_{MAX} specification of the device is not violated.

9.1.2 On/Off Control

The ON terminal controls the state of the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON terminal is compatible with standard GPIO logic thresholds. It can be used with any microcontroller with 1.2 V or higher GPIO voltage. This terminal cannot be left floating and must be driven either high or low for proper functionality.

9.1.3 Input Capacitor (Optional)

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between VIN and GND. A 1- μ F ceramic capacitor, C_{IN} , placed close to the terminals, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high current applications. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

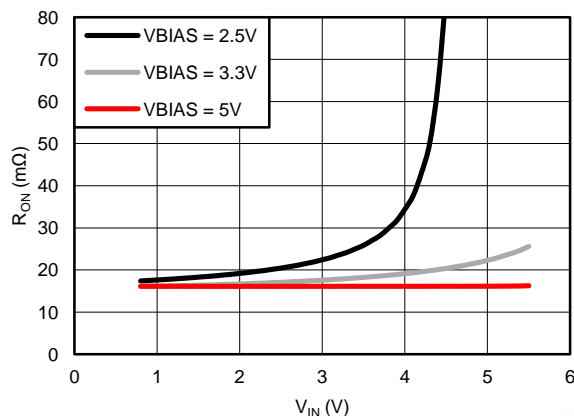
9.1.4 Output Capacitor (Optional)

Due to the integrated body diode in the NMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN} . A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup, however a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause slightly more V_{IN} dip upon turn-on due to inrush currents. This can be mitigated by increasing the capacitance on the CT terminal for a longer rise time (see ADJUSTABLE RISE TIME section).

9.1.5 VIN and VBIAS Voltage Range

For optimal R_{ON} performance, make sure $V_{IN} \leq V_{BIAS}$. The device will still be functional if $V_{IN} > V_{BIAS}$ but it will exhibit R_{ON} greater than what is listed in the ELECTRICAL CHARACTERISTICS table. See [Figure 33](#) for an example of a typical device. Notice the increasing R_{ON} as V_{IN} exceeds V_{BIAS} voltage. Be sure to never exceed the maximum voltage rating for V_{IN} and V_{BIAS} .

Application Information (continued)



$I_{VOUT} = -200\text{mA}$ $T_A = 25^\circ\text{C}$

Figure 33. R_{ON} vs. V_{IN} (V_{IN} > V_{BIAS})

9.2 Typical Application

This application demonstrates how the TPS22965-Q1 can be used to power downstream modules.

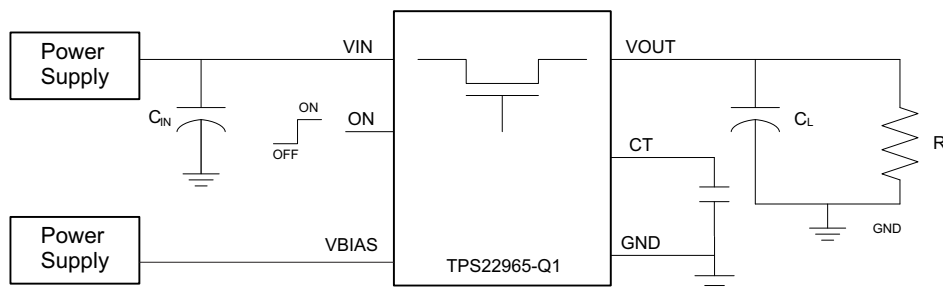


Figure 34. Schematic for Powering a Downstream Module

9.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
V _{IN}	3.3-V
V _{BIAS}	5-V
C _L	22-μF
Maximum Acceptable Inrush Current	400-mA

9.2.2 Detailed Design Procedure

9.2.2.1 Inrush Current

When the switch is enabled, the output capacitors must be charged up from 0-V to the set value (3.3-V in this example). This charge arrives in the form of inrush current. Inrush current can be calculated using the following equation:

$$\text{Inrush Current} = C \times dV/dt \tag{3}$$

Where:

- C = output capacitance
- dV = output voltage
- dt = rise time

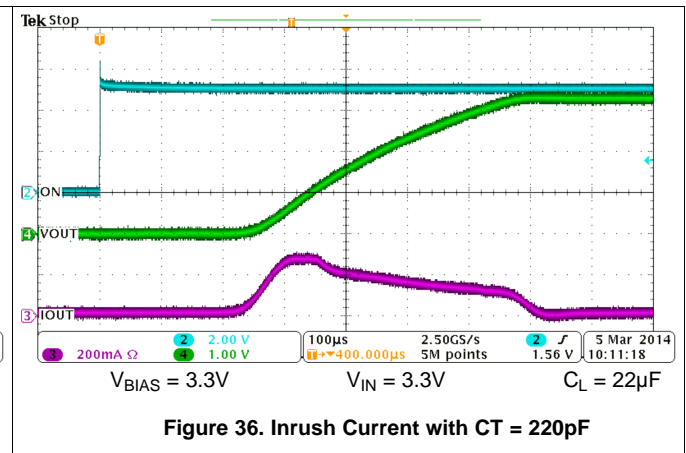
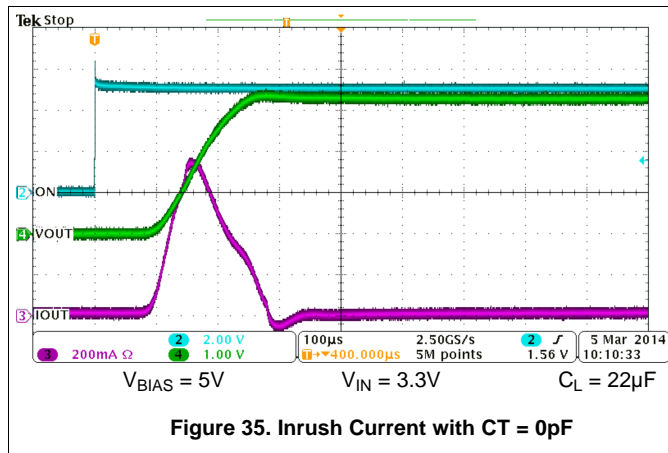
The TPS22965-Q1 offers adjustable rise time for VOUT. This feature allows the user to control the inrush current during turn-on. The appropriate rise time can be calculated using the design requirements and the inrush current equation.

$$400\text{mA} = 22\mu\text{F} \times 3.3\text{V} / dt \tag{4}$$

$$dt = 181.5\mu\text{s} \tag{5}$$

To ensure an inrush current of less than 400mA, choose a CT value that will yield a rise time of more than 181.5µs. See the oscilloscope captures below for an example of how the CT capacitor can be used to reduce inrush current.

9.2.3 Application Curves



10 Power Supply Recommendations

The device is designed to operate from a VBIAS range of 2.5-V to 5.5-V and a VIN range of 0.8-V to VBIAS.

11 Layout

11.1 Board Layout and Thermal Considerations

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance. The CT trace should be as short as possible to avoid parasitic capacitance.

The maximum IC junction temperature should be restricted to 150°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use the following equation as a guideline:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\Theta_{JA}} \quad (6)$$

Where:

$P_{D(max)}$ = maximum allowable power dissipation

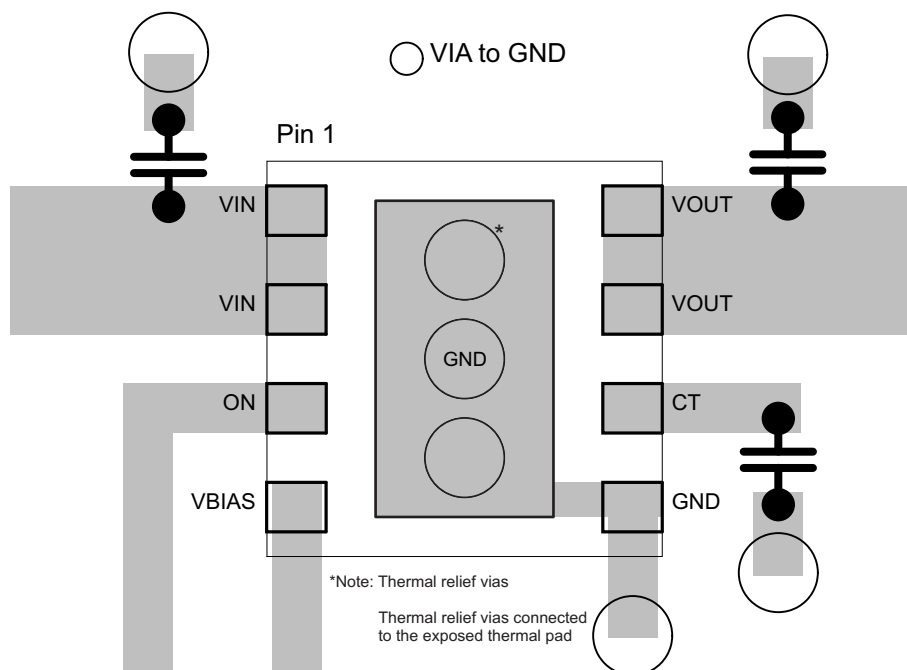
$T_{J(max)}$ = maximum allowable junction temperature (150°C for the TPS22965-Q1)

T_A = ambient temperature of the device

Θ_{JA} = junction to air thermal impedance. See Thermal Information section. This parameter is highly dependent upon board layout.

The figure below shows an example of a layout. Notice the thermal vias located under the exposed thermal pad of the device. This allows for thermal diffusion away from the device.

11.2 Layout Example



12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22965TDSGRQ1	PREVIEW	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105		
TPS22965TDSGTQ1	PREVIEW	WSON	DSG	8	250	TBD	Call TI	Call TI	-40 to 105		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS22965-Q1 :

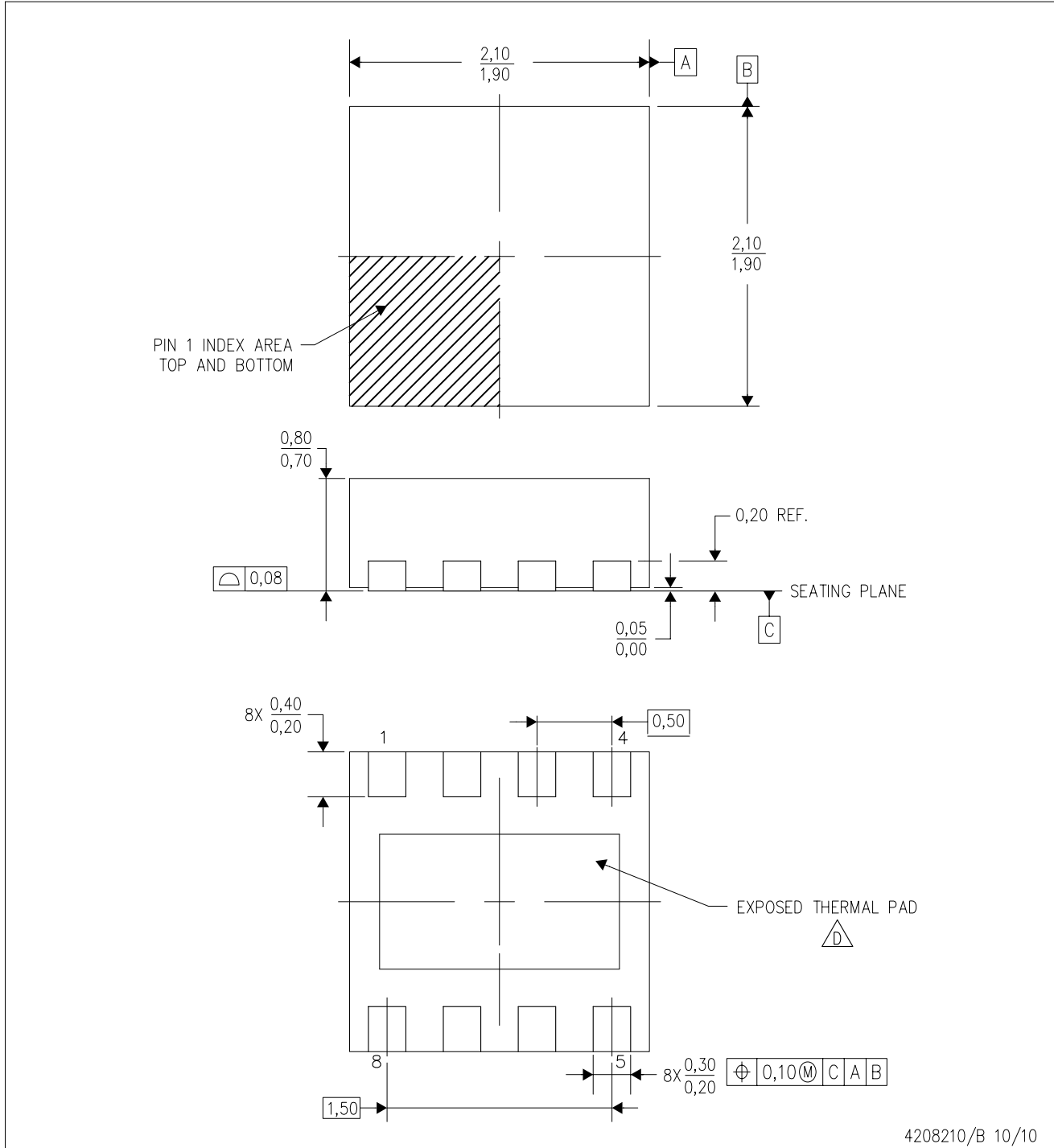
- Catalog: [TPS22965](#)

NOTE: Qualified Version Definitions:


- Catalog - TI's standard catalog product

DSG (S-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



4208210/B 10/10

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-Leads (QFN) package configuration.
 -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. Falls within JEDEC MO-229.

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