TPDxE05U06 1, 4, 6 Channel ESD Protection Device for Super-Speed (up to 6 GBPS) Interface

1 Features

- IEC 61000-4-2 Level 4 ESD Protection
  - ±12-kV Contact Discharge
  - ±15-kV Air Gap Discharge
- IEC 61000-4-4 EFT Protection
  - 80 A (5/50 ns)
- IEC 61000-4-5 Surge Protection
  - 2.5 A (8/20 µs)
- IO Capacitance 0.42 pF to 0.5 pF (Typ)
- DC Breakdown Voltage 6.5 V (Min)
- Ultra low Leakage Current 10 nA (Max)
- Low ESD Clamping Voltage
- Industrial Temperature Range: –40°C to 125°C
- Easy Straight-Through Routing Packages

2 Applications

- HDMI1.4
- HDMI2.0 (TPD1E05U06)
- USB 3.0
- MHL
- LVDS Interfaces
- DisplayPort
- PCI Express
- eSata Interfaces

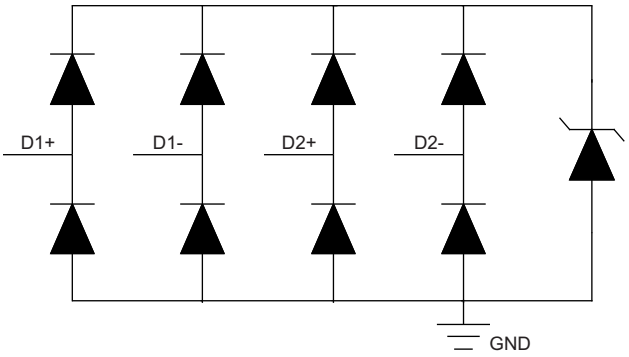
3 Description

The TPDxE05U06 is a family of unidirectional Transient Voltage Suppressor (TVS) based Electrostatic Discharge (ESD) protection diodes with ultra-low capacitance. Each device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 international standard. The TPDxE05U06's ultra-low loading capacitance makes it ideal for protecting any high-speed signal pins.

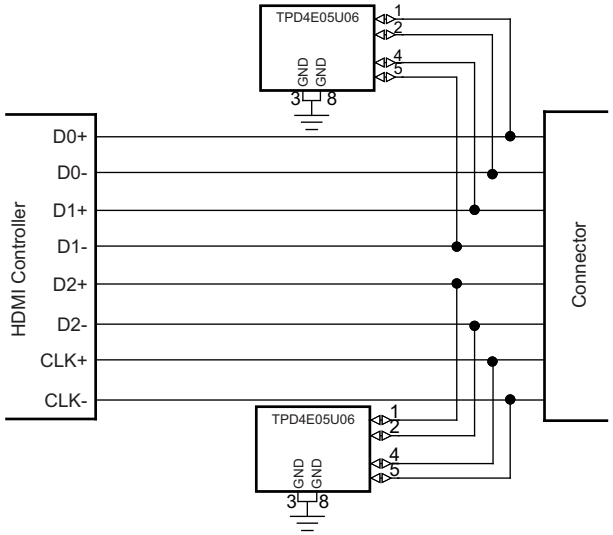
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD1E05U06	X2SON (2)	1.00 mm × 0.60 mm
TPD4E05U06	USON (10)	2.50 mm × 1.00 mm
TPD6E05U06	USON (14)	3.50 mm × 1.35 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



4 Simplified Schematic



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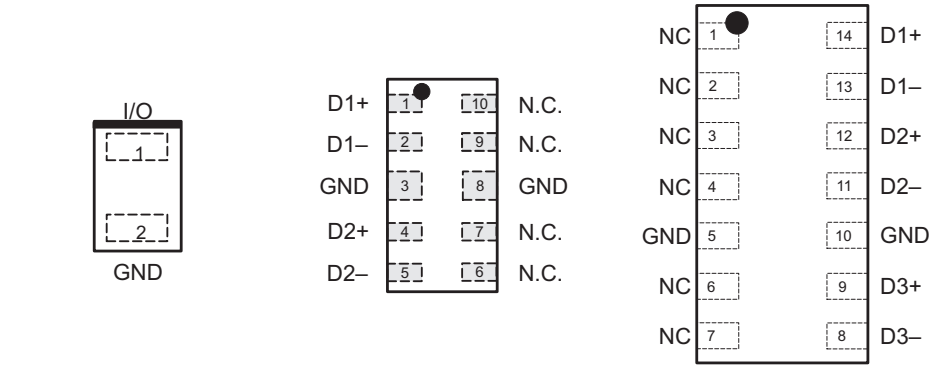
- Updated Title. 1
- Removed Ordering Information table. 4

Changes from Revision D (August 2013) to Revision E **Page**

- Updated document formatting. 1
- Added additional application. 1

6 Terminal Configuration and Functions



DPY
TOP VIEW
1 mm x 0.6 mm x 0.35 mm
(0.65-mm pitch)

DQA
TOP VIEW
2.5 mm x 1 mm x 0.5 mm
(0.5-mm pitch)

RVZ
TOP VIEW
3.5 mm x 1.35 mm x 0.5 mm
(0.5-mm pitch)

Pin Functions TPD1E05U06 DPY

PIN		DESCRIPTION
NAME	NO.	
I/O	1	ESD Protected Channel(1)
GND	2	Ground; Connect to ground

(1) Place as close to the connector as possible.

Pin Functions TPD4E05U06 DQA

PIN		DESCRIPTION
NAME	NO.	
D1+	1	ESD Protected Channel(1)
D1-	2	ESD Protected Channel(1)
D2+	4	ESD Protected Channel(1)
D2-	5	ESD Protected Channel(1)
NC	6, 7, 9, 10	Not Connected; Used for optional straight-through routing. Can be left floating or grounded.
GND	3, 8	Ground; Connect to ground

(1) Place as close to the connector as possible.

Pin Functions TPD6E05U06 RVZ

PIN		DESCRIPTION
NAME	NO.	
D1+	14	ESD Protected Channel(1)
D1-	13	Ground; Connect to ground
D2+	12	ESD Protected Channel(1)
D2-	11	ESD Protected Channel(1)
D3+	9	ESD Protected Channel(1)
D3-	8	ESD Protected Channel(1)
NC	1, 2, 3, 4, 6, 7	Not Connected; Used for optional straight-through routing. Can be left floating or grounded.
GND	5, 10	Ground; Connect to ground

(1) Place as close to the connector as possible.

7 Specifications

7.1 Absolute Maximum Ratings (1)(2)(3)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Operating Temperature		-40	125	°C
Electrical Fast Transient	IEC 61000-4-4 (5/50 ns)		80	A
Peak Pulse	IEC 61000-4-5 Current (tp – 8/20 µs) (4)		2.5	A
	IEC 61000-4-5 Power (tp – 8/20 µs) (4)		40	W

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.
(2) Absolute maximum ratings apply over recommended junction temperature range.
(3) Voltages are with respect to GND unless otherwise noted.
(4) Measured at 25°C.

7.2 Handling Ratings

				MIN	MAX	UNIT
T_{stg}	Storage temperature range			–65	155	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)		–4	4	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)		–1.5	1.5	
		61000-4-2 ESD ratings	Contact	–12	12	
			Air	–15	15	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as 4 kV may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as 1.5 kV may actually have higher performance.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	Input pin voltage	0	5.5	V
T_A	Operating free-air temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC (1)		TPD1E05U06	TPD4E05U06	TPD6E05U06	UNIT
		DPY	DQA	RVZ	
		2 PINS	10 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	697.3	327	197.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	471	189.5	119.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	575.9	257.7	92.6	
ψ_{JT}	Junction-to-top characterization parameter	175.7	60.9	22	
ψ_{JB}	Junction-to-board characterization parameter	575.1	257	91.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 10 µA				5.5	V
V_{BR}	Break-down Voltage	I_{IO} = 1 mA		6		8.5	V
V_{clamp}	Clamp voltage	I = 1A, TLP, I/O to ground(1)			10		V
		I = 5A, TLP, I/O to ground(1)			14		
		I = 1A, TLP, ground to I/O(1)			3		
		I = 5A, TLP, ground to I/O(1)			7		
I_{LEAK}	Leakage current	V_{IO} = 2.5 V			.01	10	nA
R_{DYN}	DPY package dynamic resistance	I/O to GND(2)			0.8		Ω
		GND to I/O(2)			0.8		
	DQA package dynamic resistance	I/O to GND(2)			0.8		Ω
		GND to I/O(2)			0.8		
	RVZ package dynamic resistance	I/O to GND(2)			0.8		Ω
		GND to I/O(2)			0.8		
Capacitance							
C_L	Line capacitance(3)	V_{IO} = 2.5 V, f = 1 MHz, I/O to GND	TPD1E05U06 DPY package		0.42		pF
			TPD4E05U06 DQA package		0.5		
			TPD6E05U06 RVZ package		0.47		
$\Delta C_{IO\text{-}TO\text{-}GND}$	Variation of channel input capacitance	GND Pin = 0 V, F = 1 GHz, V_{BIAS} = 2.5 V, channel_x pin to GND – channel_y pin to GND			0.05	0.07	pF
C_{CROSS}	Channel to channel input capacitance	GND Pin = 0 V, F = 1 GHz, V_{BIAS} = 2.5 V, between channel pins			0.01	0.06	pF

(1) Transition line pulse with 100 ns width, 200 ps rise time.
(2) Extraction of R_{DYN} using least squares fit of TLP characteristics between I = 10 A and I = 20 A.
(3) Capacitance data is taken at 25°C.

7.6 Typical Characteristics

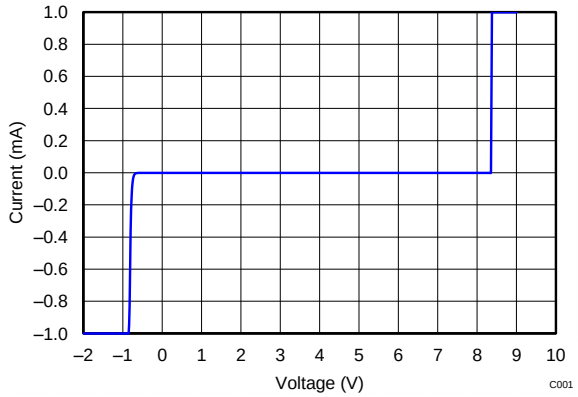


Figure 1. DC Voltage Sweep I-V Curve

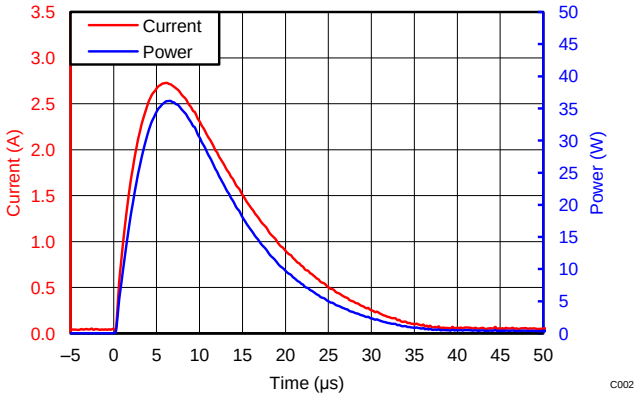


Figure 2. Surge Curve (tp = 8/20 µs), Pin IO to GND

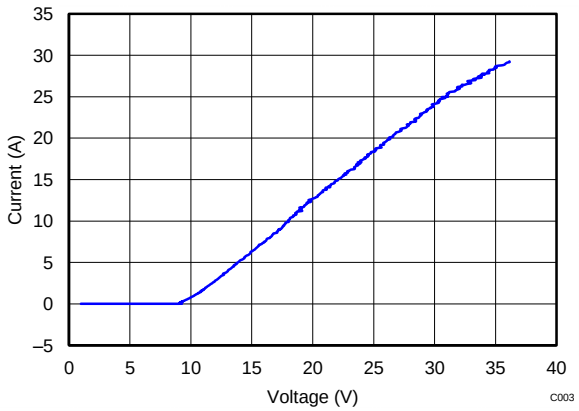


Figure 3. Positive TLP Plot IO to GND

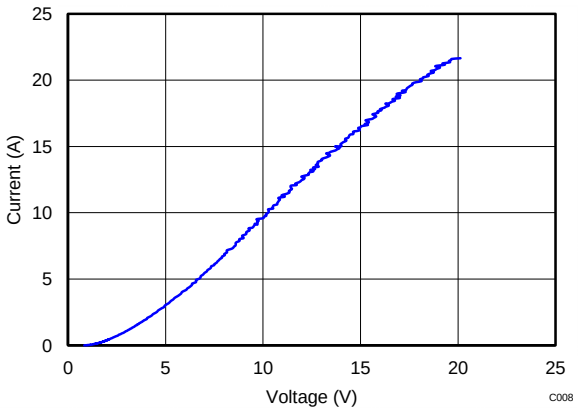


Figure 4. Negative TLP Plot IO to GND

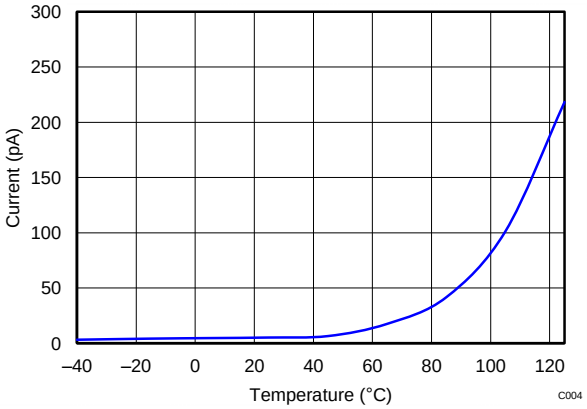


Figure 5. Leakage vs Temperature

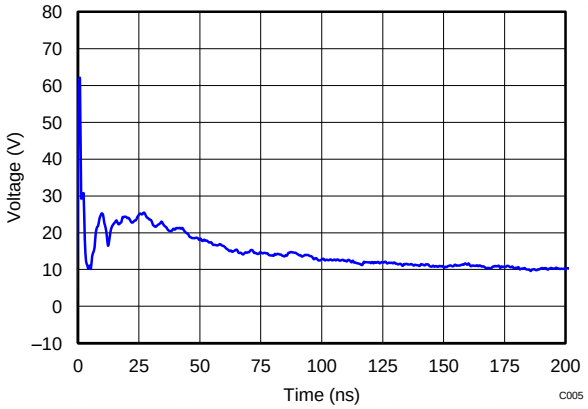


Figure 6. +8-kV IEC Waveform

Typical Characteristics (continued)

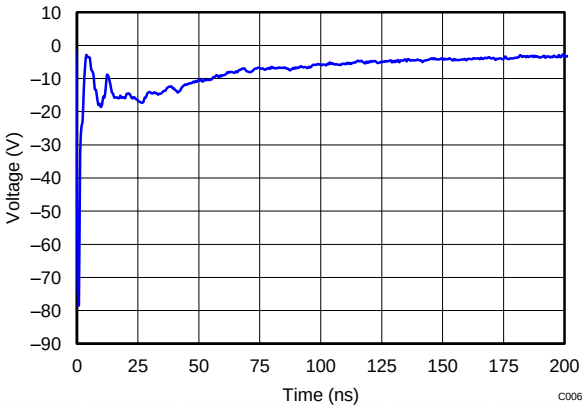


Figure 7. –8-kV IEC Waveform

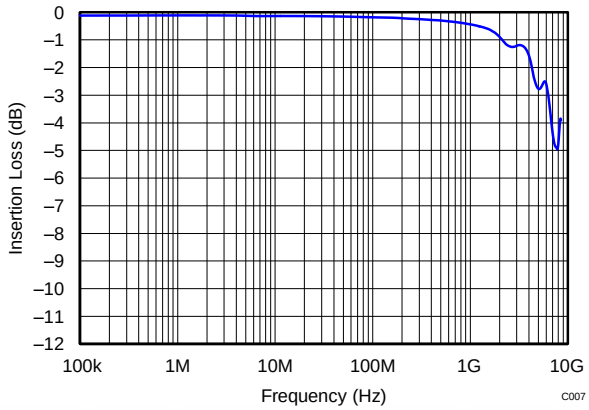


Figure 8. TPD1E05U06 Insertion Loss

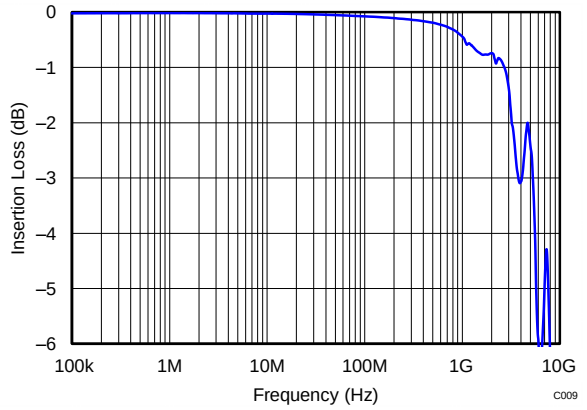


Figure 9. TPD4E05U06 Insertion Loss

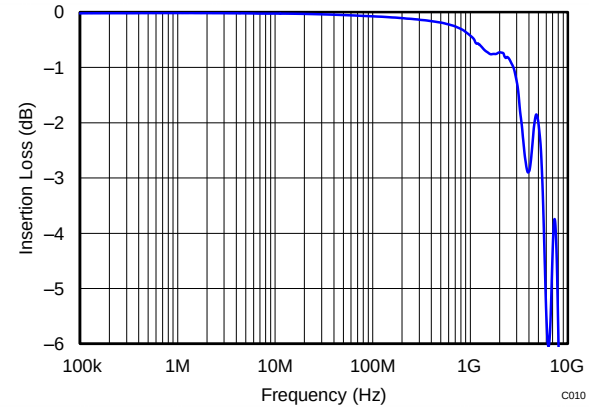


Figure 10. TPD6E05U06 Insertion Loss

8 Detailed Description

8.1 Overview

The TPDxE05U06 is a family of unidirectional Transient Voltage Suppressor (TVS) based Electrostatic Discharge (ESD) protection diodes with ultra-low capacitance. Each device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 international standard. The TPDxE05U06's ultra-low loading capacitance makes it ideal for protecting any high-speed signal pins.

8.2 Functional Block Diagrams

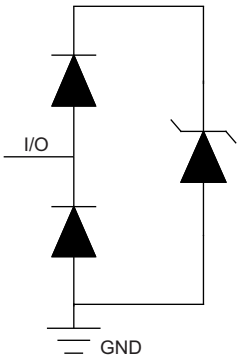


Figure 11. TPD1E05U06 Block Diagram

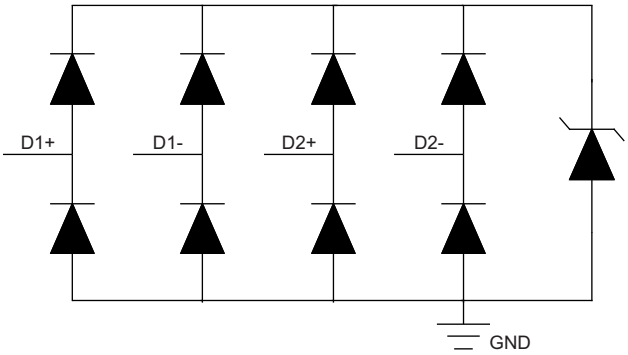


Figure 12. TPD4E05U06 Block Diagram

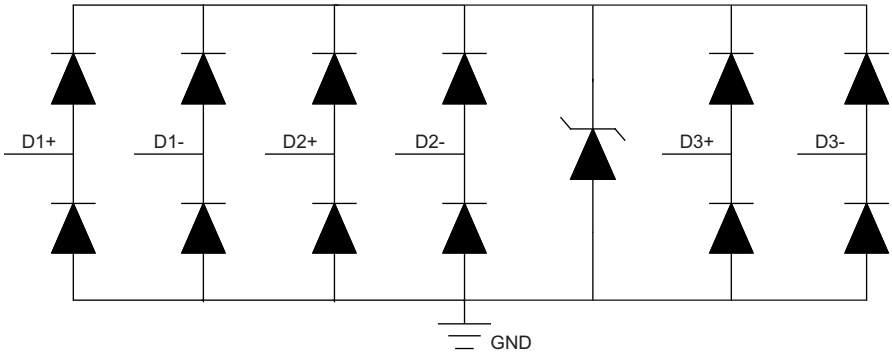


Figure 13. TPD4E05U06 Block Diagram

8.3 Feature Description

The TPDxE05U06 is a family of unidirectional Transient Voltage Suppressor (TVS) Electrostatic Discharge (ESD) protection diodes with ultra-low capacitance. Each device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 international standard. The TPDxE05U06's ultra-low loading capacitance makes it ideal for protecting any high-speed signal pins.

8.3.1 ±15-kV IEC61000-4-2 Level 4 ESD Protection

The I/O pins can withstand ESD events up to ±12-kV contact and ±15-kV air. An ESD/surge clamp diverts the current to ground.

8.3.2 IEC61000-4-4 EFT Protection

The I/O pins can withstand an electrical fast transient burst of up to 80 A (5/50 ns waveform, 4 kV with 50 Ω impedance). An ESD/surge clamp diverts the current to ground. This has been validated on the TPD4E05U06 only.

8.3.3 IEC61000-4-5 Surge Protection

The I/O pins can withstand surge events up to 2.5 A and 40 W (8/20 µs waveform). An ESD/surge clamp diverts this current to ground.

8.3.4 I/O Capacitance

The capacitance between each I/O pin to ground is 0.42 pF (TPD1E05U06), 0.5 pF (TPD4E05U06) or 0.47 pF (TPD6E05U06). These capacitances support data rates up to 5.0 Gbps, and up to 6.0 Gbps (TPD1E05U06).

8.3.5 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is a minimum of 6 V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of 5 V.

8.3.6 Ultra-Low Leakage Current

The I/O pins feature an ultra-low leakage current of 10 nA (Max) with a bias of 2.5 V.

8.3.7 Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 10 V (I_{PP} = 1 A).

8.3.8 Industrial Temperature Range

This device features an industrial operating range of –40°C to 125°C.

8.3.9 Easy Flow-Through Routing

The layout of this device makes it simple and easy to add protection to an existing layout. The packages offers flow-through routing, requiring minimal modification to an existing layout.

8.4 Device Functional Modes

TPDxE05U06 is a passive integrated circuit that triggers when voltages are above VBR or below the lower diodes V_f (–0.6 V). During ESD events, voltages as high as ±15 kV (air) can be directed to ground via the internal diode network. Once the voltages on the protected line fall below the trigger levels of TPDxE05U06 (usually within 10’s of nano-seconds) the device reverts to passive.

9 Application and Implementation

9.1 Application Information

TPDxE05U06 is a diode type TVS which is typically used to provide a path to ground for dissipating ESD events on hi-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

9.2 Typical Applications

9.2.1 HDMI 1.4 Application

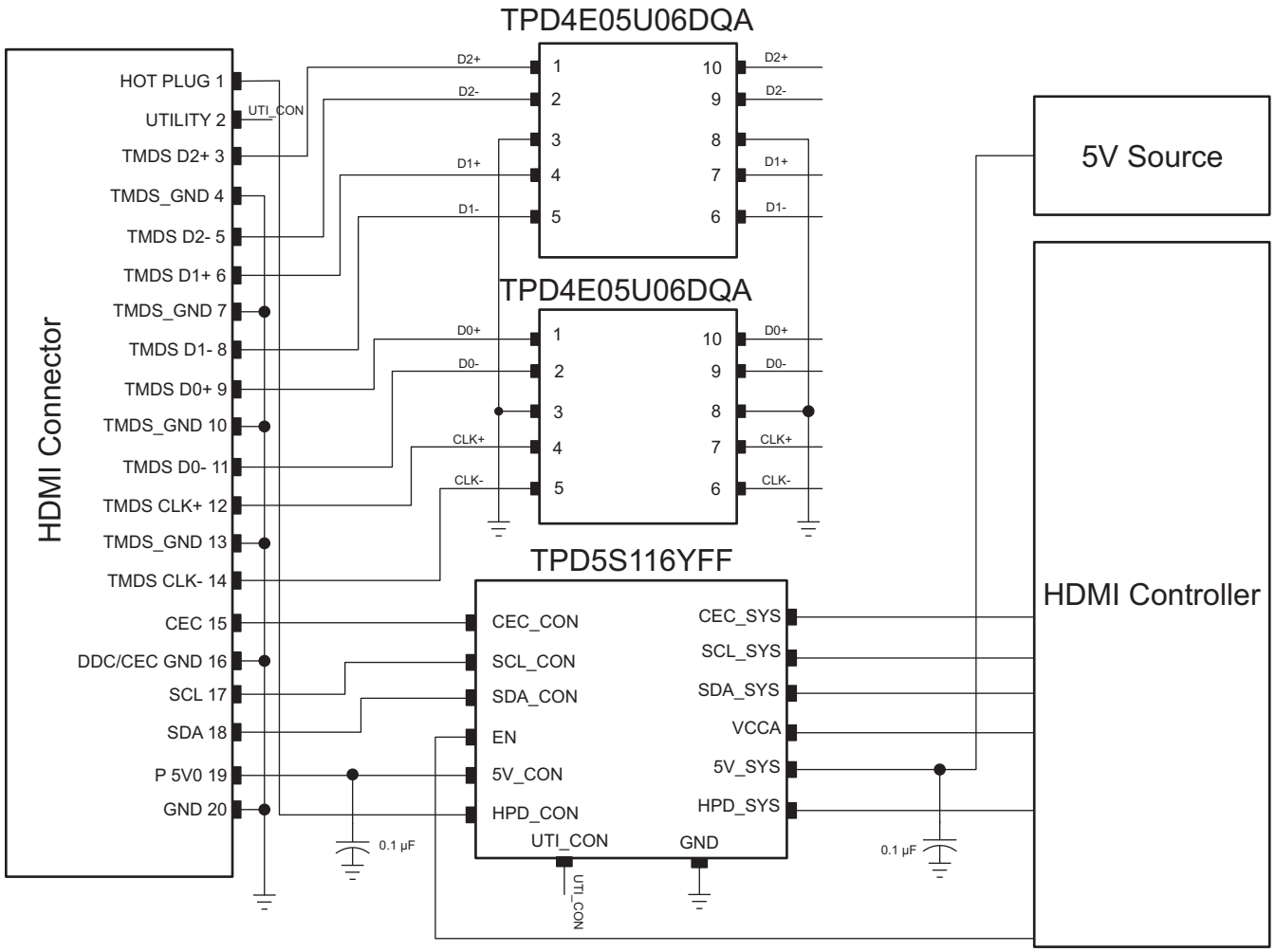


Figure 14. HDMI 1.4 Schematic

9.2.1.1 Design Requirements

For this design example, two TPD4E05U06 devices, and a TPD6S116 are being used in an HDMI 1.4 application. This will provide a complete port protection scheme.

Given the HDMI 1.4 application, the following parameters are known.

DESIGN PARAMETER	VALUE
Signal range on Pins 1, 2, 4, or 5	0 V to 5 V
Operating Frequency	1.7 GHz

9.2.1.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer needs to know the following:

- Signal range on all the protected lines
- Operating frequency

9.2.1.2.1 Signal Range on Pin 1, 2, 4, or 5

TPD4E05U06 has 4 identical protection channels for signal lines. The symmetry of the device provides flexibility when selecting which of the 4 I/O channels will protect which signal lines. Any I/O will support a signal range of 0 to 5.5 V.

9.2.1.2.2 Operating Frequency

The TPD4E05U06 has a capacitance of 0.5 pF (Typ), supporting HDMI 1.4 data rates.

9.2.1.3 Application Curves

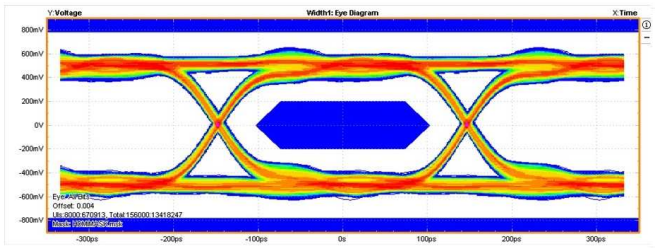


Figure 15. 3.4 Gbps HDMI Eye Diagram TPD1E05U06

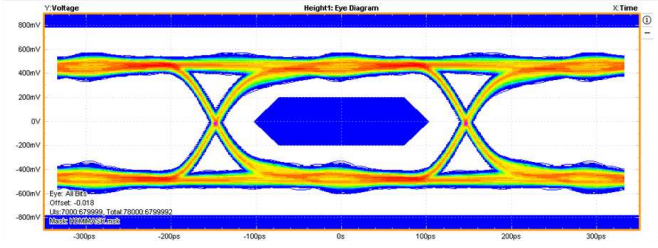


Figure 16. 3.4 Gbps HDMI Eye Diagram TPD4E05U06

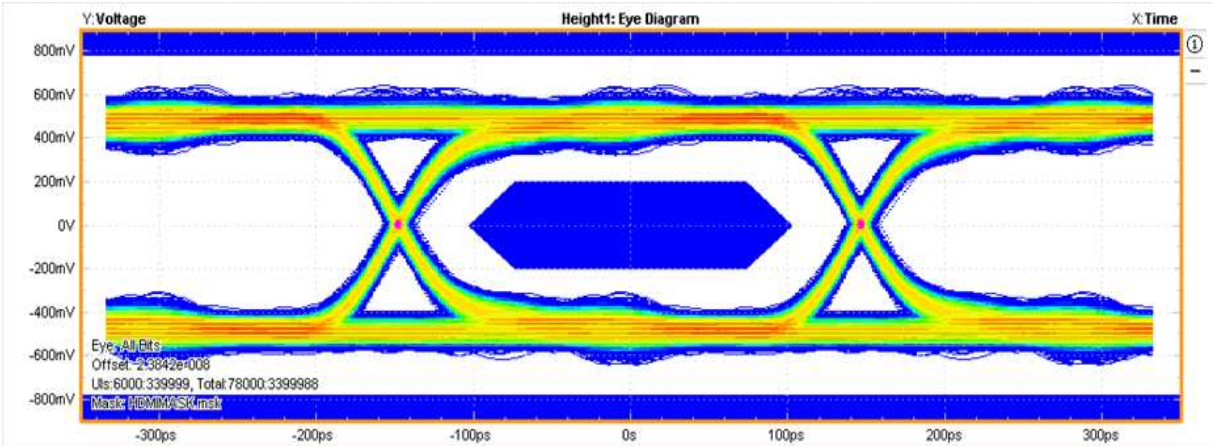


Figure 17. 3.4 Gbps HDMI Eye Diagram TPD6E05U06

9.2.2 HDMI 2.0 Application

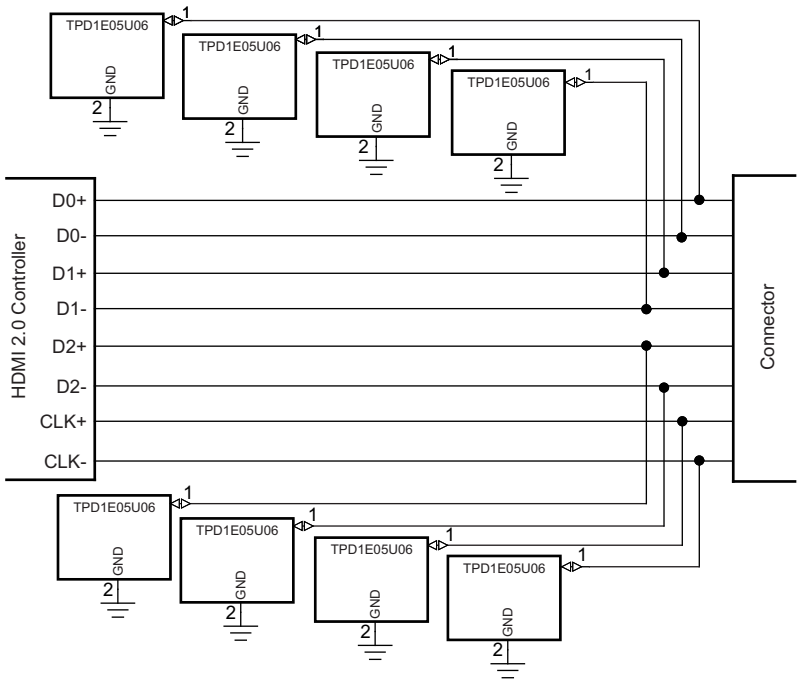


Figure 18. HDMI 2.0 Schematic

9.2.2.1 Design Requirements

For this design example, the TPD1E05U06 and the TPD5S116 will be used to protect the data pairs and control lines of the HDMI 2.0 connection. This will provide full HDMI 2.0 port protection.

Given the HDMI 2.0 application, the following parameters are known.

DESIGN PARAMETER	VALUE
Signal Range on Data Lines	0 V to 5 V
Operating Frequency	3 GHz

9.2.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer needs to know the following:

- Signal range on all the protected lines
- Operating frequency

9.2.2.2.1 Signal Range

TPD1E05U06 has 1 protection channel for signal lines, supporting a signal range of 0 to 5.5 V.

9.2.2.2.2 Operating Frequency

The TPD1E05U06 has 0.42 pF of capacitance, which supports HDMI 2.0 data rates.

9.2.2.3 Application Curves

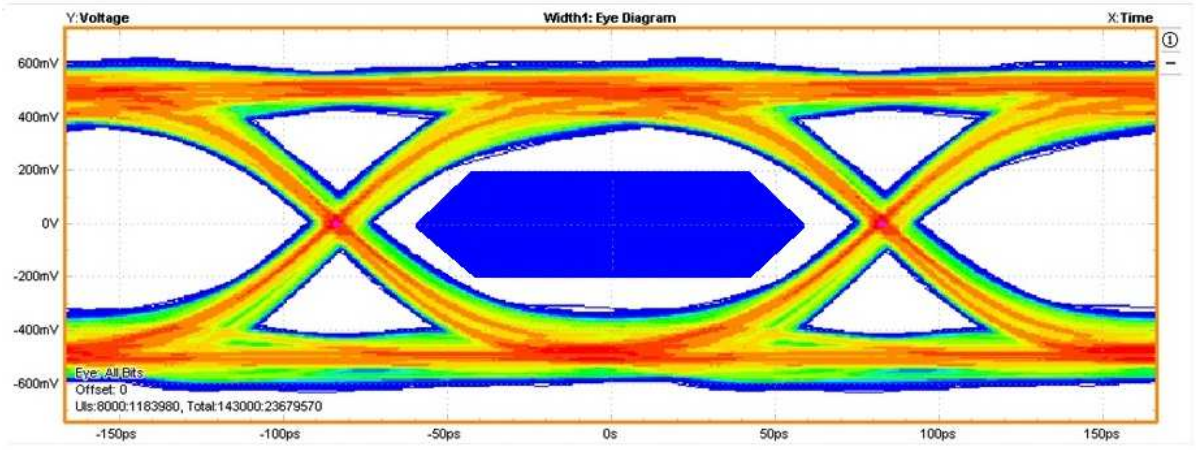


Figure 19. 6.0 Gbps HDMI Eye Diagram TPD1E05U06

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

10.2.1 TPD4E05U06 Layout Example

This application is typical of an HDMI 1.4 layout.

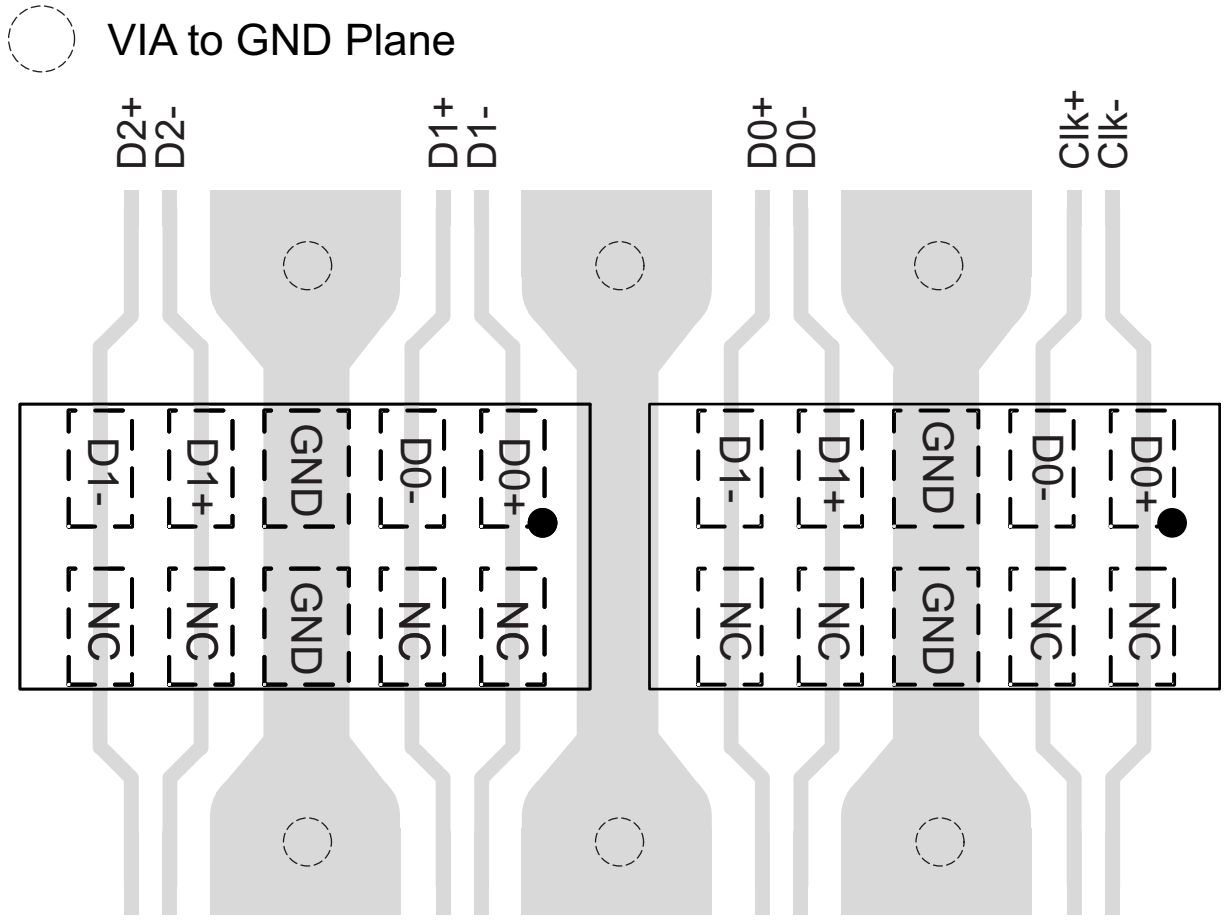


Figure 20. TPD4E05U06 Layout

Layout Example (continued)

10.2.2 TPD1E05U06 Layout Example

This application is typical of an HDMI 2.0 layout.

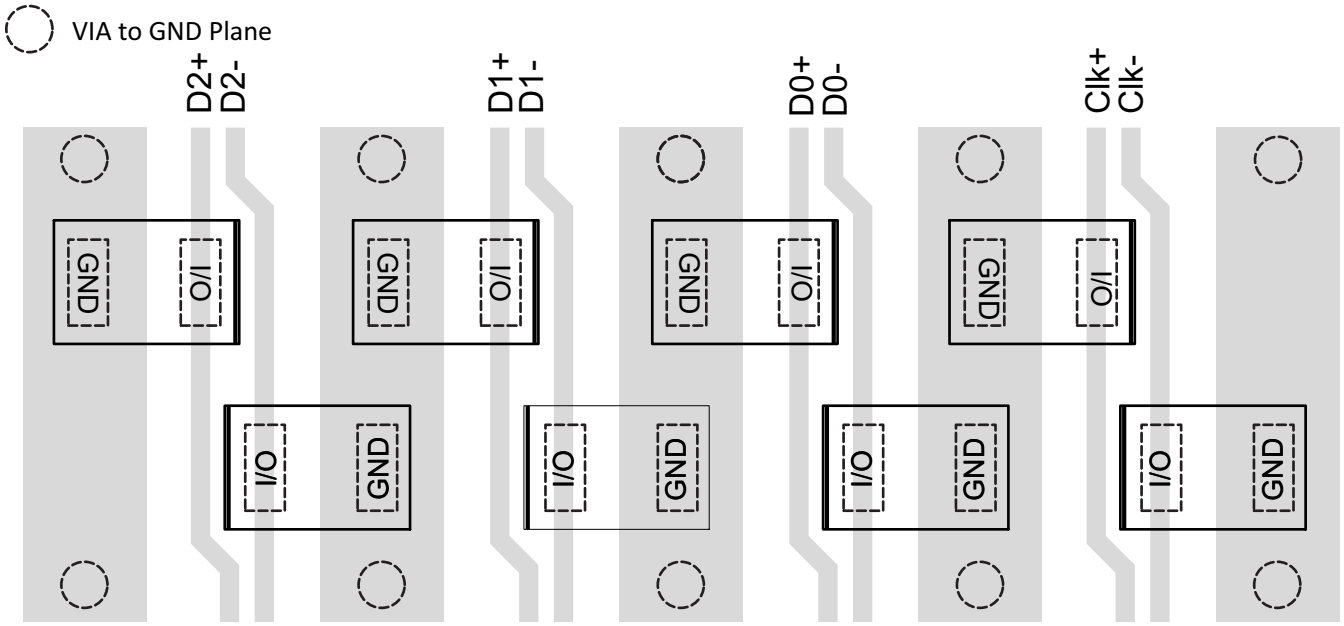


Figure 21. TPD1E05U06 Layout

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPD1E05U06	Click here	Click here	Click here	Click here	Click here
TPD4E05U06	Click here	Click here	Click here	Click here	Click here
TPD6E05U06	Click here	Click here	Click here	Click here	Click here

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD1E05U06DPYR	ACTIVE	X1SON	DPY	2	10000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C1	Samples
TPD1E05U06DPYT	ACTIVE	X1SON	DPY	2	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C1	Samples
TPD4E05U06DQAR	ACTIVE	USON	DQA	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BR	Samples
TPD6E05U06RVZR	ACTIVE	USON	RVZ	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BVL	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPD4E05U06 :

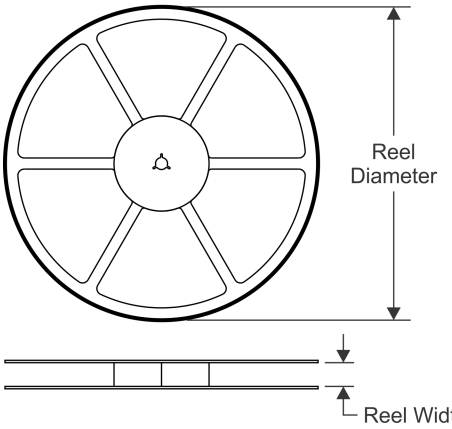
- Automotive: TPD4E05U06-Q1

NOTE: Qualified Version Definitions:

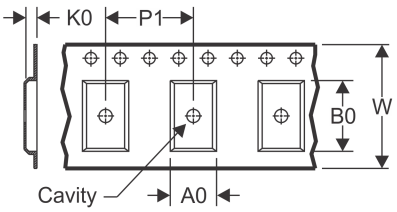
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

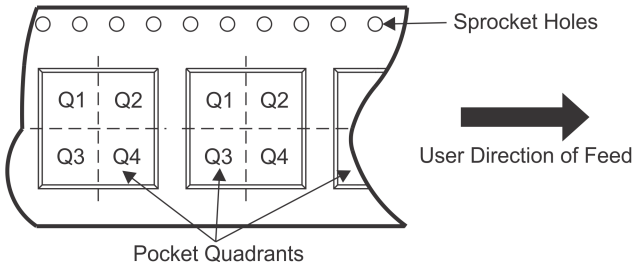


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

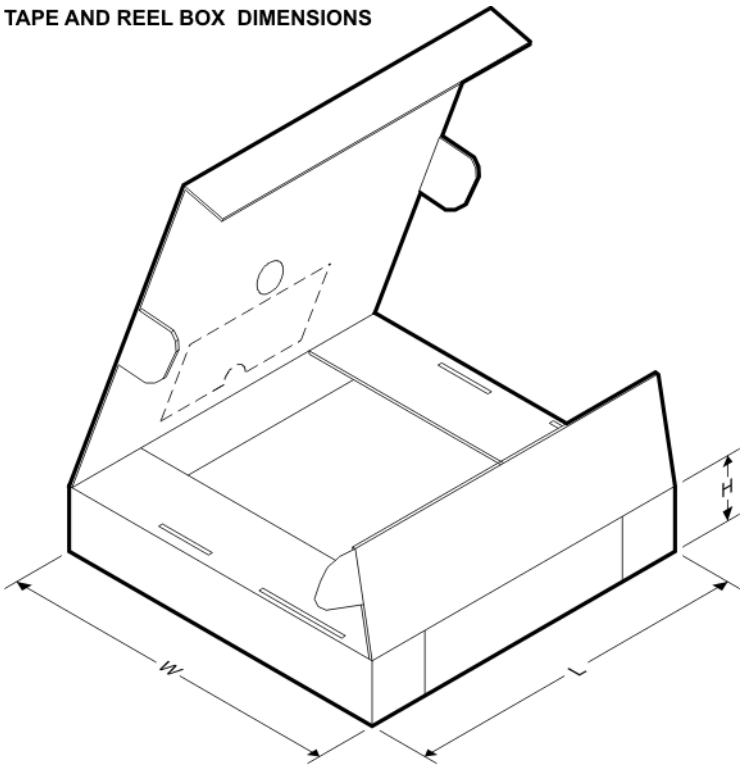
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD1E05U06DPYR	X1SON	DPY	2	10000	180.0	9.5	0.66	1.15	0.66	2.0	8.0	Q1
TPD1E05U06DPYT	X1SON	DPY	2	250	180.0	9.5	0.66	1.15	0.66	2.0	8.0	Q1
TPD4E05U06DQAR	USON	DQA	10	3000	180.0	9.5	1.23	2.7	0.7	4.0	8.0	Q1
TPD6E05U06RVZR	USON	RVZ	14	3000	180.0	13.2	1.65	3.8	0.7	4.0	12.0	Q1

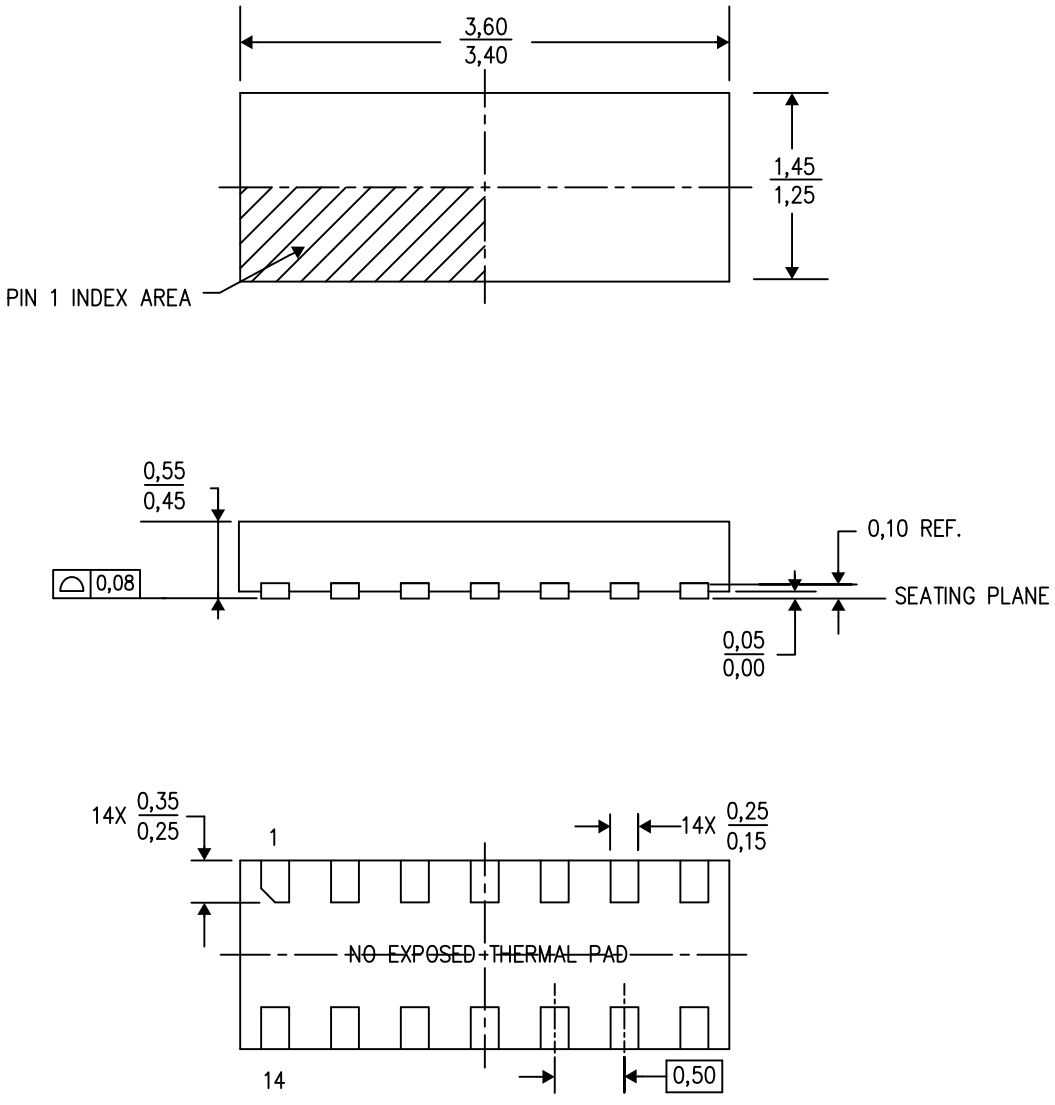
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD1E05U06DPYR	X1SON	DPY	2	10000	184.0	184.0	19.0
TPD1E05U06DPYT	X1SON	DPY	2	250	184.0	184.0	19.0
TPD4E05U06DQAR	USON	DQA	10	3000	184.0	184.0	19.0
TPD6E05U06RVZR	USON	RVZ	14	3000	184.0	184.0	19.0

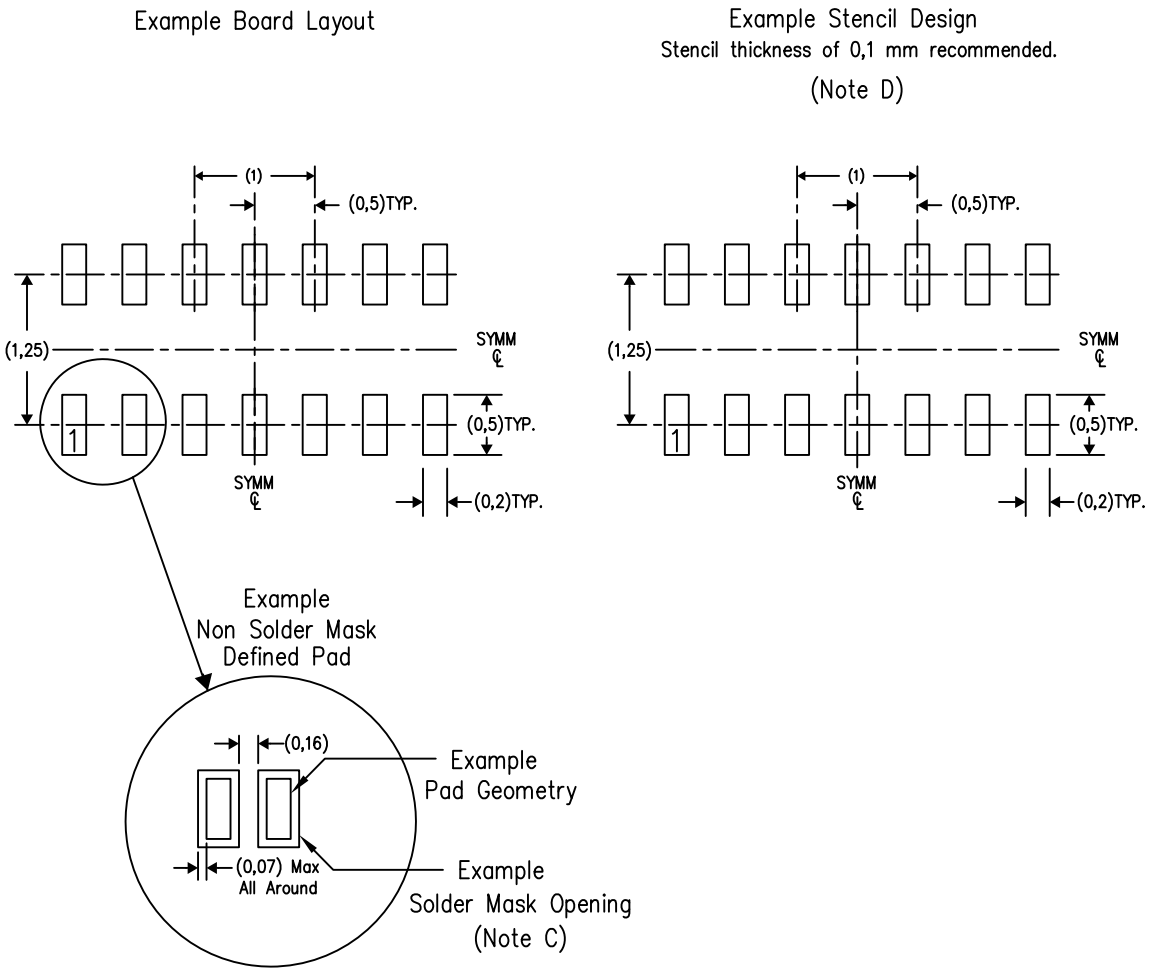
RVZ (R–PUSON–N14) PLASTIC SMALL OUTLINE NO–LEAD



4218112/B 04/14

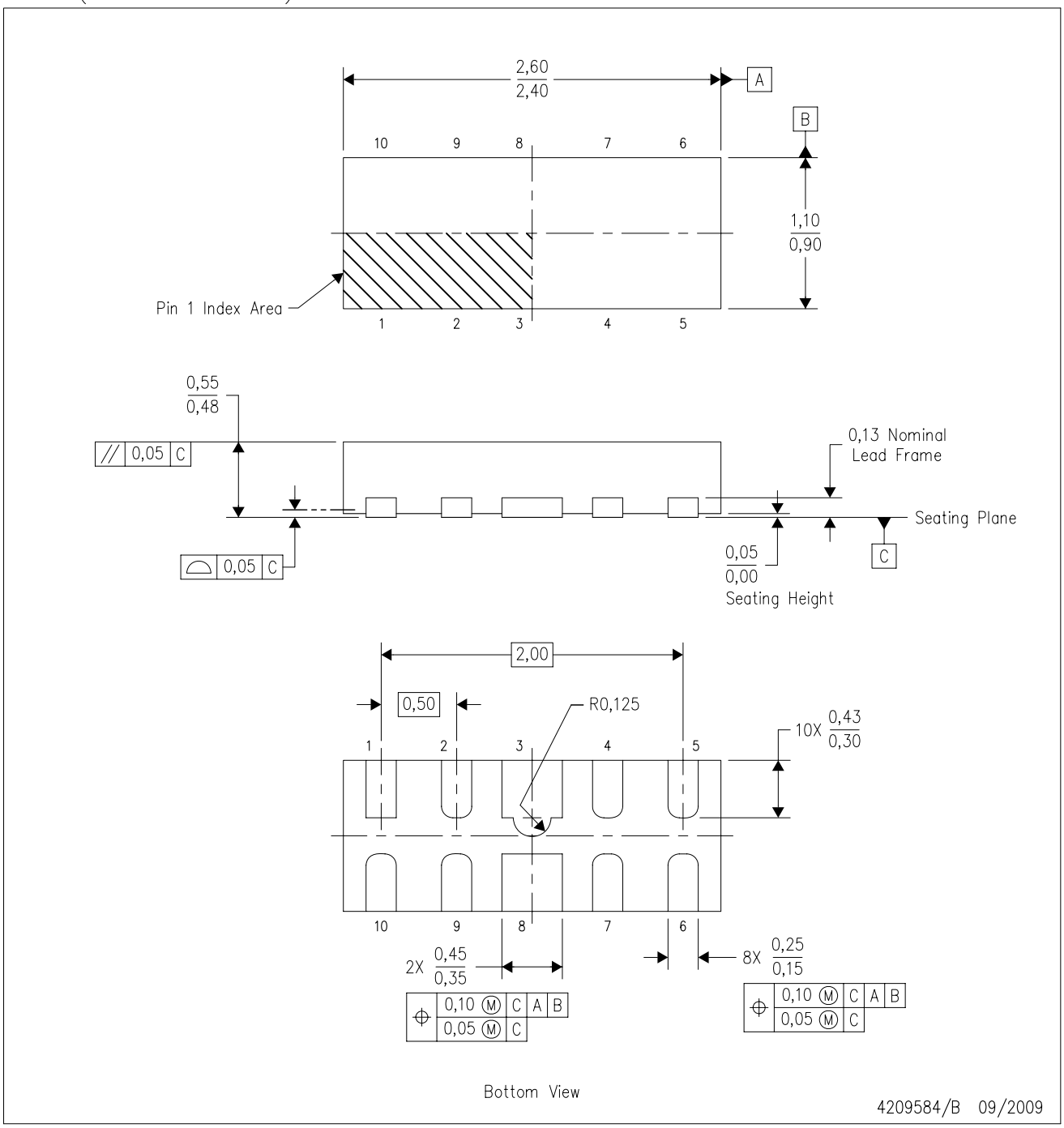
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.

RVZ (R–PUSON–N14) PLASTIC SMALL OUTLINE NO–LEAD



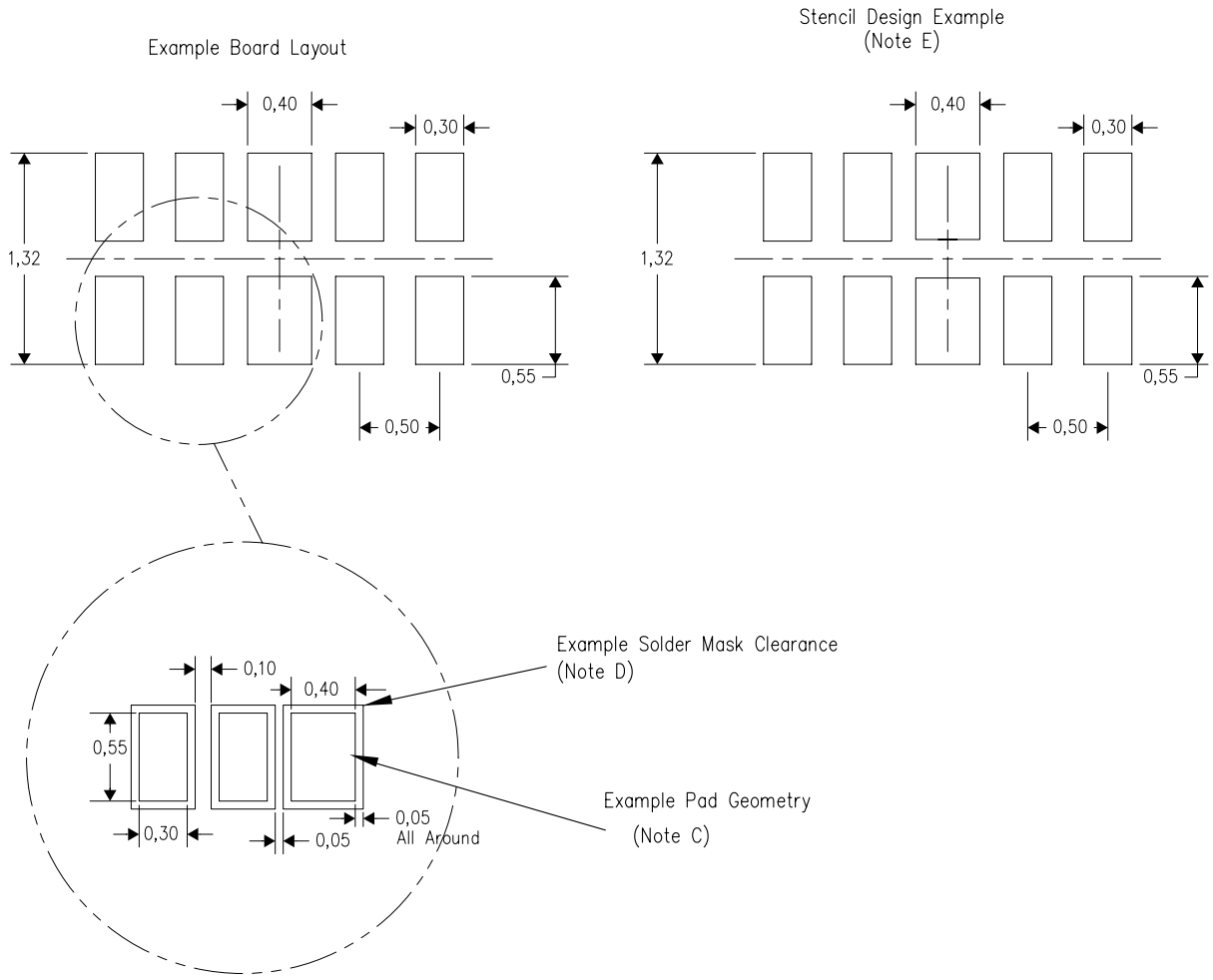
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.

DQA (R–PSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



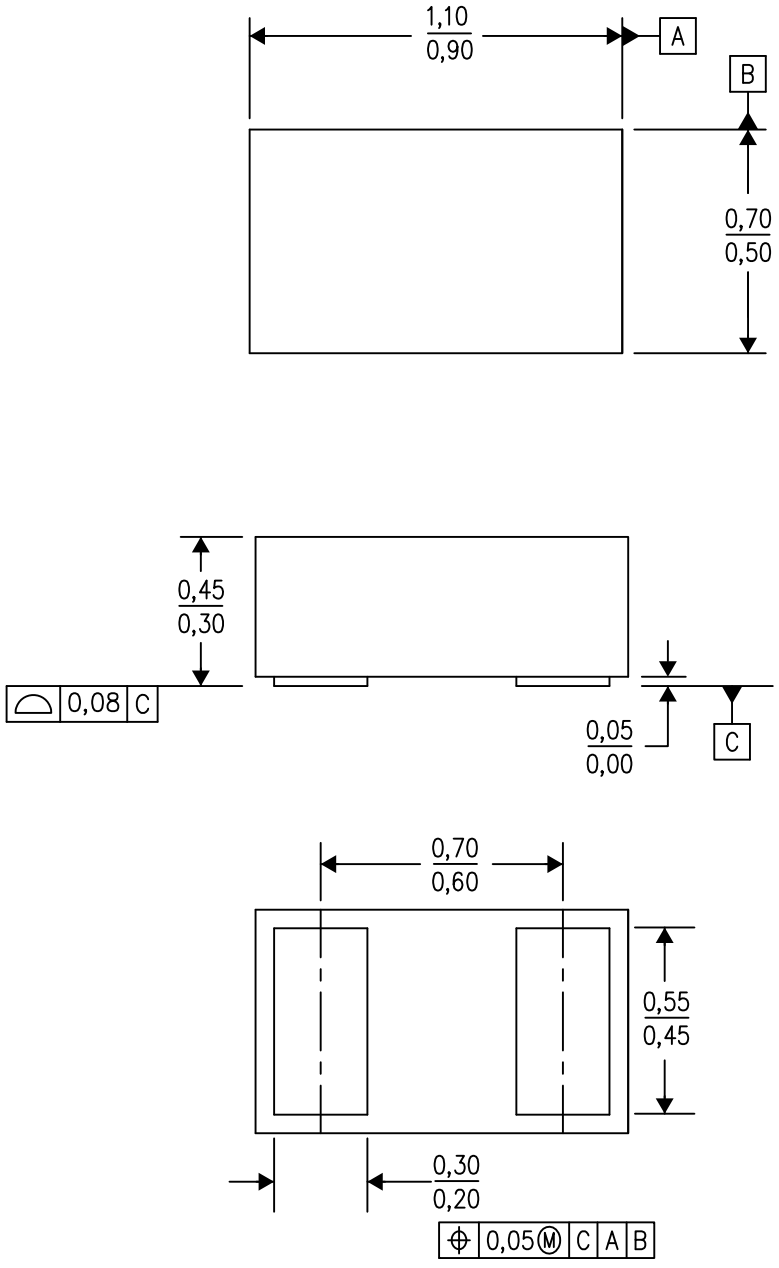
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.

DQA (R–PUSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DPY (R–PX1SON–N2) PLASTIC SMALL OUTLINE NO–LEAD

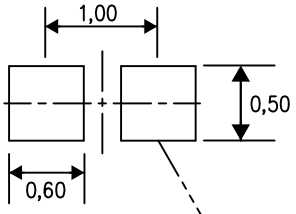


4211012/D 08/14

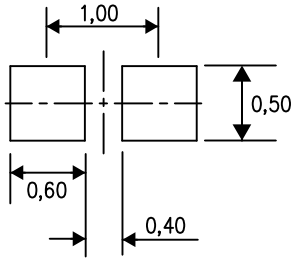
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.

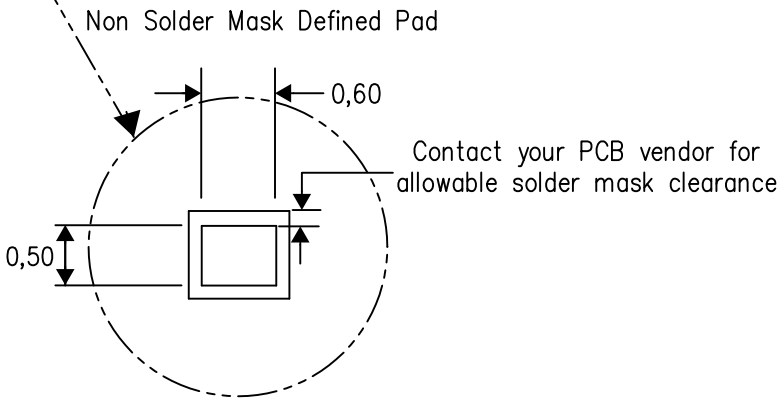
DPY (S–PX2SON–N2) PLASTIC SMALL OUTLINE NO–LEAD

Example Board Layout



Example Stencil Design
(Note E)





4215270/A 08/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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