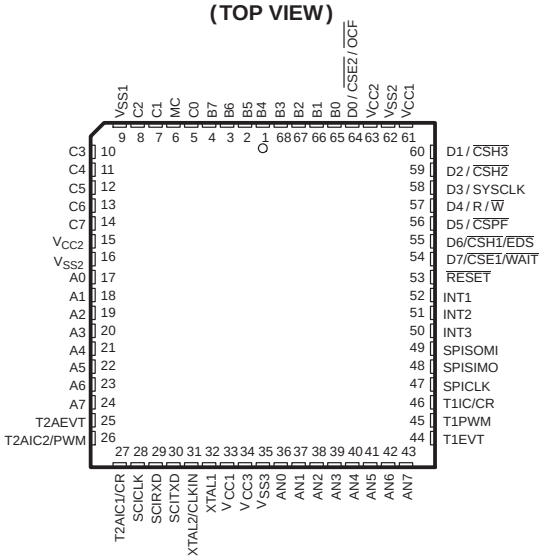
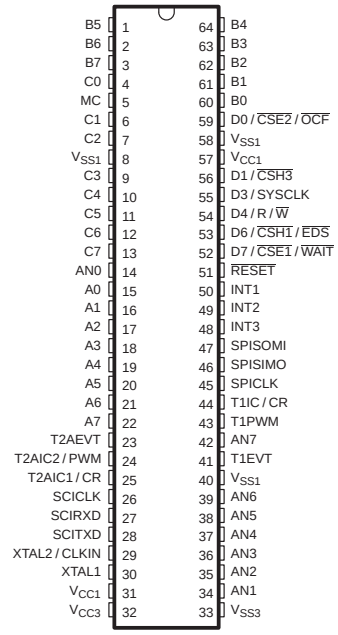
- **CMOS/EEPROM/EPROM Technologies on a Single Device**
  - **Mask-ROM Devices for High-Volume Production**
  - **One-Time-Programmable (OTP) EPROM Devices for Low-Volume Production**
  - **Reprogrammable EPROM Devices for Prototyping Purposes**
- **Internal System Memory Configurations**
  - **On-Chip Program Memory Versions**
    - **ROM: 4K to 48K Bytes**
    - **EPROM: 16K to 48K Bytes**
    - **ROM-less**
  - **Data EEPROM: 256 or 512 Bytes**
  - **Static RAM: 256 to 3.5K Bytes**
  - **External Memory/Peripheral Wait States**
  - **Precoded External Chip-Select Outputs in Microcomputer Mode**
- **Flexible Operating Features**
  - **Low-Power Modes: STANDBY and HALT**
  - **Commercial, Industrial, and Automotive Temperature Ranges**
  - **Clock Options**
    - **Divide-by-4 (0.5 MHz – 5 MHz SYSCLK)**
    - **Divide-by-1 (2 MHz – 5 MHz SYSCLK)**
    - **Phase-Locked Loop (PLL)**
  - **Supply Voltage (V_{CC}): 5 V ± 10%**
- **Eight-Channel 8-Bit Analog-to-Digital Converter 1 (ADC1)**
- **Two 16-Bit General-Purpose Timers**
- **On-Chip 24-Bit Watchdog Timer**
- **Two Communication Modules**
  - **Serial Communications Interface 1 (SCI1)**
  - **Serial Peripheral Interface (SPI)**
- **Flexible Interrupt Handling**
- **TMS370 Series Compatibility**
- **CMOS/Package/TTL-Compatible I/O Pins**
  - **64-Pin Plastic and Ceramic Shrink Dual-In-Line Packages/44 Bidirectional, 9 Input Pins**
  - **68-Pin Plastic and Ceramic Leaded Chip Carrier Packages/46 Bidirectional, 9 Input Pins**
  - **All Peripheral Function Pins Are Software Configurable for Digital I/O**

FN/FZ PACKAGE
(TOP VIEW)



JN/NM PACKAGE
(TOP VIEW)



- **Workstation/PC-Based Development System**
  - **C Compiler and C Source Debugger**
  - **Real-Time In-Circuit Emulation**
  - **Extensive Breakpoint/Trace Capability**
  - **Software Performance Analysis**
  - **Multi-Window User Interface**
  - **Microcontroller Programmer**

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Pin Descriptions

PIN				I/O†	DESCRIPTION‡
NAME	ALTERNATE FUNCTION	SDIP (64)	LCC (68)		
A0	DATA0	15	17	I/O	Single-chip mode: Port A is a general-purpose bidirectional I/O port. Expansion mode: Port A can be individually programmed as the external bidirectional data bus (DATA0–DATA7).
A1	DATA1	16	18		
A2	DATA2	17	19		
A3	DATA3	18	20		
A4	DATA4	19	21		
A5	DATA5	20	22		
A6	DATA6	21	23		
A7	DATA7	22	24		
B0	ADDR0	60	65	I/O	Single-chip mode: Port B is a general-purpose bidirectional I/O port. Expansion mode: Port B can be individually programmed as the low-order address output bus (ADDR0–ADDR7).
B1	ADDR1	61	66		
B2	ADDR2	62	67		
B3	ADDR3	63	68		
B4	ADDR4	64	1		
B5	ADDR5	1	2		
B6	ADDR6	2	3		
B7	ADDR7	3	4		
C0	ADDR8	4	5	I/O	Single-chip mode: Port C is a general-purpose bidirectional I/O port. Expansion mode: Port C can be individually programmed as the high-order address output bus (ADDR8–ADDR15).
C1	ADDR9	6	7		
C2	ADDR10	7	8		
C3	ADDR11	9	10		
C4	ADDR12	10	11		
C5	ADDR13	11	12		
C6	ADDR14	12	13		
C7	ADDR15	13	14		
INT1	NMI	50	52	I	External (nonmaskable or maskable) interrupt/general-purpose input pin
INT2	—	49	51	I/O	External maskable interrupt input/general-purpose bidirectional pin
INT3	—	48	50	I/O	External maskable interrupt input/general-purpose bidirectional pin
AN0	E0	14	36	I	ADC1 analog input (AN0–AN7) or positive reference pins (AN1–AN7) Port E can be individually programmed as general-purpose input pins if not used as ADC1 analog input or positive reference input.
AN1	E1	34	37		
AN2	E2	35	38		
AN3	E3	36	39		
AN4	E4	37	40		
AN5	E5	38	41		
AN6	E6	39	42		
AN7	E7	42	43		
V_{CC3}		32	34		ADC1 positive-supply voltage and optional positive-reference input pin
V_{SS3}		33	35		ADC1 ground reference pin
$\overline{\text{RESET}}$		51	53	I/O	System reset bidirectional pin. $\overline{\text{RESET}}$, as an input, initializes the microcontroller; as open-drain output, $\overline{\text{RESET}}$ indicates an internal failure was detected by the watchdog or oscillator fault circuit.
MC		5	6	I	Mode control (MC) pin. MC enables EEPROM write-protection override (WPO) mode, also EPROM V_{PP}.
XTAL2/CLKIN		29	31	I	Internal oscillator crystal input/external clock source input
XTAL1		30	32	O	Internal oscillator output for crystal
V_{CC1}		31, 57	33, 61		Positive supply voltage
V_{CC2}		—	15,63		Positive supply voltage

† I = input, O = output

‡ Ports A, B, C, and D can be configured only as general-purpose I/O pins. Also, port D3 can be configured as SYSCLK.

Pin Descriptions (Continued)

PIN				I/O†	DESCRIPTION‡
NAME	ALTERNATE FUNCTION	SDIP (64)	LCC (68)		
V_{SS1}		8, 58,40	9		Ground reference for digital logic
V_{SS2}		—	16,62		Ground reference for digital I/O logic
	FUNCTION			I/O	Single-chip mode: Port D is a general-purpose bidirectional I/O port. Each of the port D pins can be individually configured as a general-purpose I/O pin, primary memory control signal (function A), or secondary memory control signal (function B). All chip selects are independent and can be used for memory bank switching. Refer to Table 1 for function A memory accesses.
	A / B				
D0	$\overline{CSE2}$ / $\overline{OCF}$	59	64		I/O pin A: Chip select eighth output 2 goes low during memory accesses I/O pin B: Opcode fetch goes low during the opcode fetch memory cycle.
D1	$\overline{CSH3}$ / —	56	60		I/O pin A: Chip select half output 3 goes low during memory accesses. I/O pin B: Reserved
D2	$\overline{CSH2}$ / —	—	59		I/O pin A: Chip select half output 2 goes low during memory accesses. I/O pin B: Reserved
D3	SYSCLK / SYSCLK	55	58		I/O pin A, B: Internal clock signal is 1/1 (PLL) or 1/4 XTAL2/CLKIN frequency.
D4	R/$\overline{W}$ / R/$\overline{W}$	54	57		I/O pin A, B: Read/write output pin
D5	$\overline{CSPF}$ / —	—	56		I/O pin A: Chip select peripheral output for peripheral file goes low during memory accesses. I/O pin B: Reserved
D6	$\overline{CSH1}$ / $\overline{EDS}$	53	55		I/O pin A: Chip select half output 1 goes low during memory accesses. I/O pin B: External data strobe output goes low during memory accesses from external memory and has the same timings as the five chip selects.
D7	$\overline{CSE1}$ / $\overline{WAIT}$	52	54		I/O pin A: Chip select eighth output goes low during memory accesses. I/O pin B: Wait input pin extends bus signals.
SCITXD	SCIIO1	28	30	I/O	SCI transmit data output pin/general-purpose bidirectional pin (see Note 1)
SCIRXD	SCIIO2	27	29		SCI receive data input pin/general-purpose bidirectional pin
SCICLK	SCIIO3	26	28		SCI bidirectional serial clock pin/general-purpose bidirectional pin
T1IC/CR	T1IO1	44	46	I/O	Timer1 input capture/counter reset input pin/general-purpose bidirectional pin
T1PWM	T1IO2	43	45		Timer1 pulse-width-modulation (PWM) output pin/general-purpose bidirectional pin
T1EVT	T1IO3	41	44		Timer1 external event input pin/general-purpose bidirectional pin
T2AIC1/CR	T2AIO1	25	27	I/O	Timer2A input capture 1/counter reset input pin/general-purpose bidirectional pin
T2AIC2/PWM	T2AIO2	24	26		Timer2A input capture 2/PWM output pin/general-purpose bidirectional pin
T2AEVT	T2AIO3	23	25		Timer2A external event input pin/general-purpose bidirectional pin
SPISOMI	SPIIO1	47	49	I/O	SPI slave output pin, master input pin/general-purpose bidirectional pin
SPISIMO	SPIIO2	46	48		SPI slave input pin, master output pin/general-purpose bidirectional pin
SPICLK	SPIIO3	45	47		SPI bidirectional serial clock pin/general-purpose bidirectional pin

† I = input, O = output

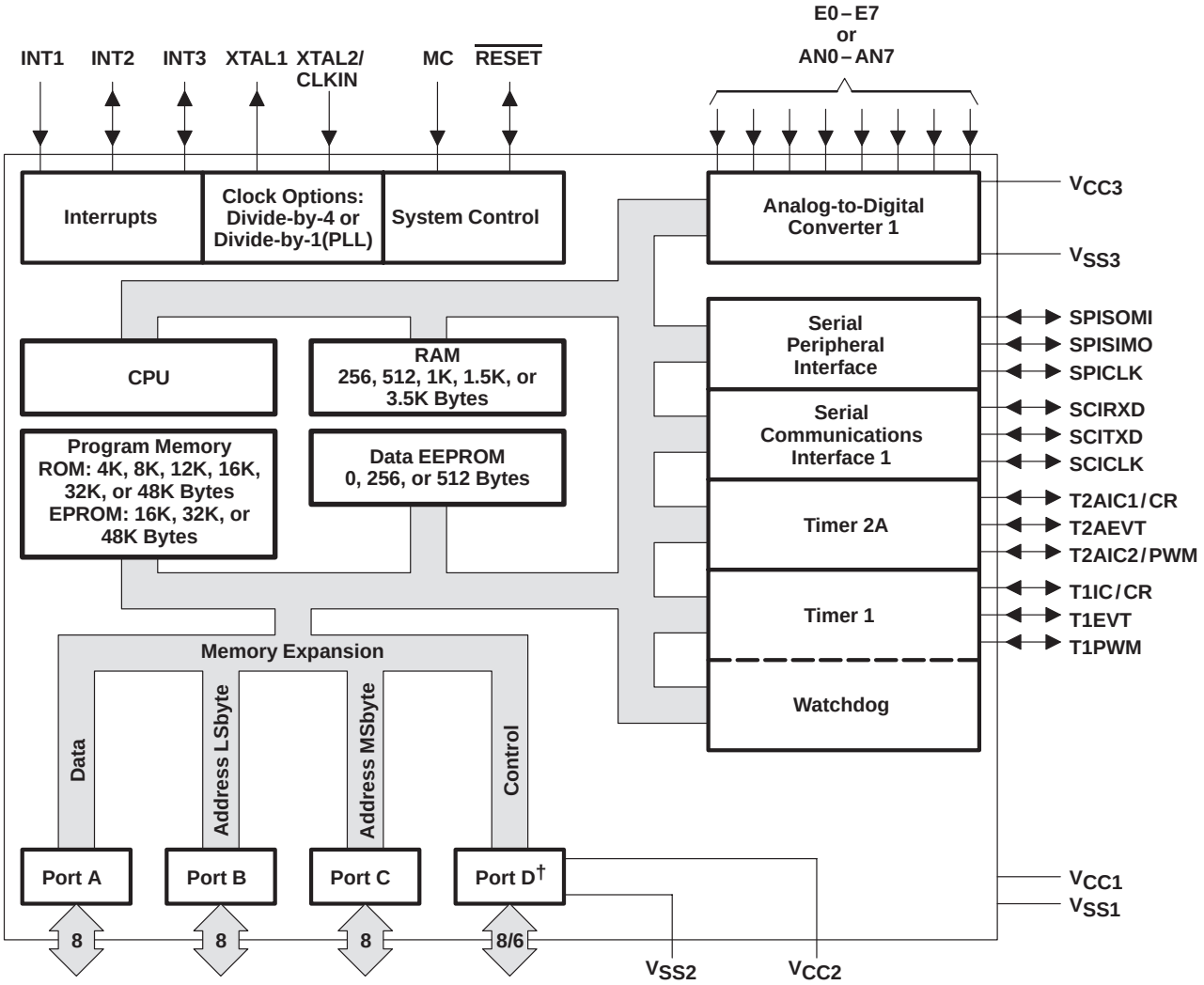
‡ Ports A, B, C, and D can be configured only as general-purpose I/O pins. Port D3 also can be configured as SYSCLK.

NOTE 1: The three-pin configuration SCI is referred to as SCI1.

Table 1. Function A: Memory Accesses Locations for ‘x5x Devices

FUNCTION A	‘X50, ‘X52, ‘X53, AND ‘X56	‘X58	‘X59
$\overline{CSEx}$	2000h – 3FFFh (8K bytes)	A000h – BFFFh (8K bytes)	E000h – EFFFh (4K bytes)
$\overline{CSHx}$	8000h – FFFFh (32K bytes)	C000h – FFFFh (16K bytes)	F000h – FFFFh (4K bytes)
$\overline{CSPF}$	10C0h – 10FFh (64 bytes)	10C0h – 10FFh (64 bytes)	10C0h – 10FFh (64 bytes)

functional block diagram



† For the 64-pin devices, there are only six pins for port D.

description

The TMS370Cx5x family of single-chip 8-bit microcontrollers provides cost-effective real-time system control through integration of advanced peripheral function modules and various on-chip memory configurations. The TMS370Cx5x family presently consists of twenty-one devices which are grouped into seven main sub-families: the TMS370Cx50, TMS370Cx52, TMS370Cx53, TMS370Cx56, TMS370Cx58, TMS370Cx59, and SE370C75x.

The TMS370Cx5x family of devices is implemented using high-performance silicon-gate CMOS EPROM and EEPROM technologies. The low-operating power, wide-operating temperature range, and noise immunity of CMOS technology, coupled with the high performance and extensive on-chip peripheral functions, make the TMS370Cx5x devices attractive in system designs for automotive electronics, industrial motor control, computer peripheral control, telecommunications, and consumer application. Table 2 provides a memory configuration overview of the TMS370Cx5x devices.

description (continued)

Table 2. Memory Configurations

DEVICE	PROGRAM MEMORY (BYTES)		OFF-CHIP MEMORY EXP. (BYTES)	DATA MEMORY (BYTES)		OPERATING MODES		PACKAGES 68 PIN PLCC/CLCC, OR 64 PIN PSDIP/CSDIP
	ROM	EPROM		RAM	EEPROM	μC†	μP†	
TMS370Cx50: TMS370C050, TMS370C150, TMS370C250, AND TMS370C350								
TMS370C050A	4K	—	112K	256	256	√	√	FN – PLCC / NM –PSDIP
TMS370C150A	—	—	56K	256	—	—	√	FN – PLCC
TMS370C250A	—	—	56K	256	256	—	√	FN – PLCC
TMS370C350A	4K	—	112K	256	—	√	√	FN – PLCC / NM –PSDIP
TMS370Cx52: TMS370C052, TMS370C352, AND TMS370C452								
TMS370C052A	8K	—	112K	256	256	√	√	FN – PLCC / NM –PSDIP
TMS370C352A	8K	—	112K	256	—	√	√	FN – PLCC / NM –PSDIP
TMS370C452A‡	8K	—	112K	256	256	√	√	FN – PLCC
TMS370Cx53: TMS370C353								
TMS370C353A	12K	—	112K	1.5K	—	√	√	FN – PLCC
TMS370Cx56: TMS370C056, TMS370C156, TMS370C256, TMS370C356, TMS370C456, AND TMS370C756								
TMS370C056A	16K	—	112K	512	512	√	√	FN – PLCC / NM –PSDIP
TMS370C156A	—	—	56K	512	—	—	√	FN – PLCC
TMS370C256A	—	—	56K	512	512	—	√	FN – PLCC
TMS370C356A	16K	—	112K	512	—	√	√	FN – PLCC / NM –PSDIP
TMS370C456A‡	16K	—	112K	512	512	√	√	FN – PLCC
TMS370C756A	—	16K	112K	512	512	√	√	FN – PLCC / NM –PSDIP
TMS370Cx58: TMS370C058, TMS370C358, AND TMS370C758								
TMS370C058A	32K	—	64K	1K	256	√	√	FN – PLCC / NM –PSDIP
TMS370C358A	32K	—	64K	1K	—	√	√	FN – PLCC / NM –PSDIP
TMS370C758A, TMS370C758B	—	32K	64K	1K	256	√	√	FN – PLCC / NM –PSDIP
TMS370Cx59: TMS370C059 AND TMS370C759								
TMS370C059A§	48K	—	20K	3.5K	256	√	√	FN – PLCC
TMS370C759A§	—	48K	20K	3.5K	256	√	√	FN – PLCC
EPROM DEVICE: SE370C756, SE370C758, and SE370C759								
SE370C756A¶	—	16K	112K	512	512	√	√	FZ – CLCC / JN –CSDIP
SE370C758A¶, SE370C758B¶	—	32K	64K	1K	256	√	√	FZ – CLCC / JN –CSDIP
SE370C759A§¶	—	48K	20K	3.5K	256	√	√	FZ – CLCC

† μC – Microcomputer mode
μP – Microprocessor mode
‡ TMS370C45x support ROM memory security. Refer to the program ROM section.
§ Only operate up to 3 MHz SYSCLK
¶ System evaluators and development tools are for use only in a prototype environment, and their reliability has not been characterized.