TMS320VC5416

Digital Signal Processor

Silicon Errata

SPRZ172F
April 2000
Revised January 2006

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REVISION HISTORY

This silicon errata revision history highlights the technical changes made to the SPRZ172E revision to make it an SPRZ172F revision.

PAGE(S) NO.	ADDITIONS/CHANGES/DELETIONS
6	Added Die Revision table

Contents

1 Introduction

This document describes the silicon updates to the functional specifications for the TMS320VC5416 silicon. The errata are applicable to:

- TMS320VC5416 (144-pin LQFP, PGE suffix)
- TMS320VC5416 (144-pin MicroStar BGA™, GGU suffix)

1.1 Device and Development Tool Support Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320™ DSP devices and support tools. Each TMS320™ DSP commercial family member has one of three prefixes: TMX, TMP, or TMS. Texas Instruments recommends two of three possible prefix designators for support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices/tools TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

TMS Fully qualified production device

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully qualified development-support product

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

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1.2 Device Markings

Figure 1 provides an example of the 5416 device markings and defines each of the markings. The device revision can be determined by the symbols marked on the top of the package as shown in Figure 1. Some prototype devices may have markings different from those illustrated.

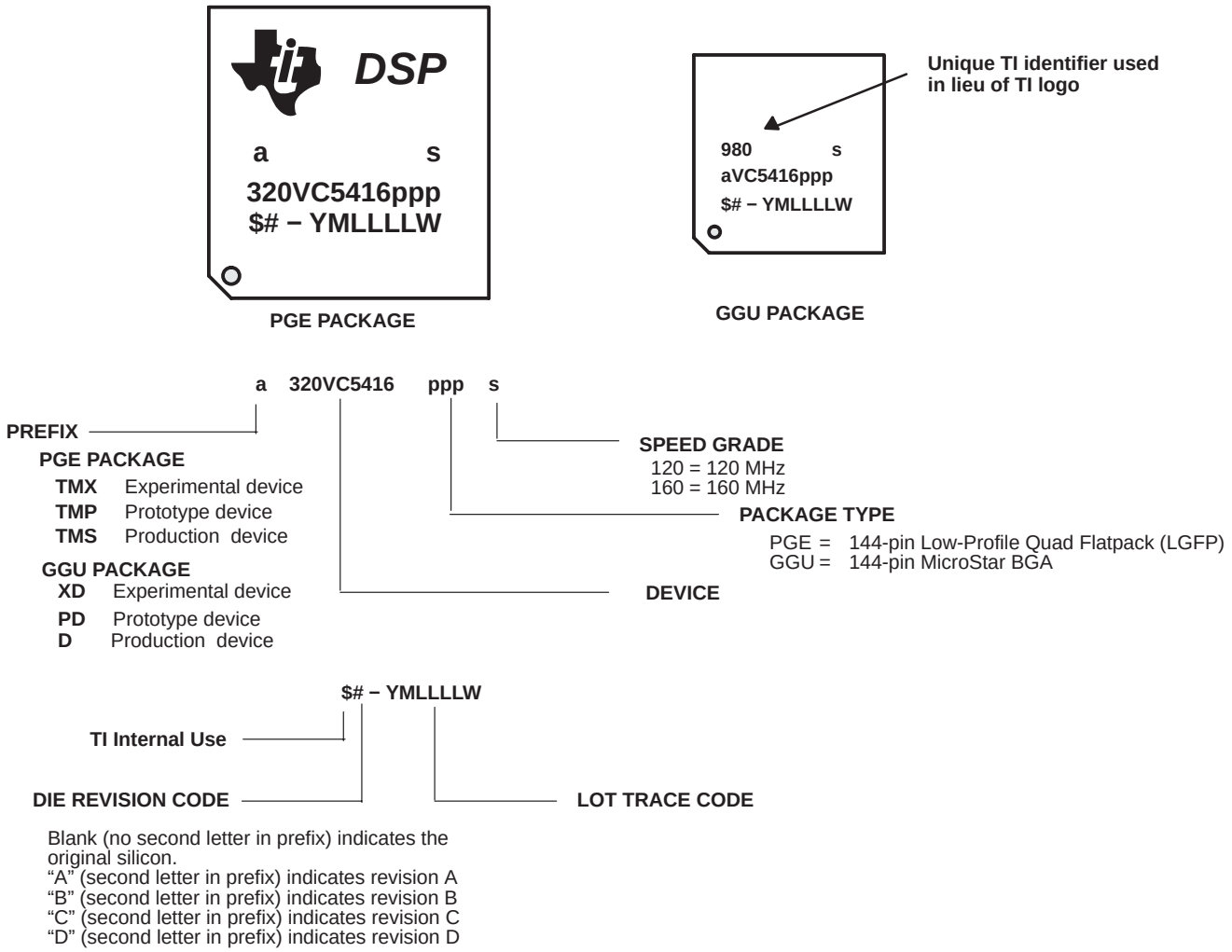

Figure 1. Example Markings for 5416 Packages

Table 1. Die Revision Code

Die Revision	Silicon Revision	Comments
Blank (no second letter in prefix)	Indicates Original Silicon	
A (second letter in prefix is A)	Indicates Silicon Revision A	
B (second letter in prefix is B)	Indicates Silicon Revision B	
C (second letter in prefix is C)	Indicates Silicon Revision C	Internal Improvement
D (second letter in prefix is D)	Indicates Silicon Revision D	Internal improvement

2 Known Design Marginality/Exceptions to Functional Specifications

Table 2. Summary of Advisories

Description	Revision Affected	Page
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Advisory *HPI HINT*

Revision(s) Affected: Original, A, B, C, and D

Details: The HPI will become locked up, with HRDY stuck low, if both the host processor and the TMS320VC5416 CPU write a one (1) to HINT as the same time.

Workaround: Avoid performing redundant operations to the HINT bit. Both the Host and the CPU should check to see if HINT is set before trying to write a one (1) to this bit.

For:	If...	Then...
the HOST	HINT is ***not*** set...	Do not try to clear HINT by writing a one (1) to it, because the CPU may try to set it.
the CPU	HINT is ***already*** set...	Do not try to set HINT again by writing a one (1) to it, since the HOST may try to clear it.

Advisory *Bootloader: 8-Bit Parallel Mode*

Revision(s) Affected: Original and Revision A

Details: In 8-bit parallel boot mode, the bootloader may incorrectly interpret the end-of-data blocks because of a failure to mask the upper bits in the accumulator when the end-of-block marker (0000h) is evaluated.

Workaround: D8−D15 should be pulled down or driven low during bootload in this mode.

Advisory *Far Branches/Calls/Interrupts from Active Repeat Blocks (BRAF)*

Revision(s) Affected: Original, A, B, C, and D

Details: When a block repeat is interrupted by a far call, far branch, or interrupt to another page; and a program memory address in the called routine happens to have the same lower 16 bits as the block-repeat end address (REA), a branch to the 16-bit block-repeat start address (RSA) is executed on the current page until the block-repeat counter decrements to 0. The XPC is ignored during these occurrences.

Workaround: Use one of the following workarounds:

1. If the called routine must be on a different page and has a program memory address that has the same lower 16 bits as the REA, save ST1 and clear the BRAF in the vector table before entering the called routine with the following two instructions:

```
PSHM ST1
RSBX BRAF
```

   Then, restore ST1 before returning from the called routine. In the case of an interrupt service routine, these two instructions can be included in the delay slots following a delayed-branch instruction (BD) at the interrupt vector location. Then, the ST1 is restored before returning from the routine. With this method, BRAF is always inactive while in the called routine. If BRAF was not active at the time of the call, the RSBX BRAF has no effect.

2. Put the called routine on the same page as the interruptible block-repeat code. This can be achieved automatically by placing the interrupt vector table and the interrupt service routines or other called routines on the overlay pages. If this approach is used, far branches/calls are not necessary and the situation is completely avoided.
3. Avoid putting the called routine on other pages where a program memory address has the same lower 16 bits as the REA.
4. Use the BANZ instruction as a substitute for the block repeat.

Advisory *Round (RND) Instruction Clears Pending Interrupts*

Revision(s) Affected: Original, A, B, C, and D

Details: The RND (round) instruction opcode is decoded incorrectly and will write to the interrupt flag register (IFR) with the data from the data write bus (E bus). Therefore, it could cause the pending interrupt to be missed.

Workaround: Do not use the RND instruction. Replace the RND instruction with an ADD instruction as follows:

For this instruction ...	Use ...
`RND src[,dst]`	`ADD #1,15,src[,dst]`

Advisory *TOUT Jitter*

Revision(s) Affected: Original, A, B, C, and D

Details: When the CLKOUT divide factor is set to a non-zero value, the timer output exhibits jitter because pulse width differ by one or two CLKOUT periods.

Workaround: Set DIVFCT to 0.

Advisory *DMA 1: External DMA/CPU Write*

Revision(s) Affected: Original and Revision A

Details: When the DMA is being used to perform external accesses, it can cause a CPU write pending error. That is, a CPU write followed by a CPU read of the same location can fail, with the read producing corrupted data. The following characteristics apply to this problem:

- This occurs when external DMA writes are active. That is, whenever the destination of a DMA transfer is an external memory address (program, data, or I/O).
- The source of the DMA transfer is not relevant to the problem.
- The DMA and CPU do not have to be accessing the same block of memory for the problem to occur.
- This can affect CPU reads of either SARAM or DARAM memory blocks.

Workaround: Either of the following provides adequate workarounds:

1. Do not perform external DMA accesses at the same time as a CPU accesses.
2. Never perform a CPU read of a memory location immediately after that location has been written. A dummy write to a different location prior to the read will avoid the problem.

Advisory	DMA 2: DMPREC

Revision(s) Affected: Original and Revision A

Details:

When updating the DE bits of the DMPREC register while one or more DMA channel transfers are in progress, it is possible for the write to the DMPREC to cause an additional transfer on one of the active channels.

The problem occurs when an active channel completes a transfer at the same time that the user updates the DMPREC register. When the transfer completes, the DMA logic attempts to clear the DE bit corresponding to the complete channel transfer, but the register is instead updated with the CPU write (usually an ORM instruction) which can set the bit and cause an additional transfer on the channel. Refer to the example below for further clarification:

Example:

DMPREC value = 00C1h, corresponding to the following channel activity:

Channel 0 – enabled and running	(DE0 = 1)
Channel 1 – disabled	(DE1 = 0)
Channel 2 – disabled	(DE2 = 0)
Channel 3 – disabled	(DE3 = 0)
Channel 4 – disabled	(DE4 = 0)
Channel 5 – disabled	(DE5 = 0)

If the following conditions occur simultaneously:

- Channel 0 transfer completes and DMA logic clears DE0 internally.
- User code attempts to enable another channel (e.g. ORM #2, DMPREC)

The user code will re-enable channel 0 (DMPREC value written = 00C3h), and an additional, unintended transfer will begin on channel 0.

Workaround:

There are a few conditions under which this problem does not occur. If all active DMA channels are configured in ABU mode or in autoinitialization mode, then the problem does not occur because the channels remain enabled until they are disabled by user code. The problem is also avoided in applications that use only one DMA channel at a time.

Systems that use multiple DMA channels simultaneously in multiframe mode without autoinitialization are most likely to have this problem. In such systems one of the following methods can be used to avoid the problem:

- Always wait for all channels to complete existing transfers before re-enabling any channels, and always enable all channels at the same time.
- Before enabling a channel, check the progress of any on-going transfers by reading the element and frame counts of each active channel. If any active channel is within two element transfers of completing a block transfer, then wait until the active channel completes the block transfer before writing to the DMPREC register. Otherwise, if all active channels have more than two element transfers left in a block transfer, it is safe to update the DMPREC register.

Advisory *Boundary Scan “SAMPLE”*

Revision(s) Affected: Original and Revision A

Details: The boundary scan “SAMPLE” instruction does not function properly, and therefore, prevents the proper reading of the BDXx pins.

Workaround: None

Advisory *Debugger Single Step Command*

Revision(s) Affected: Original and Revision A

Details: When the debugger single step command is used to step through write instructions with the addressing mode of the Stack Pointer relative to the same block of memory, the write instruction does not function properly (i.e., the wrong value is written).

Workaround: Use the debugger RUN command with a software or analysis breakpoint.

Advisory *On-Chip Oscillator Support*

Revision(s) Affected: Original and Revision A

Details: On-chip oscillator does not function properly.

Workaround: Avoid using crystal as clock source with the on-chip oscillator. Functionality described in *TMS320VC5416 Fixed-Point Digital Signal Processor* data manual (literature number SPRS095) is not supported until silicon revision B.

3 Documentation Support

For device-specific datasheets and related documentation, visit the TI web site at: **http://www.ti.com**

To access documentation on the web site:

1. Go to **http://www.ti.com**
2. Click on the **"TMS320™ DSP Products"** link
3. Scroll to "**C54x™ DSP Generation**" or "**C55x™ DSP Generation**" and click on "**DEVICE INFORMATION**"
4. Click on a device name and then click on the documentation type you prefer.

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