TMS320VC5409 Fixed-Point Digital Signal Processor

Data Manual

Literature Number: SPRS082E
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TEXAS INSTRUMENTS

1 TMS320VC5409 Features

- **Advanced Multibus Architecture With Three Separate 16-Bit Data Memory Buses and One Program Memory Bus**
- **40-Bit Arithmetic Logic Unit (ALU), Including a 40-Bit Barrel Shifter and Two Independent 40-Bit Accumulators**
- **17- × 17-Bit Parallel Multiplier Coupled to a 40-Bit Dedicated Adder for Non-Pipelined Single-Cycle Multiply/Accumulate (MAC) Operation**
- **Compare, Select, and Store Unit (CSSU) for the Add/Compare Selection of the Viterbi Operator**
- **Exponent Encoder to Compute an Exponent Value of a 40-Bit Accumulator Value in a Single Cycle**
- **Two Address Generators With Eight Auxiliary Registers and Two Auxiliary Register Arithmetic Units (ARAUs)**
- **Data Bus With a Bus-Holder Feature**
- **Extended Addressing Mode for 8M × 16-Bit Maximum Addressable External Program Space**
- **16K x 16-Bit On-Chip ROM**
- **32K x 16-Bit Dual-Access On-Chip RAM**
- **Single-Instruction-Repeat and Block-Repeat Operations for Program Code**
- **Block-Memory-Move Instructions for Better Program and Data Management**
- **Instructions With a 32-Bit Long Word Operand**
- **Instructions With Two- or Three-Operand Reads**
- **Arithmetic Instructions With Parallel Store and Parallel Load**
- **Conditional Store Instructions**
- **Fast Return From Interrupt**
- **On-Chip Peripherals**
  - **Software-Programmable Wait-State Generator and Programmable Bank Switching**
  - **On-Chip Phase-Locked Loop (PLL) Clock Generator With Internal Oscillator or External Clock Source**
  - **Three Multichannel Buffered Serial Ports (McBSPs)**
  - **Enhanced 8-Bit Parallel Host-Port Interface With 16-Bit Data/Addressing**
  - **One 16-Bit Timer**
  - **Six-Channel Direct Memory Access (DMA) Controller**
- **Power Consumption Control With IDLE1, IDLE2, and IDLE3 Instructions With Power-Down Modes**
- **CLKOUT Off Control to Disable CLKOUT**
- **On-Chip Scan-Based Emulation Logic, IEEE Std 1149.1[†] (JTAG) Boundary Scan Logic**
- **12.5-ns Single-Cycle Fixed-Point Instruction Execution Time (80 MIPS) for 3.3-V Power Supply (1.8-V Core)**
- **10-ns Single-Cycle Fixed-Point Instruction Execution Time (100 MIPS) for 3.3-V Power Supply (1.8-V Core)**
- **Available in a 144-Pin Plastic Thin Quad Flatpack (TQFP) (PGE Suffix) and a 144-Pin Ball Grid Array (BGA) (GGU Suffix)**

[†] IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.

15	14	12	11	9	8
XPA	**I/O**		**DATA**		**DATA**
R/W-0	**R/W-111**		**R/W-111**		

7	6	5	3	2	0
DATA		**PROGRAM**		**PROGRAM**	
R/W−111		**R/W−111**		**R/W−111**	

LEGEND: R = Read, W = Write, *n* = value present after reset

Figure 3−2. Software Wait-State Register (SWWSR) [Memory-Mapped Register (MMR) Address 0028h]

Table 3−1. Software Wait-State Register (SWWSR) Bit Fields

BIT NO.	BIT NAME	RESET VALUE	FUNCTION
15	XPA	0	Extended program address control bit. XPA is used in conjunction with the program space fields (bits 0 through 5) to select the address range for program space wait states.
14−12	I/O	1	I/O space. The field value (0−7) corresponds to the base number of wait states for I/O space accesses within addresses 0000−FFFFh. The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states.
11−9	Data	1	Upper data space. The field value (0−7) corresponds to the base number of wait states for external data space accesses within addresses 8000−FFFFh. The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states.
8−6	Data	1	Lower data space. The field value (0−7) corresponds to the base number of wait states for external data space accesses within addresses 0000−7FFFh. The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states.
5−3	Program	1	Upper program space. The field value (0−7) corresponds to the base number of wait states for external program space accesses within the following addresses: ☐ XPA = 0: x8000 − xFFFFh ☐ XPA = 1: The upper program space bit field has no effect on wait states. The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states.
2−0	Program	1	Program space. The field value (0−7) corresponds to the base number of wait states for external program space accesses within the following addresses: ☐ XPA = 0: x0000−x7FFFh ☐ XPA = 1: 00000−FFFFFh The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states.

The software wait-state multiplier bit of the software wait-state configuration register is used to extend the base number of wait states selected by the SWWSR. The SWCR bit fields are shown in Figure 3−3 and described in Table 3−2.

15 – 8
Reserved
R/W-0

7 – 1	0
Reserved	**SWSM**
R/W-0	**R/W–0**

LEGEND: R = Read, W = Write, *n* = value present after reset

Figure 3–3. Software Wait-State Configuration Register (SWCR) [MMR Address 002Bh]

Table 3–2. Software Wait-State Configuration Register (SWCR) Bit Fields

PIN		RESET VALUE	FUNCTION
NO.	**NAME**		
15–1	Reserved	0	These bits are reserved and are unaffected by writes.
0	SWSM	0	Software wait-state multiplier. Used to multiply the number of wait states defined in the SWWSR by a factor of 1 or 2. ☐ SWSM = 0: wait-state base values are unchanged (multiplied by 1). ☐ SWSM = 1: wait-state base values are multiplied by 2 for a maximum of 14 wait states.

3.1.2 Programmable Bank-Switching Wait States

The programmable bank-switching logic of the 5409 is functionally equivalent to that of the 548/549 devices. This feature automatically inserts one cycle when accesses cross memory-bank boundaries within program or data memory space. A bank-switching wait state can also be automatically inserted when accesses cross the data space boundary into program space.

The bank-switching control register (BSCR) defines the bank size for bank-switching wait-states. Figure 3–4 shows the BSCR and its bits are described in Table 3–3.

15 – 12	11	10 – 8
BNKCMP	**PS–DS**	**Reserved**
R/W-1111	**R/W–1**	**R–0**

7 – 3	2	1	0
Reserved	**HBH**	**BH**	**EXIO**
R–0	**R/W-0**	**R/W-0**	**R/W-0**

LEGEND: R = Read, W = Write, *n* = value present after reset

Figure 3–4. Bank-Switching Control Register (BSCR) [MMR Address 0029h]

Table 3–3. Bank-Switching Control Register Fields

BIT		RESET VALUE	FUNCTION
NO.	**NAME**		
15–12	BNKCMP	1111	Bank compare. BNKCMP determines the external memory-bank size. BNKCMP is used to mask the four MSBs of an address. For example, if BNKCMP = 1111b, the four MSBs (bits 12–15) are compared, resulting in a bank size of 4K words. Bank sizes of 4K words to 64K words are allowed.
11	PS-DS	1	Program read – data read access. PS-DS inserts an extra cycle between consecutive accesses of program read and data read or data read and program read. PS-DS = 0 No extra cycles are inserted by this feature. PS-DS = 1 One extra cycle is inserted between consecutive data and program reads.
10–3	Reserved	0	These bits are reserved and are unaffected by writes.
2	HBH	0	HPI bus holder. HBH controls the HPI bus holder feature. HBH is cleared to 0 at reset. **8-bit Mode** HBH = 0 The bus holder is disabled for the HPI data bus (HD[7:0]). HBH = 1 The bus holders are enabled on HD[7:0]. When not driven, the HPI data bus (HD[7:0]) is held in the previous logic level.
			HPI bus holder. HBH controls the HPI bus holder feature. HBH is cleared to 0 at reset. **16-bit Mode** HBH = 0 The bus holder is disabled for the HPI address bus (HA[15:0]). The HPI GPIO pins (HD[7:0]) are held in the previous logic level. HBH = 1 The bus holders are enabled on HA[15:0]. When not driven, the HPI address bus (A[15:0]) and HPI GPIO pins (HD[7:0]) are held in the previous logic level.
1	BH	0	Bus holder. BH controls the data bus holder feature. BH is cleared to 0 at reset. BH = 0 The bus holder is disabled. BH = 1 The bus holder is enabled. When not driven, the data bus (D[15:0]) is held in the previous logic level.
0	EXIO	0	External bus interface off. The EXIO bit controls the external bus-off function. EXIO = 0 The external bus interface functions as usual. EXIO = 1 The address bus, data bus, and control signals become inactive after completing the current bus cycle. Note that the DROM, MP/$\overline{\text{MC}}$, and OVLY bits in the PMST and the HM bit of ST1 cannot be modified when the interface is disabled.

3.1.3 CPU Memory-Mapped Registers

The 5409 has 27 memory-mapped CPU registers, which are mapped in data memory space addresses 0h to 1Fh.

Table 3–4. CPU Memory-Mapped Registers

NAME	ADDRESS		DESCRIPTION
	DEC	HEX	
IMR	0	0	Interrupt mask register
IFR	1	1	Interrupt flag register
–	2–5	2–5	Reserved for testing
ST0	6	6	Status register 0
ST1	7	7	Status register 1
AL	8	8	Accumulator A low word (15–0)
AH	9	9	Accumulator A high word (31–16)
AG	10	A	Accumulator A guard bits (39–32)
BL	11	B	Accumulator B low word (15–0)
BH	12	C	Accumulator B high word (31–16)
BG	13	D	Accumulator B guard bits (39–32)
TREG	14	E	Temporary register
TRN	15	F	Transition register
AR0	16	10	Auxiliary register 0
AR1	17	11	Auxiliary register 1
AR2	18	12	Auxiliary register 2
AR3	19	13	Auxiliary register 3
AR4	20	14	Auxiliary register 4
AR5	21	15	Auxiliary register 5
AR6	22	16	Auxiliary register 6
AR7	23	17	Auxiliary register 7
SP	24	18	Stack pointer register
BK	25	19	Circular buffer size register
BRC	26	1A	Block repeat counter
RSA	27	1B	Block repeat start address
REA	28	1C	Block repeat end address
PMST	29	1D	Processor mode status (PMST) register
XPC	30	1E	Extended program page register
–	31	1F	Reserved

3.2.2 On-Chip ROM With Bootloader

A bootloader is available in the standard 5409 on-chip ROM. This bootloader can be used to automatically transfer user code from an external source to anywhere in the program memory at power up. If the MP/$\overline{\text{MC}}$ pin is sampled low during a hardware reset, execution begins at location FF80h of the on-chip ROM. This location contains a branch instruction to the start of the bootloader program. The standard 5409 bootloader provides different ways to download the code to accommodate various system requirements:

- Parallel from 8-bit or 16-bit-wide EPROM
- Parallel from I/O space 8-bit or 16-bit mode
- Serial boot from serial ports 8-bit or 16-bit mode
- Host-port interface boot
- SPI serial EEPROM 8-bit boot mode

The standard on-chip ROM layout is shown in Table 3−5.

Table 3−5. Standard On-Chip ROM Layout†

ADDRESS RANGE	DESCRIPTION
0x0000h − 0xBFFFh	External program space
0xC000h − 0xF7FFh	Reserved
0xF800h − 0xFBFFh	Bootloader
0xFC00h − 0xFEFFh	Reserved
0xFF00h − 0xFF7Fh	Reserved†
0xFF80h − 0xFFFFh	Interrupt vector table

† In the VC5409 ROM, 128 words are reserved for factory device-testing purposes. Application code to be implemented in on-chip ROM must reserve these 128 words at addresses FF00h–FF7Fh in program space.

3.2.3 On-Chip RAM

The 5409 device contains 32K × 16-bit of on-chip dual-access RAM (DARAM). The DARAM is composed of four blocks of 8K words each. Each block in the DARAM can support two reads in one cycle, or a read and a write in one cycle. The DARAM is located in the address range 0080h−7FFFh in data space, and can be mapped into program/data space by setting the OVLY bit to one.

3.2.4 On-Chip Memory Security

The 5409 features a 16K-word × 16-bit on-chip maskable ROM.

Customers can arrange to have the ROM of the 5409 programmed with contents unique to any particular application. A security option is available to protect a custom ROM. The ROM and ROM/RAM security options are available on the 5409. These security options are described in the *TMS320C54x DSP Reference Set, Volume 1: CPU and Peripherals* (literature number SPRU131). When the security options are enabled, JTAG emulation is inhibited or nonfunctional.

3.2.5 Relocatable Interrupt Vector Table

The reset, interrupt, and trap vectors are addressed in program space. These vectors are soft — meaning that the processor, when taking the trap, loads the program counter (PC) with the trap address and executes the code at the vector location. Four words are reserved at each vector location to accommodate a delayed branch instruction, either two 1-word instructions or one 2-word instruction, which allows branching to the appropriate interrupt service routine with minimal overhead.

At device reset, the reset, interrupt, and trap vectors are mapped to address FF80h in program space. However, these vectors can be remapped to the beginning of any 128-word page in program space after device reset. This is done by loading the interrupt vector pointer (IPTR) bits in the PMST register with the appropriate 128-word page boundary address. After loading IPTR, any user interrupt or trap vector is mapped to the new 128-word page.

NOTE: The hardware reset ($\overline{\text{RS}}$) vector cannot be remapped because a hardware reset loads the IPTR with 1s. Therefore, the reset vector is always fetched at location FF80h in program space.

3.2.6 Extended Program Memory

The 5409 CPU uses a paged extended memory scheme in program space to allow access of up to 8M program memory locations. In order to implement this scheme, the 5409 includes several features that are also present on the 548/549 devices:

- Twenty-three address lines, instead of sixteen
- An extra memory-mapped register, the XPC register defines the page selection. This register is memory-mapped into data space to address 001Eh. At a hardware reset, the XPC is initialized to 0.
- Six extra instructions for addressing extended program space. These six instructions affect the XPC.
  - *FB[D]* pmad (23 bits) – Far branch
  - *FBACC[D]* Accu[22:0] – Far branch to the location specified by the value in accumulator A or accumulator B
  - *FCALL[D]* pmad (23 bits) – Far call
  - *FCALA[D]* Accu[22:0] – Far call to the location specified by the value in accumulator A or accumulator B
  - *FRET[D]* – Far return
  - *FRETE[D]* – Far return with interrupts enabled
- In addition to these new instructions, two 54x instructions are extended to use 23 bits in the 5409:
  - READA data_memory (using 23-bit accumulator address)
  - WRITA data_memory (using 23-bit accumulator address)

All other instructions, software interrupts, and hardware interrupts do not modify the XPC register and access only memory within the current page.

Program memory in the 5409 is organized into 127 pages that are each 64K in length, as shown in Figure 3–6.

Table 3−7. Pin Control Register (PCR) Bit Field Description

BIT	NAME	FUNCTION
15 – 14	Reserved	Reserved. Pins are not used.
13	XIOEN	Transmit/Receive general-purpose I/O mode ONLY when $\overline{\text{XRST}}$=0 in the SPCR(1/2) XIOEN = 0 DX pin is not a general-purpose output. FSX and CLKX are not general-purpose I/Os. XIOEN = 1 DX pin is a general-purpose output. FSX and CLKX are general-purpose I/Os. These serial port pins do not perform serial port operations.
12	RIOEN	Transmit/Receive general-purpose I/O mode ONLY when $\overline{\text{RRST}}$=0 in the SPCR(1/2) RIOEN = 0 DR and CLKS pins are not general-purpose inputs. FSR and CLKR are not general-purpose I/Os. RIOEN = 1 DR and CLKS pins are general-purpose inputs. FSR and CLKR are general-purpose I/Os. These serial port pins do not perform serial port operations. The CLKS pin is affected by a combination of $\overline{\text{RRST}}$ and RIOEN signals of the receiver.
11	FSXM	Transmit frame synchronization mode FSRM = 0 Frame synchronization signal derived from an external source. FSRM = 1 Frame synchronization is determined by the sample rate generator frame synchronization mode bit (FSGM) in the SRGR2.
10	FSRM	Receive frame synchronization mode FSRM = 0 Frame synchronization pulses generated by an external device. FSR is an input pin. FSRM = 1 Frame synchronization generated internally by the sample rate generator. FSR is an output pin except when GSYNC=1 in the SRGR.
9	CLKXM	Transmitter clock mode CLKXM = 0 Receiver/transmitter clock is driven by an external clock with CLK(R/X) as an input pin CLKXM= 1 CLK(R/X) is an output pin and is driven by the internal sample rate generator During SPI mode (CLKSTP is a non-zero value): CLKXM = 0 McBSP is a slave and clock (CLKX) is driven by the SPI master in the system. CLKR is internally driven by CLKX. CLKXM= 1 McBSP is a master and generates the clock (CLKX) to drive its receive clock (CLKR) and the shift clock of the SPI-compliant slaves in the system.
8	CLKRM	Receiver clock mode Case 1: Digital loop-back mode is not set (DLB=0) in SPCR1. CLKRM = 0 Receive clock (CLKR) is an input pin driven by an external clock. CLKRM= 1 CLKR is an output pin and is driven by the internal sample rate generator Case 2: Digital loop-back mode set (DLB=1) in SPCR1 CLKRM = 0 Receive clock (*Not* the CLKR pin) is driven by transmit clock (CLKX), which is based on CLKXM bit in the PCR. CLKR pin is in high-impedance mode. CLKRM= 1 CLKR is an output pin and is driven by the transmit clock. The transmit clock is derived based on the CLKXM bit in the PCR.
7	SCLKME	Sample rate clock mode extended SCLKME = 0 External clock via CLKS or CPU clock is used as a reference by the sample rate generator. SCLKME = 1 External clock via CLKR or CLKX clock is used as a reference by the sample rate generator.
6	CLKS STAT	CLKS pin status. CLKS STAT reflects value on CLKS pin when selected as a general-purpose input.

Table 3−7. Pin Control Register (PCR) Bit Field Description (Continued)

BIT	NAME	FUNCTION
5	DX STAT	DX pin status. DX STAT reflects value on DX pin when it is selected as a general-purpose output.
4	DR STAT	DR pin status. DR STAT reflects value on DR pin when it is selected as a general-purpose input.
3 2	FSXP FSRP	Receive/Transmit frame synchronization polarity. FS(R/X)P = 0 Frame synchronization pulse FS(R/X) is active high FS(R/X)P = 1 Frame synchronization pulse FS(R/X) is active low
1	CLKXP	Transmit clock polarity CLKXP = 0 Transmit data sampled on rising edge of CLKR CLKXP = 1 Transmit data sampled on falling edge of CLKR
0	CLKRP	Receive clock polarity CLKRP = 0 Receive data sampled on falling edge of CLKR CLKRP = 1 Receive data sampled on rising edge of CLKR

3.3.2.1 Sample Rate Generator

The 5409 sample rate generator has four clock input options that are only available when both the PCR and SRGR2 are used. Table 3−8 shows the sample rate generator clock input options.

Table 3−8. Sample Rate Generator Clock Input Options

MODE	SCLKME (PCR.7)	CLKSM (SRGR2.13)
CLKS pin	0	0
CPU	0	1
CLKR pin	1	0
CLKX pin	1	1

15	14	13	12	11 8
GSYNC	CLKSP	CLKSM	FSGM	FPER
R/W-0	R/W	R/W	R/W	R/W

7 0
FPER
R/W

LEGEND: R = Read, W = Write, *n* = value present after reset

Figure 3−9. Sample Rate Generator Register 2 (SRGR2)

Table 3−9. Sample Rate Generator Register 2 (SRGR2) Bit Field Descriptions

BIT	NAME	FUNCTION
15	GSYNC	Sample rate generator clock synchronization. Only used when the external clock (CLKS) drives the sample rate generator clock (CLKSM=0) GSYNC = 0 The sample rate generator clock (CLKG) is free-running. GSYNC = 1 The sample rate generator clock (CLKG) is running. But CLKG is resynchronized and frame sync signal (FSG) is generated only after detecting the receive frame synchronization signal (FSR). Also, frame period (FPER) is a don’t care because the period is dictated by the external frame sync pulse.
14	CLKSP	CLKS polarity clock edge select. Only used when the external clock (CLKS) drives the sample rate generator clock (CLKSM=0). CLKSP = 0 Rising edge of CLKS generates CLKG and FSG. CLKSP = 1 Falling edge of CLKS generates CLKG and FSG.
13	CLKSM	McBSP sample rate generator clock mode SCLKME = 0 CLKSM = 0 Sample rate generator clock derived from the CLKS pin (in PCR) CLKSM = 1 Sample rate generator clock derived from CPU clock SCLKME = 1 CLKSM = 0 Sample rate generator clock derived from CLKR pin (in PCR) CLKSM = 1 Sample rate generator clock derived from CLKX pin
12	FSGM	Sample rate generator transmit frame synchronization mode. Used when FSXM=1 in the PCR. FSGM = 0 Transmit frame sync signal (FSX) due to DXR(1/2) copy FSGN = 1 Transmit frame sync signal driven by the sample rate generator frame sync signal (FSG)
11 − 0	FPER	Frame period. This determines when the next frame sycn signal should become active. Range: up to 2^{12}; 1 to 4096 CLKG periods.

3.3.2.2 McBSP Control Registers and Subaddresses

The control registers for the multichannel buffered serial port (McBSP) are accessed using the subbank addressing scheme. This allows a set or subbank of registers to be accessed through a single memory location. The serial port subbank address (SPSA) register is used as a pointer to select a particular register within the subbank. The serial port subbank data (SPSD) register is used to access (read or write) the selected register. Table 3−10 shows the McBSP control registers and their corresponding subaddresses.

Table 3−10. McBSP Control Registers and Subaddresses

McBSP0		McBSP1		McBSP2		SUB ADDRESS	DESCRIPTION
NAME	ADDRESS	NAME	ADDRESS	NAME	ADDRESS		
SPCR10	39h	SPCR11	49h	SPCR12	35h	00h	Serial port control register 1
SPCR20	39h	SPCR21	49h	SPCR22	35h	01h	Serial port control register 2
RCR10	39h	RCR11	49h	RCR12	35h	02h	Receive control register 1
RCR20	39h	RCR21	49h	RCR22	35h	03h	Receive control register 2
XCR10	39h	XCR11	49h	XCR12	35h	04h	Transmit control register 1
XCR20	39h	XCR21	49h	XCR22	35h	05h	Transmit control register 2
SRGR10	39h	SRGR11	49h	SRGR12	35h	06h	Sample rate generator register 1
SRGR20	39h	SRGR21	49h	SRGR22	35h	07h	Sample rate generator register 2
MCR10	39h	MCR11	49h	MCR12	35h	08h	Multichannel register 1
MCR20	39h	MCR21	49h	MCR22	35h	09h	Multichannel register 2
RCERA0	39h	RCERA1	49h	RCERA2	35h	0Ah	Receive channel enable register partition A
RCERB0	39h	RCERB1	49h	RCERB2	35h	0Bh	Receive channel enable register partition B
XCERA0	39h	XCERA1	49h	XCERA2	35h	0Ch	Transmit channel enable register partition A
XCERB0	39h	XCERB1	49h	XCERB2	35h	0Dh	Transmit channel enable register partition B
PCR0	39h	PCR1	49h	PCR2	35h	0Eh	Pin control register

3.3.3 Hardware Timer

The 5409 device features one 16-bit timing circuit with a 4-bit prescaler. The main counter of each timer is decremented by one every CPU clock cycle. Each time the counter decrements to 0, a timer interrupt is generated. The timer can be stopped, restarted, reset, or disabled by specific control bits.

3.3.4 Clock Generator

The clock generator provides clocks to the 5409 device, and consists of an internal oscillator and a phase-locked loop (PLL) circuit. The clock generator requires a reference clock input, which can be provided by using a crystal resonator with the internal oscillator, or from an external clock source. The reference clock input is then divided by two (DIV mode) to generate clocks for the 5409 device, or the PLL circuit can be used (PLL mode) to generate the device clock by multiplying the reference clock frequency by a scale factor, allowing use of a clock source with a lower frequency than that of the CPU.The PLL is an adaptive circuit that, once synchronized, locks onto and tracks an input clock signal.

When the PLL is initially started, it enters a transitional mode during which the PLL acquires lock with the input signal. Once the PLL is locked, it continues to track and maintain synchronization with the input signal. Then, other internal clock circuitry allows the synthesis of new clock frequencies for use as master clock for the 5409 device.

This clock generator allows system designers to select the clock source. The sources that drive the clock generator are:

- A crystal resonator circuit. The crystal resonator circuit is connected across the X1 and X2/CLKIN pins of the 5409 to enable the internal oscillator.
- An external clock. The external clock source is directly connected to the X2/CLKIN pin, and X1 is left unconnected.

The software-programmable PLL features a high level of flexibility, and includes a clock scaler that provides various clock multiplier ratios, capability to directly enable and disable the PLL, and a PLL lock timer that can be used to delay switching to PLL clocking mode of the device until lock is achieved. Devices that have a built-in software-programmable PLL can be configured in one of two clock modes:

- PLL mode. The input clock (X2/CLKIN) is multiplied by 1 of 31 possible ratios. These ratios are achieved using the PLL circuitry.
- DIV (divider) mode. The input clock is divided by 2 or 4. Note that when DIV mode is used, the PLL can be completely disabled in order to minimize power dissipation.

The software-programmable PLL is controlled using the 16-bit memory-mapped (address 0058h) clock mode register (CLKMD). The CLKMD register is used to define the clock configuration of the PLL clock module. Upon reset, the CLKMD register is initialized with a predetermined value dependent only upon the state of the CLKMD1 − CLKMD3 pins as shown in Table 3−11.

Table 3−11. Clock Mode Settings at Reset

CLKMD1	CLKMD2	CLKMD3	CLKMD RESET VALUE	CLOCK MODE
0	0	0	E007h	PLL x 15
0	0	1	9007h	PLL x 10
0	1	0	4007h	PLL x 5
1	0	0	1007h	PLL x 2
1	1	0	F007h	PLL x 1
1	1	1	0000h	1/2 (PLL disabled)
1	0	1	F000h	1/4 (PLL disabled)
0	1	1	—	Reserved

Table 5–34. HPI16 Mode Switching Characteristics[†‡§¶]

PARAMETER			MIN	MAX	UNIT
$t_{\text{en(DSL-HD)}}$	Enable time, Dx driven from DS low		6	19	ns
$t_{\text{d(DSL-HDV1)}}$	Delay time, DS low to Dx valid for an HPI read	Case 1a: Memory accesses when DMAC is active in 16-bit mode and $t_{\text{w(DSH)}} < 18\text{H}$		$18\text{H}+19 - t_{\text{w(DSH)}}$	ns
		Case 1b: Memory accesses when DMAC is active in 16-bit mode and $t_{\text{w(DSH)}} \geq 18\text{H}$		19	
		Case 2a: Memory accesses when DMAC is inactive and $t_{\text{w(DSH)}} < 10\text{H}$		$10\text{H}+19 - t_{\text{w(DSH)}}$	
		Case 2b: Memory accesses when DMAC is inactive and $t_{\text{w(DSH)}} \geq 10\text{H}$		19	
		Case 3: Register accesses		19	
$t_{\text{h(DSH-HDV)R}}$	Hold time, Dx valid after DS rising edge, read		1	8	ns
$t_{\text{v(HYH-HDV)}}$	Valid time, Dx valid before HRDY rising edge		0	6	ns
$t_{\text{d(DSH-HYL)}}$	Delay time, DS or $\overline{\text{HCS}}$ high to HRDY low			10	ns
$t_{\text{d(DSH-HYH)}}$	Delay time, DS high to HRDY high (writes and autoincrement reads)	Case 1: Memory access when DMAC is active in 16-bit mode		18H+10	ns
		Case 2: Memory access when DMAC is inactive		10H+10	
$t_{\text{d(DSL-HYL)}}$	Delay time, HDS or $\overline{\text{HCS}}$ low/high to HRDY low/high			10	ns
$t_{\text{d(COH–HYH)}}$	Delay time, CLKOUT high to HRDY high			2	ns

NOTE: The HRDY output is always high when the $\overline{\text{HCS}}$ input is high, regardless of DS timings.

[†] DS refers to the logical OR of $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$, or $\overline{\text{HDS2}}$.

[‡] Dx refers to any of the DPI data bus pins (D0, D1, D2, etc.).

[§] DMAC stands for direct memory access (DMA) controller. The HPI16 shares the internal DMA bus with the DMAC, thus HPI16 access times are affected by DMAC activity.

[¶] GPIO refers to the HD pins when they are configured as general-purpose input/outputs.

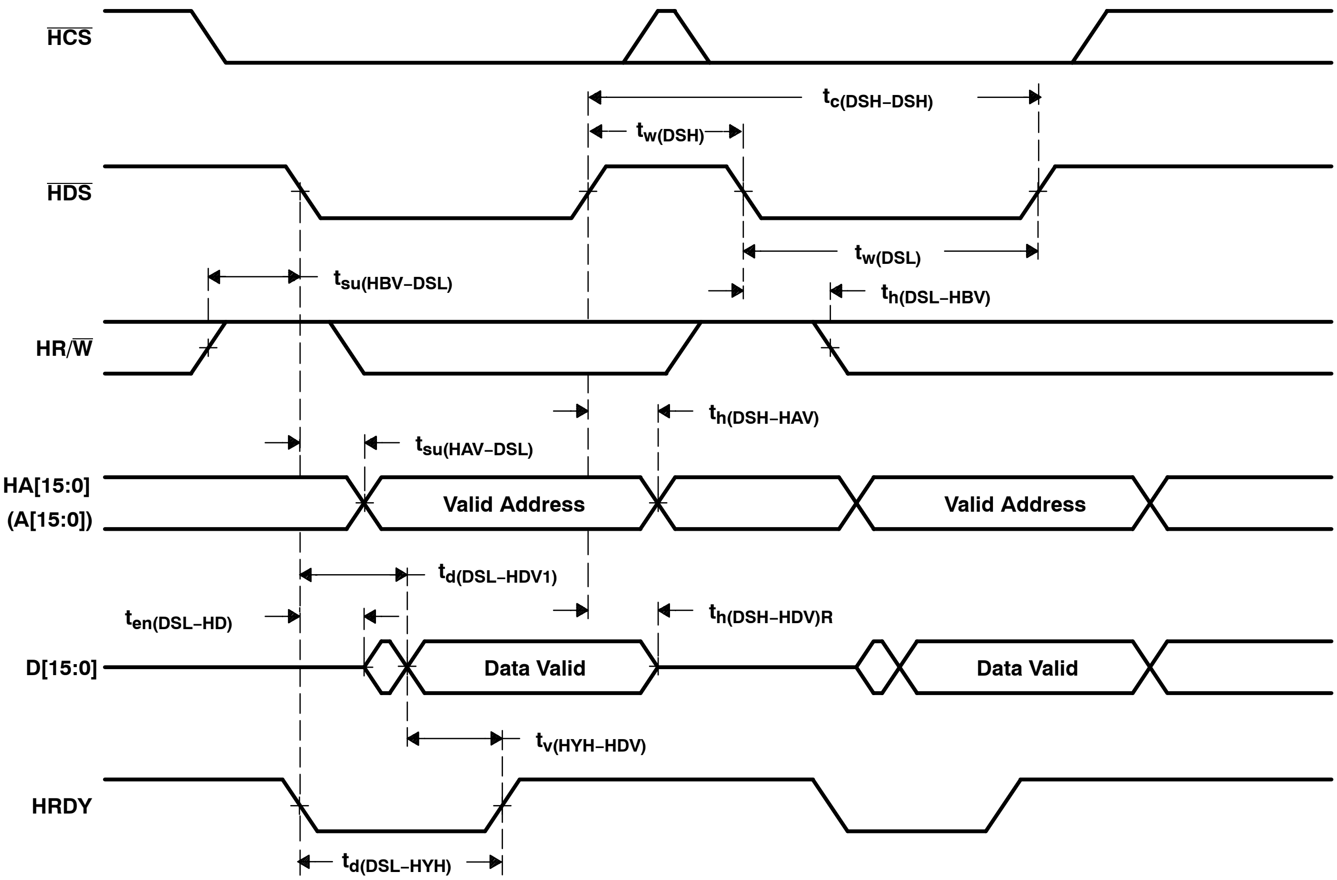


Figure 5−31. Nonmultiplexed Read Timings

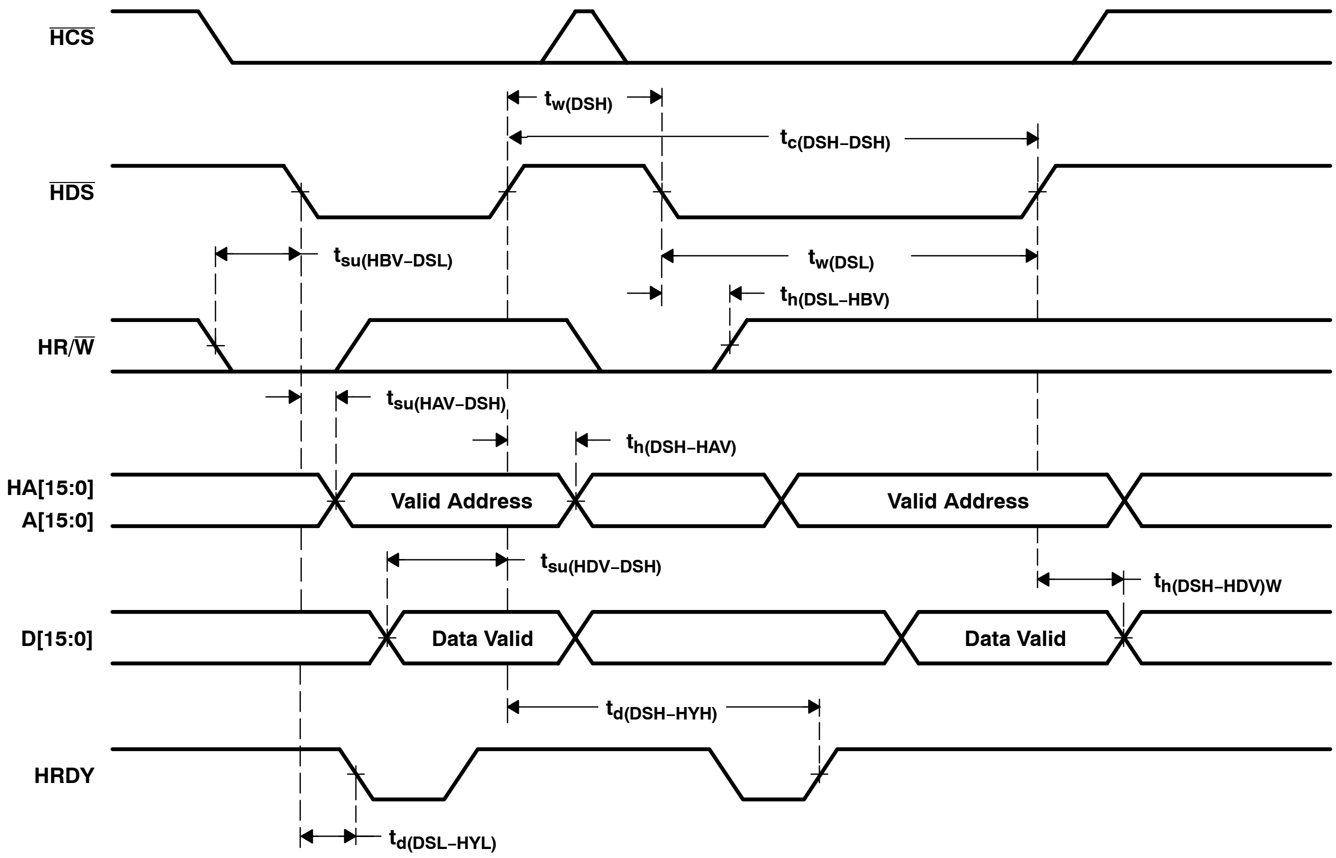


Figure 5−32. Nonmultiplexed Write Timings

5.15 GPIO Timing Requirements

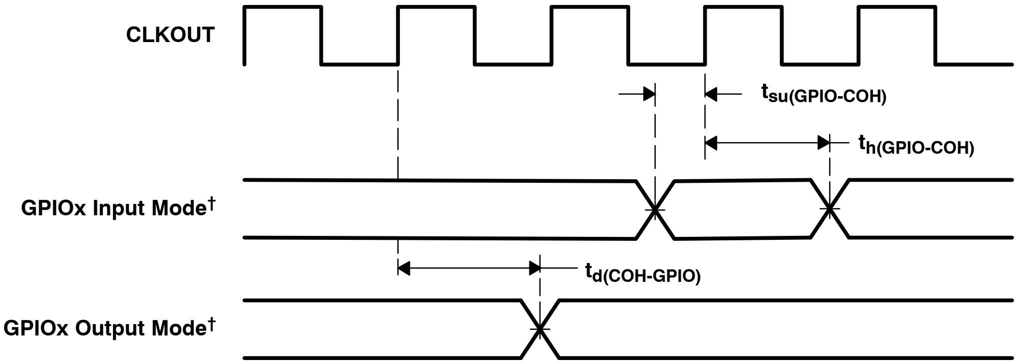
Table 5−35 to Table 5−36 assume testing over recommended operating conditions (see Figure 5−33).

Table 5−35. GPIO Timing Requirements

		MIN	MAX	UNIT
$t_{su(GPIO-COH)}$	Setup time, GPIOx input valid before CLKOUT high, GPIOx configured as general-purpose input.	7		ns
$t_{h(GPIO-COH)}$	Hold time, GPIOx input valid after CLKOUT high, GPIOx configured as general-purpose input.	0		ns

Table 5−36. GPIO Switching Characteristics

PARAMETER		MIN	MAX	UNIT
$t_{d(COH-GPIO)}$	Delay time, CLKOUT high to GPIOx output change. GPIOx configured as general-purpose output.	0	6	ns



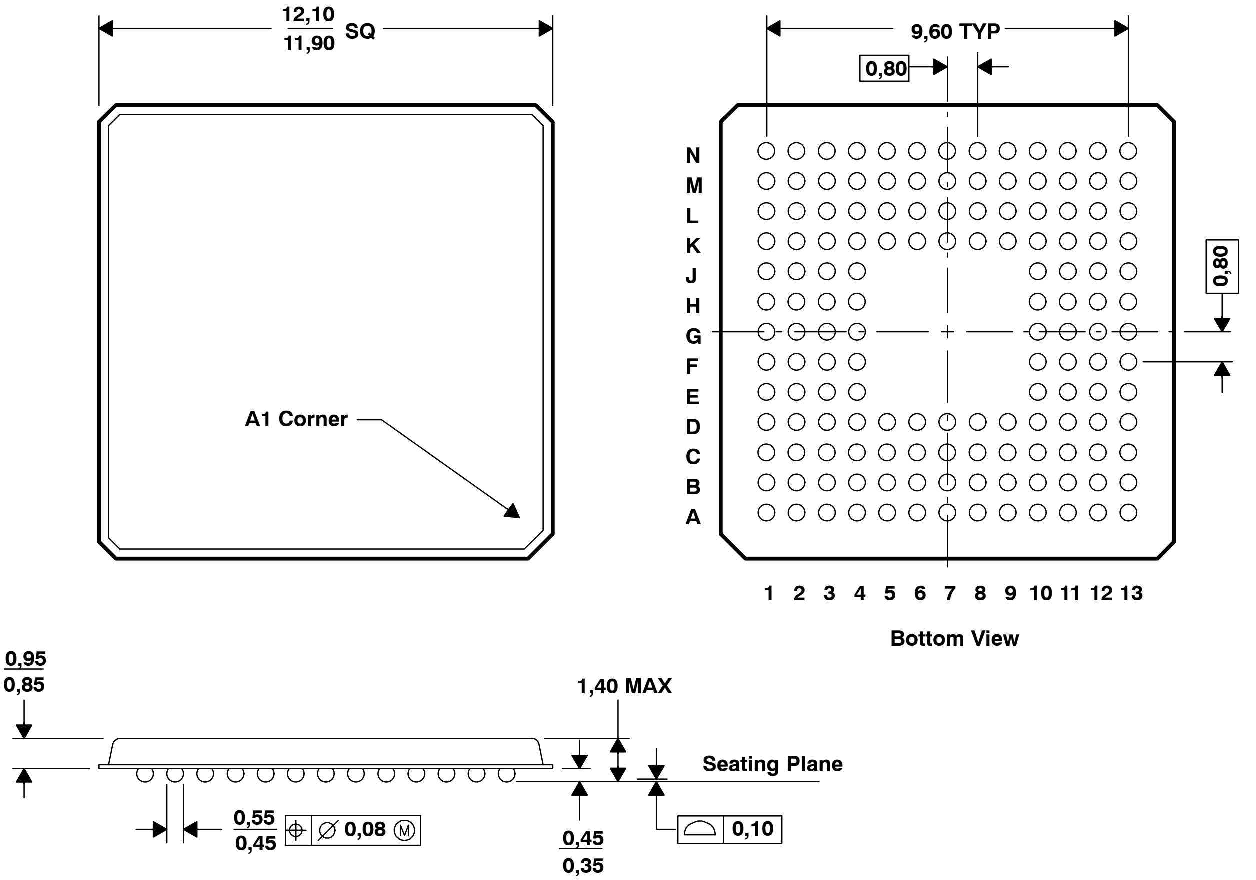
† GPIOx refers to HD0, HD1, HD2, ...HD7, when the HD bus is configured for general-purpose input/output (I/O).

Figure 5−33. GPIOx† Timings

6 Mechanical Data

6.1 Ball Grid Array Mechanical Data

GGU (S–PBGA–N144) **PLASTIC BALL GRID ARRAY**



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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice
C. MicroStar BGA™ configuration

Figure 6–1. TMS320VC5416 144-Ball Plastic Ball Grid Array Package (GGU)

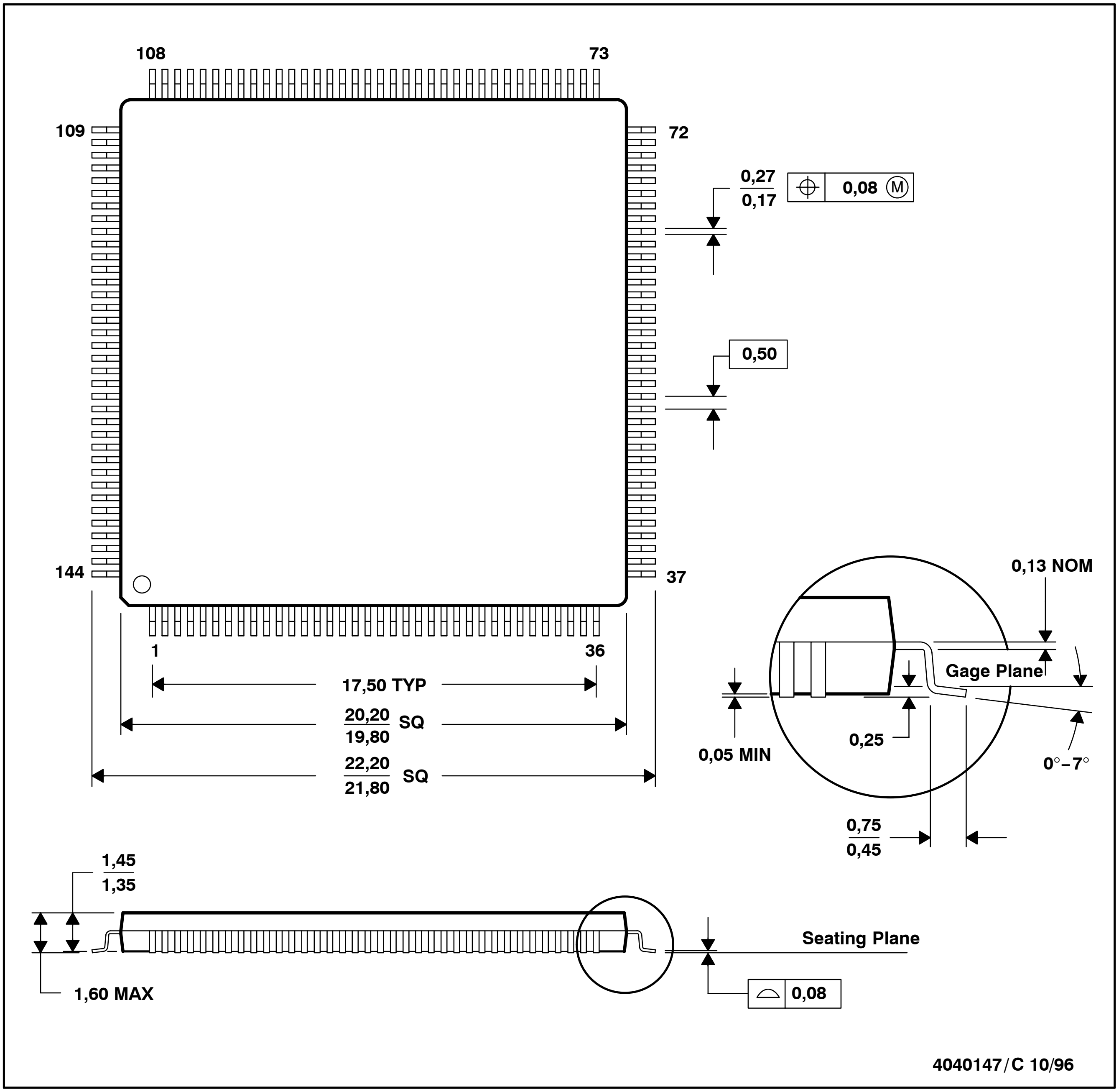
Table 6–1. Thermal Resistance Characteristics for 144-Ball GGU Package

PARAMETER	°C/W
$R_{\Theta JA}$	56
$R_{\Theta JC}$	5

MicroStar BGA is a trademark of Texas Instruments.

6.2 Low-Profile Quad Flatpack Mechanical Data

PGE (S-PQFP-G144) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

Figure 6–2. TMS320VC5416 144-Pin Low-Profile Quad Flatpack (PGE)

Table 6–2. Thermal Resistance Characteristics for 144-Ball PGE Package

PARAMETER	°C/W
$R_{\Theta JA}$	38
$R_{\Theta JC}$	5

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TMS320VC5409GGU-80	ACTIVE	BGA	GGU	144	160	TBD	SNPB	Level-3-220C-168HR
TMS320VC5409GGU100	ACTIVE	BGA	GGU	144	160	TBD	SNPB	Level-3-220C-168HR
TMS320VC5409PGE-80	ACTIVE	LQFP	PGE	144	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TMS320VC5409PGE100	ACTIVE	LQFP	PGE	144	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TMS320VC5409ZGU100	ACTIVE	BGA	ZGU	144	160	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168HR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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