- **Advanced Multibus Architecture With Three Separate 16-Bit Data Memory Buses and One Program Memory Bus**
- **40-Bit Arithmetic Logic Unit (ALU), Including a 40-Bit Barrel Shifter and Two Independent 40-Bit Accumulators**
- **17- × 17-Bit Parallel Multiplier Coupled to a 40-Bit Dedicated Adder for Non-Pipelined Single-Cycle Multiply/Accumulate (MAC) Operation**
- **Compare, Select, and Store Unit (CSSU) for the Add/Compare Selection of the Viterbi Operator**
- **Exponent Encoder to Compute an Exponent Value of a 40-Bit Accumulator Value in a Single Cycle**
- **Two Address Generators With Eight Auxiliary Registers and Two Auxiliary Register Arithmetic Units (ARAUs)**
- **Data Bus With a Bus-Holder Feature**
- **Extended Addressing Mode for 1M × 16-Bit Maximum Addressable External Program Space**
- **4K x 16-Bit On-Chip ROM**
- **16K x 16-Bit Dual-Access On-Chip RAM**
- **Single-Instruction-Repeat and Block-Repeat Operations for Program Code**
- **Block-Memory-Move Instructions for Efficient Program and Data Management**
- **Instructions With a 32-Bit Long Word Operand**
- **Instructions With Two- or Three-Operand Reads**
- **Arithmetic Instructions With Parallel Store and Parallel Load**
- **Conditional Store Instructions**
- **Fast Return From Interrupt**
- **On-Chip Peripherals**
  - **Software-Programmable Wait-State Generator and Programmable Bank Switching**
  - **On-Chip Phase-Locked Loop (PLL) Clock Generator With Internal Oscillator or External Clock Source**
  - **Two Multichannel Buffered Serial Ports (McBSPs)**
  - **Enhanced 8-Bit Parallel Host-Port Interface (HPI8)**
  - **Two 16-Bit Timers**
  - **Six-Channel Direct Memory Access (DMA) Controller**
- **Power Consumption Control With IDLE1, IDLE2, and IDLE3 Instructions With Power-Down Modes**
- **CLKOUT Off Control to Disable CLKOUT**
- **On-Chip Scan-Based Emulation Logic, IEEE Std 1149.1† (JTAG) Boundary Scan Logic**
- **10-ns Single-Cycle Fixed-Point Instruction Execution Time (100 MIPS) for 3.3-V Power Supply (1.8-V Core)**
- **Available in a 144-Pin Plastic Low-Profile Quad Flatpack (LQFP) (PGE Suffix) and a 144-Pin Ball Grid Array (BGA) (GGU Suffix)**

NOTE: This data sheet is designed to be used in conjunction with the *TMS320C5000 DSP Family Functional Overview* (literature number SPRU307).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.

TABLE OF CONTENTS

Description 3
Pin Assignments 6
Terminal Functions 7
Memory 12
On-Chip Peripherals 16
Software-Programmable Wait-State Generator 16
Programmable Bank-Switching Wait States 18
Parallel I/O Ports 19
Enhanced 8-Bit Host-Port Interface 19
Multichannel Buffered Serial Ports 20
Hardware Timer 21
Clock Generator 21
DMA Controller 23
Memory-Mapped Registers 27
McBSP Control Registers And Subaddresses 29
DMA Subbank Addressed Registers 29
Interrupts 31
Documentation Support 33
Absolute Maximum Ratings 34
Recommended Operating Conditions 34
Electrical Characteristics 35
Parameter Measurement Information 35
Internal Oscillator With External Crystal 36
Divide-By-Two Clock Option (PLL Disabled) 37
Multiply-By-N Clock Option 38
Memory and Parallel I/O Interface Timing 39
Ready Timing For Externally Generated Wait States 45
HOLD and HOLDA Timings 49
Reset, BIO, Interrupt, and MP/MC Timings 50
Instruction Acquisition (IAQ), Interrupt Acknowledge (IACK), External Flag (XF), and TOUT Timings 52
Multichannel Buffered Serial Port Timing 54
HPI8 Timing 61
Mechanical Data 65

REVISION HISTORY

REVISION	DATE	PRODUCT STATUS	HIGHLIGHTS
*	October 1998	Advanced Information	Original
A	April 1999	Advanced Information	Revised to update characteristic data
B	July 1999	Advanced Information	Revised to update characteristic data
C	September 1999	Advanced Information	Revised to update characteristic data
D	January 2000	Production Data	Revised to release production data.
E	August 2000	Production Data	Added Table of Contents, Revision History, and corrected IDLE3 current on page 35.

description

The TMS320VC5402 fixed-point, digital signal processor (DSP) (hereafter referred to as the ’5402 unless otherwise specified) is based on an advanced modified Harvard architecture that has one program memory bus and three data memory buses. This processor provides an arithmetic logic unit (ALU) with a high degree of parallelism, application-specific hardware logic, on-chip memory, and additional on-chip peripherals. The basis of the operational flexibility and speed of this DSP is a highly specialized instruction set.

Separate program and data spaces allow simultaneous access to program instructions and data, providing the high degree of parallelism. Two read operations and one write operation can be performed in a single cycle. Instructions with parallel store and application-specific instructions can fully utilize this architecture. In addition, data can be transferred between data and program spaces. Such parallelism supports a powerful set of arithmetic, logic, and bit-manipulation operations that can be performed in a single machine cycle. In addition, the ’5402 includes the control mechanisms to manage interrupts, repeated operations, and function calls.

terminal functions

The following table lists each signal, function, and operating mode(s) grouped by function.

Terminal Functions

TERMINAL NAME	TYPE†	DESCRIPTION
DATA SIGNALS		
A19 (MSB) A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 (LSB)	O/Z	Parallel address bus A19 [most significant bit (MSB)] through A0 [least significant bit (LSB)]. The lower sixteen address pins (A0 to A15) are multiplexed to address all external memory (program, data) or I/O, while the upper four address pins (A16 to A19) are only used to address external program space. These pins are placed in the high-impedance state when the hold mode is enabled, or when $\overline{\text{OFF}}$ is low.
D15 (MSB) D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 (LSB)	I/O/Z	Parallel data bus D15 (MSB) through D0 (LSB). The sixteen data pins (D0 to D15) are multiplexed to transfer data between the core CPU and external data/program memory or I/O devices. The data bus is placed in the high-impedance state when not outputting or when $\overline{\text{RS}}$ or $\overline{\text{HOLD}}$ is asserted. The data bus also goes into the high-impedance state when $\overline{\text{OFF}}$ is low. The data bus has bus holders to reduce the static power dissipation caused by floating, unused pins. These bus holders also eliminate the need for external bias resistors on unused pins. When the data bus is not being driven by the ’5402, the bus holders keep the pins at the previous logic level. The data bus holders on the ’5402 are disabled at reset and can be enabled/disabled via the BH bit of the bank-switching control register (BSCR).
INITIALIZATION, INTERRUPT, AND RESET OPERATIONS		
$\overline{\text{IACK}}$	O/Z	Interrupt acknowledge signal. $\overline{\text{IACK}}$ Indicates receipt of an interrupt and that the program counter is fetching the interrupt vector location designated by A15–A0. $\overline{\text{IACK}}$ also goes into the high-impedance state when $\overline{\text{OFF}}$ is low.
$\overline{\text{INT0}}$ $\overline{\text{INT1}}$ $\overline{\text{INT2}}$ $\overline{\text{INT3}}$	I	External user interrupts. $\overline{\text{INT0}}$–$\overline{\text{INT3}}$ are prioritized and are maskable by the interrupt mask register (IMR) and the interrupt mode bit. $\overline{\text{INT0}}$ –$\overline{\text{INT3}}$ can be polled and reset by way of the interrupt flag register (IFR).
$\overline{\text{NMI}}$	I	Nonmaskable interrupt. $\overline{\text{NMI}}$ is an external interrupt that cannot be masked by way of the INTM or the IMR. When $\overline{\text{NMI}}$ is activated, the processor traps to the appropriate vector location.

† I = input, O = output, Z = high impedance, S = supply

‡ All revisions of the ’5402 can be operated with an external clock source, provided that the proper voltage levels be driven on the X2/CLKIN pin. It should be noted that the X2/CLKIN pin is referenced to the device 1.8V power supply (CV_{DD}), rather than the 3V I/O supply (DV_{DD}). Refer to the recommended operating conditions section of this document for the allowable voltage levels of the X2/CLKIN pin.

Terminal Functions (Continued)

TERMINAL NAME	TYPE†	DESCRIPTION
INITIALIZATION, INTERRUPT, AND RESET OPERATIONS (CONTINUED)		
$\overline{RS}$	I	Reset. $\overline{RS}$ causes the digital signal processor (DSP) to terminate execution and causes a reinitialization of the CPU and peripherals. When $\overline{RS}$ is brought to a high level, execution begins at location 0FF80h of program memory. $\overline{RS}$ affects various registers and status bits.
MP/$\overline{MC}$	I	Microprocessor/microcomputer mode select. If active low at reset, microcomputer mode is selected, and the internal program ROM is mapped into the upper 4K words of program memory space. If the pin is driven high during reset, microprocessor mode is selected, and the on-chip ROM is removed from program space. This pin is only sampled at reset, and the MP/$\overline{MC}$ bit of the processor mode status (PMST) register can override the mode that is selected at reset.
MULTIPROCESSING SIGNALS		
$\overline{BIO}$	I	Branch control. A branch can be conditionally executed when $\overline{BIO}$ is active. If low, the processor executes the conditional instruction. For the XC instruction, the $\overline{BIO}$ condition is sampled during the decode phase of the pipeline; all other instructions sample $\overline{BIO}$ during the read phase of the pipeline.
XF	O/Z	External flag output (latched software-programmable signal). XF is set high by the SSBX XF instruction, set low by the RSBX XF instruction or by loading ST1. XF is used for signaling other processors in multiprocessor configurations or used as a general-purpose output pin. XF goes into the high-impedance state when $\overline{OFF}$ is low, and is set high at reset.
MEMORY CONTROL SIGNALS		
$\overline{DS}$ $\overline{PS}$ $\overline{IS}$	O/Z	Data, program, and I/O space select signals. $\overline{DS}$, $\overline{PS}$, and $\overline{IS}$ are always high unless driven low for accessing a particular external memory space. Active period corresponds to valid address information. $\overline{DS}$, $\overline{PS}$, and $\overline{IS}$ are placed into the high-impedance state in the hold mode; the signals also go into the high-impedance state when $\overline{OFF}$ is low.
$\overline{MSTRB}$	O/Z	Memory strobe signal. $\overline{MSTRB}$ is always high unless low-level asserted to indicate an external bus access to data or program memory. $\overline{MSTRB}$ is placed in the high-impedance state in the hold mode; it also goes into the high-impedance state when $\overline{OFF}$ is low.
READY	I	Data ready. READY indicates that an external device is prepared for a bus transaction to be completed. If the device is not ready (READY is low), the processor waits one cycle and checks READY again. Note that the processor performs ready detection if at least two software wait states are programmed. The READY signal is not sampled until the completion of the software wait states.
R/$\overline{W}$	O/Z	Read/write signal. R/$\overline{W}$ indicates transfer direction during communication to an external device. R/$\overline{W}$ is normally in the read mode (high), unless it is asserted low when the DSP performs a write operation. R/$\overline{W}$ is placed in the high-impedance state in hold mode; it also goes into the high-impedance state when $\overline{OFF}$ is low.
$\overline{IOSTRB}$	O/Z	I/O strobe signal. $\overline{IOSTRB}$ is always high unless low-level asserted to indicate an external bus access to an I/O device. $\overline{IOSTRB}$ is placed in the high-impedance state in the hold mode; it also goes into the high-impedance state when $\overline{OFF}$ is low.
$\overline{HOLD}$	I	Hold. $\overline{HOLD}$ is asserted to request control of the address, data, and control lines. When acknowledged by the 'C54x, these lines go into the high-impedance state.
$\overline{HOLDA}$	O/Z	Hold acknowledge. $\overline{HOLDA}$ indicates that the '5402 is in a hold state and that the address, data, and control lines are in the high-impedance state, allowing the external memory interface to be accessed by other devices. $\overline{HOLDA}$ also goes into the high-impedance state when $\overline{OFF}$ is low.
$\overline{MSC}$	O/Z	Microstate complete. $\overline{MSC}$ indicates completion of all software wait states. When two or more software wait states are enabled, the $\overline{MSC}$ pin goes active at the beginning of the first software wait state and goes inactive high at the beginning of the last software wait state. If connected to the READY input, $\overline{MSC}$ forces one external wait state after the last internal wait state is completed. $\overline{MSC}$ also goes into the high-impedance state when $\overline{OFF}$ is low.
$\overline{IAQ}$	O/Z	Instruction acquisition signal. $\overline{IAQ}$ is asserted (active low) when there is an instruction address on the address bus. $\overline{IAQ}$ goes into the high-impedance state when $\overline{OFF}$ is low.

† I = input, O = output, Z = high impedance, S = supply

‡ All revisions of the '5402 can be operated with an external clock source, provided that the proper voltage levels be driven on the X2/CLKIN pin. It should be noted that the X2/CLKIN pin is referenced to the device 1.8V power supply (CV_{DD}), rather than the 3V I/O supply (DV_{DD}). Refer to the recommended operating conditions section of this document for the allowable voltage levels of the X2/CLKIN pin.

Terminal Functions (Continued)

TERMINAL NAME	TYPE†	DESCRIPTION
OSCILLATOR/TIMER SIGNALS		
CLKOUT	O/Z	Master clock output signal. CLKOUT cycles at the machine-cycle rate of the CPU. The internal machine cycle is bounded by rising edges of this signal. CLKOUT also goes into the high-impedance state when $\overline{\text{OFF}}$ is low.
CLKMD1 CLKMD2 CLKMD3	I	Clock mode select signals. These inputs select the mode that the clock generator is initialized to after reset. The logic levels of CLKMD1–CLKMD3 are latched when the reset pin is low, and the clock mode register is initialized to the selected mode. After reset, the clock mode can be changed through software, but the clock mode select signals have no effect until the device is reset again.
X2/CLKIN	I	Oscillator input. This is the input to the on-chip oscillator. If the internal oscillator is not used, X2/CLKIN functions as the clock input, and can be driven by an external clock source.‡
X1	O	Output pin from the internal oscillator for the crystal. If the internal oscillator is not used, X1 should be left unconnected. X1 does not go into the high-impedance state when $\overline{\text{OFF}}$ is low.‡
TOUT0	O/Z	Timer0 output. TOUT0 signals a pulse when the on-chip timer 0 counts down past zero. The pulse is a CLKOUT cycle wide. TOUT0 also goes into the high-impedance state when $\overline{\text{OFF}}$ is low.
TOUT1	O/Z	Timer1 output. TOUT1 signals a pulse when the on-chip timer1 counts down past zero. The pulse is one CLKOUT cycle wide. The TOUT1 output is multiplexed with the $\overline{\text{HINT}}$ pin of the HPI and is only available when the HPI is disabled. TOUT1 also goes into the high-impedance state when $\overline{\text{OFF}}$ is low.
MULTICHANNEL BUFFERED SERIAL PORT SIGNALS		
BCLKR0 BCLKR1	I/O/Z	Receive clock input. BCLKR can be configured as an input or an output; it is configured as an input following reset. BCLKR serves as the serial shift clock for the buffered serial port receiver.
BDR0 BDR1	I	Serial data receive input
BFSR0 BFSR1	I/O/Z	Frame synchronization pulse for receive input. BFSR can be configured as an input or an output; it is configured as an input following reset. The BFSR pulse initiates the receive data process over BDR.
BCLKX0 BCLKX1	I/O/Z	Transmit clock. BCLKX serves as the serial shift clock for the McBSP transmitter. BCLKX can be configured as an input or an output; it is configured as an input following reset. BCLKX enters the high-impedance state when $\overline{\text{OFF}}$ goes low.
BDX0 BDX1	O/Z	Serial data transmit output. BDX is placed in the high-impedance state when not transmitting, when $\overline{\text{RS}}$ is asserted, or when $\overline{\text{OFF}}$ is low.
BFSX0 BFSX1	I/O/Z	Frame synchronization pulse for transmit input/output. The BFSX pulse initiates the transmit data process. BFSX can be configured as an input or an output; it is configured as an input following reset. BFSX goes into the high-impedance state when $\overline{\text{OFF}}$ is low.
MISCELLANEOUS SIGNAL		
NC		No connection
HOST-PORT INTERFACE SIGNALS		
HD0–HD7	I/O/Z	Parallel bidirectional data bus. The HPI data bus is used by a host device bus to exchange information with the HPI registers. These pins can also be used as general-purpose I/O pins. HD0–HD7 is placed in the high-impedance state when not outputting data or when $\overline{\text{OFF}}$ is low. The HPI data bus includes bus holders to reduce the static power dissipation caused by floating, unused pins. When the HPI data bus is not being driven by the ’5402, the bus holders keep the pins at the previous logic level. The HPI data bus holders are disabled at reset and can be enabled/disabled via the HBH bit of the BSCR.
HCNTL0 HCNTL1	I	Control. HCNTL0 and HCNTL1 select a host access to one of the three HPI registers. The control inputs have internal pullup resistors that are only enabled when HPIENA = 0.

† I = input, O = output, Z = high impedance, S = supply

‡ All revisions of the ’5402 can be operated with an external clock source, provided that the proper voltage levels be driven on the X2/CLKIN pin. It should be noted that the X2/CLKIN pin is referenced to the device 1.8V power supply (CV_{DD}), rather than the 3V I/O supply (DV_{DD}). Refer to the recommended operating conditions section of this document for the allowable voltage levels of the X2/CLKIN pin.

Terminal Functions (Continued)

TERMINAL NAME	TYPE†	DESCRIPTION
HOST-PORT INTERFACE SIGNALS (CONTINUED)		
HBIL	I	Byte identification. HBIL identifies the first or second byte of transfer. The HBIL input has an internal pullup resistor that is only enabled when HPIENA = 0.
$\overline{\text{HCS}}$	I	Chip select. $\overline{\text{HCS}}$ is the select input for the HPI and must be driven low during accesses. The chip-select input has an internal pullup resistor that is only enabled when HPIENA = 0.
$\overline{\text{HDS1}}$ $\overline{\text{HDS2}}$	I	Data strobe. $\overline{\text{HDS1}}$ and $\overline{\text{HDS2}}$ are driven by the host read and write strobes to control transfers. The strobe inputs have internal pullup resistors that are only enabled when HPIENA = 0.
$\overline{\text{HAS}}$	I	Address strobe. Hosts with multiplexed address and data pins require $\overline{\text{HAS}}$ to latch the address in the HPIA register. $\overline{\text{HAS}}$ has an internal pullup resistor that is only enabled when HPIENA = 0.
HR/$\overline{\text{W}}$	I	Read/write. HR/$\overline{\text{W}}$ controls the direction of an HPI transfer. R/$\overline{\text{W}}$ has an internal pullup resistor that is only enabled when HPIENA = 0.
HRDY	O/Z	Ready. The ready output informs the host when the HPI is ready for the next transfer. HRDY goes into the high-impedance state when $\overline{\text{OFF}}$ is low.
$\overline{\text{HINT}}$	O/Z	Host interrupt. This output is used to interrupt the host. When the DSP is in reset, $\overline{\text{HINT}}$ is driven high. $\overline{\text{HINT}}$ can also be configured as the timer 1 output (TOUT1), when the HPI is disabled. The signal goes into the high-impedance state when $\overline{\text{OFF}}$ is low.
HPIENA	I	HPI module select. HPIENA must be driven high during reset to enable the HPI. An internal pulldown resistor is always active and the HPIENA pin is sampled on the rising edge of $\overline{\text{RS}}$. If HPIENA is left open or is driven low during reset, the HPI module is disabled. Once the HPI is disabled, the HPIENA pin has no effect until the ’5402 is reset.
SUPPLY PNS		
CV_{DD}	S	$+V_{DD}$. Dedicated 1.8-V power supply for the core CPU
DV_{DD}	S	$+V_{DD}$. Dedicated 3.3-V power supply for the I/O pins
V_{SS}	S	Ground
TEST PINS		
TCK	I	IEEE standard 1149.1 test clock. TCK is normally a free-running clock signal with a 50% duty cycle. The changes on the test access port (TAP) of input signals TMS and TDI are clocked into the TAP controller, instruction register, or selected test data register on the rising edge of TCK. Changes at the TAP output signal (TDO) occur on the falling edge of TCK.
TDI	I	IEEE standard 1149.1 test data input pin with internal pullup device. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
TDO	O/Z	IEEE standard 1149.1 test data output. The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. TDO is in the high-impedance state except when the scanning of data is in progress. TDO also goes into the high-impedance state when $\overline{\text{OFF}}$ is low.
TMS	I	IEEE standard 1149.1 test mode select. Pin with internal pullup device. This serial control input is clocked into the TAP controller on the rising edge of TCK.
$\overline{\text{TRST}}$	I	IEEE standard 1149.1 test reset. $\overline{\text{TRST}}$, when high, gives the IEEE standard 1149.1 scan system control of the operations of the device. If $\overline{\text{TRST}}$ is not connected or is driven low, the device operates in its functional mode, and the IEEE standard 1149.1 signals are ignored. Pin with internal pulldown device.

† I = input, O = output, Z = high impedance, S = supply

‡ All revisions of the ’5402 can be operated with an external clock source, provided that the proper voltage levels be driven on the X2/CLKIN pin. It should be noted that the X2/CLKIN pin is referenced to the device 1.8V power supply (CV_{DD}), rather than the 3V I/O supply (DV_{DD}). Refer to the recommended operating conditions section of this document for the allowable voltage levels of the X2/CLKIN pin.

Terminal Functions (Continued)

TERMINAL NAME	TYPE†	DESCRIPTION
TEST PINS (CONTINUED)		
EMU0	I/O/Z	Emulator 0 pin. When $\overline{\text{TRST}}$ is driven low, EMU0 must be high for activation of the $\overline{\text{OFF}}$ condition. When $\overline{\text{TRST}}$ is driven high, EMU0 is used as an interrupt to or from the emulator system and is defined as input/output by way of the IEEE standard 1149.1 scan system.
EMU1/$\overline{\text{OFF}}$	I/O/Z	Emulator 1 pin/disable all outputs. When $\overline{\text{TRST}}$ is driven high, EMU1/$\overline{\text{OFF}}$ is used as an interrupt to or from the emulator system and is defined as input/output by way of the IEEE standard 1149.1 scan system. When $\overline{\text{TRST}}$ is driven low, EMU1/$\overline{\text{OFF}}$ is configured as $\overline{\text{OFF}}$. The EMU1/$\overline{\text{OFF}}$ signal, when active low, puts all output drivers into the high-impedance state. Note that $\overline{\text{OFF}}$ is used exclusively for testing and emulation purposes (not for multiprocessing applications). The $\overline{\text{OFF}}$ feature is selected by the following pin combinations: $\overline{\text{TRST}}$ = low EMU0 = high EMU1/$\overline{\text{OFF}}$ = low

† I = input, O = output, Z = high impedance, S = supply

‡ All revisions of the ’5402 can be operated with an external clock source, provided that the proper voltage levels be driven on the X2/CLKIN pin. It should be noted that the X2/CLKIN pin is referenced to the device 1.8V power supply (CV_{DD}), rather than the 3V I/O supply (DV_{DD}). Refer to the recommended operating conditions section of this document for the allowable voltage levels of the X2/CLKIN pin.

memory

The ’5402 device provides both on-chip ROM and RAM memories to aid in system performance and integration.

on-chip ROM with bootloader

The ’5402 features a 4K-word × 16-bit on-chip maskable ROM. Customers can arrange to have the ROM of the ’5402 programmed with contents unique to any particular application. A security option is available to protect a custom ROM. This security option is described in the *TMS320C54x DSP CPU and Peripherals Reference Set, Volume 1* (literature number SPRU131). Note that only the ROM security option, and not the ROM/RAM option, is available on the ’5402 .

A bootloader is available in the standard ’5402 on-chip ROM. This bootloader can be used to automatically transfer user code from an external source to anywhere in the program memory at power up. If the MP/$\overline{\text{MC}}$ pin is sampled low during a hardware reset, execution begins at location FF80h of the on-chip ROM. This location contains a branch instruction to the start of the bootloader program. The standard ’5402 bootloader provides different ways to download the code to accomodate various system requirements:

- Parallel from 8-bit or 16-bit-wide EPROM
- Parallel from I/O space 8-bit or 16-bit mode
- Serial boot from serial ports 8-bit or 16-bit mode
- Host-port interface boot

The standard on-chip ROM layout is shown in Table 1.

Table 1. Standard On-Chip ROM Layout†

ADDRESS RANGE	DESCRIPTION
F000h – F7FFh	Reserved
F800h – FBFFh	Bootloader
FC00h – FCFFh	μ-law expansion table
FD00h – FDFFh	A-law expansion table
FE00h – FEFFh	Sine look-up table
FF00h – FF7Fh	Reserved
FF80h – FFFFh	Interrupt vector table

† In the ’VC5402 ROM, 128 words are reserved for factory device-testing purposes. Application code to be implemented in on-chip ROM must reserve these 128 words at addresses FF00h–FF7Fh in program space.

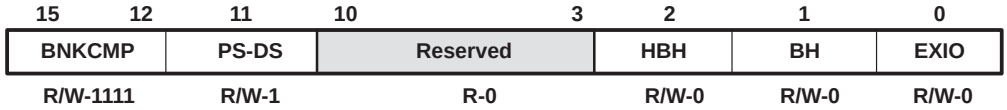
on-chip RAM

The ’5402 device contains 16K × 16-bit of on-chip dual-access RAM (DARAM). The DARAM is composed of two blocks of 8K words each. Each block in the DARAM can support two reads in one cycle, or a read and a write in one cycle. The DARAM is located in the address range 0060h–3FFFh in data space, and can be mapped into program/data space by setting the OVLY bit to one.

programmable bank-switching wait states

The programmable bank-switching logic of the ’5402 is functionally equivalent to that of the ’548/’549 devices. This feature automatically inserts one cycle when accesses cross memory-bank boundaries within program or data memory space. A bank-switching wait state can also be automatically inserted when accesses cross the data space boundary into program space.

The bank-switching control register (BSCR) defines the bank size for bank-switching wait states. Figure 6 shows the BSCR and its bits are described in Table 4.



LEGEND: R = Read, W = Write

Figure 6. Bank-Switching Control Register (BSCR), MMR Address 0029h

Table 4. Bank-Switching Control Register (BSCR) Fields

BIT NO.	BIT NAME	RESET VALUE	FUNCTION
15–12	BNKCMP	1111	Bank compare. Determines the external memory-bank size. BNKCMP is used to mask the four MSBs of an address. For example, if BNKCMP = 1111b, the four MSBs (bits 12–15) are compared, resulting in a bank size of 4K words. Bank sizes of 4K words to 64K words are allowed.
11	PS - DS	1	Program read – data read access. Inserts an extra cycle between consecutive accesses of program read and data read or data read and program read. PS-DS = 0 No extra cycles are inserted by this feature. PS-DS = 1 One extra cycle is inserted between consecutive data and program reads.
10–3	Reserved	0	These bits are reserved and are unaffected by writes.
2	HBH	0	HPI Bus holder. Controls the HPI bus holder feature. HBH is cleared to 0 at reset. HBH = 0 The bus holder is disabled. HBH = 1 The bus holder is enabled. When not driven, the HPI data bus (HD[7:0]) is held in the previous logic level.
1	BH	0	Bus holder. Controls the data bus holder feature. BH is cleared to 0 at reset. BH = 0 The bus holder is disabled. BH = 1 The bus holder is enabled. When not driven, the data bus (D[15:0]) is held in the previous logic level.
0	EXIO	0	External bus interface off. The EXIO bit controls the external bus-off function. EXIO = 0 The external bus interface functions as usual. EXIO = 1 The address bus, data bus, and control signals become inactive after completing the current bus cycle. Note that the DROM, MP/$\overline{MC}$, and OVLY bits in the PMST and the HM bit of ST1 cannot be modified when the interface is disabled.

DMA channel index registers (continued)

The element index and the frame index affect address adjustment as follows:

- Element index: For all except the last transfer in the frame, the element index determines the amount to be added to the DMA channel for the source/destination address register (DMSRCx/DMDSTx) as selected by the SIND/DIND bits.
- Frame index: If the transfer is the last in a frame, the frame index is used for address adjustment as selected by the SIND/DIND bits. This occurs in both single-frame and multi-frame transfer.

DMA interrupts

The ability of the DMA to interrupt the CPU based on the status of the data transfer is configurable and is determined by the IMOD and DINM bits in the DMA channel mode control register (DMMCRn). The available modes are shown in Table 6.

Table 6. DMA Interrupts

MODE	DINM	IMOD	INTERRUPT
ABU (non-decrement)	1	0	At full buffer only
ABU (non-decrement)	1	1	At half buffer and full buffer
Multi-Frame	1	0	At block transfer complete (DMCTRn = DMSEFCn[7:0] = 0)
Multi-Frame	1	1	At end of frame and end of block (DMCTRn = 0)
Either	0	X	No interrupt generated
Either	0	X	No interrupt generated

DMA controller synchronization events

The transfers associated with each DMA channel can be synchronized to one of several events. The DSYN bit field of the DMA channel x sync select and frame count (DMSFCx) register selects the synchronization event for a channel. The list of possible events and the DSYN values are shown in Table 7.

Table 7. DMA Synchronization Events

DSYN VALUE	DMA SYNCHRONIZATION EVENT
0000b	No synchronization used
0001b	McBSP0 receive event
0010b	McBSP0 transmit event
0011–0100b	Reserved
0101b	McBSP1 receive event
0110b	McBSP1 transmit event
0111b–0110b	Reserved
1101b	Timer0 interrupt
1110b	External interrupt 3
1111b	Timer1 interrupt

DMA channel interrupt selection

The DMA controller can generate a CPU interrupt for each of the six channels. However, the interrupt sources for channels 0,1, 2, and 3 are multiplexed with other interrupt sources. DMA channels 2 and 3 share an interrupt line with the receive and transmit portions of McBSP1 (IMR/IFR bits 10 and 11), and DMA channel 1 shares an interrupt line with timer 1 (IMR/IFR bit 7). The interrupt source for DMA channel 0 is shared with a reserved interrupt source. When the ’5402 is reset, the interrupts from these four DMA channels are deselected. The INTSEL bit field in the DMA channel priority and enable control (DMPREC) register can be used to select these interrupts, as shown in Table 8.

Table 8. DMA Channel Interrupt Selection

INTSEL Value	IMR/IFR[6]	IMR/IFR[7]	IMR/IFR[10]	IMR/IFR[11]
00b (reset)	Reserved	TINT1	BRINT1	BXINT1
01b	Reserved	TINT1	DMAC2	DMAC3
10b	DMAC0	DMAC1	DMAC2	DMAC3
11b	Reserved			

memory-mapped registers

The ’5402 has 27 memory-mapped CPU registers, which are mapped in data memory space addresses 0h to 1Fh. Table 9 gives a list of CPU memory-mapped registers (MMRs) available on ’5402. The device also has a set of memory-mapped registers associated with peripherals. Table 10, Table 11, and Table 12 show additional peripheral MMRs associated with the ’5402.

Table 9. CPU Memory-Mapped Registers

NAME	ADDRESS		DESCRIPTION
	DEC	HEX	
IMR	0	0	Interrupt mask register
IFR	1	1	Interrupt flag register
–	2–5	2–5	Reserved for testing
ST0	6	6	Status register 0
ST1	7	7	Status register 1
AL	8	8	Accumulator A low word (15–0)
AH	9	9	Accumulator A high word (31–16)
AG	10	A	Accumulator A guard bits (39–32)
BL	11	B	Accumulator B low word (15–0)
BH	12	C	Accumulator B high word (31–16)
BG	13	D	Accumulator B guard bits (39–32)
TREG	14	E	Temporary register
TRN	15	F	Transition register
AR0	16	10	Auxiliary register 0
AR1	17	11	Auxiliary register 1
AR2	18	12	Auxiliary register 2
AR3	19	13	Auxiliary register 3
AR4	20	14	Auxiliary register 4
AR5	21	15	Auxiliary register 5
AR6	22	16	Auxiliary register 6
AR7	23	17	Auxiliary register 7
SP	24	18	Stack pointer register
BK	25	19	Circular buffer size register
BRC	26	1A	Block repeat counter
RSA	27	1B	Block repeat start address
REA	28	1C	Block repeat end address
PMST	29	1D	Processor mode status (PMST) register
XPC	30	1E	Extended program page register
–	31	1F	Reserved

memory-mapped registers (continued)

Table 10. Peripheral Memory-Mapped Registers

NAME	ADDRESS	DESCRIPTION	TYPE
DRR20	20h	McBSP0 data receive register 2	McBSP #0
DRR10	21h	McBSP0 data receive register 1	McBSP #0
DXR20	22h	McBSP0 data transmit register 2	McBSP #0
DXR10	23h	McBSP0 data transmit register 1	McBSP #0
TIM	24h	Timer0 register	Timer0
PRD	25h	Timer0 period counter	Timer0
TCR	26h	Timer0 control register	Timer0
–	27h	Reserved	
SWWSR	28h	Software wait-state register	External Bus
BSCR	29h	Bank-switching control register	External Bus
–	2Ah	Reserved	
SWCR	2Bh	Software wait-state control register	External Bus
HPIC	2Ch	HPI control register	HPI
–	2Dh–2Fh	Reserved	
TIM1	30h	Timer1 register	Timer1
PRD1	31h	Timer1 period counter	Timer1
TCR1	32h	Timer1 control register	Timer1
–	33h–37h	Reserved	
SPSA0	38h	McBSP0 subbank address register†	McBSP #0
SPSD0	39h	McBSP0 subbank data register†	McBSP #0
–	3Ah–3Bh	Reserved	
GPIOCR	3Ch	General-purpose I/O pins control register	GPIO
GPIOSR	3Dh	General-purpose I/O pins status register	GPIO
–	3Eh–3Fh	Reserved	
DRR21	40h	McBSP1 data receive register 2	McBSP #1
DRR11	41h	McBSP1 data receive register 1	McBSP #1
DXR21	42h	McBSP1 data transmit register 2	McBSP #1
DXR11	43h	McBSP1 data transmit register 1	McBSP #1
–	44h–47h	Reserved	
SPSA1	48h	McBSP1 subbank address register†	McBSP #1
SPSD1	49h	McBSP1 subbank data register†	McBSP #1
–	4Ah–53h	Reserved	
DMPREC	54h	DMA channel priority and enable control register	DMA
DMSA	55h	DMA subbank address register‡	DMA
DMSDI	56h	DMA subbank data register with autoincrement‡	DMA
DMSDN	57h	DMA subbank data register‡	DMA
CLKMD	58h	Clock mode register	PLL
–	59h–5Fh	Reserved	

† See Table 11 for a detailed description of the McBSP control registers and their sub-addresses.
‡ See Table 12 for a detailed description of the DMA subbank addressed registers.

McBSP control registers and subaddresses

The control registers for the multichannel buffered serial port (McBSP) are accessed using the subbank addressing scheme. This allows a set or subbank of registers to be accessed through a single memory location. The serial port subbank address (SPSA) register is used as a pointer to select a particular register within the subbank. The serial port subbank data (SPSD) register is used to access (read or write) the selected register. Table 11 shows the McBSP control registers and their corresponding sub-addresses.

Table 11. McBSP Control Registers and Subaddresses

McBSP0		McBSP1			
NAME	ADDRESS	NAME	ADDRESS	SUB-ADDRESS	DESCRIPTION
SPCR10	39h	SPCR11	49h	00h	Serial port control register 1
SPCR20	39h	SPCR21	49h	01h	Serial port control register 2
RCR10	39h	RCR11	49h	02h	Receive control register 1
RCR20	39h	RCR21	49h	03h	Receive control register 2
XCR10	39h	XCR11	49h	04h	Transmit control register 1
XCR20	39h	XCR21	49h	05h	Transmit control register 2
SRGR10	39h	SRGR11	49h	06h	Sample rate generator register 1
SRGR20	39h	SRGR21	49h	07h	Sample rate generator register 2
MCR10	39h	MCR11	49h	08h	Multichannel register 1
MCR20	39h	MCR21	49h	09h	Multichannel register 2
RCERA0	39h	RCERA1	49h	0Ah	Receive channel enable register partition A
RCERB0	39h	RCERB1	49h	0Bh	Receive channel enable register partition B
XCERA0	39h	XCERA1	49h	0Ch	Transmit channel enable register partition A
XCERB0	39h	XCERB1	49h	0Dh	Transmit channel enable register partition B
PCR0	39h	PCR1	49h	0Eh	Pin control register

DMA subbank addressed registers

The direct memory access (DMA) controller has several control registers associated with it. The main control register (DMPREC) is a standard memory-mapped register. However, the other registers are accessed using the subbank addressing scheme. This allows a set or subbank of registers to be accessed through a single memory location. The DMA subbank address (DMSA) register is used as a pointer to select a particular register within the subbank, while the DMA subbank data (DMSDN) register or the DMA subbank data register with autoincrement (DMSDI) is used to access (read or write) the selected register.

When the DMSDI register is used to access the subbank, the subbank address is automatically post-incremented so that a subsequent access affects the next register within the subbank. This autoincrement feature is intended for efficient, successive accesses to several control registers. If the autoincrement feature is not required, the DMSDN register should be used to access the subbank. Table 12 shows the DMA controller subbank addressed registers and their corresponding subaddresses.

DMA subbank addressed registers (continued)

Table 12. DMA Subbank Addressed Registers

DMA NAME	DMA ADDRESS	SUB-ADDRESS	DESCRIPTION
DMSRC0	56h/57h	00h	DMA channel 0 source address register
DMDST0	56h/57h	01h	DMA channel 0 destination address register
DMCTR0	56h/57h	02h	DMA channel 0 element count register
DMSFC0	56h/57h	03h	DMA channel 0 sync select and frame count register
DMMCR0	56h/57h	04h	DMA channel 0 transfer mode control register
DMSRC1	56h/57h	05h	DMA channel 1 source address register
DMDST1	56h/57h	06h	DMA channel 1 destination address register
DMCTR1	56h/57h	07h	DMA channel 1 element count register
DMSFC1	56h/57h	08h	DMA channel 1 sync select and frame count register
DMMCR1	56h/57h	09h	DMA channel 1 transfer mode control register
DMSRC2	56h/57h	0Ah	DMA channel 2 source address register
DMDST2	56h/57h	0Bh	DMA channel 2 destination address register
DMCTR2	56h/57h	0Ch	DMA channel 2 element count register
DMSFC2	56h/57h	0Dh	DMA channel 2 sync select and frame count register
DMMCR2	56h/57h	0Eh	DMA channel 2 transfer mode control register
DMSRC3	56h/57h	0Fh	DMA channel 3 source address register
DMDST3	56h/57h	10h	DMA channel 3 destination address register
DMCTR3	56h/57h	11h	DMA channel 3 element count register
DMSFC3	56h/57h	12h	DMA channel 3 sync select and frame count register
DMMCR3	56h/57h	13h	DMA channel 3 transfer mode control register
DMSRC4	56h/57h	14h	DMA channel 4 source address register
DMDST4	56h/57h	15h	DMA channel 4 destination address register
DMCTR4	56h/57h	16h	DMA channel 4 element count register
DMSFC4	56h/57h	17h	DMA channel 4 sync select and frame count register
DMMCR4	56h/57h	18h	DMA channel 4 transfer mode control register
DMSRC5	56h/57h	19h	DMA channel 5 source address register
DMDST5	56h/57h	1Ah	DMA channel 5 destination address register
DMCTR5	56h/57h	1Bh	DMA channel 5 element count register
DMSFC5	56h/57h	1Ch	DMA channel 5 sync select and frame count register
DMMCR5	56h/57h	1Dh	DMA channel 5 transfer mode control register
DMSRCP	56h/57h	1Eh	DMA source program page address (common channel)
DMDSTP	56h/57h	1Fh	DMA destination program page address (common channel)
DMIDX0	56h/57h	20h	DMA element index address register 0
DMIDX1	56h/57h	21h	DMA element index address register 1
DMFRI0	56h/57h	22h	DMA frame index register 0
DMFRI1	56h/57h	23h	DMA frame index register 1
DMGSA	56h/57h	24h	DMA global source address reload register
DMGDA	56h/57h	25h	DMA global destination address reload register
DMGCR	56h/57h	26h	DMA global count reload register
DMGFR	56h/57h	27h	DMA global frame count reload register

interrupts

Vector-relative locations and priorities for all internal and external interrupts are shown in Table 13.

Table 13. Interrupt Locations and Priorities

NAME	LOCATION DECIMAL	LOCATION HEX	PRIORITY	FUNCTION
$\overline{RS}$, SINTR	0	00	1	Reset (hardware and software reset)
$\overline{NMI}$, SINT16	4	04	2	Nonmaskable interrupt
SINT17	8	08	—	Software interrupt #17
SINT18	12	0C	—	Software interrupt #18
SINT19	16	10	—	Software interrupt #19
SINT20	20	14	—	Software interrupt #20
SINT21	24	18	—	Software interrupt #21
SINT22	28	1C	—	Software interrupt #22
SINT23	32	20	—	Software interrupt #23
SINT24	36	24	—	Software interrupt #24
SINT25	40	28	—	Software interrupt #25
SINT26	44	2C	—	Software interrupt #26
SINT27	48	30	—	Software interrupt #27
SINT28	52	34	—	Software interrupt #28
SINT29	56	38	—	Software interrupt #29
SINT30	60	3C	—	Software interrupt #30
$\overline{INT0}$, SINT0	64	40	3	External user interrupt #0
$\overline{INT1}$, SINT1	68	44	4	External user interrupt #1
$\overline{INT2}$, SINT2	72	48	5	External user interrupt #2
TINT0, SINT3	76	4C	6	Timer0 interrupt
BRINT0, SINT4	80	50	7	McBSP #0 receive interrupt
BXINT0, SINT5	84	54	8	McBSP #0 transmit interrupt
Reserved(DMAC0), SINT6	88	58	9	Reserved (default) or DMA channel 0 interrupt. The selection is made in the DMPREC register.
TINT1(DMAC1), SINT7	92	5C	10	Timer1 interrupt (default) or DMA channel 1 interrupt. The selection is made in the DMPREC register.
$\overline{INT3}$, SINT8	96	60	11	External user interrupt #3
HPINT, SINT9	100	64	12	HPI interrupt
BRINT1(DMAC2), SINT10	104	68	13	McBSP #1 receive interrupt (default) or DMA channel 2 interrupt. The selection is made in the DMPREC register.
BXINT1(DMAC3), SINT11	108	6C	14	McBSP #1 transmit interrupt (default) or DMA channel 3 interrupt. The selection is made in the DMPREC register.
DMAC4,SINT12	112	70	15	DMA channel 4 interrupt
DMAC5,SINT13	116	74	16	DMA channel 5 interrupt
Reserved	120–127	78–7F	—	Reserved

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TMS320VC5402GGU100	ACTIVE	BGA	GGU	144	160	TBD	SNPB	Level-3-220C-168HR
TMS320VC5402GGUR10	ACTIVE	BGA	GGU	144	1000	TBD	SNPB	Level-3-220C-168HR
TMS320VC5402PGE100	ACTIVE	LQFP	PGE	144	60	TBD	CU NIPDAU	Level-1-220C-UNLIM
TMS320VC5402PGER10	ACTIVE	LQFP	PGE	144	500	TBD	CU NIPDAU	Level-1-220C-UNLIM
TMX320VC5402GGU100	OBSOLETE	BGA	GGU	144		TBD	Call TI	Call TI
TMX320VC5402PGE100	OBSOLETE	LQFP	PGE	144		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265