TMS320F2837xD Dual-Core Delfino™ Microcontrollers

1 Device Overview

1.1 Features

- Dual-Core Architecture
  - Two TMS320C28x 32-Bit CPUs
  - 200 MHz
  - IEEE 754 Single-Precision Floating-Point
  - Trigonometric Math Unit (TMU)
  - Viterbi/Complex Math Unit (VCU-II)
- Two Programmable Control Law Accelerators
  - 200 MHz
  - IEEE 754 Single-Precision Floating-Point Executes Code Independently of Main CPU
- On-Chip Memory
  - 512KB or 1MB of Flash (ECC-Protected)
  - 172KB or 204KB of RAM (ECC or Parity)
  - Dual-Zone Security Supporting Third-Party Development
- Clock and System Control
  - Two Internal Zero-Pin 10-MHz Oscillators
  - On-Chip Crystal Oscillator and External Clock Input
  - Windowed Watchdog Timer Module
  - Missing Clock Detection Circuitry
- 1.2-V Core, 3.3-V I/O Design
- System Peripherals
  - Two External Memory Interfaces (EMIFs) With ASRAM and SDRAM Support
  - Dual 6-Channel Direct Memory Access (DMA) Controller
  - Up to 169 Individually Programmable, Multiplexed General-Purpose Input/Output (GPIO) Pins With Input Filtering
  - HW Interrupt Controller
  - Multiple Low-Power Mode Support With External Wakeup
  - JTAG Emulation Connection
- Communications Peripherals
  - USB 2.0 (MAC + PHY)
  - Two CAN-Bus Ports (Pin-Bootable)
  - Three High-Speed (40-MHz) SPI Ports (Pin-Bootable)
  - Two Multichannel Buffered Serial Ports
  - Four Serial Communications Interfaces (SCIs) (Pin-Bootable)
  - Two I^2C Interfaces (Pin-Bootable)
- Analog Subsystem
  - Four Dual-Mode Analog-to-Digital Converters (ADCs)
    - 16-Bit Mode
      - 1.1 MSPS Each (up to 4.4-MSPS System)
      - Differential
      - Up to 12 External Channels
    - 12-Bit Mode
      - 3.5 MSPS Each (up to 14-MSPS System)
      - Single-Ended
      - Up to 24 External Channels
    - Single Sample-and-Hold (S/H) on Each ADC
    - HW Integrated Post-Processing of ADC Conversions
      - Saturating Offset Calibration
      - Error From Setpoint Calculation
      - High, Low, and Zero-Crossing Compare, With Interrupt Capability
      - Trigger-to-Sample Delay Capture
  - Eight Windowed Comparators With 12-Bit DAC References
  - Three 12-Bit Buffered DAC Outputs
- Enhanced Control Peripherals
  - 24 Pulse Width Modulator (PWM) Channels With Enhanced Features
  - 16 High-Resolution Pulse Width Modulator (HRPWM) Channels
    - High Resolution on Both A and B Channels of 8 PWM Modules
    - Dead-Band Support (on Both Standard and High Resolution)
  - Six Enhanced Capture (eCAP) Modules
  - Three Enhanced Quadrature Encoder Pulse (eQEP) Modules
  - 8 Sigma-Delta Filter Module (SDFM) Input Channels, 2 Parallel Filters per Channel
    - Standard SDFM Data Filtering
    - Comparator Filter for Fast Action for Out of Range

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- Package Options:
  - Lead-Free, Green Packaging
  - 337-Ball New Fine Pitch Ball Grid Array (nFBGA) [ZWT Suffix]
  - 176-Pin PowerPAD™ Thermally Enhanced Low-Profile Quad Flatpack (HLQFP) [PTP Suffix]
- Temperature Options:
  - T: –40ºC to 105ºC Junction
  - S: –40ºC to 125ºC Junction
  - Q: –40ºC to 125ºC Free-Air (Q100 Qualification for Automotive Applications)

1.2 Applications

- Industrial Drives
- Solar Micro Inverters and Converters
- Radar
- Digital Power
- Smart Metering
- Automotive Transportation
- Power Line Communications
- Software-Defined Radio

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1.3 Description

The Delfino™ TMS320F2837xD is a powerful 32-bit floating-point microcontroller unit (MCU) that lets designers consolidate control architectures and eliminate multiprocessor use in high-end systems. While the Delfino product line is not new to the TMS320C2000™ portfolio, the dual-core F2837xD supports a new dual-core C28x architecture that significantly boosts system performance while further providing consolidation through integrated analog and control peripherals.

The dual real-time control subsystems are based on TI's 32-bit C28x floating-point CPUs, which provide 200 MHz of signal processing performance in each core. The C28x CPUs are further boosted by the new TMU accelerator, which enables fast execution of algorithms with trigonometric operations common in transforms and torque loop calculations; and the VCU accelerator, which reduces the latency for complex math operations common in encoded applications.

The F2837xD features two real-time control accelerators, also known as Control Law Accelerators (CLAs). The CLA provides an additional floating-point accelerator used to run parallel time-critical control algorithms, providing bandwidth for the C28x to focus on system tasks. The dual C28x + CLA architecture also provides intelligent partitioning of system-critical tasks and allows simultaneous management of these tasks, such as tracking speed and position in one core while managing control-side algorithms to calculate torque loops in the other CPU + CLA.

The TMS320F2837xD supports up to 1MB of onboard flash memory with error correction code (ECC) and up to 204KB of SRAM. Two 128-bit secure zones are also available on each CPU for code protection.

Performance analog and control peripherals are also integrated on the F2837xD MCU to further enable system consolidation. Four independent 16-bit ADCs provide precise and efficient management of multiple analog signals, which ultimately boosts system throughput. New sigma-delta peripherals enable isolated current shunt measurements and windowed comparators allow protection of power stage when current limit conditions are exceeded or not met. Other analog and control peripherals include digital-to-analog converters (DACs), PWMs, eCAPs, eQEPs, and other peripherals.

Peripherals such as dual EMIFs and dual ISO11898-1 (CAN 2.0B) extend the connectivity of the F2837xD. A USB 2.0 host port with MAC and PHY lets users easily add universal serial bus (USB) connectivity to their application.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE
TMS320F28377DZWT	nFBGA (337)	16.0 mm × 16.0 mm
TMS320F28376DZWT	nFBGA (337)	16.0 mm × 16.0 mm
TMS320F28375DZWT	nFBGA (337)	16.0 mm × 16.0 mm
TMS320F28374DZWT	nFBGA (337)	16.0 mm × 16.0 mm
TMS320F28377DPTP	HLQFP (176)	24.0 mm × 24.0 mm
TMS320F28376DPTP	HLQFP (176)	24.0 mm × 24.0 mm
TMS320F28375DPTP	HLQFP (176)	24.0 mm × 24.0 mm
TMS320F28374DPTP	HLQFP (176)	24.0 mm × 24.0 mm

(1) For more information on these devices, see Section 8, *Mechanical Packaging and Orderable Information*.

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1.4 Functional Block Diagram

Figure 1-1 shows the CPU system and associated peripherals.

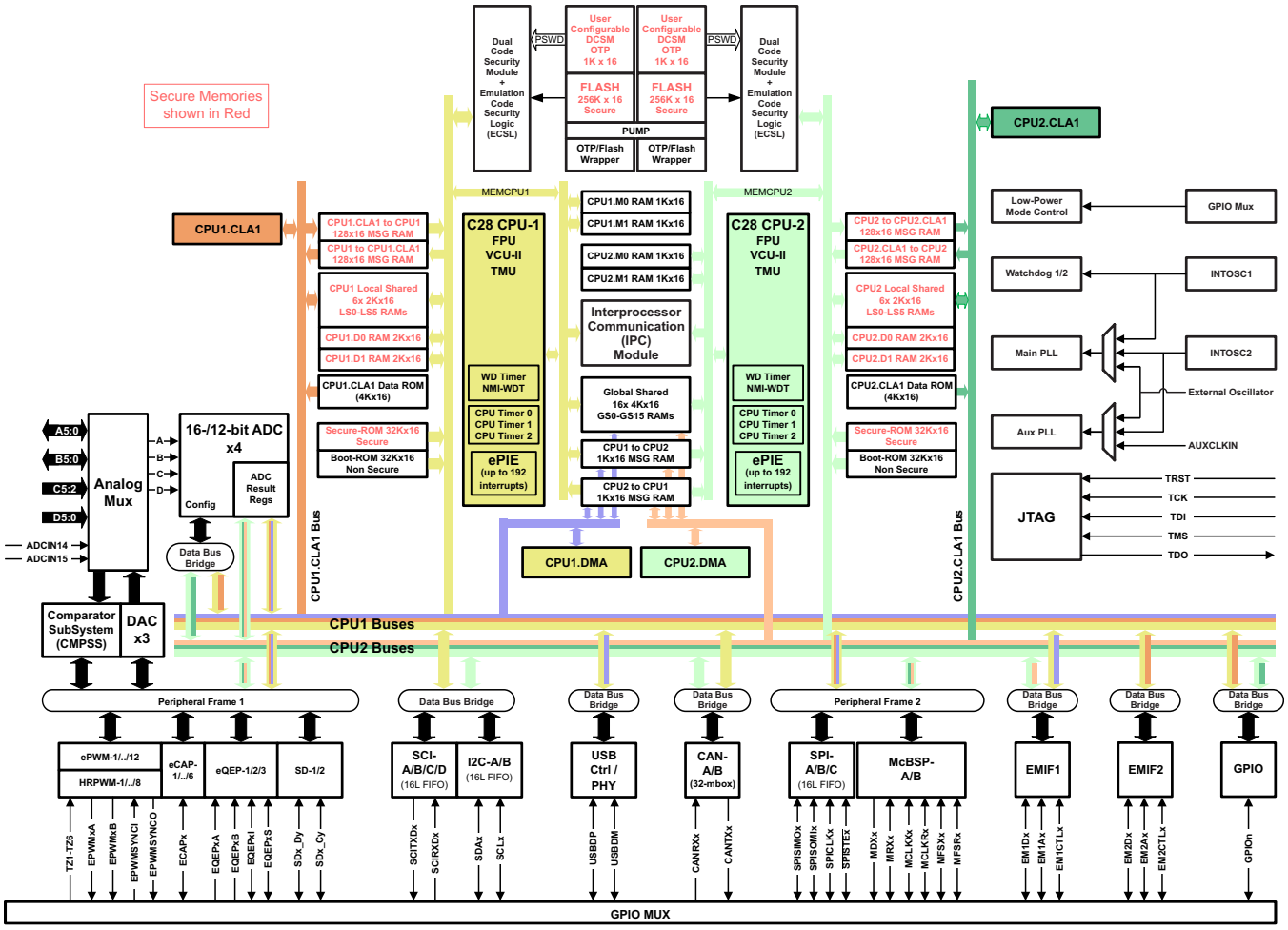

Figure 1-1. Functional Block Diagram

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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from August 11, 2014 to January 13, 2015 (from B Revision (AUGUST 2014) to C Revision) **Page**

- **Global:** Restructured document. 1
- **Global:** Removed Differential Mode for 12-bit ADC. 1
- **Global:** Removed Universal Parallel Port (uPP). 1
- **Global:** T temperature range (–40°C to 105°C) is Junction temperature (T_J). 1
- **Global:** S temperature range (–40°C to 125°C) is Junction temperature (T_J). 1
- **Global:** Q temperature range (–40°C to 150°C, Q100 qualification) is Junction temperature (T_J). 1
- **Global:** Q temperature range (–40°C to 125°C, Q100 qualification) is Free-Air temperature (T_A). 1
- **Global:** Changed "CAN 2.0" to "ISO11898-1 (CAN 2.0B)". 1
- **Global:** Changed $t_{c(SCO)}$ to $t_{c(SYSCLK)}$ 1
- **Global:** Changed SYSCLKOUT to SYSCLK. 1
- **Global:** Changed $t_{c(LCO)}$ to $t_{c(LSPCLK)}$ 1
- **Global:** Removed "Message RAM (MSGRAM)" section (this was Section 6.5.6.4 in SPRS880B). 1
- **Global:** Removed "Peripheral Information and Timings" section title (this was Section 6.6 in SPRS880B). 1
- **Global:** Removed "Comparator/DAC Electrical Characteristics" table (this was Table 5-7 in SPRS880B). 1
- Section 1.1 (Features): Updated section. 1
- Section 1.3 (Description): Updated paragraph about connectivity. 3
- Figure 1-1 (Functional Block Diagram): Changed CPU1.D0 RAM, CPU1.D1 RAM, CPU2.D0 RAM, and CPU2.D1 RAM to secure memory. 4
- Figure 1-1: Moved ADCIN14 and ADCIN15 to "Analog Mux". 4
- Table 3-1 (Device Comparison Table): ADC 12-bit mode: Changed "Channels (**differential/**single-ended)" to "Channels (single-ended)". Updated number of channels. 10
- Table 3-1: EMIF: Changed "16/32-bit" to "**EMIF1** 16/32-bit". Changed "16-bit" to "**EMIF2** 16-bit". 10
- Table 3-1: Changed "On-chip crystal oscillator/External clock input" to "Crystal oscillator/External clock input". 10
- Table 3-1: Updated temperature ranges (see **Global** changes). 10
- Table 3-1: Added footnote about sample-and-hold window. 10
- Section 4.1 (Signal Descriptions): Changed "**With the exception of the JTAG pins,** the GPIO function is the default at reset ..." to "The GPIO function is the default at reset ..." 17
- Table 4-1 (Signal Descriptions): Updated DESCRIPTION of V_{REFHIA}, V_{REFHIB}, V_{REFHIC}, V_{REFHID}, ADCINA0, ADCINA1, ADCINB0, VDAC, ADCINB1, GPIO41, XCLKOUT, $\overline{XRS}$, and TDO. 17
- Section 4.2 (Pins With Internal Pullup and Pulldown): Added section. 38
- Section 4.3.3 (High-Speed SPI Pin Muxing): Added section. 43
- Section 5.1 (Absolute Maximum Ratings): Reformatted table. 44
- Section 5.1: Changed "Input clamp current, I_{IK}" to the following: Digital input (per pin), I_{IK}; Analog input (per pin), $I_{IKANALOG}$; and Total for all inputs, $I_{IKTOTAL}$ 44
- Section 5.1: Changed "Output clamp current, I_{OK}" to "Output current, I_{OUT}" 44
- Section 5.1: Added Operating junction temperature, T_J 44
- Section 5.1: Added Storage temperature, T_{stg} 44
- Section 5.1: Removed "Continuous clamp current per pin is ± 2 mA" footnote. 44
- Section 5.2 (ESD Ratings): Changed section title from "Handling Ratings" to "ESD Ratings". 44
- Section 5.2: Updated section. 44
- Section 5.3 (Recommended Operating Conditions): Updated temperature ranges (see **Global** changes). 45
- Section 5.3: Updated "V_{DDIO}, V_{DDSFL}, V_{DDOSC}, and V_{DDA} ..." footnote. 45
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- Section 6.6.8 (Timers): "CPU-Timer 2 can be clocked by any one of the following" list: Changed "**CPUx.**SYSCLK (default)" to "SYSCLK (default)". 96
- Section 6.7 (Emulation/JTAG): Added section. 98
- Section 6.8 (Analog Peripherals): Changed "each containing a 12-bit reference DAC" to "each containing two 12-bit reference DACs". 100
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- Section 6.10.3 (Inter-Integrated Circuit): Changed "One **4**-word receive FIFO and one **4**-word transmit FIFO" to "One **16**-word receive FIFO and one **16**-word transmit FIFO". 153
- Section 6.10.3.1 (I^2C Electrical Data and Timing): Added section. 155
- Section 6.10.4.1 (McBSP Electrical Data and Timing): Added section. 158
- Section 6.10.5 (Universal Serial Bus Controller): Added NOTE about accuracy of on-chip zero-pin oscillator. 165
- Section 6.10.5.1 (USB Electrical Data and Timing): Added section. 166
- Section 6.10.6 (Controller Area Network): Updated list of CAN module features. 167
- Section 6.10.6: Added NOTE about accuracy of the on-chip zero-pin oscillator. 167
- Section 6.10.7 (External Memory Interface): Updated section. 168

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- Section 6.10.7.2 (Synchronous DRAM Support): Updated section. 168
- Section 6.10.7.3 (EMIF Electrical Data and Timing): Added section. 169
- Section 7.1.1.1 (Getting Started and Next Steps): Added section. 176

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3 Device Comparison

Table 3-1. Device Comparison Table

FEATURE[1]		28377D		28376D		28375D		28374D	
Package Type (ZWT is an nFBGA package. PTP is an HLQFP package.)		**337-Ball ZWT**	**176-Pin PTP**	**337-Ball ZWT**	**176-Pin PTP**	**337-Ball ZWT**	**176-Pin PTP**	**337-Ball ZWT**	**176-Pin PTP**
Processor speed (MHz)		200							
Floating-Point Unit (FPU)		Yes							
VCU-II		Yes							
TMU – Type 0		Yes							
CLA – Type 1		2 (1 per CPU)							
6-Channel DMA – Type 0		2 (1 per CPU)							
Flash (16-bit words)		512KW (256KW per CPU)		256KW (128KW per CPU)		512KW (256KW per CPU)		256KW (128KW per CPU)	
RAM (16-bit words)	Dedicated and Local Shared RAM	36KW (18KW per CPU)							
	Global Shared RAM	64KW		48KW		64KW		48KW	
	Message RAM	2KW (1KW per CPU)							
	Total RAM	**102KW**		**86KW**		**102KW**		**86KW**	
Code security for on-chip Flash, RAM, and OTP blocks		Yes							
Boot ROM		Yes							
One-Time Programmable (OTP) memory (16-bit words)		2KW							
Enhanced Pulse Width Modulator (ePWM) Type-4 channels		24							
High-resolution ePWM Type-4 channels		16							
eCAP inputs – Type 0		6							
eQEP modules – Type 0		3							
32-bit CPU timers		6 (3 per CPU)							
Watchdog timers		2 (1 per CPU)							
Nonmaskable Interrupt Watchdog (NMIWD) timers		2 (1 per CPU)							
ADC 16-bit mode	MSPS	1.1				–			
	Conversion Time (ns)[2]	915				–			
	Input pins	24	20	24	20	–			
	Channels (differential)	12	9	12	9	–			
ADC 12-bit mode	MSPS	3.5							
	Conversion Time (ns)[2]	290							
	Input pins	24	20	24	20	24	20	24	20
	Channels (single-ended)	24	20	24	20	24	20	24	20
Number of 16-bit or 12-bit ADCs		4				–			
Number of 12-bit only ADCs		–				4			
Temperature sensor		1							
CMPSS (each CMPSS has two Comparators and two internal DACs)		8							
Buffered DAC		3							
SDFM channels		8							
Inter-Integrated Circuit (I^2C) – Type 0		2							
Multichannel Buffered Serial Port (McBSP) – Type 1		2							
Controller Area Network (CAN) – Type 0		2							
Serial Peripheral Interface (SPI) – Type 2		3							
SCI – Type 0		4							
USB – Type 0		1							

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Table 3-1. Device Comparison Table (continued)

FEATURE[1]		28377D		28376D		28375D		28374D	
Package Type (ZWT is an nFBGA package. PTP is an HLQFP package.)		**337-Ball ZWT**	**176-Pin PTP**	**337-Ball ZWT**	**176-Pin PTP**	**337-Ball ZWT**	**176-Pin PTP**	**337-Ball ZWT**	**176-Pin PTP**
EMIF	EMIF1 16/32-bit	1							
	EMIF2 16-bit	1	–	1	–	1	–	1	–
Crystal oscillator/External clock input		1							
0-pin internal oscillator		2							
I/O pins (shared)	GPIO	169	97	169	97	169	97	169	97
External interrupts		5							
Junction Temperature (T_J)	T: –40°C to 105°C	Yes							
	S: –40°C to 125°C	Yes							
	Q: –40°C to 150°C[3]	Yes							
Free-Air Temperature (T_A)	Q: –40°C to 125°C[3]	Yes							
Product status[4]		TMX							

(1) A type change represents a major functional feature difference in a peripheral module. Within a peripheral type, there may be minor differences between devices that do not affect the basic functionality of the module.

(2) Time between start of sample-and-hold window to start of sample-and-hold window of the next conversion.

(3) "Q" refers to Q100 qualification for automotive applications.

(4) The "TMX" product status denotes an experimental device that does not necessarily represent the electrical specifications of the final device.

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4 Terminal Configuration and Functions

Figure 4-1 to Figure 4-4 show in four quadrants the terminal assignments on the 337-ball ZWT New Fine Pitch Ball Grid Array. Figure 4-5 shows the pin assignments on the 176-pin PTP PowerPAD Thermally Enhanced Low-Profile Quad Flatpack.

	1	2	3	4	5	6	7	8	9	10	
W	V_{SSA}	ADCINB1	ADCINB3	ADCINB5	V_{REFHIB}	V_{REFLOD}	V_{SS}	V_{DDIO}	GPIO128	GPIO116	W
V	V_{REFHIA}	ADCINB0	ADCINB2	ADCINB4	V_{REFHID}	V_{REFLOB}	V_{SSA}	GPIO124	GPIO127	GPIO131	V
U	ADCINA0	ADCINA2	ADCINA4	ADCIN15	ADCIND1	ADCIND3	ADCIND5	GPIO123	GPIO126	GPIO130	U
T	ADCINA1	ADCINA3	ADCINA5	ADCIN14	ADCIND0	ADCIND2	ADCIND4	GPIO122	GPIO125	GPIO129	T
R	V_{REFHIC}	V_{REFLOA}	ADCINC2	ADCINC4	V_{SSA}	V_{DDA}	V_{SS}	V_{SS}	V_{DDIO}	V_{DD}	R
P	V_{SSA}	V_{REFLOC}	ADCINC3	ADCINC5	V_{SSA}	V_{DDA}	V_{SS}	V_{SS}	V_{DDIO}	V_{DD}	P
N	V_{SS}	GPIO109	GPIO114	GPIO113	V_{SS}	V_{SS}	N				
M	V_{DDIO}	GPIO110	GPIO112	GPIO111	V_{DDIO}	V_{DDIO}	M	V_{SS}	V_{SS}	V_{SS}	M
L	GPIO27	GPIO106	GPIO107	GPIO108	V_{SS}	V_{SS}	L	V_{SS}	V_{SS}	V_{SS}	L
K	GPIO26	GPIO25	GPIO24	GPIO23	V_{DD}	V_{DD}	K	V_{SS}	V_{SS}	V_{SS}	K
	1	2	3	4	5	6	7	8	9	10	

A. Only the GPIO function is shown on GPIO terminals. See Table 4-1 for the complete, muxed signal name.

Figure 4-1. 337-Ball ZWT New Fine Pitch Ball Grid Array (Bottom View) – [Quadrant A]

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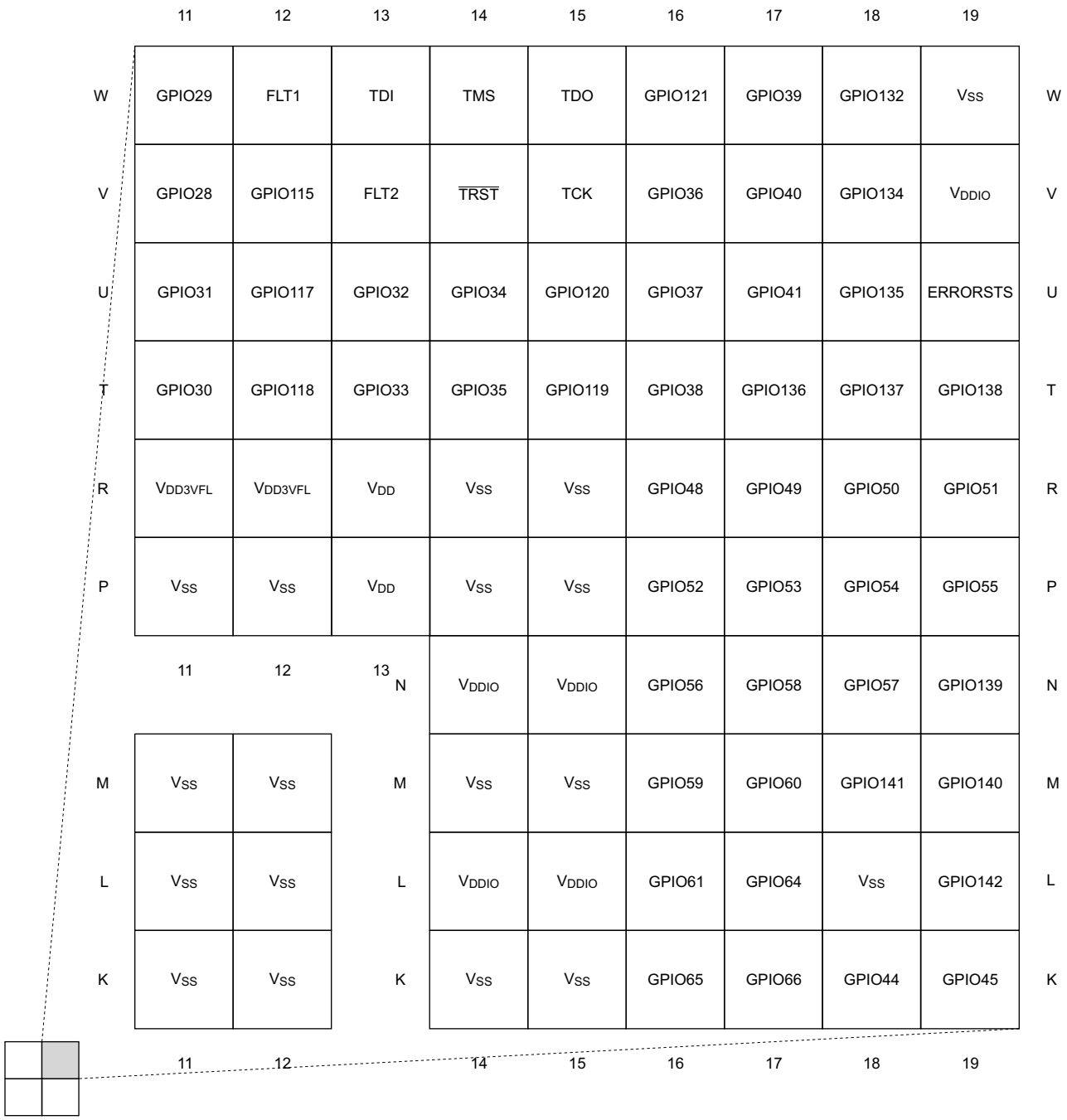

	11	12	13	14	15	16	17	18	19	
W	GPIO29	FLT1	TDI	TMS	TDO	GPIO121	GPIO39	GPIO132	V_{SS}	W
V	GPIO28	GPIO115	FLT2	$\overline{TRST}$	TCK	GPIO36	GPIO40	GPIO134	V_{DDIO}	V
U	GPIO31	GPIO117	GPIO32	GPIO34	GPIO120	GPIO37	GPIO41	GPIO135	ERRORSTS	U
T	GPIO30	GPIO118	GPIO33	GPIO35	GPIO119	GPIO38	GPIO136	GPIO137	GPIO138	T
R	V_{DD3VFL}	V_{DD3VFL}	V_{DD}	V_{SS}	V_{SS}	GPIO48	GPIO49	GPIO50	GPIO51	R
P	V_{SS}	V_{SS}	V_{DD}	V_{SS}	V_{SS}	GPIO52	GPIO53	GPIO54	GPIO55	P
N	V_{DDIO}	V_{DDIO}	GPIO56	GPIO58	GPIO57	GPIO139				N
M	V_{SS}	V_{SS}	V_{SS}	V_{SS}	GPIO59	GPIO60	GPIO141	GPIO140		M
L	V_{SS}	V_{SS}	V_{DDIO}	V_{DDIO}	GPIO61	GPIO64	V_{SS}	GPIO142		L
K	V_{SS}	V_{SS}	V_{SS}	V_{SS}	GPIO65	GPIO66	GPIO44	GPIO45		K

A. Only the GPIO function is shown on GPIO terminals. See Table 4-1 for the complete, muxed signal name.

Figure 4-2. 337-Ball ZWT New Fine Pitch Ball Grid Array (Bottom View) – [Quadrant B]

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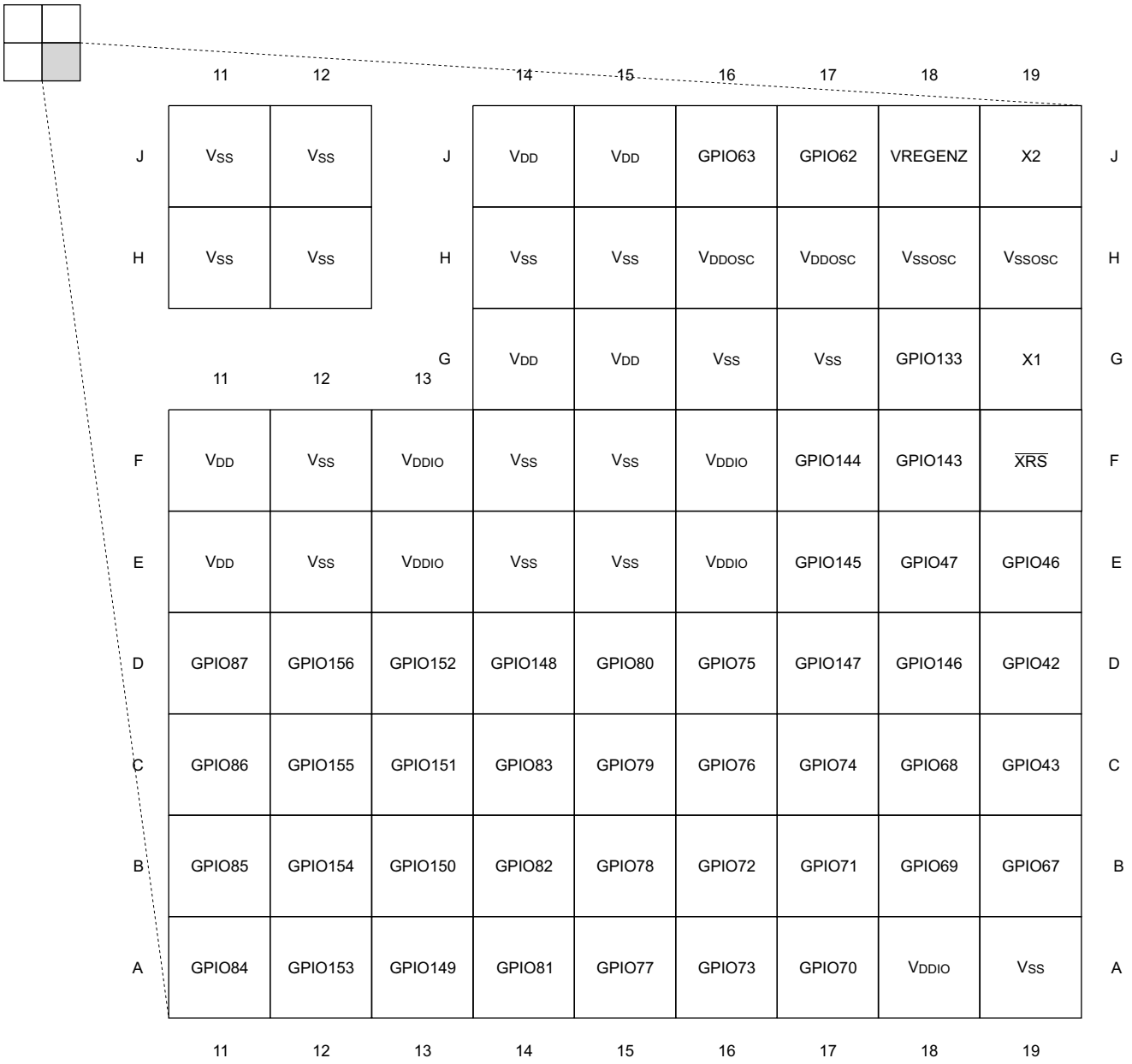

	11	12	13	14	15	16	17	18	19	
J	V_{SS}	V_{SS}	J	V_{DD}	V_{DD}	GPIO63	GPIO62	VREGENZ	X2	J
H	V_{SS}	V_{SS}	H	V_{SS}	V_{SS}	V_{DDOSC}	V_{DDOSC}	V_{SSOSC}	V_{SSOSC}	H
G	11	12	13	V_{DD}	V_{DD}	V_{SS}	V_{SS}	GPIO133	X1	G
F	V_{DD}	V_{SS}	V_{DDIO}	V_{SS}	V_{SS}	V_{DDIO}	GPIO144	GPIO143	$\overline{XRS}$	F
E	V_{DD}	V_{SS}	V_{DDIO}	V_{SS}	V_{SS}	V_{DDIO}	GPIO145	GPIO47	GPIO46	E
D	GPIO87	GPIO156	GPIO152	GPIO148	GPIO80	GPIO75	GPIO147	GPIO146	GPIO42	D
C	GPIO86	GPIO155	GPIO151	GPIO83	GPIO79	GPIO76	GPIO74	GPIO68	GPIO43	C
B	GPIO85	GPIO154	GPIO150	GPIO82	GPIO78	GPIO72	GPIO71	GPIO69	GPIO67	B
A	GPIO84	GPIO153	GPIO149	GPIO81	GPIO77	GPIO73	GPIO70	V_{DDIO}	V_{SS}	A
	11	12	13	14	15	16	17	18	19	

A. Only the GPIO function is shown on GPIO terminals. See Table 4-1 for the complete, muxed signal name.

Figure 4-3. 337-Ball ZWT New Fine Pitch Ball Grid Array (Bottom View) – [Quadrant C]

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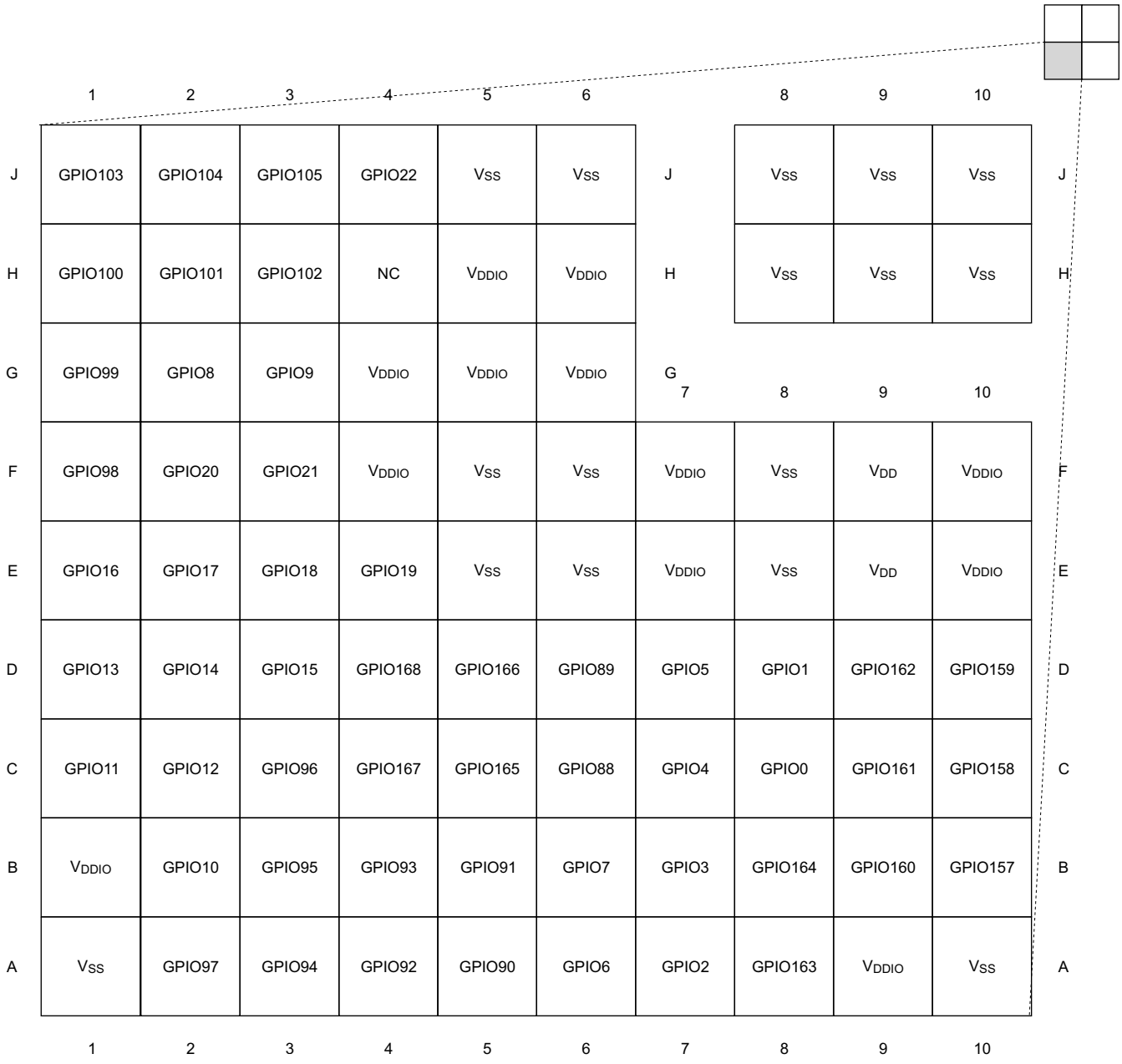

	1	2	3	4	5	6	7	8	9	10	
J	GPIO103	GPIO104	GPIO105	GPIO22	V_{SS}	V_{SS}		V_{SS}	V_{SS}	V_{SS}	J
H	GPIO100	GPIO101	GPIO102	NC	V_{DDIO}	V_{DDIO}		V_{SS}	V_{SS}	V_{SS}	H
G	GPIO99	GPIO8	GPIO9	V_{DDIO}	V_{DDIO}	V_{DDIO}					G
F	GPIO98	GPIO20	GPIO21	V_{DDIO}	V_{SS}	V_{SS}	V_{DDIO}	V_{SS}	V_{DD}	V_{DDIO}	F
E	GPIO16	GPIO17	GPIO18	GPIO19	V_{SS}	V_{SS}	V_{DDIO}	V_{SS}	V_{DD}	V_{DDIO}	E
D	GPIO13	GPIO14	GPIO15	GPIO168	GPIO166	GPIO89	GPIO5	GPIO1	GPIO162	GPIO159	D
C	GPIO11	GPIO12	GPIO96	GPIO167	GPIO165	GPIO88	GPIO4	GPIO0	GPIO161	GPIO158	C
B	V_{DDIO}	GPIO10	GPIO95	GPIO93	GPIO91	GPIO7	GPIO3	GPIO164	GPIO160	GPIO157	B
A	V_{SS}	GPIO97	GPIO94	GPIO92	GPIO90	GPIO6	GPIO2	GPIO163	V_{DDIO}	V_{SS}	A
	1	2	3	4	5	6	7	8	9	10	

A. Only the GPIO function is shown on GPIO terminals. See Table 4-1 for the complete, muxed signal name.

Figure 4-4. 337-Ball ZWT New Fine Pitch Ball Grid Array (Bottom View) – [Quadrant D]

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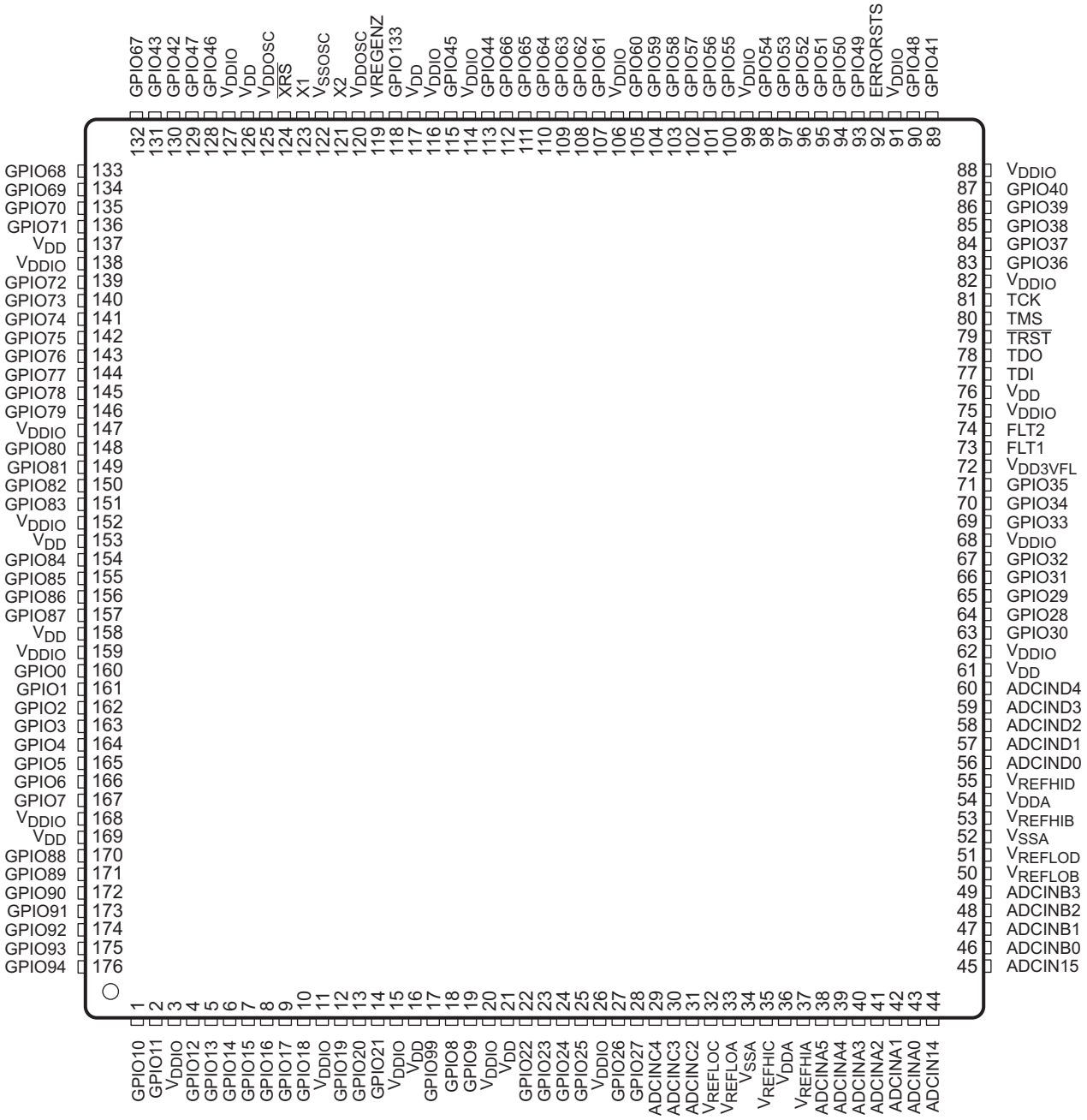

A. Only the GPIO function is shown on GPIO pins. See Table 4-1 for the complete, muxed signal name.

Figure 4-5. 176-Pin PTP PowerPAD Thermally Enhanced Low-Profile Quad Flatpack (Top View)

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4.1 Signal Descriptions

Table 4-1 describes the signals. The GPIO function is the default at reset, unless otherwise mentioned. The peripheral signals that are listed under them are alternate functions. Some peripheral functions may not be available in all devices. See Table 3-1 for details. All GPIO pins are I/O/Z and have an internal pullup, which can be selectively enabled or disabled on a per-pin basis. This feature only applies to the GPIO pins. The pullups are not enabled at reset.

Table 4-1. Signal Descriptions

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
ADC, DAC, AND COMPARATOR SIGNALS					
V_{REFHIA}		V1	37	I	ADC-A high reference. Place at least a 1-µF capacitor on this pin for the 12-bit mode, or at least a 22-µF capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the V_{REFHIA} and V_{REFLOA} pins.
V_{REFHIB}		W5	53	I	ADC-B high reference. Place at least a 1-µF capacitor on this pin for the 12-bit mode, or at least a 22-µF capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the V_{REFHIB} and V_{REFLOB} pins.
V_{REFHIC}		R1	35	I	ADC-C high reference. Place at least a 1-µF capacitor on this pin for the 12-bit mode, or at least a 22-µF capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the V_{REFHIC} and V_{REFLOC} pins.
V_{REFHID}		V5	55	I	ADC-D high reference. Place at least a 1-µF capacitor on this pin for the 12-bit mode, or at least a 22-µF capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the V_{REFHID} and V_{REFLOD} pins.
V_{REFLOA}		R2	33	I	ADC-A low reference
V_{REFLOB}		V6	50	I	ADC-B low reference
V_{REFLOC}		P2	32	I	ADC-C low reference
V_{REFLOD}		W6	51	I	ADC-D low reference
ADCIN14		T4	44	I	Input 14 to all ADCs. This pin can be used as a general-purpose ADCIN pin or it can be used to calibrate all ADCs together (either single-ended or differential) from an external reference.
CMPIN4P				I	Comparator 4 positive input
ADCIN15		U4	45	I	Input 15 to all ADCs. This pin can be used as a general-purpose ADCIN pin or it can be used to calibrate all ADCs together (either single-ended or differential) from an external reference.
CMPIN4N				I	Comparator 4 negative input
ADCINA0		U1	43	I	ADC-A input 0. There is a 50-kΩ internal pulldown on this pin in both an ADC input or DAC output mode which cannot be disabled.
DACOUTA				O	DAC-A output
ADCINA1		T1	42	I	ADC-A input 1. There is a 50-kΩ internal pulldown on this pin in both an ADC input or DAC output mode which cannot be disabled.
DACOUTB				O	DAC-B output
ADCINA2		U2	41	I	ADC-A input 2
CMPIN1P				I	Comparator 1 positive input
ADCINA3		T2	40	I	ADC-A input 3
CMPIN1N				I	Comparator 1 negative input
ADCINA4		U3	39	I	ADC-A input 4
CMPIN2P				I	Comparator 2 positive input

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Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
ADCINA5		T3	38	I	ADC-A input 5
CMPIN2N				I	Comparator 2 negative input
ADCINB0		V2	46	I	ADC-B input 0. There is a 100-pF capacitor to V_{SSA} on this pin in both ADC input or DAC reference mode which cannot be disabled. If this pin is being used as a reference for the on-chip DACs, place at least a 1-µF capacitor on this pin.
VDAC				I	Optional external reference voltage for on-chip DACs. There is a 100-pF capacitor to V_{SSA} on this pin in both ADC input or DAC reference mode which cannot be disabled. If this pin is being used as a reference for the on-chip DACs, place at least a 1-µF capacitor on this pin.
ADCINB1		W2	47	I	ADC-B input 1. There is a 50-kΩ internal pulldown on this pin in both an ADC input or DAC output mode which cannot be disabled.
DACOUTC				O	DAC-C output
ADCINB2		V3	48	I	ADC-B input 2
CMPIN3P				I	Comparator 3 positive input
ADCINB3		W3	49	I	ADC-B input 3
CMPIN3N				I	Comparator 3 negative input
ADCINB4		V4	–	I	ADC-B input 4
ADCINB5		W4	–	I	ADC-B input 5
ADCINC2		R3	31	I	ADC-C input 2
CMPIN6P				I	Comparator 6 positive input
ADCINC3		P3	30	I	ADC-C input 3
CMPIN6N				I	Comparator 6 negative input
ADCINC4		R4	29	I	ADC-C input 4
CMPIN5P				I	Comparator 5 positive input
ADCINC5		P4	–	I	ADC-C input 5
CMPIN5N				I	Comparator 5 negative input
ADCIND0		T5	56	I	ADC-D input 0
CMPIN7P				I	Comparator 7 positive input
ADCIND1		U5	57	I	ADC-D input 1
CMPIN7N				I	Comparator 7 negative input
ADCIND2		T6	58	I	ADC-D input 2
CMPIN8P				I	Comparator 8 positive input
ADCIND3		U6	59	I	ADC-D input 3
CMPIN8N				I	Comparator 8 negative input
ADCIND4		T7	60	I	ADC-D input 4
ADCIND5		U7	–	I	ADC-D input 5
GPIO AND PERIPHERAL SIGNALS[2]					
GPIO0	0, 4, 8, 12	C8	160	I/O	General-purpose input/output 0
EPWM1A	1			O	Enhanced PWM1 output A and HRPWM channel
SDAA	6			I/OD	I2C-A data open-drain bidirectional port
GPIO1	0, 4, 8, 12	D8	161	I/O	General-purpose input/output 1
EPWM1B	1			O	Enhanced PWM1 output B and HRPWM channel
MFSRB	3			I/O	McBSP-B receive frame synch
SCLA	6			I/OD	I2C-A clock open-drain bidirectional port

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Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
GPIO2	0, 4, 8, 12	A7	162	I/O	General-purpose input/output 2
EPWM2A	1			O	Enhanced PWM2 output A and HRPWM channel
OUTPUTXBAR1	5			O	Output 1 of the output XBAR
SDAB	6			I/OD	I2C-B data open-drain bidirectional port
GPIO3	0, 4, 8, 12	B7	163	I/O	General-purpose input/output 3
EPWM2B	1			O	Enhanced PWM2 output B and HRPWM channel
OUTPUTXBAR2	2			O	Output 2 of the output XBAR
MCLKRB	3			I/O	McBSP-B receive clock
OUTPUTXBAR2	5			O	Output 2 of the output XBAR
SCLB	6			I/OD	I2C-B clock open-drain bidirectional port
GPIO4	0, 4, 8, 12	C7	164	I/O	General-purpose input/output 4
EPWM3A	1			O	Enhanced PWM3 output A and HRPWM channel
OUTPUTXBAR3	5			O	Output 3 of the output XBAR
CANTXA	6			O	CAN-A transmit
GPIO5	0, 4, 8, 12	D7	165	I/O	General-purpose input/output 5
EPWM3B	1			O	Enhanced PWM3 output B and HRPWM channel
MFSRA	2			I/O	McBSP-A receive frame synch
OUTPUTXBAR3	3			O	Output 3 of the output XBAR
CANRXA	6			I	CAN-A receive
GPIO6	0, 4, 8, 12	A6	166	I/O	General-purpose input/output 6
EPWM4A	1			O	Enhanced PWM4 output A and HRPWM channel
OUTPUTXBAR4	2			O	Output 4 of the output XBAR
EPWMSYNCO	3			O	External ePWM synch pulse output
EQEP3A	5			I	Enhanced QEP3 input A
CANTXB	6			O	CAN-B transmit
GPIO7	0, 4, 8, 12	B6	167	I/O	General-purpose input/output 7
EPWM4B	1			O	Enhanced PWM4 output B and HRPWM channel
MCLKRA	2			I/O	McBSP-A receive clock
OUTPUTXBAR5	3			O	Output 5 of the output XBAR
EQEP3B	5			I	Enhanced QEP3 input B
CANRXB	6			I	CAN-B receive
GPIO8	0, 4, 8, 12	G2	18	I/O	General-purpose input/output 8
EPWM5A	1			O	Enhanced PWM5 output A and HRPWM channel
CANTXB	2			O	CAN-B transmit
ADCSOCAO	3			O	ADC start-of-conversion A
EQEP3S	5			I/O	Enhanced QEP3 strobe
SCITXDA	6			O	SCI-A transmit data
GPIO9	0, 4, 8, 12	G3	19	I/O	General-purpose input/output 9
EPWM5B	1			O	Enhanced PWM5 output B and HRPWM channel
SCITXDB	2			O	SCI-B transmit data
OUTPUTXBAR6	3			O	Output 6 of the output XBAR
EQEP3I	5			I/O	Enhanced QEP3 index
SCIRXDA	6			I	SCI-A receive data

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Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
GPIO10	0, 4, 8, 12	B2	1	I/O	General-purpose input/output 10
EPWM6A	1			O	Enhanced PWM6 output A and HRPWM channel
CANRXB	2			I	CAN-B receive
ADCSOCBO	3			O	ADC start-of-conversion B
EQEP1A	5			I	Enhanced QEP1 input A
SCITXDB	6			O	SCI-B transmit data
GPIO11	0, 4, 8, 12	C1	2	I/O	General-purpose input/output 11
EPWM6B	1			O	Enhanced PWM6 output B and HRPWM channel
SCIRXDB	2, 6			I	SCI-B receive data
OUTPUTXBAR7	3			O	Output 7 of the output XBAR
EQEP1B	5			I	Enhanced QEP1 input B
GPIO12	0, 4, 8, 12	C2	4	I/O	General-purpose input/output 12
EPWM7A	1			O	Enhanced PWM7 output A and HRPWM channel
CANTXB	2			O	CAN-B transmit
MDXB	3			O	McBSP-B transmit serial data
EQEP1S	5			I/O	Enhanced QEP1 strobe
SCITXDC	6			O	SCI-C transmit data
GPIO13	0, 4, 8, 12	D1	5	I/O	General-purpose input/output 13
EPWM7B	1			O	Enhanced PWM7 output B and HRPWM channel
CANRXB	2			I	CAN-B receive
MDRB	3			I	McBSP-B receive serial data
EQEP1I	5			I/O	Enhanced QEP1 index
SCIRXDC	6			I	SCI-C receive data
GPIO14	0, 4, 8, 12	D2	6	I/O	General-purpose input/output 14
EPWM8A	1			O	Enhanced PWM8 output A and HRPWM channel
SCITXDB	2			O	SCI-B transmit data
MCLKXB	3			I/O	McBSP-B transmit clock
OUTPUTXBAR3	6			O	Output 3 of the output XBAR
GPIO15	0, 4, 8, 12	D3	7	I/O	General-purpose input/output 15
EPWM8B	1			O	Enhanced PWM8 output B and HRPWM channel
SCIRXDB	2			I	SCI-B receive data
MFSXB	3			I/O	McBSP-B transmit frame synch
OUTPUTXBAR4	6			O	Output 4 of the output XBAR
GPIO16	0, 4, 8, 12	E1	8	I/O	General-purpose input/output 16
SPISIMOA	1			I/O	SPI-A slave in, master out
CANTXB	2			O	CAN-B transmit
OUTPUTXBAR7	3			O	Output 7 of the output XBAR
EPWM9A	5			O	Enhanced PWM9 output A
SD1_D1	7			I	Sigma-Delta 1 channel 1 data input
GPIO17	0, 4, 8, 12	E2	9	I/O	General-purpose input/output 17
SPISOMIA	1			I/O	SPI-A slave out, master in
CANRXB	2			I	CAN-B receive
OUTPUTXBAR8	3			O	Output 8 of the output XBAR
EPWM9B	5			O	Enhanced PWM9 output B
SD1_C1	7			I	Sigma-Delta 1 channel 1 clock input

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Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
GPIO18	0, 4, 8, 12	E3	10	I/O	General-purpose input/output 18
SPICLKA	1			I/O	SPI-A clock
SCITXDB	2			O	SCI-B transmit data
CANRXA	3			I	CAN-A receive
EPWM10A	5			O	Enhanced PWM10 output A
SD1_D2	7			I	Sigma-Delta 1 channel 2 data input
GPIO19	0, 4, 8, 12	E4	12	I/O	General-purpose input/output 19
$\overline{\text{SPISTEA}}$	1			I/O	SPI-A slave transmit enable
SCIRXDB	2			I	SCI-B receive data
CANTXA	3			O	CAN-A transmit
EPWM10B	5			O	Enhanced PWM10 output B
SD1_C2	7			I	Sigma-Delta 1 channel 2 clock input
GPIO20	0, 4, 8, 12	F2	13	I/O	General-purpose input/output 20
EQEP1A	1			I	Enhanced QEP1 input A
MDXA	2			O	McBSP-A transmit serial data
CANTXB	3			O	CAN-B transmit
EPWM11A	5			O	Enhanced PWM11 output A
SD1_D3	7			I	Sigma-Delta 1 channel 3 data input
GPIO21	0, 4, 8, 12	F3	14	I/O	General-purpose input/output 21
EQEP1B	1			I	Enhanced QEP1 input B
MDRA	2			I	McBSP-A receive serial data
CANRXB	3			I	CAN-B receive
EPWM11B	5			O	Enhanced PWM11 output B
SD1_C3	7			I	Sigma-Delta 1 channel 3 clock input
GPIO22	0, 2, 4, 8	J4	22	I/O	General-purpose input/output 22
EQEP1S	1			I/O	Enhanced QEP1 strobe
MCLKXA	2			I/O	McBSP-A transmit clock
SCITXDB	3			O	SCI-B transmit data
EPWM12A	5			O	Enhanced PWM12 output A
SPICLKB	6			I/O	SPI-B clock
SD1_D4	7			I	Sigma-Delta 1 channel 4 data input
GPIO23	0, 2, 4, 8	K4	23	I/O	General-purpose input/output 23
EQEP1I	1			I/O	Enhanced QEP1 index
MFSXA	2			I/O	McBSP-A transmit frame synch
SCIRXDB	3			I	SCI-B receive data
EPWM12B	5			O	Enhanced PWM12 output B
$\overline{\text{SPISTEB}}$	6			I/O	SPI-B slave transmit enable
SD1_C4	7			I	Sigma-Delta 1 channel 4 clock input
GPIO24	0, 4, 8, 12	K3	24	I/O	General-purpose input/output 24
OUTPUTXBAR1	1			O	Output 1 of the output XBAR
EQEP2A	2			I	Enhanced QEP2 input A
MDXB	3			O	McBSP-B transmit serial data
SPISIMOB	6			I/O	SPI-B slave in, master out
SD2_D1	7			I	Sigma-Delta 2 channel 1 data input

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Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
GPIO25	0, 4, 8, 12	K2	25	I/O	General-purpose input/output 25
OUTPUTXBAR2	1			O	Output 2 of the output XBAR
EQEP2B	2			I	Enhanced QEP2 input B
MDRB	3			I	McBSP-B receive serial data
SPISOMIB	6			I/O	SPI-B slave out, master in
SD2_C1	7			I	Sigma-Delta 2 channel 1 clock input
GPIO26	0, 4, 8, 12	K1	27	I/O	General-purpose input/output 26
OUTPUTXBAR3	1			O	Output 3 of the output XBAR
EQEP2I	2			I/O	Enhanced QEP2 index
MCLKXB	3			I/O	McBSP-B transmit clock
OUTPUTXBAR3	5			O	Output 3 of the output XBAR
SPICLKB	6			I/O	SPI-B clock
SD2_D2	7			I	Sigma-Delta 2 channel 2 data input
GPIO27	0, 4, 8, 12	L1	28	I/O	General-purpose input/output 27
OUTPUTXBAR4	1			O	Output 4 of the output XBAR
EQEP2S	2			I/O	Enhanced QEP2 strobe
MFSXB	3			I/O	McBSP-B transmit frame synch
OUTPUTXBAR4	5			O	Output 4 of the output XBAR
$\overline{\text{SPISTEB}}$	6			I/O	SPI-B slave transmit enable
SD2_C2	7			I	Sigma-Delta 2 channel 2 clock input
GPIO28	0, 4, 8, 12	V11	64	I/O	General-purpose input/output 28
SCIRXDA	1			I	SCI-A receive data
$\overline{\text{EM1CS4}}$	2			O	External memory interface 1 chip select 4
OUTPUTXBAR5	5			O	Output 5 of the output XBAR
EQEP3A	6			I	Enhanced QEP3 input A
SD2_D3	7			I	Sigma-Delta 2 channel 3 data input
GPIO29	0, 4, 8, 12	W11	65	I/O	General-purpose input/output 29
SCITXDA	1			O	SCI-A transmit data
EM1SDCKE	2			O	External memory interface 1 SDRAM clock enable
OUTPUTXBAR6	5			O	Output 6 of the output XBAR
EQEP3B	6			I	Enhanced QEP3 input B
SD2_C3	7			I	Sigma-Delta 2 channel 3 clock input
GPIO30	0, 4, 8, 12	T11	63	I/O	General-purpose input/output 30
CANRXA	1			I	CAN-A receive
EM1CLK	2			O	External memory interface 1 clock
OUTPUTXBAR7	5			O	Output 7 of the output XBAR
EQEP3S	6			I/O	Enhanced QEP3 strobe
SD2_D4	7			I	Sigma-Delta 2 channel 4 data input
GPIO31	0, 4, 8, 12	U11	66	I/O	General-purpose input/output 31
CANTXA	1			O	CAN-A transmit
$\overline{\text{EM1WE}}$	2			O	External memory interface1 write enable
OUTPUTXBAR8	5			O	Output 8 of the output XBAR
EQEP3I	6			I/O	Enhanced QEP3 index
SD2_C4	7			I	Sigma-Delta 2 channel 4 clock input

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Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
GPIO32	0, 4, 8, 12	U13	67	I/O	General-purpose input/output 32
SDAA	1			I/OD	I2C-A data open-drain bidirectional port
$\overline{\text{EM1CS0}}$	2			O	External memory interface 1 chip select 0
GPIO33	0, 4, 8, 12	T13	69	I/O	General-purpose input/output 33
SCLA	1			I/OD	I2C-A clock open-drain bidirectional port
EM1RNW	2			O	External memory interface 1 read not write
GPIO34	0, 4, 8, 12	U14	70	I/O	General-purpose input/output 34
OUTPUTXBAR1	1			O	Output 1 of the output XBAR
$\overline{\text{EM1CS2}}$	2			O	External memory interface 1 chip select 2
SDAB	6			I/OD	I2C-B data open-drain bidirectional port
GPIO35	0, 4, 8, 12	T14	71	I/O	General-purpose input/output 35
SCIRXDA	1			I	SCI-A receive data
$\overline{\text{EM1CS3}}$	2			O	External memory interface 1 chip select 3
SCLB	6			I/OD	I2C-B clock open-drain bidirectional port
GPIO36	0, 4, 8, 12	V16	83	I/O	General-purpose input/output 36
SCITXDA	1			O	SCI-A transmit data
EM1WAIT	2			I	External memory interface 1 Asynchronous SRAM WAIT
CANRXA	6			I	CAN-A receive
GPIO37	0, 4, 8, 12	U16	84	I/O	General-purpose input/output 37
OUTPUTXBAR2	1			O	Output 2 of the output XBAR
$\overline{\text{EM1OE}}$	2			O	External memory interface 1 output enable
CANTXA	6			O	CAN-A transmit
GPIO38	0, 4, 8, 12	T16	85	I/O	General-purpose input/output 38
EM1A0	2			O	External memory interface 1 address line 0
SCITXDC	5			O	SCI-C transmit data
CANTXB	6			O	CAN-B transmit
GPIO39	0, 4, 8, 12	W17	86	I/O	General-purpose input/output 39
EM1A1	2			O	External memory interface 1 address line 1
SCIRXDC	5			I	SCI-C receive data
CANRXB	6			I	CAN-B receive
GPIO40	0, 4, 8, 12	V17	87	I/O	General-purpose input/output 40
EM1A2	2			O	External memory interface 1 address line 2
SDAB	6			I/OD	I2C-B data open-drain bidirectional port
GPIO41	0, 4, 8, 12	U17	89	I/O	General-purpose input/output 41. For applications using the Hibernate low-power mode, this pin serves as the $\overline{\text{GPIOHIBWAKE}}$ signal. For details, see the "Low Power Modes" section of the System Control chapter in the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual* (SPRUHM8).
EM1A3	2			O	External memory interface 1 address line 3
SCLB	6			I/OD	I2C-B clock open-drain bidirectional port
GPIO42	0, 4, 8, 12	D19	130	I/O	General-purpose input/output 42
SDAA	6			I/OD	I2C-A data open-drain bidirectional port
SCITXDA	15			O	SCI-A transmit data
USB0DM	Analog			I/O	USB PHY differential data

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Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
GPIO43	0, 4, 8, 12	C19	131	I/O	General-purpose input/output 43
SCLA	6			I/OD	I2C-A clock open-drain bidirectional port
SCIRXDA	15			I	SCI-A receive data
USB0DP	Analog			I/O	USB PHY differential data
GPIO44	0, 4, 8, 12	K18	113	I/O	General-purpose input/output 44
EM1A4	2			O	External memory interface 1 address line 4
GPIO45	0, 4, 8, 12	K19	115	I/O	General-purpose input/output 45
EM1A5	2			O	External memory interface 1 address line 5
GPIO46	0, 4, 8, 12	E19	128	I/O	General-purpose input/output 46
EM1A6	2			O	External memory interface 1 address line 6
SCIRXDD	6			I	SCI-D receive data
GPIO47	0, 4, 8, 12	E18	129	I/O	General-purpose input/output 47
EM1A7	2			O	External memory interface 1 address line 7
SCITXDD	6			O	SCI-D transmit data
GPIO48	0, 4, 8, 12	R16	90	I/O	General-purpose input/output 48
OUTPUTXBAR3	1			O	Output 3 of the output XBAR
EM1A8	2			O	External memory interface 1 address line 8
SCITXDA	6			O	SCI-A transmit data
SD1_D1	7			I	Sigma-Delta 1 channel 1 data input
GPIO49	0, 4, 8, 12	R17	93	I/O	General-purpose input/output 49
OUTPUTXBAR4	1			O	Output 4 of the output XBAR
EM1A9	2			O	External memory interface 1 address line 9
SCIRXDA	6			I	SCI-A receive data
SD1_C1	7			I	Sigma-Delta 1 channel 1 clock input
GPIO50	0, 4, 8, 12	R18	94	I/O	General-purpose input/output 50
EQEP1A	1			I	Enhanced QEP1 input A
EM1A10	2			O	External memory interface 1 address line 10
SPISIMOC	6			I/O	SPI-C slave in, master out
SD1_D2	7			I	Sigma-Delta 1 channel 2 data input
GPIO51	0, 4, 8, 12	R19	95	I/O	General-purpose input/output 51
EQEP1B	1			I	Enhanced QEP1 input B
EM1A11	2			O	External memory interface 1 address line 11
SPISOMIC	6			I/O	SPI-C slave out, master in
SD1_C2	7			I	Sigma-Delta 1 channel 2 clock input
GPIO52	0, 4, 8, 12	P16	96	I/O	General-purpose input/output 52
EQEP1S	1			I/O	Enhanced QEP1 strobe
EM1A12	2			O	External memory interface 1 address line 12
SPICLKC	6			I/O	SPI-C clock
SD1_D3	7			I	Sigma-Delta 1 channel 3 data input
GPIO53	0, 4, 8, 12	P17	97	I/O	General-purpose input/output 53
EQEP1I	1			I/O	Enhanced QEP1 index
EM1D31	2			I/O	External memory interface 1 data line 31
EM2D15	3			I/O	External memory interface 2 data line 15
$\overline{\text{SPISTEC}}$	6			I/O	SPI-C slave transmit enable
SD1_C3	7			I	Sigma-Delta 1 channel 3 clock input

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Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
GPIO54	0, 4, 8, 12			I/O	General-purpose input/output 54
SPISIMOA	1			I/O	SPI-A slave in, master out
EM1D30	2			I/O	External memory interface 1 data line 30
EM2D14	3	P18	98	I/O	External memory interface 2 data line 14
EQEP2A	5			I	Enhanced QEP2 input A
SCITXDB	6			O	SCI-B transmit data
SD1_D4	7			I	Sigma-Delta 1 channel 4 data input
GPIO55	0, 4, 8, 12			I/O	General-purpose input/output 55
SPISOMIA	1			I/O	SPI-A slave out, master in
EM1D29	2			I/O	External memory interface 1 data line 29
EM2D13	3	P19	100	I/O	External memory interface 2 data line 13
EQEP2B	5			I	Enhanced QEP2 input B
SCIRXDB	6			I	SCI-B receive data
SD1_C4	7			I	Sigma-Delta 1 channel 4 clock input
GPIO56	0, 4, 8, 12			I/O	General-purpose input/output 56
SPICLKA	1			I/O	SPI-A clock
EM1D28	2			I/O	External memory interface 1 data line 28
EM2D12	3	N16	101	I/O	External memory interface 2 data line 12
EQEP2S	5			I/O	Enhanced QEP2 strobe
SCITXDC	6			O	SCI-C transmit data
SD2_D1	7			I	Sigma-Delta 2 channel 1 data input
GPIO57	0, 4, 8, 12			I/O	General-purpose input/output 57
$\overline{\text{SPISTEA}}$	1			I/O	SPI-A slave transmit enable
EM1D27	2			I/O	External memory interface 1 data line 27
EM2D11	3	N18	102	I/O	External memory interface 2 data line 11
EQEP2I	5			I/O	Enhanced QEP2 index
SCIRXDC	6			I	SCI-C receive data
SD2_C1	7			I	Sigma-Delta 2 channel 1 clock input
GPIO58	0, 4, 8, 12			I/O	General-purpose input/output 58
MCLKRA	1			I/O	McBSP-A receive clock
EM1D26	2			I/O	External memory interface 1 data line 26
EM2D10	3	N17	103	I/O	External memory interface 2 data line 10
OUTPUTXBAR1	5			O	Output 1 of the output XBAR
SPICLKB	6			I/O	SPI-B clock
SD2_D2	7			I	Sigma-Delta 2 channel 2 data input
SPISIMOA	15			I/O	SPI-A slave in, master out[3]
GPIO59	0, 4, 8, 12			I/O	General-purpose input/output 59[4]
MFSRA	1			I/O	McBSP-A receive frame synch
EM1D25	2			I/O	External memory interface 1 data line 25
EM2D9	3	M16	104	I/O	External memory interface 2 data line 9
OUTPUTXBAR2	5			O	Output 2 of the output XBAR
$\overline{\text{SPISTEB}}$	6			I/O	SPI-B slave transmit enable
SD2_C2	7			I	Sigma-Delta 2 channel 2 clock input
SPISOMIA	15			I/O	SPI-A slave out, master in[3]

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Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
GPIO60	0, 4, 8, 12	M17	105	I/O	General-purpose input/output 60
MCLKRB	1			I/O	McBSP-B receive clock
EM1D24	2			I/O	External memory interface 1 data line 24
EM2D8	3			I/O	External memory interface 2 data line 8
OUTPUTXBAR3	5			O	Output 3 of the output XBAR
SPISIMOB	6			I/O	SPI-B slave in, master out
SD2_D3	7			I	Sigma-Delta 2 channel 3 data input
SPICLKA	15			I/O	SPI-A clock[3]
GPIO61	0, 4, 8, 12	L16	107	I/O	General-purpose input/output 61[4]
MFSRB	1			I/O	McBSP-B receive frame synch
EM1D23	2			I/O	External memory interface 1 data line 23
EM2D7	3			I/O	External memory interface 2 data line 7
OUTPUTXBAR4	5			O	Output 4 of the output XBAR
SPISOMIB	6			I/O	SPI-B slave out, master in
SD2_C3	7			I	Sigma-Delta 2 channel 3 clock input
$\overline{\text{SPISTEA}}$	15			I/O	SPI-A slave transmit enable[3]
GPIO62	0, 4, 8, 12	J17	108	I/O	General-purpose input/output 62
SCIRXDC	1			I	SCI-C receive data
EM1D22	2			I/O	External memory interface 1 data line 22
EM2D6	3			I/O	External memory interface 2 data line 6
EQEP3A	5			I	Enhanced QEP3 input A
CANRXA	6			I	CAN-A receive
SD2_D4	7			I	Sigma-Delta 2 channel 4 data input
GPIO63	0, 4, 8, 12	J16	109	I/O	General-purpose input/output 63
SCITXDC	1			O	SCI-C transmit data
EM1D21	2			I/O	External memory interface 1 data line 21
EM2D5	3			I/O	External memory interface 2 data line 5
EQEP3B	5			I	Enhanced QEP3 input B
CANTXA	6			O	CAN-A transmit
SD2_C4	7			I	Sigma-Delta 2 channel 4 clock input
SPISIMOB	15			I/O	SPI-B slave in, master out[3]
GPIO64	0, 4, 8, 12	L17	110	I/O	General-purpose input/output 64[4]
EM1D20	2			I/O	External memory interface 1 data line 20
EM2D4	3			I/O	External memory interface 2 data line 4
EQEP3S	5			I/O	Enhanced QEP3 strobe
SCIRXDA	6			I	SCI-A receive data
SPISOMIB	15			I/O	SPI-B slave out, master in[3]
GPIO65	0, 4, 8, 12	K16	111	I/O	General-purpose input/output 65
EM1D19	2			I/O	External memory interface 1 data line 19
EM2D3	3			I/O	External memory interface 2 data line 3
EQEP3I	5			I/O	Enhanced QEP3 index
SCITXDA	6			O	SCI-A transmit data
SPICLKB	15			I/O	SPI-B clock[3]

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Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
GPIO66	0, 4, 8, 12			I/O	General-purpose input/output 66[4]
EM1D18	2			I/O	External memory interface 1 data line 18
EM2D2	3	K17	112	I/O	External memory interface 2 data line 2
SDAB	6			I/OD	I2C-B data open-drain bidirectional port
$\overline{\text{SPISTEB}}$	15			I/O	SPI-B slave transmit enable[3]
GPIO67	0, 4, 8, 12			I/O	General-purpose input/output 67
EM1D17	2	B19	132	I/O	External memory interface 1 data line 17
EM2D1	3			I/O	External memory interface 2 data line 1
GPIO68	0, 4, 8, 12			I/O	General-purpose input/output 68
EM1D16	2	C18	133	I/O	External memory interface 1 data line 16
EM2D0	3			I/O	External memory interface 2 data line 0
GPIO69	0, 4, 8, 12			I/O	General-purpose input/output 69
EM1D15	2	B18	134	I/O	External memory interface 1 data line 15
SCLB	6			I/OD	I2C-B clock open-drain bidirectional port
SPISIMOC	15			I/O	SPI-C slave in, master out[3]
GPIO70	0, 4, 8, 12			I/O	General-purpose input/output 70[4]
EM1D14	2			I/O	External memory interface 1 data line 14
CANRXA	5	A17	135	I	CAN-A receive
SCITXDB	6			O	SCI-B transmit data
SPISOMIC	15			I/O	SPI-C slave out, master in[3]
GPIO71	0, 4, 8, 12			I/O	General-purpose input/output 71
EM1D13	2			I/O	External memory interface 1 data line 13
CANTXA	5	B17	136	O	CAN-A transmit
SCIRXDB	6			I	SCI-B receive data
SPICLKC	15			I/O	SPI-C clock[3]
GPIO72	0, 4, 8, 12			I/O	General-purpose input/output 72[4]
EM1D12	2			I/O	External memory interface 1 data line 12
CANTXB	5	B16	139	O	CAN-B transmit
SCITXDC	6			O	SCI-C transmit data
$\overline{\text{SPISTEC}}$	15			I/O	SPI-C slave transmit enable[3]
GPIO73	0, 4, 8, 12			I/O	General-purpose input/output 73
EM1D11	2			I/O	External memory interface 1 data line 11
XCLKOUT	3	A16	140	O/Z	External clock output. This pin outputs a divided-down version of a chosen clock signal from within the device. The clock signal is chosen using the CLKSRCCTL3.XCLKOUTSEL bit field while the divide ratio is chosen using the XCLKOUTDIVSEL.XCLKOUTDIV bit field.
CANRXB	5			I	CAN-B receive
SCIRXDC	6			I	SCI-C receive
GPIO74	0, 4, 8, 12	C17	141	I/O	General-purpose input/output 74
EM1D10	2			I/O	External memory interface 1 data line 10
GPIO75	0, 4, 8, 12	D16	142	I/O	General-purpose input/output 75
EM1D9	2			I/O	External memory interface 1 data line 9
GPIO76	0, 4, 8, 12			I/O	General-purpose input/output 76
EM1D8	2	C16	143	I/O	External memory interface 1 data line 8
SCITXDD	6			O	SCI-D transmit data

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Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
GPIO77	0, 4, 8, 12	A15	144	I/O	General-purpose input/output 77
EM1D7	2			I/O	External memory interface 1 data line 7
SCIRXDD	6			I	SCI-D receive data
GPIO78	0, 4, 8, 12	B15	145	I/O	General-purpose input/output 78
EM1D6	2			I/O	External memory interface 1 data line 6
EQEP2A	6			I	Enhanced QEP2 input A
GPIO79	0, 4, 8, 12	C15	146	I/O	General-purpose input/output 79
EM1D5	2			I/O	External memory interface 1 data line 5
EQEP2B	6			I	Enhanced QEP2 input B
GPIO80	0, 4, 8, 12	D15	148	I/O	General-purpose input/output 80
EM1D4	2			I/O	External memory interface 1 data line 4
EQEP2S	6			I/O	Enhanced QEP2 strobe
GPIO81	0, 4, 8, 12	A14	149	I/O	General-purpose input/output 81
EM1D3	2			I/O	External memory interface 1 data line 3
EQEP2I	6			I/O	Enhanced QEP2 index
GPIO82	0, 4, 8, 12	B14	150	I/O	General-purpose input/output 82
EM1D2	2			I/O	External memory interface 1 data line 2
GPIO83	0, 4, 8, 12	C14	151	I/O	General-purpose input/output 83
EM1D1	2			I/O	External memory interface 1 data line 1
GPIO84	0, 4, 8, 12	A11	154	I/O	General-purpose input/output 84
SCITXDA	5			O	SCI-A transmit data
MDXB	6			O	McBSP-B transmit serial data
MDXA	15			O	McBSP-A transmit serial data
GPIO85	0, 4, 8, 12	B11	155	I/O	General-purpose input/output 85
EM1D0	2			I/O	External memory interface 1 data line 0
SCIRXDA	5			I	SCI-A receive data
MDRB	6			I	McBSP-B receive serial data
MDRA	15			I	McBSP-A receive serial data
GPIO86	0, 4, 8, 12	C11	156	I/O	General-purpose input/output 86
EM1A13	2			O	External memory interface 1 address line 13
EM1CAS	3			O	External memory interface 1 column address strobe
SCITXDB	5			O	SCI-B transmit data
MCLKXB	6			I/O	McBSP-B transmit clock
MCLKXA	15			I/O	McBSP-A transmit clock
GPIO87	0, 2, 4, 8	D11	157	I/O	General-purpose input/output 87
EM1A14	2			O	External memory interface 1 address line 14
EM1RAS	3			O	External memory interface 1 row address strobe
SCIRXDB	5			I	SCI-B receive data
MFSXB	6			I/O	McBSP-B transmit frame synch
MFSXA	15			I/O	McBSP-A transmit frame synch
GPIO88	0, 2, 4, 8	C6	170	I/O	General-purpose input/output 88
EM1A15	2			O	External memory interface 1 address line 15
EM1DQM0	3			O	External memory interface 1 Input/output mask for byte 0

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Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
GPIO89	0, 2, 4, 8	D6	171	I/O	General-purpose input/output 89
EM1A16	2			O	External memory interface 1 address line 16
EM1DQM1	3			O	External memory interface 1 Input/output mask for byte 1
SCITXDC	6			O	SCI-C transmit data
GPIO90	0, 2, 4, 8	A5	172	I/O	General-purpose input/output 90
EM1A17	2			O	External memory interface 1 address line 17
EM1DQM2	3			O	External memory interface 1 Input/output mask for byte 2
SCIRXDC	6			I	SCI-C receive data
GPIO91	0, 2, 4, 8	B5	173	I/O	General-purpose input/output 91
EM1A18	2			O	External memory interface 1 address line 18
EM1DQM3	3			O	External memory interface 1 Input/output mask for byte 3
SDAA	6			I/OD	I2C-A data open-drain bidirectional port
GPIO92	0, 2, 4, 8	A4	174	I/O	General-purpose input/output 92
EM1A19	2			O	External memory interface 1 address line 19
EM1BA1	3			O	External memory interface 1 bank address 1
SCLA	6			I/OD	I2C-A clock open-drain bidirectional port
GPIO93	0, 2, 4, 8	B4	175	I/O	General-purpose input/output 93
EM1BA0	3			O	External memory interface 1 bank address 0
SCITXDD	6			O	SCI-D transmit data
GPIO94	0, 2, 4, 8	A3	176	I/O	General-purpose input/output 94
SCIRXDD	6			I	SCI-D receive data
GPIO95	0, 2, 4, 8	B3	–	I/O	General-purpose input/output 95
GPIO96	0, 2, 4, 8	C3	–	I/O	General-purpose input/output 96
EM2DQM1	3			O	External memory interface 2 Input/output mask for byte 1
EQEP1A	5			I	Enhanced QEP1 input A
GPIO97	0, 2, 4, 8	A2	–	I/O	General-purpose input/output 97
EM2DQM0	3			O	External memory interface 2 Input/output mask for byte 0
EQEP1B	5			I	Enhanced QEP1 input B
GPIO98	0, 2, 4, 8	F1	–	I/O	General-purpose input/output 98
EM2A0	3			O	External memory interface 2 address line 0
EQEP1S	5			I/O	Enhanced QEP1 strobe
GPIO99	0, 2, 4, 8	G1	17	I/O	General-purpose input/output 99
EM2A1	3			O	External memory interface 2 address line 1
EQEP1I	5			I/O	Enhanced QEP1 index
GPIO100	0, 4, 8, 12	H1	–	I/O	General-purpose input/output 100
EM2A2	3			O	External memory interface 2 address line 2
EQEP2A	5			I	Enhanced QEP2 input A
SPISIMOC	6			I/O	SPI-C slave in, master out
GPIO101	0, 4, 8, 12	H2	–	I/O	General-purpose input/output 101
EM2A3	3			O	External memory interface 2 address line 3
EQEP2B	5			I	Enhanced QEP2 input B
SPISOMIC	6			I/O	SPI-C slave out, master in

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Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
GPIO102	0, 4, 8, 12	H3	–	I/O	General-purpose input/output 102
EM2A4	3			O	External memory interface 2 address line 4
EQEP2S	5			I/O	Enhanced QEP2 strobe
SPICLKC	6			I/O	SPI-C clock
GPIO103	0, 4, 8, 12	J1	–	I/O	General-purpose input/output 103
EM2A5	3			O	External memory interface 2 address line 5
EQEP2I	5			I/O	Enhanced QEP2 index
$\overline{\text{SPISTEC}}$	6			I/O	SPI-C slave transmit enable
GPIO104	0, 4, 8, 12	J2	–	I/O	General-purpose input/output 104
SDAA	1			I/OD	I2C-A data open-drain bidirectional port
EM2A6	3			O	External memory interface 2 address line 6
EQEP3A	5			I	Enhanced QEP3 input A
SCITXDD	6			O	SCI-D transmit data
GPIO105	0, 4, 8, 12	J3	–	I/O	General-purpose input/output 105
SCLA	1			I/OD	I2C-A clock open-drain bidirectional port
EM2A7	3			O	External memory interface 2 address line 7
EQEP3B	5			I	Enhanced QEP3 input B
SCIRXDD	6			I	SCI-D receive data
GPIO106	0, 4, 8, 12	L2	–	I/O	General-purpose input/output 106
EM2A8	3			O	External memory interface 2 address line 8
EQEP3S	5			I/O	Enhanced QEP3 strobe
SCITXDC	6			O	SCI-C transmit data
GPIO107	0, 4, 8, 12	L3	–	I/O	General-purpose input/output 107
EM2A9	3			O	External memory interface 2 address line 9
EQEP3I	5			I/O	Enhanced QEP3 index
SCIRXDC	6			I	SCI-C receive data
GPIO108	0, 4, 8, 12	L4	–	I/O	General-purpose input/output 108
EM2A10	3			O	External memory interface 2 address line 10
GPIO109	0, 4, 8, 12	N2	–	I/O	General-purpose input/output 109
EM2A11	3			O	External memory interface 2 address line 11
GPIO110	0, 4, 8, 12	M2	–	I/O	General-purpose input/output 110
EM2WAIT	3			I	External memory interface 2 Asynchronous SRAM WAIT
GPIO111	0, 4, 8, 12	M4	–	I/O	General-purpose input/output 111
EM2BA0	3			O	External memory interface 2 bank address 0
GPIO112	0, 4, 8, 12	M3	–	I/O	General-purpose input/output 112
EM2BA1	3			O	External memory interface 2 bank address 1
GPIO113	0, 4, 8, 12	N4	–	I/O	General-purpose input/output 113
EM2CAS	3			O	External memory interface 2 column address strobe
GPIO114	0, 4, 8, 12	N3	–	I/O	General-purpose input/output 114
EM2RAS	3			O	External memory interface 2 row address strobe
GPIO115	0, 4, 8, 12	V12	–	I/O	General-purpose input/output 115
$\overline{\text{EM2CS0}}$	3			O	External memory interface 2 chip select 0
GPIO116	0, 4, 8, 12	W10	–	I/O	General-purpose input/output 116
$\overline{\text{EM2CS2}}$	3			O	External memory interface 2 chip select 2

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Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
GPIO117	0, 4, 8, 12	U12	–	I/O	General-purpose input/output 117
EM2SDCKE	3			O	External memory interface 2 SDRAM clock enable
GPIO118	0, 4, 8, 12	T12	–	I/O	General-purpose input/output 118
EM2CLK	3			O	External memory interface 2 clock
GPIO119	0, 4, 8, 12	T15	–	I/O	General-purpose input/output 119
EM2RNW	3			O	External memory interface 2 read not write
GPIO120	0, 4, 8, 12	U15	–	I/O	General-purpose input/output 120
$\overline{\text{EM2WE}}$	3			O	External memory interface 2 write enable
USB0PFLT	15			I/O	USB external regulator power fault indicator
GPIO121	0, 4, 8, 12	W16	–	I/O	General-purpose input/output 121
$\overline{\text{EM2OE}}$	3			O	External memory interface 2 output enable
USB0EPEN	15			I/O	USB external regulator enable
GPIO122	0, 4, 8, 12	T8	–	I/O	General-purpose input/output 122
SPISIMOC	6			I/O	SPI-C slave in, master out
SD1_D1	7			I	Sigma-Delta 1 channel 1 data input
GPIO123	0, 4, 8, 12	U8	–	I/O	General-purpose input/output 123
SPISOMIC	6			I/O	SPI-C slave out, master in
SD1_C1	7			I	Sigma-Delta 1 channel 1 clock input
GPIO124	0, 4, 8, 12	V8	–	I/O	General-purpose input/output 124
SPICLKC	6			I/O	SPI-C clock
SD1_D2	7			I	Sigma-Delta 1 channel 2 data input
GPIO125	0, 4, 8, 12	T9	–	I/O	General-purpose input/output 125
$\overline{\text{SPISTEC}}$	6			I/O	SPI-C slave transmit enable
SD1_C2	7			I	Sigma-Delta 1 channel 2 clock input
GPIO126	0, 4, 8, 12	U9	–	I/O	General-purpose input/output 126
SD1_D3	7			I	Sigma-Delta 1 channel 3 data input
GPIO127	0, 4, 8, 12	V9	–	I/O	General-purpose input/output 127
SD1_C3	7			I	Sigma-Delta 1 channel 3 clock input
GPIO128	0, 4, 8, 12	W9	–	I/O	General-purpose input/output 128
SD1_D4	7			I	Sigma-Delta 1 channel 4 data input
GPIO129	0, 4, 8, 12	T10	–	I/O	General-purpose input/output 129
SD1_C4	7			I	Sigma-Delta 1 channel 4 clock input
GPIO130	0, 4, 8, 12	U10	–	I/O	General-purpose input/output 130
SD2_D1	7			I	Sigma-Delta 2 channel 1 data input
GPIO131	0, 4, 8, 12	V10	–	I/O	General-purpose input/output 131
SD2_C1	7			I	Sigma-Delta 2 channel 1 clock input
GPIO132	0, 4, 8, 12	W18	–	I/O	General-purpose input/output 132
SD2_D2	7			I	Sigma-Delta 2 channel 2 data input
GPIO133/AUXCLKIN	0, 4, 8, 12	G18	118	I/O	General-purpose input/output 133. The AUXCLKIN function of this GPIO pin could be used to provide a single-ended 3.3-V level clock signal to the Auxiliary Phase-locked Loop (AUXPLL), whose output is used for the USB module. The AUXCLKIN clock may also be used for the CAN module.
SD2_C2	7			I	Sigma-Delta 2 channel 2 clock input
GPIO134	0, 4, 8, 12	V18	–	I/O	General-purpose input/output 134
SD2_D3	7			I	Sigma-Delta 2 channel 3 data input

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Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
GPIO135	0, 4, 8, 12	U18	–	I/O	General-purpose input/output 135
SCITXDA	6			O	SCI-A transmit data
SD2_C3	7			I	Sigma-Delta 2 channel 3 clock input
GPIO136	0, 4, 8, 12	T17	–	I/O	General-purpose input/output 136
SCIRXDA	6			I	SCI-A receive data
SD2_D4	7			I	Sigma-Delta 2 channel 4 data input
GPIO137	0, 4, 8, 12	T18	–	I/O	General-purpose input/output 137
SCITXDB	6			O	SCI-B transmit data
SD2_C4	7			I	Sigma-Delta 2 channel 4 clock input
GPIO138	0, 4, 8, 12	T19	–	I/O	General-purpose input/output 138
SCIRXDB	6			I	SCI-B receive data
GPIO139	0, 4, 8, 12	N19	–	I/O	General-purpose input/output 139
SCIRXDC	6			I	SCI-C receive data
GPIO140	0, 4, 8, 12	M19	–	I/O	General-purpose input/output 140
SCITXDC	6			O	SCI-C transmit data
GPIO141	0, 4, 8, 12	M18	–	I/O	General-purpose input/output 141
SCIRXDD	6			I	SCI-D receive data
GPIO142	0, 4, 8, 12	L19	–	I/O	General-purpose input/output 142
SCITXDD	6			O	SCI-D transmit data
GPIO143	0, 4, 8, 12	F18	–	I/O	General-purpose input/output 143
GPIO144	0, 4, 8, 12	F17	–	I/O	General-purpose input/output 144
GPIO145	0, 4, 8, 12	E17	–	I/O	General-purpose input/output 145
EPWM1A	1			O	Enhanced PWM1 output A and HRPWM channel
GPIO146	0, 4, 8, 12	D18	–	I/O	General-purpose input/output 146
EPWM1B	1			O	Enhanced PWM1 output B and HRPWM channel
GPIO147	0, 4, 8, 12	D17	–	I/O	General-purpose input/output 147
EPWM2A	1			O	Enhanced PWM2 output A and HRPWM channel
GPIO148	0, 4, 8, 12	D14	–	I/O	General-purpose input/output 148
EPWM2B	1			O	Enhanced PWM2 output B and HRPWM channel
GPIO149	0, 4, 8, 12	A13	–	I/O	General-purpose input/output 149
EPWM3A	1			O	Enhanced PWM3 output A and HRPWM channel
GPIO150	0, 4, 8, 12	B13	–	I/O	General-purpose input/output 150
EPWM3B	1			O	Enhanced PWM3 output B and HRPWM channel
GPIO151	0, 4, 8, 12	C13	–	I/O	General-purpose input/output 151
EPWM4A	1			O	Enhanced PWM4 output A and HRPWM channel
GPIO152	0, 4, 8, 12	D13	–	I/O	General-purpose input/output 152
EPWM4B	1			O	Enhanced PWM4 output B and HRPWM channel
GPIO153	0, 4, 8, 12	A12	–	I/O	General-purpose input/output 153
EPWM5A	1			O	Enhanced PWM5 output A and HRPWM channel
GPIO154	0, 4, 8, 12	B12	–	I/O	General-purpose input/output 154
EPWM5B	1			O	Enhanced PWM5 output B and HRPWM channel
GPIO155	0, 4, 8, 12	C12	–	I/O	General-purpose input/output 155
EPWM6A	1			O	Enhanced PWM6 output A and HRPWM channel
GPIO156	0, 4, 8, 12	D12	–	I/O	General-purpose input/output 156
EPWM6B	1			O	Enhanced PWM6 output B and HRPWM channel

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Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
GPIO157	0, 4, 8, 12	B10	–	I/O	General-purpose input/output 157
EPWM7A	1			O	Enhanced PWM7 output A and HRPWM channel
GPIO158	0, 4, 8, 12	C10	–	I/O	General-purpose input/output 158
EPWM7B	1			O	Enhanced PWM7 output B and HRPWM channel
GPIO159	0, 4, 8, 12	D10	–	I/O	General-purpose input/output 159
EPWM8A	1			O	Enhanced PWM8 output A and HRPWM channel
GPIO160	0, 4, 8, 12	B9	–	I/O	General-purpose input/output 160
EPWM8B	1			O	Enhanced PWM8 output B and HRPWM channel
GPIO161	0, 4, 8, 12	C9	–	I/O	General-purpose input/output 161
EPWM9A	1			O	Enhanced PWM9 output A
GPIO162	0, 4, 8, 12	D9	–	I/O	General-purpose input/output 162
EPWM9B	1			O	Enhanced PWM9 output B
GPIO163	0, 4, 8, 12	A8	–	I/O	General-purpose input/output 163
EPWM10A	1			O	Enhanced PWM10 output A
GPIO164	0, 4, 8, 12	B8	–	I/O	General-purpose input/output 164
EPWM10B	1			O	Enhanced PWM10 output B
GPIO165	0, 4, 8, 12	C5	–	I/O	General-purpose input/output 165
EPWM11A	1			O	Enhanced PWM11 output A
GPIO166	0, 4, 8, 12	D5	–	I/O	General-purpose input/output 166
EPWM11B	1			O	Enhanced PWM11 output B
GPIO167	0, 4, 8, 12	C4	–	I/O	General-purpose input/output 167
EPWM12A	1			O	Enhanced PWM12 output A
GPIO168	0, 4, 8, 12	D4	–	I/O	General-purpose input/output 168
EPWM12B	1			O	Enhanced PWM12 output B
RESET					
$\overline{\text{XRS}}$		F19	124	I/OD	Device Reset (in) and Watchdog Reset (out). The devices have a built-in power-on reset (POR) circuit. During a power-on condition, this pin is driven low by the device. An external circuit may also drive this pin to assert a device reset. This pin is also driven low by the MCU when a watchdog reset occurs. During watchdog reset, the $\overline{\text{XRS}}$ pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. A resistor between 2.2 kΩ and 10 kΩ should be placed between $\overline{\text{XRS}}$ and V_{DDIO}. If a capacitor is placed between $\overline{\text{XRS}}$ and V_{SS} for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the $\overline{\text{XRS}}$ pin to V_{OL} within 512 OSCCLK cycles when the watchdog reset is asserted. Regardless of the source, a device reset causes the device to terminate execution. The program counter points to the address contained at the location 0x3F FFC0. When reset is deactivated, execution begins at the location designated by the program counter. The output buffer of this pin is an open-drain with an internal pullup. (↑)
CLOCKS					
X1		G19	123	I	On-chip crystal-oscillator input. To use this oscillator, a quartz crystal must be connected across X1 and X2. If this pin is not used, it must be tied to GND. This pin can also be used to feed a single-ended 3.3-V level clock. In this case, X2 is a No Connect (NC).
X2		J19	121	O	On-chip crystal-oscillator output. A quartz crystal may be connected across X1 and X2. If X2 is not used, it must be left unconnected.

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Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
NO CONNECT					
NC		H4	–		No connect. BGA ball is electrically open and not connected to the die.
JTAG					
TCK		V15	81	I	JTAG test clock with internal pullup (see Section 5.4)
TDI		W13	77	I	JTAG test data input (TDI) with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
TDO		W15	78	O/Z	JTAG scan out, test data output (TDO). The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK.[4]
TMS		W14	80	I	JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK.
$\overline{\text{TRST}}$		V14	79	I	JTAG test reset with internal pulldown. $\overline{\text{TRST}}$, when driven high, gives the scan system control of the operations of the device. If this signal is not connected or driven low, the device operates in its functional mode, and the test reset signals are ignored. NOTE: $\overline{\text{TRST}}$ is an active-low test pin and must be maintained low at all times during normal device operation. An external pulldown resistor is required on this pin. The value of this resistor should be based on drive strength of the debugger pods applicable to the design. A 2.2-kΩ resistor generally offers adequate protection. Because the value of the resistor is application-specific, TI recommends that each target board be validated for proper operation of the debugger and the application. This pin has an internal 50-ns (nominal) glitch filter.
INTERNAL VOLTAGE REGULATOR CONTROL					
VREGENZ		J18	119	I	Internal voltage regulator enable with internal pulldown. The internal VREG is not supported and must be disabled. Connect VREGENZ to V_{DDIO}.
ANALOG, DIGITAL, AND I/O POWER					
V_{DD}		E9	16		1.2-V digital logic power pins. Place a decoupling capacitor on each V_{DD} pin such that the total capacitance on the V_{DD} supply rail is evenly distributed and between 12 µF and 26.5 µF.
		E11	21		
		F9	61		
		F11	76		
		G14	117		
		G15	126		
		J14	137		
		J15	153		
		K5	158		
		K6	169		
		P10	–		
		P13	–		
		R10	–		
		R13	–		
V_{DD3VFL}		R11	72		3.3-V Flash power pin. Place a minimum 0.1-µF decoupling capacitor on each pin.
		R12	–		
V_{DDA}		P6	36		3.3-V analog power pins. Place a minimum 2.2-µF decoupling capacitor on each pin.
		R6	54		

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Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
V_{DDIO}		A9	3		3.3-V digital I/O power pins. Place a minimum 0.1-µF decoupling capacitor on each pin.
		A18	11		
		B1	15		
		E7	20		
		E10	26		
		E13	62		
		E16	68		
		F4	75		
		F7	82		
		F10	88		
		F13	91		
		F16	99		
		G4	106		
		G5	114		
		G6	116		
		H5	127		
		H6	138		
		L14	147		
		L15	152		
		M1	159		
		M5	168		
		M6	–		
		N14	–		
		N15	–		
		P9	–		
		R9	–		
		V19	–		
		W8	–		
V_{DDOSC}		H16	120		3.3-V on-chip crystal oscillator (X1 and X2) power pins. Place a minimum 0.1-µF decoupling capacitor on each pin.
		H17	125		

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Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
V_{SS}		A1	PWR PAD		Analog and digital ground. For Quad Flatpacks (QFPs), the PowerPad on the bottom of the package must be soldered to the ground plane of the PCB.
		A10			
		A19			
		E5			
		E6			
		E8			
		E12			
		E14			
		E15			
		F5			
		F6			
		F8			
		F12			
		F14			
		F15			
		G16			
		G17			
		H8			
		H9			
		H10			
		H11			
		H12			
		H14			
		H15			
		J5			
		J6			
		J8			
		J9			
		J10			
		J11			
		J12			
		K8			
		K9			
		K10			
		K11			
		K12			
		K14			
		K15			
		L5			
		L6			
		L8			
		L9			

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Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
V_{SS}		L10	PWR PAD		Analog and digital ground. For Quad Flatpacks (QFPs), the PowerPad on the bottom of the package must be soldered to the ground plane of the PCB.
		L11			
		L12			
		L18			
		M8			
		M9			
		M10			
		M11			
		M12			
		M14			
		M15			
		N1			
		N5			
		N6			
		P7			
		P8			
		P11			
		P12			
		P14			
		P15			
		R7			
		R8			
		R14			
		R15			
		W7			
		W19			
V_{SSOSC}		H18	122		Crystal oscillator (X1 and X2) ground pin. When using an external crystal, do not connect this pin to the board ground. Instead, connect it to the ground reference of the external crystal oscillator circuit. If an external crystal is not used, this pin may be connected to the board ground.
		H19	–		
V_{SSA}		P1	34		Analog module ground pins
		P5	52		
		R5	–		
		V7	–		
		W1	–		

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Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.		
SPECIAL FUNCTIONS					
ERRORSTS		U19	92	O	Error status output. This pin has pulldown.
TEST PINS					
FLT1		W12	73	I/O	Flash test pin 1. Reserved for TI. Must be left unconnected.
FLT2		V13	74	I/O	Flash test pin 2. Reserved for TI. Must be left unconnected.

(1) I = Input, O = Output, OD = Open Drain, Z = High Impedance

(2) The maximum toggling frequency of the GPIOs on F2837xD is 50 MHz.

(3) High-Speed SPI-enabled GPIO mux option. This pin mux option is required when using the SPI in High-Speed Mode (HS_MODE = 1 in SPICCR). This mux option is still available when not using the SPI in High-Speed Mode (HS_MODE = 0 in SPICCR).

(4) This pin has output impedance that can be as low as 22 Ω. This output could have fast edges and ringing depending on the system PCB characteristics. If this is a concern, the user should take precautions such as adding a 39Ω (10% tolerance) series termination resistor or implement some other termination scheme. It is also recommended that a system-level signal integrity analysis be performed with the provided IBIS models. The termination is not required if this pin is used for input function.

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4.2 Pins With Internal Pullup and Pulldown

Some pins on the device have internal pullups or pulldowns. Table 4-2 lists the pull direction and when it is active. The pullups on GPIO pins are disabled by default and can be enabled through software. In order to avoid any floating unbonded inputs, the Boot ROM will enable internal pullups on GPIO pins that are not bonded out in a particular package. Other pins noted in Table 4-2 with pullups and pulldowns are always on and cannot be disabled.

Table 4-2. Pins With Internal Pullup and Pulldown

PIN	POWER UP[1]	RESET ($\overline{XRS}$ = 0)	DEVICE BOOT	APPLICATION SOFTWARE
GPIOx	Pullup disabled		Pullup disabled[2]	Application-defined
$\overline{TRST}$	Pulldown active			
TCK	Pullup active			
TMS	Pullup active			
TDI	Pullup active			
$\overline{XRS}$	Undefined	Pullup active		
VREGENZ	Undefined	Pulldown active		
ERRORSTS	Pulldown active			
Other pins	No pullup or pulldown present			

(1) Before V_{DD} and V_{DDIO} reach recommended operating conditions.
(2) Pins not bonded out in a given package will have the internal pullups enabled by the Boot ROM.

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4.3 Pin Multiplexing

4.3.1 GPIO Muxed Pins

Table 4-3 shows the GPIO muxed pins. The default for each pin is the GPIO function, secondary functions can be selected by setting both the GPyGMUXn.GPIOz and GPyMUXn.GPIOz register bits. The GPyGMUXn register should be configured prior to the GPyMUXn to avoid transient pulses on GPIO's from alternate mux selections. Columns not shown and blank cells are reserved GPIO Mux settings.

Table 4-3. GPIO Muxed Pins(1)(2)

	GPIO Mux Selection							
GPIO Index	**0, 4, 8, 12**	**1**	**2**	**3**	**5**	**6**	**7**	**15**
GPyGMUXn. GPIOz =	**00b, 01b, 10b, 11b**	**00b**			**01b**			**11b**
GPyMUXn. GPIOz =	**00b**	**01b**	**10b**	**11b**	**01b**	**10b**	**11b**	**11b**
	GPIO0	EPWM1A (O)				SDAA (I/OD)		
	GPIO1	EPWM1B (O)		MFSRB (I/O)		SCLA (I/OD)		
	GPIO2	EPWM2A (O)			OUTPUTXBAR1 (O)	SDAB (I/OD)		
	GPIO3	EPWM2B (O)	OUTPUTXBAR2 (O)	MCLKRB (I/O)	OUTPUTXBAR2 (O)	SCLB (I/OD)		
	GPIO4	EPWM3A (O)			OUTPUTXBAR3 (O)	CANTXA (O)		
	GPIO5	EPWM3B (O)	MFSRA (I/O)	OUTPUTXBAR3 (O)		CANRXA (I)		
	GPIO6	EPWM4A (O)	OUTPUTXBAR4 (O)	EPWMSYNCO (O)	EQEP3A (I)	CANTXB (O)		
	GPIO7	EPWM4B (O)	MCLKRA (I/O)	OUTPUTXBAR5 (O)	EQEP3B (I)	CANRXB (I)		
	GPIO8	EPWM5A (O)	CANTXB (O)	ADCSOCAO (O)	EQEP3S (I/O)	SCITXDA (O)		
	GPIO9	EPWM5B (O)	SCITXDB (O)	OUTPUTXBAR6 (O)	EQEP3I (I/O)	SCIRXDA (I)		
	GPIO10	EPWM6A (O)	CANRXB (I)	ADCSOCBO (O)	EQEP1A (I)	SCITXDB (O)		UPP-WAIT (I/O)
	GPIO11	EPWM6B (O)	SCIRXDB (I)	OUTPUTXBAR7 (O)	EQEP1B (I)	SCIRXDB (I)		UPP-STRT (I/O)
	GPIO12	EPWM7A (O)	CANTXB (O)	MDXB (O)	EQEP1S (I/O)	SCITXDC (O)		UPP-ENA (I/O)
	GPIO13	EPWM7B (O)	CANRXB (I)	MDRB (I)	EQEP1I (I/O)	SCIRXDC (I)		UPP-D7 (I/O)
	GPIO14	EPWM8A (O)	SCITXDB (O)	MCLKXB (I/O)		OUTPUTXBAR3 (O)		UPP-D6 (I/O)
	GPIO15	EPWM8B (O)	SCIRXDB (I)	MFSXB (I/O)		OUTPUTXBAR4 (O)		UPP-D5 (I/O)
	GPIO16	SPISIMOA (I/O)	CANTXB (O)	OUTPUTXBAR7 (O)	EPWM9A (O)		SD1_D1 (I)	UPP-D4 (I/O)
	GPIO17	SPISOMIA (I/O)	CANRXB (I)	OUTPUTXBAR8 (O)	EPWM9B (O)		SD1_C1 (I)	UPP-D3 (I/O)
	GPIO18	SPICLKA (I/O)	SCITXDB (O)	CANRXA (I)	EPWM10A (O)		SD1_D2 (I)	UPP-D2 (I/O)
	GPIO19	$\overline{\text{SPISTEA}}$ (I/O)	SCIRXDB (I)	CANTXA (O)	EPWM10B (O)		SD1_C2 (I)	UPP-D1 (I/O)
	GPIO20	EQEP1A (I)	MDXA (O)	CANTXB (O)	EPWM11A (O)		SD1_D3 (I)	UPP-D0 (I/O)
	GPIO21	EQEP1B (I)	MDRA (I)	CANRXB (I)	EPWM11B (O)		SD1_C3 (I)	UPP-CLK (I/O)
	GPIO22	EQEP1S (I/O)	MCLKXA (I/O)	SCITXDB (O)	EPWM12A (O)	SPICLKB (I/O)	SD1_D4 (I)	
	GPIO23	EQEP1I (I/O)	MFSXA (I/O)	SCIRXDB (I)	EPWM12B (O)	$\overline{\text{SPISTEB}}$ (I/O)	SD1_C4 (I)	
	GPIO24	OUTPUTXBAR1 (O)	EQEP2A (I)	MDXB (O)		SPISIMOB (I/O)	SD2_D1 (I)	
	GPIO25	OUTPUTXBAR2 (O)	EQEP2B (I)	MDRB (I)		SPISOMIB (I/O)	SD2_C1 (I)	
	GPIO26	OUTPUTXBAR3 (O)	EQEP2I (I/O)	MCLKXB (I/O)	OUTPUTXBAR3 (O)	SPICLKB (I/O)	SD2_D2 (I)	
	GPIO27	OUTPUTXBAR4 (O)	EQEP2S (I/O)	MFSXB (I/O)	OUTPUTXBAR4 (O)	$\overline{\text{SPISTEB}}$ (I/O)	SD2_C2 (I)	
	GPIO28	SCIRXDA (I)	$\overline{\text{EM1CS4}}$ (O)		OUTPUTXBAR5 (O)	EQEP3A (I)	SD2_D3 (I)	
	GPIO29	SCITXDA (O)	EM1SDCKE (O)		OUTPUTXBAR6 (O)	EQEP3B (I)	SD2_C3 (I)	
	GPIO30	CANRXA (I)	EM1CLK (O)		OUTPUTXBAR7 (O)	EQEP3S (I/O)	SD2_D4 (I)	
	GPIO31	CANTXA (O)	$\overline{\text{EM1WE}}$ (O)		OUTPUTXBAR8 (O)	EQEP3I (I/O)	SD2_C4 (I)	
	GPIO32	SDAA (I/OD)	$\overline{\text{EM1CS0}}$ (O)					
	GPIO33	SCLA (I/OD)	EM1RNW (O)					
	GPIO34	OUTPUTXBAR1 (O)	$\overline{\text{EM1CS2}}$ (O)			SDAB (I/OD)		
	GPIO35	SCIRXDA (I)	$\overline{\text{EM1CS3}}$ (O)			SCLB (I/OD)		
	GPIO36	SCITXDA (O)	EM1WAIT (I)			CANRXA (I)		
	GPIO37	OUTPUTXBAR2 (O)	$\overline{\text{EM1OE}}$ (O)			CANTXA (O)		
	GPIO38		EM1A0 (O)		SCITXDC (O)	CANTXB (O)		
	GPIO39		EM1A1 (O)		SCIRXDC (I)	CANRXB (I)		

(1) I = Input, O = Output, OD = Open Drain
(2) GPIO Index settings of 9, 10, 11, 13, and 14 are reserved.

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Table 4-3. GPIO Muxed Pins[1][2] (continued)

	GPIO Mux Selection							
GPIO Index	**0, 4, 8, 12**	**1**	**2**	**3**	**5**	**6**	**7**	**15**
GPyGMUXn. GPIOz =	**00b, 01b, 10b, 11b**	**00b**			**01b**			**11b**
GPyMUXn. GPIOz =	**00b**	**01b**	**10b**	**11b**	**01b**	**10b**	**11b**	**11b**
	GPIO40		EM1A2 (O)			SDAB (I/OD)		
	GPIO41		EM1A3 (O)			SCLB (I/OD)		
	GPIO42					SDAA (I/OD)		SCITXDA (O)
	GPIO43					SCLA (I/OD)		SCIRXDA (I)
	GPIO44		EM1A4 (O)					
	GPIO45		EM1A5 (O)					
	GPIO46		EM1A6 (O)			SCIRXDD (I)		
	GPIO47		EM1A7 (O)			SCITXDD (O)		
	GPIO48	OUTPUTXBAR3 (O)	EM1A8 (O)			SCITXDA (O)	SD1_D1 (I)	
	GPIO49	OUTPUTXBAR4 (O)	EM1A9 (O)			SCIRXDA (I)	SD1_C1 (I)	
	GPIO50	EQEP1A (I)	EM1A10 (O)			SPISIMOC (I/O)	SD1_D2 (I)	
	GPIO51	EQEP1B (I)	EM1A11 (O)			SPISOMIC (I/O)	SD1_C2 (I)	
	GPIO52	EQEP1S (I/O)	EM1A12 (O)			SPICLKC (I/O)	SD1_D3 (I)	
	GPIO53	EQEP1I (I/O)	EM1D31 (I/O)	EM2D15 (I/O)		$\overline{\text{SPISTEC}}$ (I/O)	SD1_C3 (I)	
	GPIO54	SPISIMOA (I/O)	EM1D30 (I/O)	EM2D14 (I/O)	EQEP2A (I)	SCITXDB (O)	SD1_D4 (I)	
	GPIO55	SPISOMIA (I/O)	EM1D29 (I/O)	EM2D13 (I/O)	EQEP2B (I)	SCIRXDB (I)	SD1_C4 (I)	
	GPIO56	SPICLKA (I/O)	EM1D28 (I/O)	EM2D12 (I/O)	EQEP2S (I/O)	SCITXDC (O)	SD2_D1 (I)	
	GPIO57	$\overline{\text{SPISTEA}}$ (I/O)	EM1D27 (I/O)	EM2D11 (I/O)	EQEP2I (I/O)	SCIRXDC (I)	SD2_C1 (I)	
	GPIO58	MCLKRA (I/O)	EM1D26 (I/O)	EM2D10 (I/O)	OUTPUTXBAR1 (O)	SPICLKB (I/O)	SD2_D2 (I)	SPISIMOA[3] (I/O)
	GPIO59	MFSRA (I/O)	EM1D25 (I/O)	EM2D9 (I/O)	OUTPUTXBAR2 (O)	$\overline{\text{SPISTEB}}$ (I/O)	SD2_C2 (I)	SPISOMIA[3] (I/O)
	GPIO60	MCLKRB (I/O)	EM1D24 (I/O)	EM2D8 (I/O)	OUTPUTXBAR3 (O)	SPISIMOB (I/O)	SD2_D3 (I)	SPICLKA[3] (I/O)
	GPIO61	MFSRB (I/O)	EM1D23 (I/O)	EM2D7 (I/O)	OUTPUTXBAR4 (O)	SPISOMIB (I/O)	SD2_C3 (I)	$\overline{\text{SPISTEA}}$[3] (I/O)
	GPIO62	SCIRXDC (I)	EM1D22 (I/O)	EM2D6 (I/O)	EQEP3A (I)	CANRXA (I)	SD2_D4 (I)	
	GPIO63	SCITXDC (O)	EM1D21 (I/O)	EM2D5 (I/O)	EQEP3B (I)	CANTXA (O)	SD2_C4 (I)	SPISIMOB[3] (I/O)
	GPIO64		EM1D20 (I/O)	EM2D4 (I/O)	EQEP3S (I/O)	SCIRXDA (I)		SPISOMIB[3] (I/O)
	GPIO65		EM1D19 (I/O)	EM2D3 (I/O)	EQEP3I (I/O)	SCITXDA (O)		SPICLKB[3] (I/O)
	GPIO66		EM1D18 (I/O)	EM2D2 (I/O)		SDAB (I/OD)		$\overline{\text{SPISTEB}}$[3] (I/O)
	GPIO67		EM1D17 (I/O)	EM2D1 (I/O)				
	GPIO68		EM1D16 (I/O)	EM2D0 (I/O)				
	GPIO69		EM1D15 (I/O)			SCLB (I/OD)		SPISIMOC[3] (I/O)
	GPIO70		EM1D14 (I/O)		CANRXA (I)	SCITXDB (O)		SPISOMIC[3] (I/O)
	GPIO71		EM1D13 (I/O)		CANTXA (O)	SCIRXDB (I)		SPICLKC[3] (I/O)
	GPIO72		EM1D12 (I/O)		CANTXB (O)	SCITXDC (O)		$\overline{\text{SPISTEC}}$[3] (I/O)
	GPIO73		EM1D11 (I/O)	XCLKOUT (O)	CANRXB (I)	SCIRXDC (I)		
	GPIO74		EM1D10 (I/O)					
	GPIO75		EM1D9 (I/O)					
	GPIO76		EM1D8 (I/O)			SCITXDD (O)		
	GPIO77		EM1D7 (I/O)			SCIRXDD (I)		
	GPIO78		EM1D6 (I/O)			EQEP2A (I)		
	GPIO79		EM1D5 (I/O)			EQEP2B (I)		
	GPIO80		EM1D4 (I/O)			EQEP2S (I/O)		
	GPIO81		EM1D3 (I/O)			EQEP2I (I/O)		
	GPIO82		EM1D2 (I/O)					
	GPIO83		EM1D1 (I/O)					
	GPIO84				SCITXDA (O)	MDXB (O)		MDXA (O)
	GPIO85		EM1D0 (I/O)		SCIRXDA (I)	MDRB (I)		MDRA (I)
	GPIO86		EM1A13 (O)	EM1CAS (O)	SCITXDB (O)	MCLKXB (I/O)		MCLKXA (I/O)
	GPIO87		EM1A14 (O)	EM1RAS (O)	SCIRXDB (I)	MFSXB (I/O)		MFSXA (I/O)
	GPIO88		EM1A15 (O)	EM1DQM0 (O)				
	GPIO89		EM1A16 (O)	EM1DQM1 (O)		SCITXDC (O)		

(3) High-Speed SPI-enabled GPIO mux option. This pin mux option is required when using the SPI in High-Speed Mode (HS_MODE = 1 in SPICCR). This mux option is still available when not using the SPI in High-Speed Mode (HS_MODE = 0 in SPICCR).

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Table 4-3. GPIO Muxed Pins[1][2] (continued)

	GPIO Mux Selection							
GPIO Index	**0, 4, 8, 12**	**1**	**2**	**3**	**5**	**6**	**7**	**15**
GPyGMUXn. GPIOz =	**00b, 01b, 10b, 11b**	**00b**			**01b**			**11b**
GPyMUXn. GPIOz =	**00b**	**01b**	**10b**	**11b**	**01b**	**10b**	**11b**	**11b**
	GPIO90		EM1A17 (O)	EM1DQM2 (O)		SCIRXDC (I)		
	GPIO91		EM1A18 (O)	EM1DQM3 (O)		SDAA (I/OD)		
	GPIO92		EM1A19 (O)	EM1BA1 (O)		SCLA (I/OD)		
	GPIO93			EM1BA0 (O)		SCITXDD (O)		
	GPIO94					SCIRXDD (I)		
	GPIO95							
	GPIO96			EM2DQM1 (O)	EQEP1A (I)			
	GPIO97			EM2DQM0 (O)	EQEP1B (I)			
	GPIO98			EM2A0 (O)	EQEP1S (I/O)			
	GPIO99			EM2A1 (O)	EQEP1I (I/O)			
	GPIO100			EM2A2 (O)	EQEP2A (I)	SPISIMOC (I/O)		
	GPIO101			EM2A3 (O)	EQEP2B (I)	SPISOMIC (I/O)		
	GPIO102			EM2A4 (O)	EQEP2S (I/O)	SPICLKC (I/O)		
	GPIO103			EM2A5 (O)	EQEP2I (I/O)	$\overline{\text{SPISTEC}}$ (I/O)		
	GPIO104	SDAA (I/OD)		EM2A6 (O)	EQEP3A (I)	SCITXDD (O)		
	GPIO105	SCLA (I/OD)		EM2A7 (O)	EQEP3B (I)	SCIRXDD (I)		
	GPIO106			EM2A8 (O)	EQEP3S (I/O)	SCITXDC (O)		
	GPIO107			EM2A9 (O)	EQEP3I (I/O)	SCIRXDC (I)		
	GPIO108			EM2A10 (O)				
	GPIO109			EM2A11 (O)				
	GPIO110			EM2WAIT (I)				
	GPIO111			EM2BA0 (O)				
	GPIO112			EM2BA1 (O)				
	GPIO113			EM2CAS (O)				
	GPIO114			EM2RAS (O)				
	GPIO115			$\overline{\text{EM2CS0}}$ (O)				
	GPIO116			$\overline{\text{EM2CS2}}$ (O)				
	GPIO117			EM2SDCKE (O)				
	GPIO118			EM2CLK (O)				
	GPIO119			EM2RNW (O)				
	GPIO120			$\overline{\text{EM2WE}}$ (O)				USB0PFLT
	GPIO121			$\overline{\text{EM2OE}}$ (O)				USB0EPEN
	GPIO122					SPISIMOC (I/O)	SD1_D1 (I)	
	GPIO123					SPISOMIC (I/O)	SD1_C1 (I)	
	GPIO124					SPICLKC (I/O)	SD1_D2 (I)	
	GPIO125					$\overline{\text{SPISTEC}}$ (I/O)	SD1_C2 (I)	
	GPIO126						SD1_D3 (I)	
	GPIO127						SD1_C3 (I)	
	GPIO128						SD1_D4 (I)	
	GPIO129						SD1_C4 (I)	
	GPIO130						SD2_D1 (I)	
	GPIO131						SD2_C1 (I)	
	GPIO132						SD2_D2 (I)	
	GPIO133/ AUXCLKIN						SD2_C2 (I)	
	GPIO134						SD2_D3 (I)	
	GPIO135					SCITXDA (O)	SD2_C3 (I)	
	GPIO136					SCIRXDA (I)	SD2_D4 (I)	
	GPIO137					SCITXDB (O)	SD2_C4 (I)	
	GPIO138					SCIRXDB (I)		
	GPIO139					SCIRXDC (I)		
	GPIO140					SCITXDC (O)		

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Table 4-3. GPIO Muxed Pins[1][2] (continued)

	GPIO Mux Selection							
GPIO Index	**0, 4, 8, 12**	**1**	**2**	**3**	**5**	**6**	**7**	**15**
GPyGMUXn. GPIOz =	**00b, 01b, 10b, 11b**	**00b**			**01b**			**11b**
GPyMUXn. GPIOz =	**00b**	**01b**	**10b**	**11b**	**01b**	**10b**	**11b**	**11b**
	GPIO141					SCIRXDD (I)		
	GPIO142					SCITXDD (O)		
	GPIO143							
	GPIO144							
	GPIO145	EPWM1A (O)						
	GPIO146	EPWM1B (O)						
	GPIO147	EPWM2A (O)						
	GPIO148	EPWM2B (O)						
	GPIO149	EPWM3A (O)						
	GPIO150	EPWM3B (O)						
	GPIO151	EPWM4A (O)						
	GPIO152	EPWM4B (O)						
	GPIO153	EPWM5A (O)						
	GPIO154	EPWM5B (O)						
	GPIO155	EPWM6A (O)						
	GPIO156	EPWM6B (O)						
	GPIO157	EPWM7A (O)						
	GPIO158	EPWM7B (O)						
	GPIO159	EPWM8A (O)						
	GPIO160	EPWM8B (O)						
	GPIO161	EPWM9A (O)						
	GPIO162	EPWM9B (O)						
	GPIO163	EPWM10A (O)						
	GPIO164	EPWM10B (O)						
	GPIO165	EPWM11A (O)						
	GPIO166	EPWM11B (O)						
	GPIO167	EPWM12A (O)						
	GPIO168	EPWM12B (O)						

4.3.2 USB Pin Muxing

Table 4-4 shows assignment of the alternate USB function mapping. These can be configured with the GPBAMSEL register.

Table 4-4. Alternate USB Function

GPIO	GPBAMSEL SETTING	USB FUNCTION
GPIO42	GPBAMSEL[10] = 1	USB0DM
GPIO43	GPBAMSEL[11] = 1	USB0DP

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4.3.3 High-Speed SPI Pin Muxing

The SPI module on this device has a high-speed mode. To achieve the highest possible speed, a special GPIO configuration is used on a single GPIO mux option for each SPI. These GPIOs may also be used by the SPI when not in high-speed mode (HS_MODE = 0). Table 4-5 shows which GPIOs have the special mux option to allow SPI high-speed mode.

Table 4-5. High-Speed SPI-Enabled GPIOs

SPI PIN	SPIA	SPIB	SPIC
SPISIMO	GPIO58	GPIO63	GPIO69
SPISOMI	GPIO59	GPIO64	GPIO70
SPICLK	GPIO60	GPIO65	GPIO71
$\overline{\text{SPISTE}}$	GPIO61	GPIO66	GPIO72

To select these mux options the user should configure GPyGMUX and GPyMUX registers as shown in Table 4-6.

Table 4-6. GPIO Configuration for High-Speed SPI

GPIO	SPI SIGNAL	MUX CONFIGURATION	
GPIO58	SPISIMOA	GPBGMUX2[21:20]=0x11	GPBMUX2[21:20]=0x11
GPIO59	SPISOMIA	GPBGMUX2[23:22]=0x11	GPBMUX2[23:22]=0x11
GPIO60	SPICLKA	GPBGMUX2[25:24]=0x11	GPBMUX2[25:24]=0x11
GPIO61	$\overline{\text{SPISTEA}}$	GPBGMUX2[27:26]=0x11	GPBMUX2[27:26]=0x11
GPIO63	SPISIMOB	GPBGMUX2[31:30]=0x11	GPBMUX2[31:30]=0x11
GPIO64	SPISOMIB	GPCGMUX1[1:0]=0x11	GPCMUX1[1:0]=0x11
GPIO65	SPICLKB	GPCGMUX1[3:2]=0x11	GPCMUX1[3:2]=0x11
GPIO66	$\overline{\text{SPISTEB}}$	GPCGMUX1[5:4]=0x11	GPCMUX1[5:4]=0x11
GPIO69	SPISIMOC	GPCGMUX1[11:10]=0x11	GPCMUX1[11:10]=0x11
GPIO70	SPISOMIC	GPCGMUX1[13:12]=0x11	GPCMUX1[13:12]=0x11
GPIO71	SPICLKC	GPCGMUX1[15:14]=0x11	GPCMUX1[15:14]=0x11
GPIO72	$\overline{\text{SPISTEC}}$	GPCGMUX1[17:16]=0x11	GPCMUX1[17:16]=0x11

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5 Specifications

5.1 Absolute Maximum Ratings[1][2]

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage	V_{DDIO} with respect to V_{SS}	–0.3	4.6	V
	V_{DDSFL} with respect to V_{SS}	–0.3	4.6	
	V_{DDOSC} with respect to V_{SS}	–0.3	4.6	
	V_{DD} with respect to V_{SS}	–0.3	1.5	
Analog voltage	V_{DDA} with respect to V_{SSA}	–0.3	4.6	V
Supply ramp rate	V_{DDIO}, V_{DD}, V_{DDA}, V_{DDSFL}, V_{DDOSC} with respect to V_{SS}		10^5	V/s
Input voltage	V_{IN} (3.3 V)	–0.3	4.6	V
Output voltage	V_O	–0.3	4.6	V
Input clamp current	Digital input (per pin), I_{IK} ($V_{IN} < V_{SS}$ or $V_{IN} > V_{DDIO}$)	–20	20	mA
	Analog input (per pin), $I_{IKANALOG}$ ($V_{IN} < V_{SSA}$ or $V_{IN} > V_{DDA}$)	–20	20	
	Total for all inputs, $I_{IKTOTAL}$ ($V_{IN} < V_{SS}/V_{SSA}$ or $V_{IN} > V_{DDIO}/V_{DDA}$)	–20	20	
Output current	Digital output (per pin), I_{OUT}	–20	20	mA
Free-Air temperature	T_A	–40	125	°C
Operating junction temperature	T_J	–40	150	°C
Storage temperature[3]	T_{stg}	–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Section 5.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.
(3) Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see the *IC Package Thermal Metrics Application Report* (SPRA953).

5.2 ESD Ratings

				VALUE	UNIT
TMS320F2837xD in 337-ball ZWT package					
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	All pins	±2000	V
		Charged device model (CDM), per AEC Q100-011	All pins	±500	
			Corner balls on 337-ball ZWT: A1, A19, W1, W19	±750	
TMS320F2837xD in 176-pin PTP package					
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	All pins	±2000	V
		Charged device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins on 176-pin PTP: 1, 44, 45, 88, 89, 132, 133, 176	±750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Device supply voltage, I/O, V_{DDIO} (1)		3.14	3.3	3.47	V
Device supply voltage, V_{DD}		1.14	1.2	1.26	V
Supply ground, V_{SS}			0		V
Analog supply voltage, V_{DDA} (1)		3.14	3.3	3.47	V
Analog ground, V_{SSA}			0		V
Junction temperature, T_J	T version	–40		105	°C
	S version (2)	–40		125	
	Q version (Q100 qualification) (2)	–40		150	
Free-Air temperature, T_A	Q version (Q100 qualification) (2)	–40		125	°C

(1) V_{DDIO}, V_{DDSFL}, V_{DDOSC}, and V_{DDA} should be maintained within 0.3 V of each other.
(2) Operation above T_J = 105°C for extended duration will reduce the lifetime of the device.

5.4 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = I_{OH} MAX	V_{DDIO} * 0.8			V
			I_{OH} = 50 µA	V_{DDIO} – 0.2			
V_{OL}	Low-level output voltage		I_{OL} = I_{OL} MAX			V_{DDIO} * 0.2	V
I_{OH}	High-level output source current for all GPIO pins		V_{OH} = $V_{OH(MIN)}$	–4			mA
I_{OL}	Low-level output sink current for all GPIO pins		V_{OL} = $V_{OL(MAX)}$			4	mA
I_{OZ}	Output current, pullup or pulldown disabled		V_O = V_{DDIO} or 0 V		±2		µA
V_{IH}	High-level input voltage (3.3 V)			V_{DDIO} * 0.7		V_{DDIO} + 0.3	V
V_{IL}	Low-level input voltage (3.3 V)			V_{SS} – 0.3		V_{DDIO} * 0.3	V
I_{IH}	Input current	Digital inputs with pulldown (1)	V_{DDIO} = 3.3 V V_{DDA} = 3.3 V V_{IN} = V_{DDIO}		120		µA
		Digital inputs without pulldown (1)				±2	
		Analog inputs except pins with DACOUTx				±2	
		Analog inputs with DACOUTx			66		
I_{IL}	Input current	Digital inputs with pullup enabled (1)	V_{DDIO} = 3.3 V V_{DDA} = 3.3 V V_{IN} = 0 V		–150		µA
		Digital inputs with pullup disabled (1)				±2	
		Analog inputs				±2	
C_I	Input capacitance				2		pF

(1) See Table 4-2 for a list of pins with a pullup or pulldown.

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5.5 Thermal Resistance Characteristics for ZWT Package

		°C/W(1)	AIR FLOW (lfm)(2)
$R\Theta_{JC}$	Junction-to-case thermal resistance	8.3	N/A
$R\Theta_{JB}$	Junction-to-board thermal resistance	11.6	N/A
$R\Theta_{JA}$ (High k PCB)	Junction-to-free air thermal resistance	21.5	0
$R\Theta_{JMA}$	Junction-to-moving air thermal resistance	19.0	150
		17.8	250
		16.5	500
Psi_{JT}	Junction-to-package top	0.2	0
		0.3	150
		0.4	250
		0.5	500
Psi_{JB}	Junction-to-board	11.4	0
		11.3	150
		11.2	250
		11.0	500

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(2) lfm = linear feet per minute

5.6 Thermal Resistance Characteristics for PTP PowerPAD Package

		°C/W(1)	AIR FLOW (lfm)(2)
$R\Theta_{JC}$	Junction-to-case thermal resistance	6.97	N/A
$R\Theta_{JB}$	Junction-to-board thermal resistance	6.05	N/A
$R\Theta_{JA}$ (High k PCB)	Junction-to-free air thermal resistance	17.8	0
$R\Theta_{JMA}$	Junction-to-moving air thermal resistance	12.8	150
		11.4	250
		10.1	500
Psi_{JT}	Junction-to-package top	0.11	0
		0.24	150
		0.33	250
		0.42	500
Psi_{JB}	Junction-to-board	6.1	0
		5.5	150
		5.4	250
		5.3	500

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(2) lfm = linear feet per minute

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5.7 Timing and Switching Characteristics

5.7.1 Power Sequencing

An external power supply must be used to supply 3.3 V to V_{DDIO}, V_{DD3VFL}, V_{DDOSC}, and V_{DDA} and to provide 1.2 V to V_{DD}. The internal VREG is not supported; therefore, the VREGENZ pin must be tied high to 3.3 V.

The voltage on V_{DDIO} should be greater than V_{DD} – 0.3 V at all times. V_{DDIO}, V_{DD3VFL}, V_{DDOSC}, and V_{DDA} should be powered up together and be kept within 0.3 V of each other during operation. Before powering the device, no voltage larger than 0.3 V above V_{DDIO} should be applied to any digital pin, and no voltage larger than 0.3 V above V_{DDA} should be applied to any analog pin.

An internal power-on-reset (POR) circuit holds the device in reset and keeps the I/Os in a high-impedance state during power up. External supply voltage supervisors (SVS) can be used to monitor the voltage on the 3.3-V and 1.2-V rails and drive $\overline{XRS}$ low should supplies fall outside operational specifications.

5.7.2 Reset Timing

$\overline{XRS}$ is the Device Reset (in) and Watchdog Reset (out). The devices have a built-in POR circuit. During a power-on condition, this pin is driven low by the device. An external circuit may also drive this pin to assert a device reset.

This pin is also driven low by the MCU when a watchdog reset occurs. During watchdog reset, the $\overline{XRS}$ pin is driven low for the watchdog reset duration of 512 OSCCLK cycles.

A resistor between 2.2 kΩ and 10 kΩ should be placed between $\overline{XRS}$ and V_{DDIO}. A capacitor should be placed between $\overline{XRS}$ and V_{SS} for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the $\overline{XRS}$ pin to V_{OL} within 512 OSCCLK cycles when the watchdog reset is asserted.

Regardless of the source, a device reset causes the device to terminate execution. The program counter points to the address contained at the location 0x3F FFC0. When reset is deactivated, execution begins at the location designated by the program counter.

5.7.2.1 Reset Electrical Data and Timing

Table 5-1. Reset ($\overline{XRS}$) Timing Requirements

		MIN	MAX	UNIT
$t_{h(boot\text{-}mode)}$	Hold time for boot-mode pins	1.5		ms
$t_{w(RSL2)}$	Pulse duration, $\overline{XRS}$ low on warm reset	3.2		µs

Table 5-2. Reset ($\overline{XRS}$) Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{w(RSL1)}$	Pulse duration, $\overline{XRS}$ driven low by device after supplies are stable		100		µs
$t_{w(WDRS)}$	Pulse duration, reset pulse generated by watchdog		$512t_{c(OSCCLK)}$		cycles

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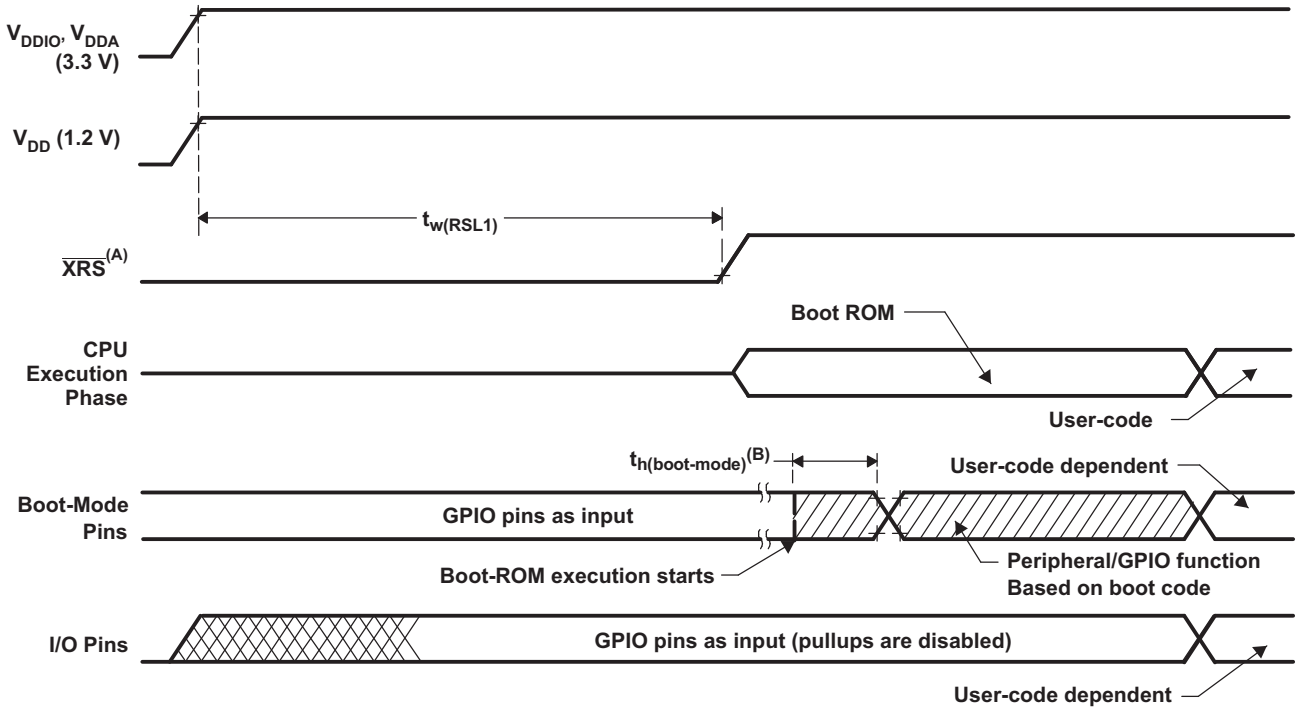
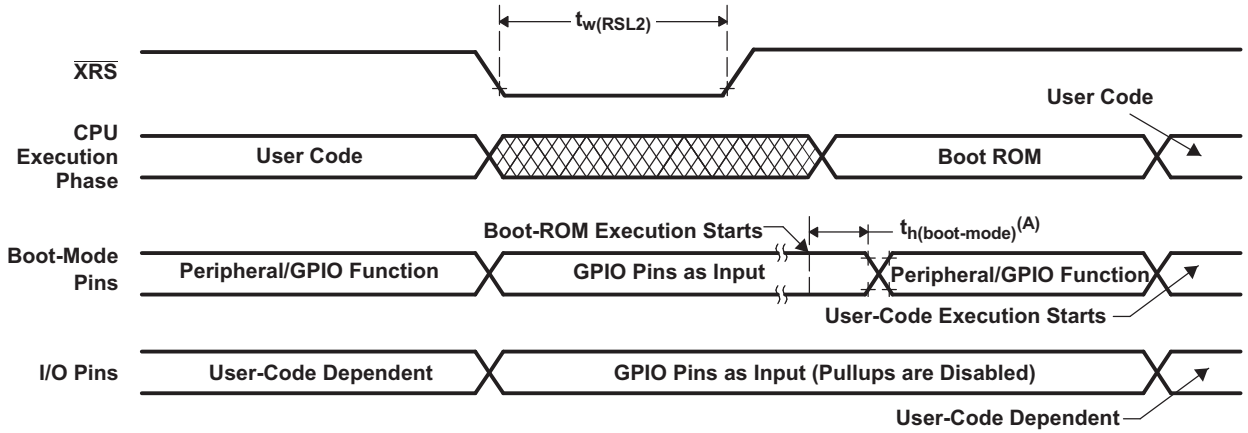


A. The $\overline{XRS}$ pin can be driven externally by a supervisor or an external pullup resistor, see Table 4-1. On-chip POR logic will hold this pin low until the supplies are in a valid range.

B. After reset, the boot ROM code samples Boot Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If boot ROM code executes after power-on conditions (in debugger environment), the boot code execution time is based on the current SYSCLK speed. The SYSCLK will be based on user environment and could be with or without PLL enabled.

Figure 5-1. Power-on Reset



A. After reset, the Boot ROM code samples BOOT Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If Boot ROM code executes after power-on conditions (in debugger environment), the Boot code execution time is based on the current SYSCLK speed. The SYSCLK will be based on user environment and could be with or without PLL enabled.

Figure 5-2. Warm Reset

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5.7.3 Clock Specifications

5.7.3.1 Clock Sources

Table 5-3 lists four possible clock sources.

Table 5-3. Possible Reference Clock Sources

CLOCK SOURCE	MODULES CLOCKED	COMMENTS
INTOSC1 (1)	Can be used to provide clock for: • Watchdog block • Main PLL • CPU-Timer 2	Internal oscillator 1. Zero-pin overhead 10-MHz internal oscillator.
INTOSC2 (1)(2)	Can be used to provide clock for: • Main PLL • Auxiliary PLL • CPU-Timer 2	Internal oscillator 2. Zero-pin overhead 10-MHz internal oscillator.
XTAL (1)	Can be used to provide clock for: • Main PLL • Auxiliary PLL • CPU-Timer 2	External crystal connected between X1 and X2 pins. On-chip crystal oscillator enables the use of external crystal/resonator to provide time base when connected to the device.
GPIO_AUXCLKIN	Can be used to provide clock for: • Auxiliary PLL • CPU-Timer 2	Single-ended 3.3-V level clock source. GPIO133/AUXCLKIN pin should be used to provide the input clock.

(1) For power savings, both zero pin internal oscillators and the XTAL oscillator can be individually powered down if they are not being used by the application.
(2) On reset, internal oscillator 2 (INTOSC2) is the default clock source for both system PLL (OSCCLK) and auxiliary PLL (AUXOSCCLK).

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Figure 5-3 shows the clocking options for system PLL.

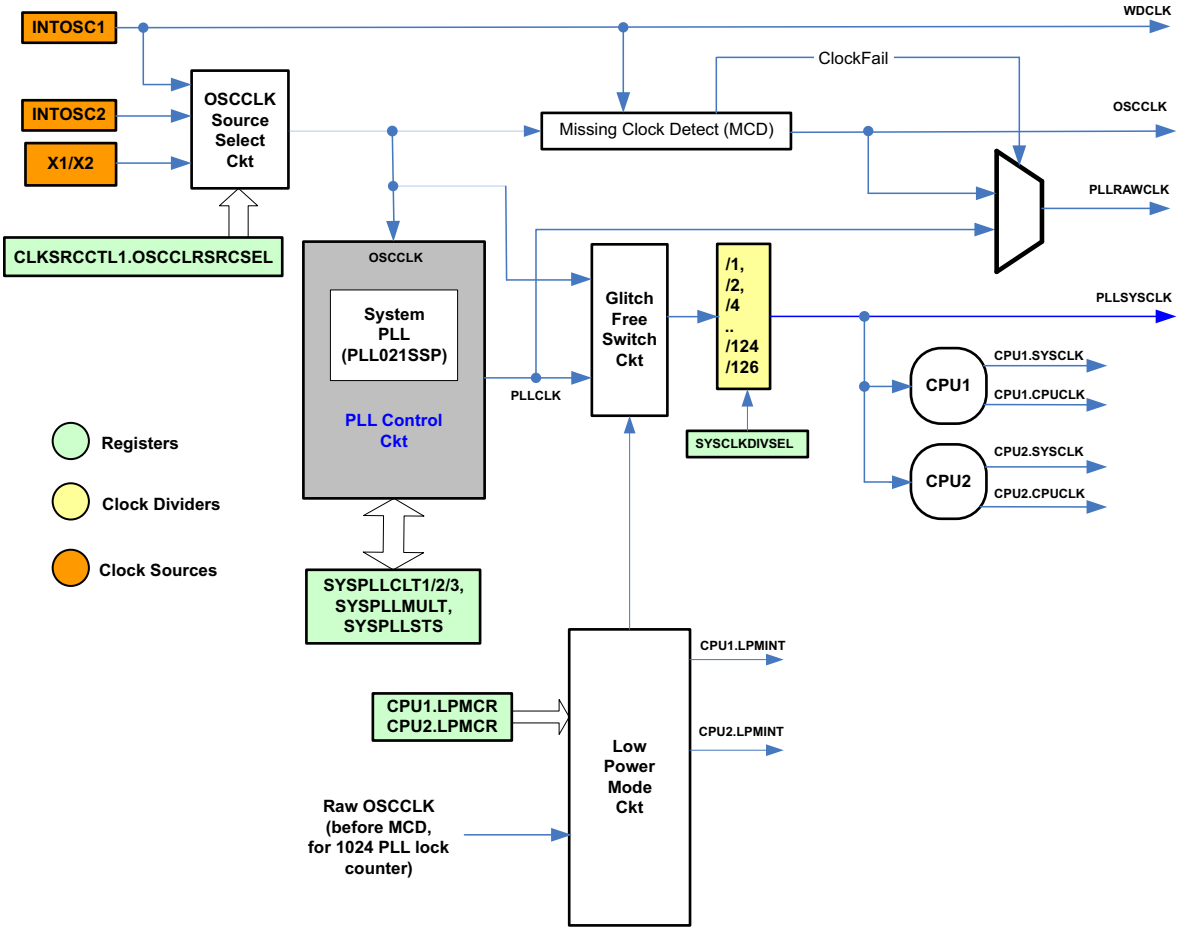

Figure 5-3. Clocking Options for System PLL

NOTE

The clock name for peripheral clocking "PERx.SYSCLK" is used interchangeably with "SYSCLK" in the device documentation.

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Figure 5-4 shows the clocking options for auxiliary PLL.

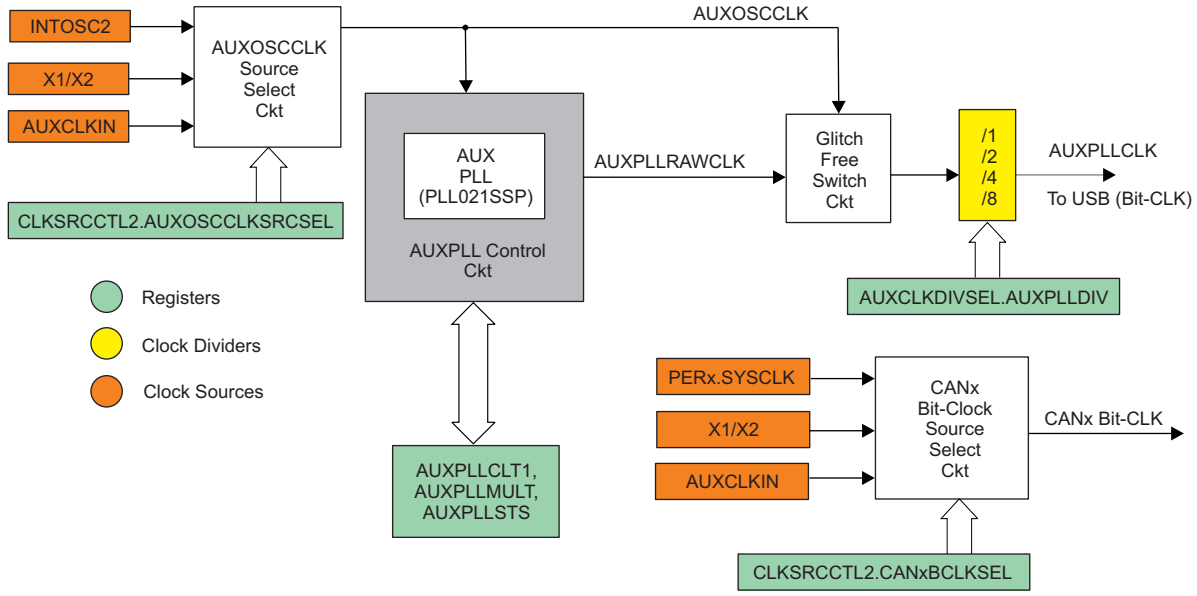

Figure 5-4. Clocking Options for Auxiliary PLL

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Figure 5-5 shows the peripheral clock options.

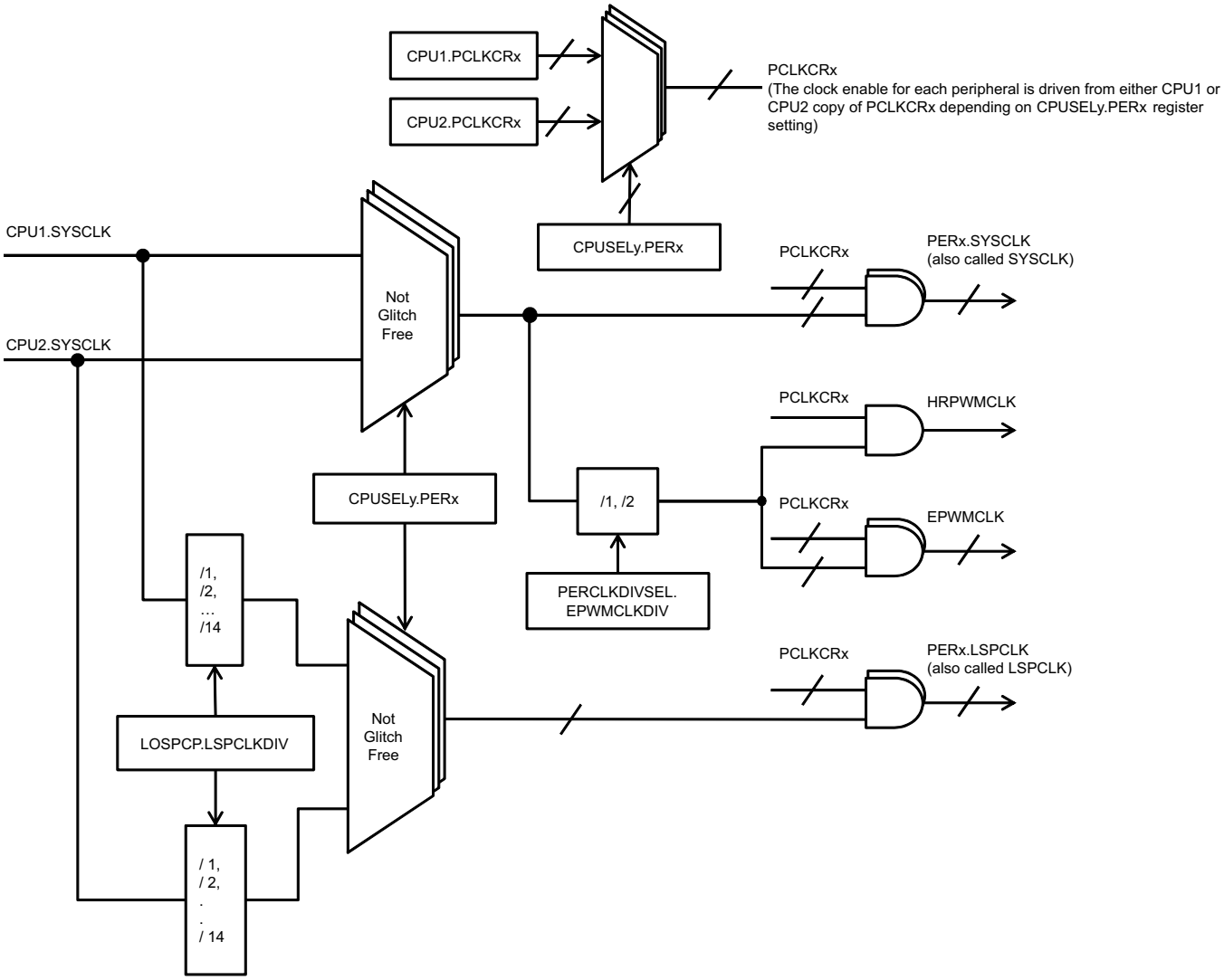

Figure 5-5. Peripheral Clock Options

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5.7.3.2 Clock Frequencies, Requirements, and Characteristics

This section provides the frequencies and timing requirements of the input clocks, PLL lock times, frequencies of the internal clocks, and the frequency and switching characteristics of the output clock.

5.7.3.2.1 Input Clock Frequency and Timing Requirements, PLL Lock Times

Table 5-4 shows the frequency requirements for the input clocks. Table 5-13 shows the crystal equivalent series resistance requirements. Table 5-6 and Table 5-7 show the timing requirements for the input clocks. Table 5-8 shows the PLL lock times for the Main PLL and the USB PLL.

Table 5-4. Input Clock Frequency

		MIN	MAX	UNIT
$f_{(OSC)}$	Frequency, X1/X2, from external crystal or resonator	2	20	MHz
$f_{(OCI)}$	Frequency, X1, from external oscillator ***(PLL enabled)***	2	20	MHz
$f_{(OCI)}$	Frequency, X1, from external oscillator ***(PLL disabled)***	2	100	MHz
$f_{(XCI)}$	Frequency, AUXCLKIN, from external oscillator	2	60	MHz

Table 5-5. X1 Input Level Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
X1 V_{IL}	Valid low-level input voltage		–0.3	0.3 * V_{DDIO}	V
X1 V_{IH}	Valid high-level input voltage		0.7 * V_{DDIO}	V_{DDIO} + 0.3	V

Table 5-6. X1 Timing Requirements

		MIN	MAX	UNIT
$t_{f(OCI)}$	Fall time, X1		6	ns
$t_{r(OCI)}$	Rise time, X1		6	ns
$t_{w(OCL)}$	Pulse duration, X1 low as a percentage of $t_{c(OCI)}$	45%	55%	
$t_{w(OCH)}$	Pulse duration, X1 high as a percentage of $t_{c(OCI)}$	45%	55%	

Table 5-7. AUXCLKIN Timing Requirements

		MIN	MAX	UNIT
$t_{f(XCI)}$	Fall time, AUXCLKIN		6	ns
$t_{r(XCI)}$	Rise time, AUXCLKIN		6	ns
$t_{w(XCL)}$	Pulse duration, AUXCLKIN low as a percentage of $t_{c(XCI)}$	45%	55%	
$t_{w(XCH)}$	Pulse duration, AUXCLKIN high as a percentage of $t_{c(XCI)}$	45%	55%	

Table 5-8. PLL Lock Times

		MIN	NOM	MAX	UNIT
$t_{(PLL)}$	Lock time, Main PLL (X1, from external oscillator)		50 µs + 2500 * $t_{c(OSCCLK)}$ (1)		µs
$t_{(USB)}$	Lock time, USB PLL (AUXCLKIN, from external oscillator)		50 µs + 2500 * $t_{c(OSCCLK)}$ (1)		µs

(1) Cycle count includes code execution of PLL initialization routine which could vary depending on compiler optimizations and flash wait states.

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5.7.3.2.2 Internal Clock Frequencies

Table 5-9 provides the clock frequencies for the internal clocks.

Table 5-9. Internal Clock Frequencies

		MIN	NOM	MAX	UNIT
$f_{(SYSCLK)}$	Frequency, device (system) clock	2		200	MHz
$t_{c(SYSCLK)}$	Period, device (system) clock	8.33		500	ns
$f_{(PLLRAWCLK)}$	Frequency, system PLL output (before SYSCLK divider)	120		400	MHz
$f_{(AUXPLLRAWCLK)}$	Frequency, auxiliary PLL output (before AUXCLK divider)	120		400	MHz
$f_{(AUX)}$	Frequency, AUXPLLCLK		60		MHz
$f_{(PLL)}$	Frequency, PLLSYSCLK	2		200	MHz
$f_{(LSP)}$	Frequency, LSPCLK (1)	2	50 (2)	200	MHz
$t_{c(LSPCLK)}$	Period, LSPCLK	8.33		500	ns
$f_{(INT)}$	Frequency, INTOSC1/2CLK		10		MHz
$f_{(EPWM)}$	Frequency, EPWMCLK (3)			100	MHz
$f_{(HRPWM)}$	Frequency, HRPWMCLK	60		100	MHz

(1) Lower LSPCLK will reduce device power consumption.
(2) The default at reset is SYSCLK/4.
(3) For SYSCLK above 100 MHz, the EPWMCLK must be half of SYSCLK.

5.7.3.2.3 Output Clock Frequency and Switching Characteristics

Table 5-10 provides the frequency of the output clock. Table 5-11 shows the switching characteristics of the output clock, XCLKOUT.

Table 5-10. Output Clock Frequency

		MIN	MAX	UNIT
$f_{(XCO)}$	Frequency, XCLKOUT	2	50	MHz

Table 5-11. XCLKOUT Switching Characteristics (PLL Bypassed or Enabled) (1) (2)

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{f(XCO)}$	Fall time, XCLKOUT		5	ns
$t_{r(XCO)}$	Rise time, XCLKOUT		5	ns
$t_{w(XCOL)}$	Pulse duration, XCLKOUT low	H – 2	H + 2	ns
$t_{w(XCOH)}$	Pulse duration, XCLKOUT high	H – 2	H + 2	ns

(1) A load of 40 pF is assumed for these parameters.
(2) $H = 0.5t_{c(XCO)}$

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5.7.3.3 Input Clocks and PLLs

In addition to the internal 0-pin oscillators, multiple external clock source options are available. Figure 5-6 shows the recommended methods of connecting crystals, resonators, and oscillators to pins X1/X2 and AUXCLKIN.

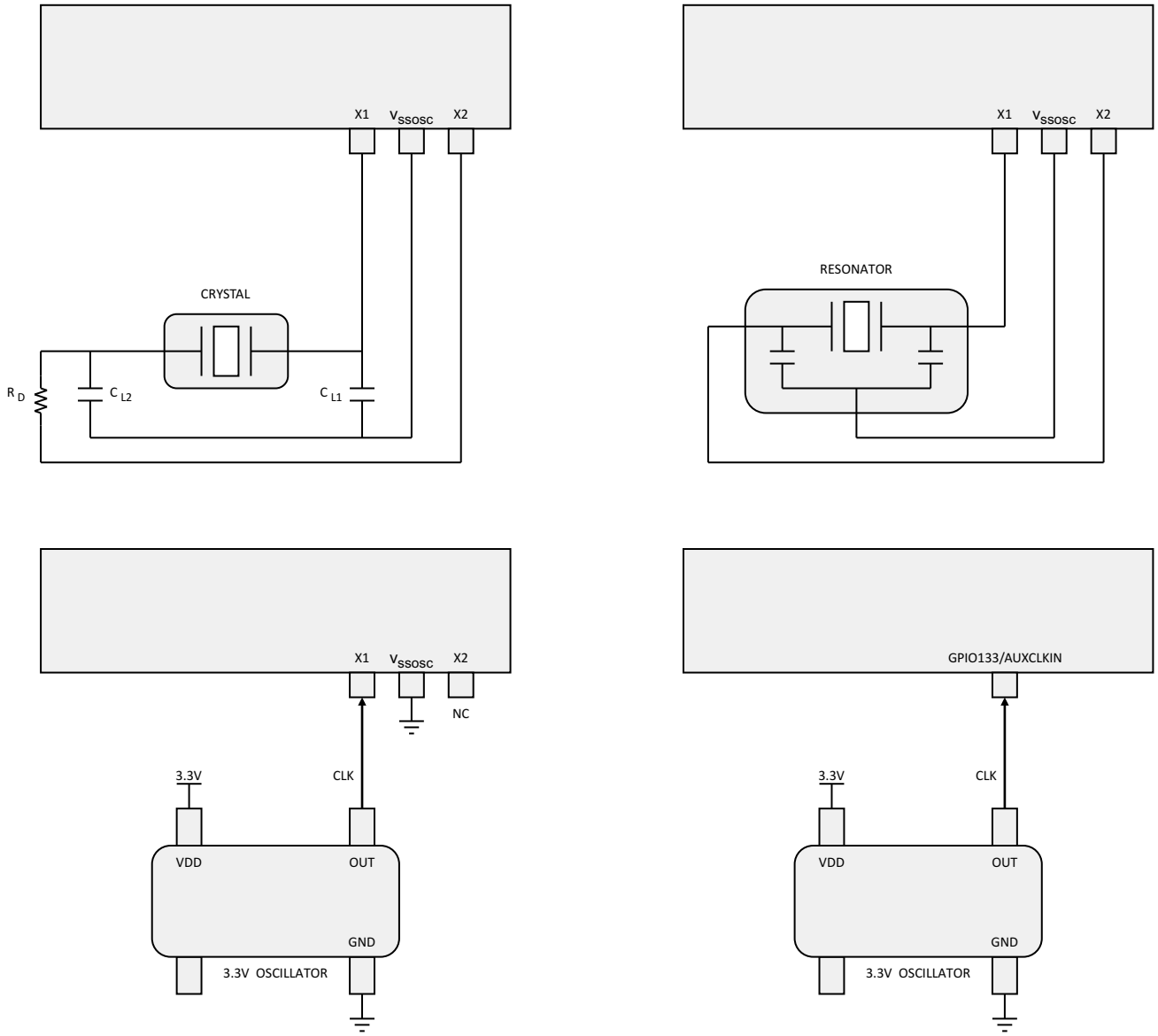

Figure 5-6. Connecting Input Clocks to a 2837xD Device

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5.7.3.4 Crystal Oscillator

When using a quartz crystal, it may be necessary to include a damping resistor (R_D) in the crystal circuit to prevent over-driving the crystal (drive level can be found in the crystal data sheet). In higher-frequency applications (10 MHz or greater), R_D is generally not required. If a damping resistor is required, R_D should be as small as possible because the size of the resistance affects start-up time (smaller R_D = faster start-up time). It is recommended that the crystal manufacturer characterize the crystal with the application board.

Table 5-12. Crystal Oscillator Parameters

		MIN	MAX	UNIT
CL1, CL2	Load capacitance	12	24	pF
C0	Crystal shunt capacitance		7	pF

Table 5-13. Crystal Equivalent Series Resistance (ESR) Requirements(1)

CRYSTAL FREQUENCY (MHz)	MAXIMUM ESR (Ω) (CL1 = CL2 = 12 pF)	MAXIMUM ESR (Ω) (CL1 = CL2 = 24 pF)
2	175	375
4	100	195
6	75	145
8	65	120
10	55	110
12	50	95
14	50	90
16	45	75
18	45	65
20	45	50

(1) Crystal shunt capacitance (C0) should be less than or equal to 7 pF.

5.7.3.5 Internal Oscillators

Table 5-14 provides the electrical characteristics of the two internal oscillators.

NOTE

This oscillator cannot be used as the PLL source if the PLLSYSCLK is configured to frequencies above 194 MHz.

Table 5-14. Internal Oscillator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Nominal frequency			10		MHz
	Frequency accuracy at room temperature	30°C		±0.1%		
	Frequency accuracy across temperature			±3%		
t_{OSCST}	Startup and settling time			22		µs

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5.7.3.6 Flash Parameters

Table 5-15. Minimum Required Flash Wait-States at Different Frequencies

CPUCLK (MHz)	FLASH WAIT-STATES (MINIMUM REQUIRED RWAIT)
151–200	3
101–150	2
51–100	1
≤50	0

Table 5-16. Flash Parameters at 200 MHz(1)

PARAMETER		MIN	TYP	MAX	UNIT
Program Time(2)	128 data bits + 16 ECC bits		40	300	µs
	8K sector		90	180	ms
	32K sector		360	720	ms
Erase Time(3) at < 25 cycles	8K sector		25	50	ms
	32K sector		30	55	
Erase Time(3) at 50k cycles	8K sector		105	4000	ms
	32K sector		110	4000	

(1) The on-chip flash memory is in an erased state when the device is shipped from TI. As such, erasing the flash memory is not required prior to programming, when programming the device for the first time. However, the erase operation is needed on all subsequent programming operations.
(2) Program time includes overhead of the Flash state machine but does not include the time to transfer the following into RAM:
- Code that uses Flash API to program the Flash
- Flash API itself
- Flash data to be programmed

In other words, the time indicated in this table is applicable after all the required code/data is available in the device RAM, ready for programming. Note that the transfer time will significantly vary depending on the speed of the emulator used.
Program time calculation is based on programming 144 bits at a time at the specified operating frequency. Program time includes Program verify by the CPU. Note that the program time does not degrade with write/erase (W/E) cycling, but the erase time does. Erase time includes Erase verify by the CPU and does not involve any data transfer.
(3) Erase time includes Erase verify by the CPU.

Table 5-17. Flash/OTP Endurance

		MIN	TYP	MAX	UNIT
N_f	Flash endurance for the array (write/erase cycles)	20000	50000		cycles
N_{OTP}	OTP endurance for the array (write cycles)			1	write

Table 5-18. Flash Data Retention Duration

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{retention}$	Data retention duration	T_J = 85°C	20		years

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5.7.4 System Timings

5.7.4.1 GPIO Electrical Data and Timing

5.7.4.1.1 GPIO - Output Timing

Table 5-19. General-Purpose Output Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			MIN	MAX	UNIT
$t_{r(GPO)}$	Rise time, GPIO switching low to high	All GPIOs		8	ns
$t_{f(GPO)}$	Fall time, GPIO switching high to low	All GPIOs		8	ns
t_{fGPO}	Toggling frequency, GPO pins			25	MHz

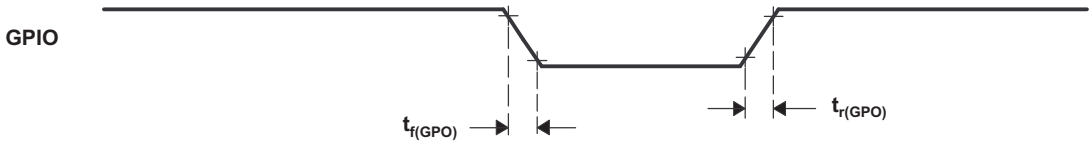

Figure 5-7. General-Purpose Output Timing

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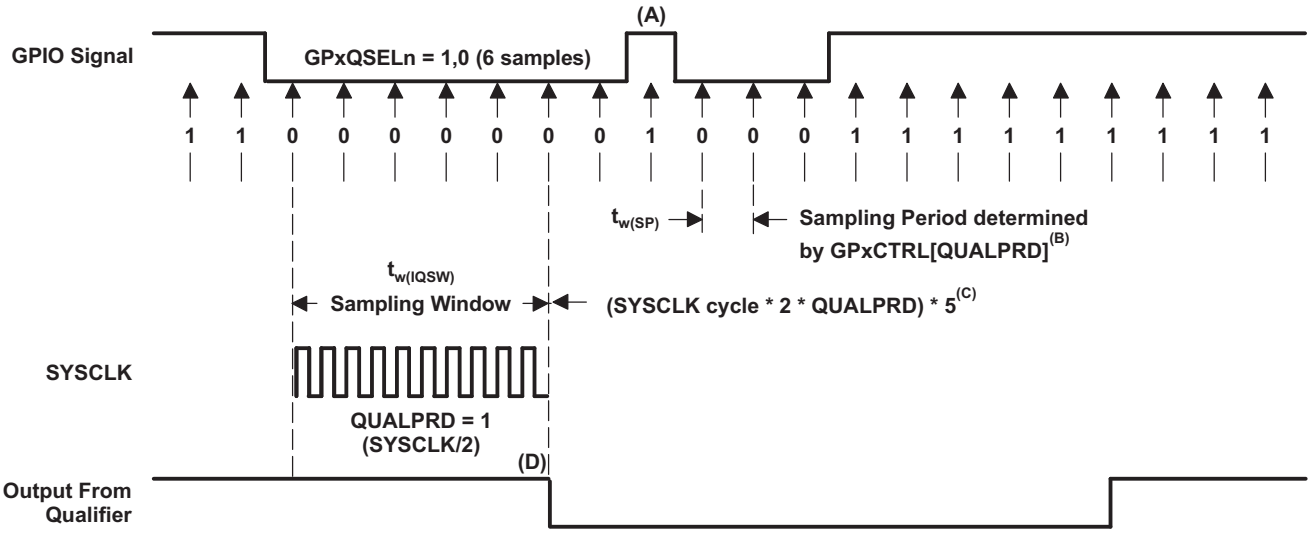
5.7.4.1.2 GPIO - Input Timing

Table 5-20. General-Purpose Input Timing Requirements

			MIN	MAX	UNIT
$t_{w(SP)}$	Sampling period	QUALPRD = 0	$1t_{c(SYSCLK)}$		cycles
		QUALPRD ≠ 0	$2t_{c(SYSCLK)}$ * QUALPRD		cycles
$t_{w(IQSW)}$	Input qualifier sampling window		$t_{w(SP)}$ * (n(1) – 1)		cycles
$t_{w(GPI)}$ (2)	Pulse duration, GPIO low/high	Synchronous mode	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$t_{w(IQSW)}$ + $t_{w(SP)}$ + $1t_{c(SYSCLK)}$		cycles

(1) "n" represents the number of qualification samples as defined by GPxQSELn register.
(2) For $t_{w(GPI)}$, pulse width is measured from V_{IL} to V_{IL} for an active low signal and V_{IH} to V_{IH} for an active high signal.



A. This glitch will be ignored by the input qualifier. The QUALPRD bit field specifies the qualification sampling period. It can vary from 00 to 0xFF. If QUALPRD = 00, then the sampling period is 1 SYSCLK cycle. For any other value "n", the qualification sampling period in 2n SYSCLK cycles (that is, at every 2n SYSCLK cycles, the GPIO pin will be sampled).
B. The qualification period selected via the GPxCTRL register applies to groups of 8 GPIO pins.
C. The qualification block can take either three or six samples. The GPxQSELn Register selects which sample mode is used.
D. In the example shown, for the qualifier to detect the change, the input should be stable for 10 SYSCLK cycles or greater. In other words, the inputs should be stable for (5 x QUALPRD x 2) SYSCLK cycles. This would ensure 5 sampling periods for detection to occur. Because external signals are driven asynchronously, an 13-SYSCLK-wide pulse ensures reliable recognition.

Figure 5-8. Sampling Mode

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5.7.4.1.3 Sampling Window Width for Input Signals

The following section summarizes the sampling window width for input signals for various input qualifier configurations.

Sampling frequency denotes how often a signal is sampled with respect to SYSCLK.

Sampling frequency = SYSCLK/(2 * QUALPRD), if QUALPRD ≠ 0

Sampling frequency = SYSCLK, if QUALPRD = 0

Sampling period = SYSCLK cycle x 2 x QUALPRD, if QUALPRD ≠ 0

In the above equations, SYSCLK cycle indicates the time period of SYSCLK.

Sampling period = SYSCLK cycle, if QUALPRD = 0

In a given sampling window, either 3 or 6 samples of the input signal are taken to determine the validity of the signal. This is determined by the value written to GPxQSELn register.

Case 1:

Qualification using 3 samples

Sampling window width = (SYSCLK cycle x 2 x QUALPRD) x 2, if QUALPRD ≠ 0

Sampling window width = (SYSCLK cycle) x 2, if QUALPRD = 0

Case 2:

Qualification using 6 samples

Sampling window width = (SYSCLK cycle x 2 x QUALPRD) x 5, if QUALPRD ≠ 0

Sampling window width = (SYSCLK cycle) x 5, if QUALPRD = 0

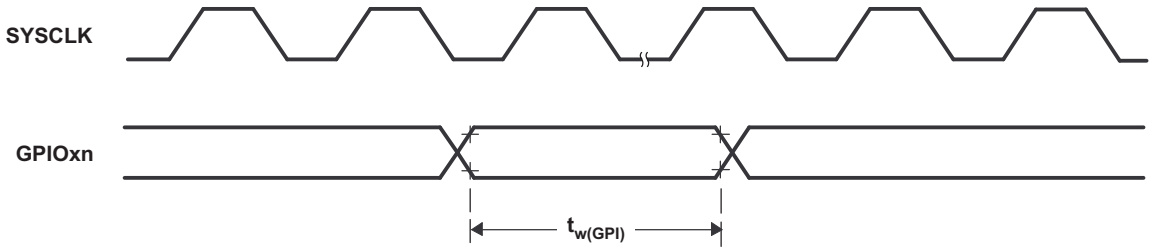

Figure 5-9. General-Purpose Input Timing

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5.7.4.2 Interrupts

Figure 5-10 provides a high-level view of the interrupt architecture.

As shown in Figure 5-10, the devices support five external interrupts (XINT1 to XINT5) that can be mapped onto any of the GPIO pins.

In this device, sixteen Expanded Peripheral Interrupt Expansion (ePIE) block interrupts are grouped into one CPU interrupt. In total, there are 12 CPU interrupt groups, with 16 interrupts per group.

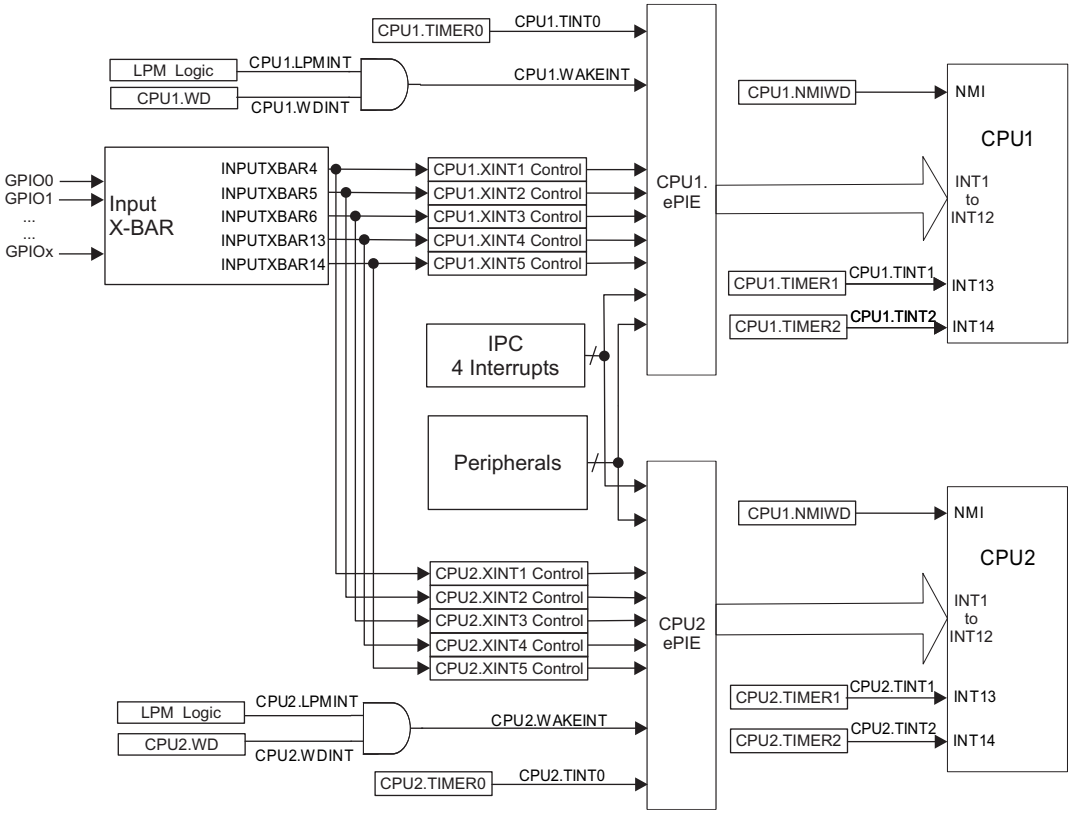

Figure 5-10. External and ePIE Interrupt Sources

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5.7.4.2.1 External Interrupt Electrical Data and Timing

Table 5-21. External Interrupt Timing Requirements(1)

			MIN	MAX	UNIT
$t_{w(INT)}$ (2)	Pulse duration, INT input low/high	Synchronous	$2t_{c(SYSCLK)}$		cycles
		With qualifier	$t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SYSCLK)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 5-20.
(2) This timing is applicable to any GPIO pin configured for ADCSOC functionality.

Table 5-22. External Interrupt Switching Characteristics(1)

over recommended operating conditions (unless otherwise noted)

PARAMETER	MIN	MAX	UNIT
$t_{d(INT)}$ Delay time, INT low/high to interrupt-vector fetch(2)	$t_{w(IQSW)} + 14t_{c(SYSCLK)}$	$t_{w(IQSW)} + t_{w(SP)} + 14t_{c(SYSCLK)}$	cycles

(1) For an explanation of the input qualifier parameters, see Table 5-20.
(2) This assumes that the ISR is in a single-cycle memory.

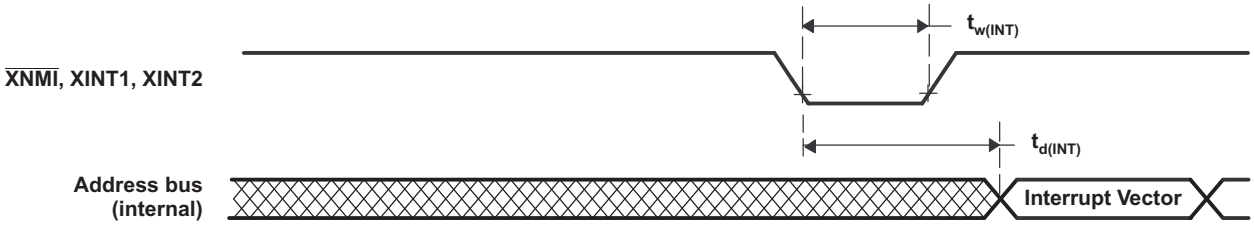

Figure 5-11. External Interrupt Timing

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5.7.4.3 Low-Power Modes

This device has three clock-gating low-power modes and a special power-gating mode.

Further details, as well as the entry and exit procedure, for all of the low-power modes can be found in the "Low Power Modes" section of the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual* (SPRUHM8).

5.7.4.3.1 Clock-Gating Low-Power Modes

IDLE, STANDBY, and HALT modes on this device are similar to those on other C28x devices. Table 5-23 describes the effect on the system when any of the clock-gating low-power modes are entered.

Table 5-23. Effect of Clock-Gating Low-Power Modes on the Device

MODULES/ CLOCK DOMAIN	CPU1 IDLE	CPU1 STANDBY	CPU2 IDLE	CPU2 STANDBY	HALT
CPU1.CLKIN	Active	Gated	N/A	N/A	Gated
CPU1.SYSCLK	Active	Gated	N/A	N/A	Gated
CPU1.CPUCLK	Gated	Gated	N/A	N/A	Gated
CPU2.CLKIN	N/A	N/A	Active	Gated	Gated
CPU2.SYSCLK	N/A	N/A	Active	Gated	Gated
CPU2.CPUCLK	N/A	N/A	Gated	Gated	Gated
Clock to modules Connected to PERx.SYSCLK	Active	Gated if CPUSEL.PERx = CPU1	Active	Gated if CPUSEL.PERx = CPU2	Gated
WD1CLK	Active	Active	Active	Active	Gated if CLKSRCCTL1.WDHALTI = 0
WD2CLK	Active	Active	Active	Active	Gated
AUXPLLCLK	Active	Active	Active	Active	Gated
PLL	Powered	Powered	Powered	Powered	Powered-Down
INTOSC1	Powered	Powered	Powered	Powered	Powered down if CLKSRCCTL1.WDHALTI = 0
INTOSC2	Powered	Powered	Powered	Powered	Powered down if CLKSRCCTL1.WDHALTI = 0
Flash	Powered	Powered	Powered	Powered	Software-Controlled
X1,X2 OSC	Powered	Powered	Powered	Powered	Powered-Down

5.7.4.3.2 Power-Gating Low-Power Modes

HIBERNATE mode is the lowest power mode on this device. It is a global low-power mode that gates the supply voltages to most of the system. HIBERNATE is essentially a controlled power-down with remote wakeup capability, and can be used to save power during long periods of inactivity. Table 5-24 describes the effects on the system when the HIBERNATE mode is entered.

Table 5-24. Effect of Power-Gating Low-Power Mode on the Device

MODULES/POWER DOMAINS	HIBERNATE
M0 and M1 memories	• Remain on with memory retention if LPMCR.M0M1MODE = 0x00 • Are off when LPMCR.M0M1MODE = 0x01
CPU1, CPU2, digital peripherals	Powered down
Dx, LSx, GSx memories	Power down, memory contents are lost
IOs	On with output state preserved
Oscillators, PLL, analog peripherals, Flash	Enters Low-Power Mode

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5.7.4.3.3 Low-Power Mode Wakeup Timing

Table 5-25 shows the IDLE mode timing requirements, Table 5-26 shows the switching characteristics, and Figure 5-12 shows the timing diagram for IDLE mode.

Table 5-25. IDLE Mode Timing Requirements(1)

			MIN	MAX	UNIT
$t_{w(WAKE)}$	Pulse duration, external wake-up signal	Without input qualifier	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$1t_{c(SYSCLK)} + t_{w(IQSW)}$		

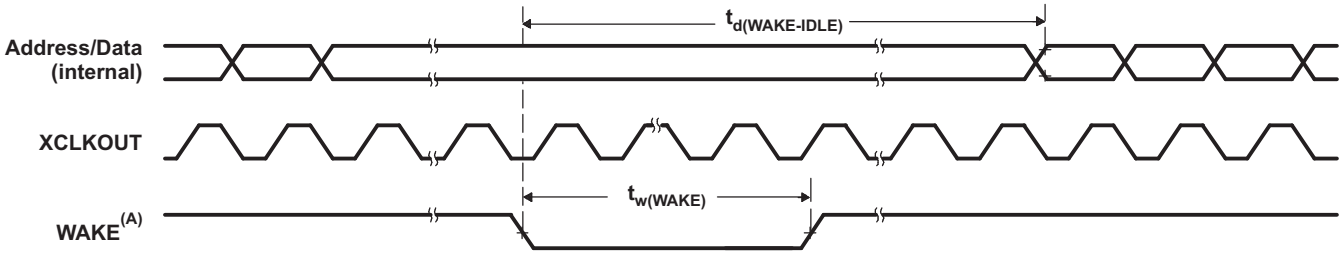
(1) For an explanation of the input qualifier parameters, see Table 5-20.

Table 5-26. IDLE Mode Switching Characteristics(1)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(WAKE-IDLE)}$	Delay time, external wake signal to program execution resume (2)				cycles
	• Wake-up from Flash – Flash module in active state	Without input qualifier		$40t_{c(SYSCLK)}$	
		With input qualifier		$40t_{c(SYSCLK)} + t_{w(WAKE)}$	
	• Wake-up from Flash – Flash module in sleep state	Without input qualifier		$6700t_{c(SYSCLK)}$	
		With input qualifier		$6700t_{c(SYSCLK)} + t_{w(WAKE)}$	
	• Wake-up from SARAM	Without input qualifier		$25t_{c(SYSCLK)}$	
		With input qualifier		$25t_{c(SYSCLK)} + t_{w(WAKE)}$	

(1) For an explanation of the input qualifier parameters, see Table 5-20.
(2) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up) signal involves additional latency.



A. WAKE can be any enabled interrupt, $\overline{\text{WDINT}}$ or $\overline{\text{XRS}}$. After the IDLE instruction is executed, a delay of 5 OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.

Figure 5-12. IDLE Entry and Exit Timing Diagram

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Table 5-27 shows the STANDBY mode timing requirements, Table 5-28 shows the switching characteristics, and Figure 5-13 shows the timing diagram for STANDBY mode.

Table 5-27. STANDBY Mode Timing Requirements

			MIN	MAX	UNIT
$t_{w(WAKE-INT)}$	Pulse duration, external wake-up signal	Without input qualification	$3t_{c(OSCCLK)}$		cycles
		With input qualification(1)	(2 + QUALSTDBY) * $t_{c(OSCCLK)}$		

(1) QUALSTDBY is a 6-bit field in the LPMCR register.

Table 5-28. STANDBY Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(IDLE-XCOS)}$	Delay time, IDLE instruction executed to XCLKOUT stop			$16t_{c(INTOSC1)}$	cycles
$t_{d(WAKE-STBY)}$	Delay time, external wake signal to program execution resume(1)				cycles
	• Wake-up from flash – Flash module in active state	Without input qualifier		$175t_{c(SYSCLK)}$	
		With input qualifier		$175t_{c(SYSCLK)} + t_{w(WAKE-INT)}$	
	• Wake-up from flash – Flash module in sleep state	Without input qualifier		$6700t_{c(SYSCLK)}$	
		With input qualifier		$6700t_{c(SYSCLK)} + t_{w(WAKE-INT)}$	
	• Wake-up from SARAM	Without input qualifier		$3t_{c(OSC)} + 15t_{c(SYSCLK)}$	
		With input qualifier		$3t_{c(OSC)} + 15t_{c(SYSCLK)} + t_{w(WAKE-INT)}$	

(1) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up signal) involves additional latency.

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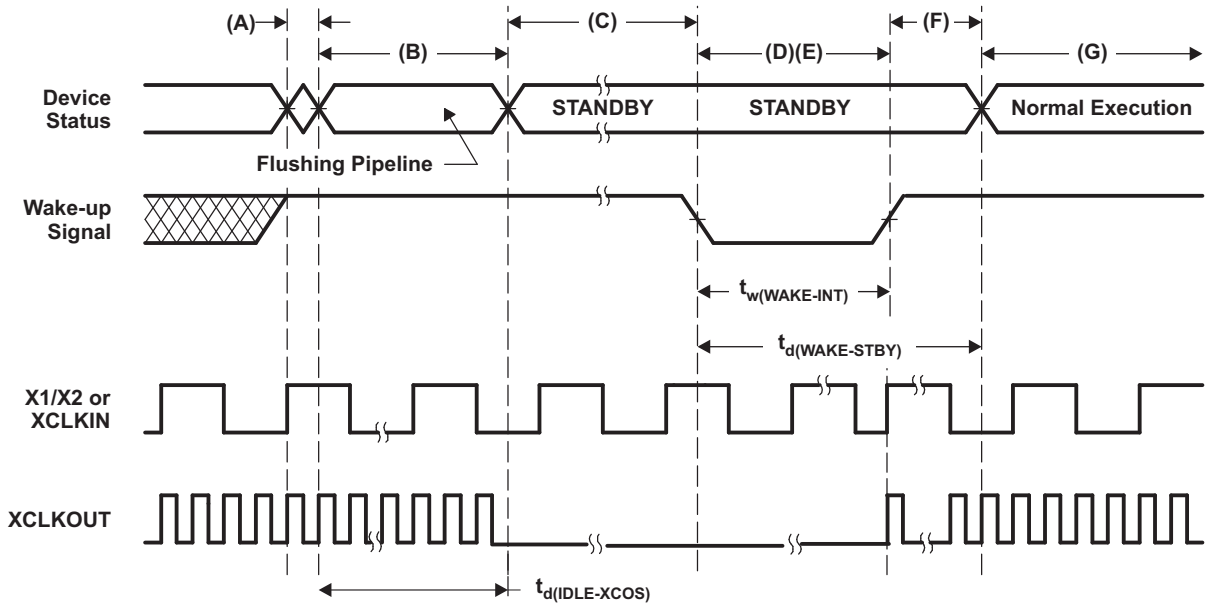

A. IDLE instruction is executed to put the device into STANDBY mode.

B. The LPM block responds to the STANDBY signal, SYSCLK is held for a maximum 16 INTOSC1 clock cycles before being turned off. This delay enables the CPU pipeline and any other pending operations to flush properly.

C. Clock to the peripherals are turned off. However, the PLL and watchdog are not shut down. The device is now in STANDBY mode. After the IDLE instruction is executed, a delay of 5 OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.

D. The external wake-up signal is driven active.

E. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wake-up behavior of the device will not be deterministic and the device may not exit low-power mode for subsequent wake-up pulses.

F. After a latency period, the STANDBY mode is exited.

G. Normal execution resumes. The device will respond to the interrupt (if enabled).

Figure 5-13. STANDBY Entry and Exit Timing Diagram

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Table 5-29 shows the HALT mode timing requirements, Table 5-30 shows the switching characteristics, and Figure 5-14 shows the timing diagram for HALT mode.

Table 5-29. HALT Mode Timing Requirements

		MIN	MAX	UNIT
$t_{w(WAKE-GPIO)}$	Pulse duration, GPIO wake-up signal	$t_{oscst} + 2t_{c(OSCCLK)}$		cycles
$t_{w(WAKE-XRS)}$	Pulse duration, $\overline{XRS}$ wake-up signal	$t_{oscst} + 8t_{c(OSCCLK)}$		cycles

Table 5-30. HALT Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{d(IDLE-XCOS)}$	Delay time, IDLE instruction executed to XCLKOUT stop		$16t_{c(INTOSC1)}$	cycles
$t_{d(WAKE-HALT)}$	Delay time, external wake signal end to CPU1 program execution resume			cycles
	• Wake-up from flash – Flash module in active state		$75t_{c(OSCCLK)}$	
	• Wake-up from flash – Flash module in sleep state		$17500t_{c(OSCCLK)}$	
	• Wake-up from SARAM		$75t_{c(OSCCLK)}$	

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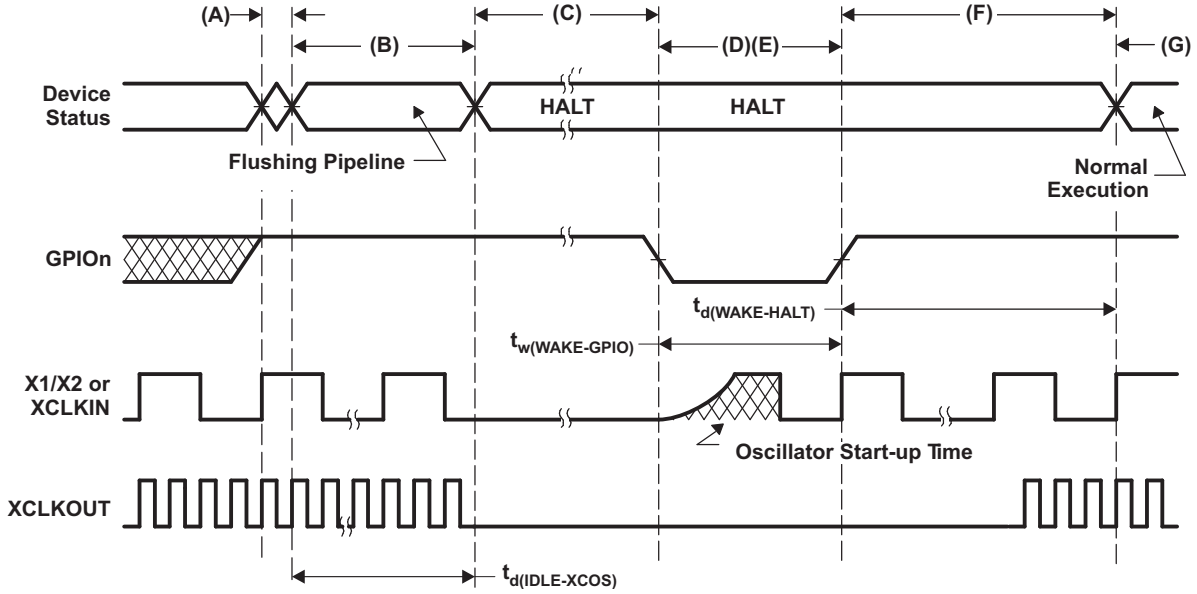

A. IDLE instruction is executed to put the device into HALT mode.

B. The LPM block responds to the HALT signal, SYSCLK is held for a maximum 16 INTOSC1 clock cycles before being turned off. This delay enables the CPU pipeline and any other pending operations to flush properly.

C. Clocks to the peripherals are turned off and the PLL is shut down. If a quartz crystal or ceramic resonator is used as the clock source, the internal oscillator is shut down as well. The device is now in HALT mode and consumes very little power. It is possible to keep the zero-pin internal oscillators (INTOSC1 and INTOSC2) and the watchdog alive in HALT MODE. This is done by writing a 1 to CLKSRCCTL1.WDHALTI. After the IDLE instruction is executed, a delay of 5 OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.

D. When the GPIOn pin (used to bring the device out of HALT) is driven low, the oscillator is turned on and the oscillator wake-up sequence is initiated. The GPIO pin should be driven high only after the oscillator has stabilized. This enables the provision of a clean clock signal during the PLL lock sequence. Because the falling edge of the GPIO pin asynchronously begins the wakeup procedure, care should be taken to maintain a low noise environment prior to entering and during HALT mode.

E. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wake-up behavior of the device will not be deterministic and the device may not exit low-power mode for subsequent wake-up pulses.

F. When CLKIN to the core is enabled, the device will respond to the interrupt (if enabled), after some latency. The HALT mode is now exited.

G. Normal operation resumes.

H. The user must re-lock the PLL upon HALT wake-up to ensure a stable PLL lock.

Figure 5-14. HALT Entry and Exit Timing Diagram

NOTE

CPU2 should enter IDLE mode before CPU1 puts the device into HALT mode. CPU1 should verify that CPU2 has entered IDLE mode using the LPMSTAT register before calling the IDLE instruction to enter HALT.

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Table 5-31 shows the HIBERNATE mode timing requirements, Table 5-32 shows the switching characteristics, and Figure 5-15 shows the timing diagram for HIBERNATE mode.

Table 5-31. HIBERNATE Mode Timing Requirements

		MIN	MAX	UNIT
$t_{w(HIBWAKE)}$	Pulse duration, $\overline{\text{HIBWAKE}}$ signal	40		µs
$t_{w(WAKEXRS)}$	Pulse duration, $\overline{\text{XRS}}$ wake-up signal	40		µs

Table 5-32. HIBERNATE Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(IDLE-XCOS)}$	Delay time, IDLE instruction executed to XCLKOUT stop			$30t_{c(SYSCLK)}$	cycles
$t_{d(WAKE-HIB)}$	Delay time, external wake signal to loRestore function start				ms
	• Wake-up from flash			1.5	

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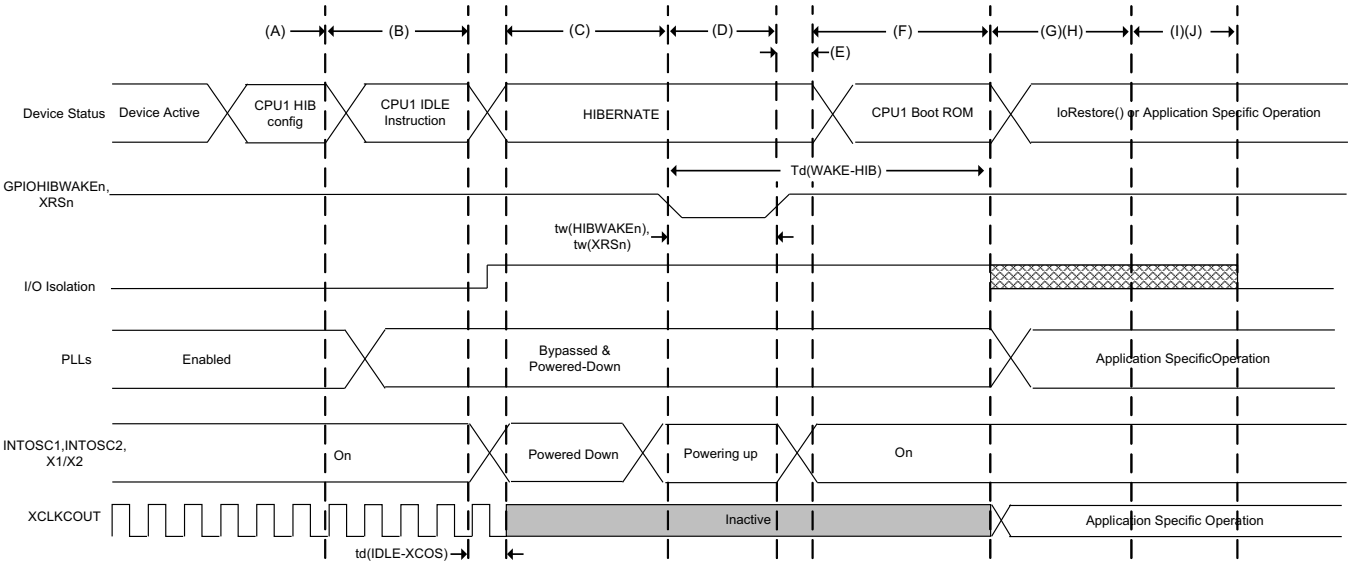

A. CPU1 does necessary application-specific context save to M0/M1 memories if required. This includes GPIO state if using I/O Isolation. Configures CPU1's LPMCR register for HIBERNATE mode. Powers down Flash Pump/Bank, USB-PHY, CMPSS, DAC, and ADC using their register configurations. The application should also power down the PLL and peripheral clocks before entering HIBERNATE. In dual-core applications, CPU1 should confirm that CPU2 has entered IDLE/STANDBY using the LPMSTAT register.

B. IDLE instruction is executed to put the device into HIBERNATE mode.

C. The device is now in HIBERNATE mode. If configured, I/O isolation is turned on, M0 and M1 memories are retained. CPU1 and CPU2 are powered down. Digital peripherals are powered down. The oscillators, PLLs, analog peripherals, and Flash are in their software-controlled Low-Power modes. Dx, LSx, and GSx memories are also powered down, and their memory contents lost.

D. A falling edge on the GPIOHIBWAKEn pin will drive the wake-up of the devices clock sources INTOSC1, INTOSC2, and X1/X2 OSC. The wake-up source must keep the GPIOHIBWAKEn pin low long enough to ensure full power-up of these clock sources.

E. After the clock sources are powered up, the GPIOHIBWAKEn must be driven high to trigger the wake-up sequence of the remainder of the device.

F. The BootROM will then begin to execute. The BootROM can distinguish a HIBERNATE wake-up by reading the CPU1.REC.HIBRESETn bit. After the OTP trims are loaded, the BootROM code will branch to the user-defined IoRestore function if it has been configured.

G. At this point, the device is out of HIBERNATE mode, and the application may continue.

H. The IoRestore function is a user defined function where the application may reconfigure GPIO states, disable I/O isolation, re-configure the PLL, restore peripheral configurations, or branch to application code. This is up to the application requirements.

I. If the application has not branched to application code, the BootROM will continue after completing IoRestore. It will disable I/O isolation automatically if it was not taken care of inside of IoRestore. CPU2 will be brought out of reset at this point as well.

J. BootROM will then boot as determined by the HIBBOOTMODE register. Refer to the "ROM Code and Peripheral Booting" chapter of the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual* (SPRUHM8) for more information.

Figure 5-15. HIBERNATE Entry and Exit Timing Diagram

NOTE

1. If the IORESTOREADDR is configured as the default value, the BootROM will continue its execution to boot as determined by the HIBBOOTMODE register. Refer to the "ROM Code and Peripheral Booting" chapter of the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual* (SPRUHM8) for more information.
2. The user may choose to disable I/O Isolation at any point in the IoRestore function. Regardless if the user has disabled Isolation in the IoRestore function or if IoRestore is not defined, the BootROM will automatically disable isolation before booting as determined by the HIBBOOTMODE register.

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NOTE

For applications using both CPU1 and CPU2, it is recommended that the application puts CPU2 in either IDLE or STANDBY before entering HIBERNATE mode. If any GPIOs are used and the state is to be preserved, data can be stored in CPU1's M0/M1 memory to be reconfigured upon wake-up. This should be done before step A of Figure 5-15.

5.7.5 Peripherals Timings

Electrical Data and Timing for each peripheral is in that peripheral's descriptive section within Section 6, Detailed Description.

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5.8 Current Consumption

Current values listed in this section are representative for the test conditions given and not the absolute maximum possible. The actual device currents in an application will vary with application code and pin configurations.

Table 5-33. Current Consumption at 200 MHz

MODE	TEST CONDITIONS(1) (2)	I_{DD}		I_{DDIO}(3)		I_{DDA}		I_{DD3VFL}	
		TYP(4)	MAX(5)	TYP(4)	MAX(5)	TYP(4)	MAX(5)	TYP(4)	MAX(5)
Operational (RAM)	The following peripherals are exercised (peripherals not listed are not active): • ePWM1 to ePWM12 • eCAP1 to eCAP6 • CAN-A, CAN-B • SPI-A to SPI-C • SCI-A to SCI-D • I^2C-A, I^2C-B • McBSP-A, McBSP-B • SDFM1 to SDFM4 • USB • ADC-A to ADC-D • DAC-A to DAC-C • CMPSS1 to CMPSS8 • CPU1.CLA1, CPU2.CLA1 • CPU1.DMA, CPU2.DMA • CPU1.TIMER0, CPU1.TIMER1, CPU1.TIMER2 • CPU2.TIMER0, CPU2.TIMER1, CPU2.TIMER2 • CPU2.FPU • CPU2.TMU • CPU2.VCU	325 mA	480 mA	30 mA	55 mA	7 mA	25 mA	33 mA	40 mA
IDLE	• Both CPU1 and CPU2 are in IDLE mode. • Flash is powered down. • All peripheral clocks are enabled. • XCLKOUT is turned off.	105 mA	210 mA	3 mA	10 mA	10 µA	150 µA	10 µA	150 µA
STANDBY	• Both CPU1 and CPU2 are in STANDBY mode. • Flash is powered down. • All peripheral clocks are gated. • XCLKOUT is turned off.	30 mA	135 mA	3 mA	10 mA	5 µA	150 µA	10 µA	150 µA

(1) The following is done in a loop on CPU1:
- Code is running out of RAM.
- All I/O pins are left unconnected.
- All of the communication peripherals are exercised in loop-back mode.
- ePWM1–ePWM12 generate 400-kHz PWM output on 24 pins.
- CPU1.DMA does 32-bit burst transfers.
- CPU1.CLA1 does multiply-accumulate tasks.
- ADC performs continuous conversion.
- DAC ramps voltage up/down at 150 kHz.
- FLASH is continuously read and in active state.
- XCLKOUT is enabled.

(2) The following is done in a loop on CPU2:
- CPU2.CLA1 does multiply-accumulate tasks.
- CPU2.VCU does complex multiply/accumulate with parallel load.
- CPU2.TMU calculates a cosine.
- CPU2.FPU does multiply/accumulate with parallel load.

(3) I_{DDIO} current is dependent on the electrical loading on the I/O pins.
(4) TYP: V_{nom}, 30°C
(5) MAX: V_{max}, 125°C

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Table 5-33. Current Consumption at 200 MHz (continued)

MODE	TEST CONDITIONS(1) (2)	I_{DD}		I_{DDIO}(3)		I_{DDA}		I_{DD3VFL}	
		TYP(4)	MAX(5)	TYP(4)	MAX(5)	TYP(4)	MAX(5)	TYP(4)	MAX(5)
HALT(6)	• CPU1 watchdog is running. • Flash is powered down. • XCLKOUT is turned off.	1.5 mA	125 mA	750 µA	1 mA	5 µA	150 µA	10 µA	150 µA
HIBERNATE(7)	• CPU1.M0 and CPU1.M1 RAMs are in low-power data retention mode. • CPU2.M0 and CPU2.M1 RAMs are in low-power data retention mode.	100 µA	4 mA	750 µA	1 mA	5 µA	75 µA	1 µA	50 µA

(6) CPU2 must go into IDLE mode before CPU1 enters HALT mode.
(7) CPU2 must go into reset/IDLE/STANDBY mode before CPU1 enters HIBERNATE mode.

NOTE

The peripheral-I/O multiplexing implemented in the device prevents all available peripherals from being used at the same time because more than one peripheral function may share an I/O pin. Although not useful, it is possible to turn on all peripheral clocks even when the peripheral is not used in the application. If the clocks to all the peripherals are turned on at the same time, the current drawn by the device will be more than the numbers specified in the current consumption table.

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5.8.1 Operational Current Consumption Graphs

The following graphs are a typical representation of the relationship between frequency and current consumption/power. The Operational test from Table 5-33 was run across Frequency at V_{max} and high temperature. Actual results will vary based on the system implementation and conditions.

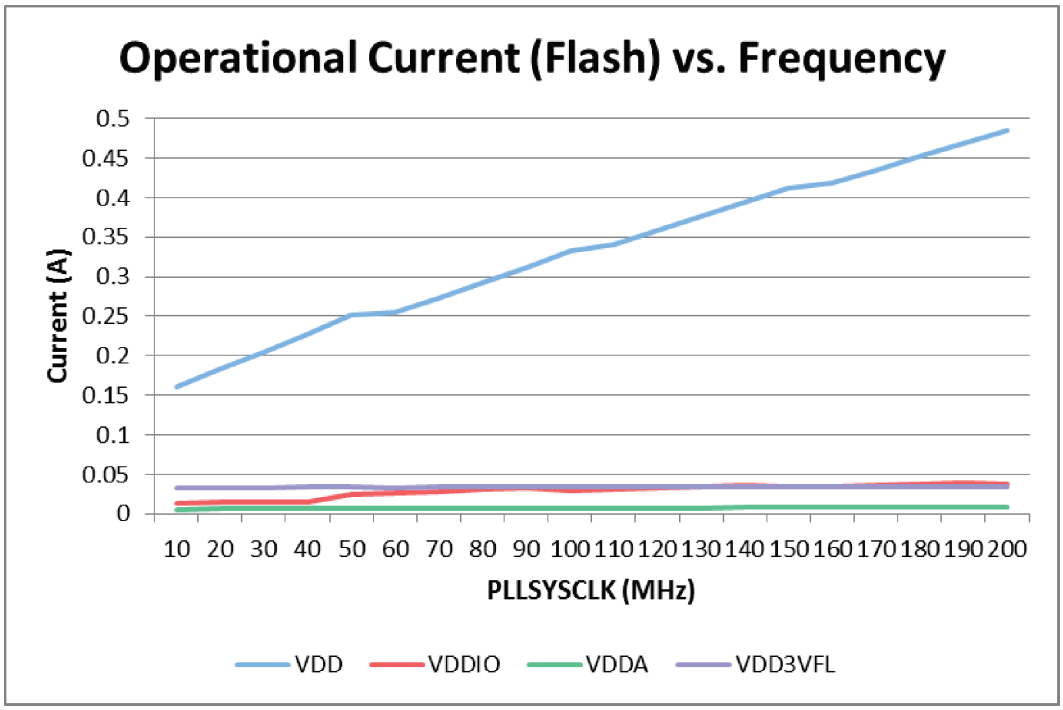

Figure 5-16. Operational Current (Flash) Versus Frequency

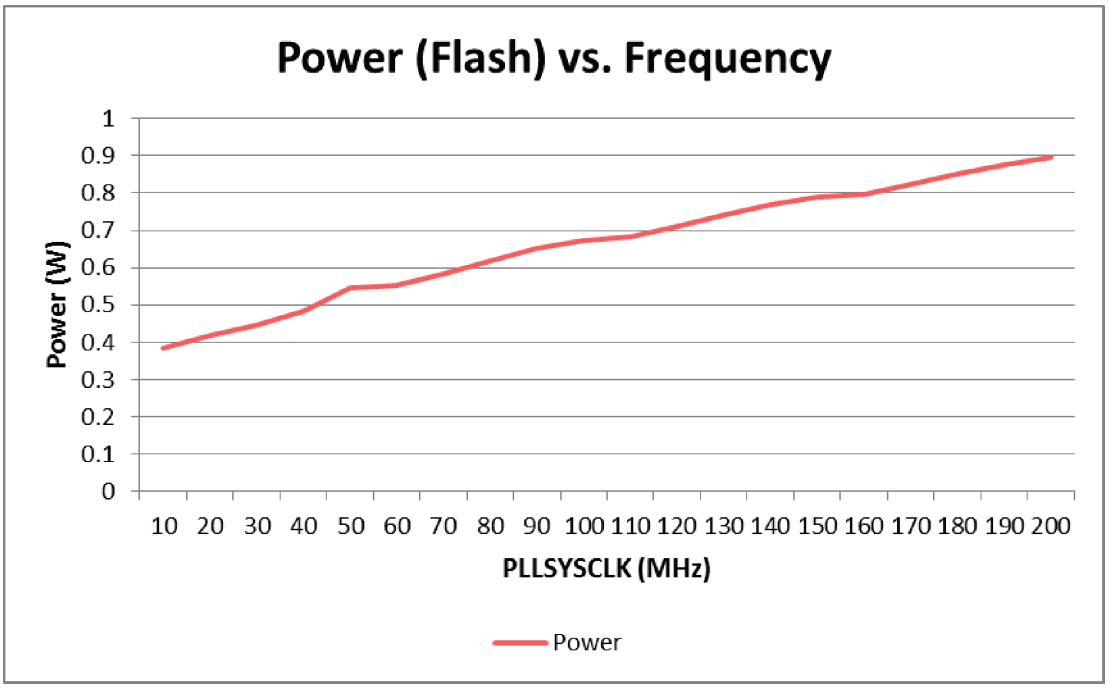

Figure 5-17. Operational Power (Flash) Versus Frequency

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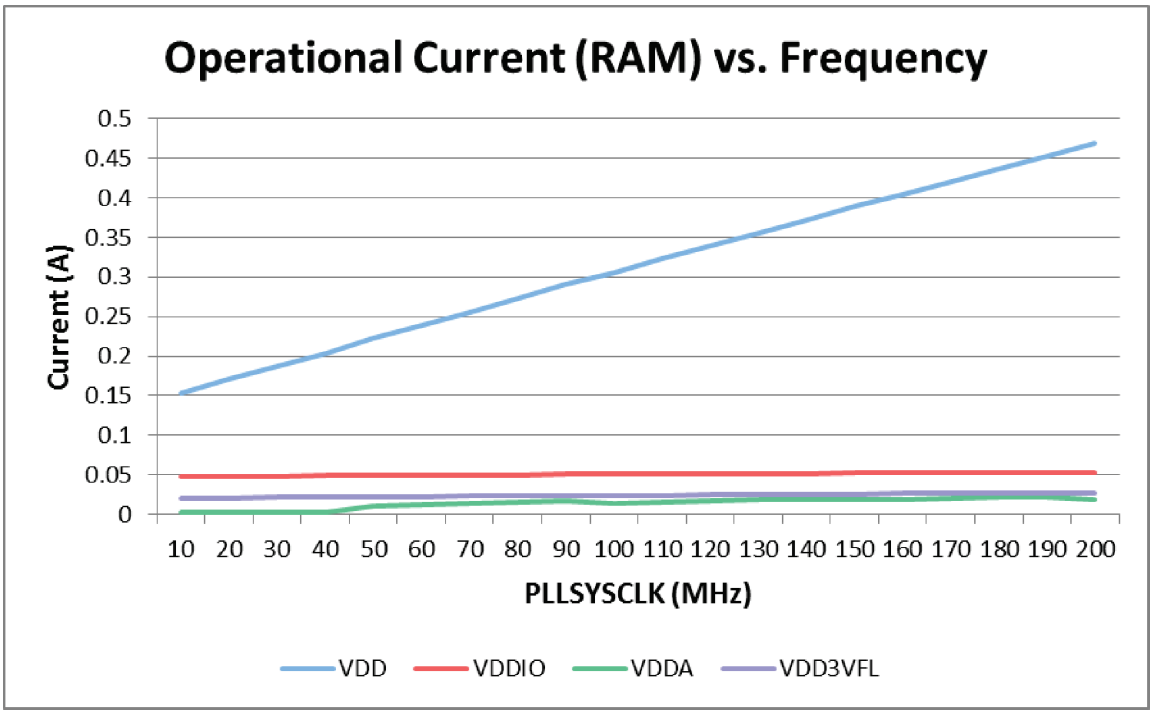

Figure 5-18. Operational Current (RAM) Versus Frequency

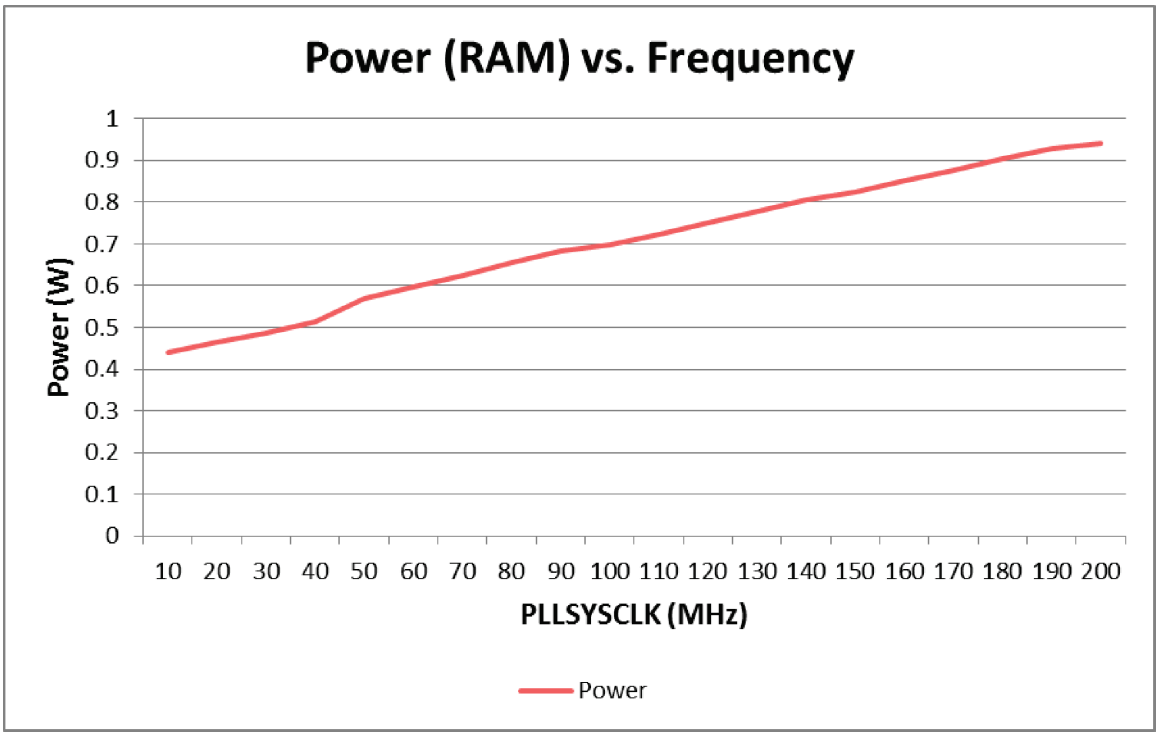

Figure 5-19. Operational Power (RAM) Versus Frequency

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5.8.2 Reducing Current Consumption

The F2837xD devices provide some methods to reduce the device current consumption:

- Each peripheral has an individual clock-enable bit. Reduction in current consumption can be achieved by turning off the clock to any peripheral module that is not used in a given application.
- Any one of the four low-power modes—IDLE, STANDBY, HALT, and HIBERNATE—could be entered to reduce the current consumption even further during idle periods in the application.
- The flash module may be powered down if the code is run from RAM.
- Disable the pullups on pins that assume an output function.

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6 Detailed Description

6.1 Overview

The Delfino TMS320F2837xD is a powerful 32-bit floating-point microcontroller unit (MCU) that lets designers consolidate control architectures and eliminate multiprocessor use in high-end systems. While the Delfino product line is not new to the TMS320C2000 portfolio, the dual-core F2837xD supports a new dual-core C28x architecture that significantly boosts system performance while further providing consolidation through integrated analog and control peripherals.

The dual real-time control subsystems are based on TI's 32-bit C28x floating-point CPUs, which provide 200 MHz of signal processing performance in each core. The C28x CPUs are further boosted by the new TMU accelerator, which enables fast execution of algorithms with trigonometric operations common in transforms and torque loop calculations; and the VCU accelerator, which reduces the latency for complex math operations common in encoded applications.

The F2837xD features two real-time control accelerators, also known as CLAs. The CLA provides an additional floating-point accelerator used to run parallel time-critical control algorithms, providing bandwidth for the C28x to focus on system tasks. The dual C28x + CLA architecture also provides intelligent partitioning of system-critical tasks and allows simultaneous management of these tasks, such as tracking speed and position in one core while managing control-side algorithms to calculate torque loops in the other CPU + CLA.

The TMS320F2837xD supports up to 1MB of onboard flash memory with ECC and up to 204KB of SRAM. Two 128-bit secure zones are also available on each CPU for code protection.

Performance analog and control peripherals are also integrated on the F2837xD MCU to further enable system consolidation. Four independent 16-bit ADCs provide precise and efficient management of multiple analog signals, which ultimately boosts system throughput. New sigma-delta peripherals enable isolated current shunt measurements and windowed comparators allow protection of power stage when current limit conditions are exceeded or not met. Other analog and control peripherals include DACs, PWMs, eCAPs, eQEPs, and other peripherals.

Peripherals such as dual EMIFs and dual ISO11898-1 (CAN 2.0B) extend the connectivity of the F2837xD. A USB 2.0 host port with MAC and PHY lets users easily add universal serial bus (USB) connectivity to their application.

6.2 Functional Block Diagram

Figure 6-1 shows the CPU system and associated peripherals.

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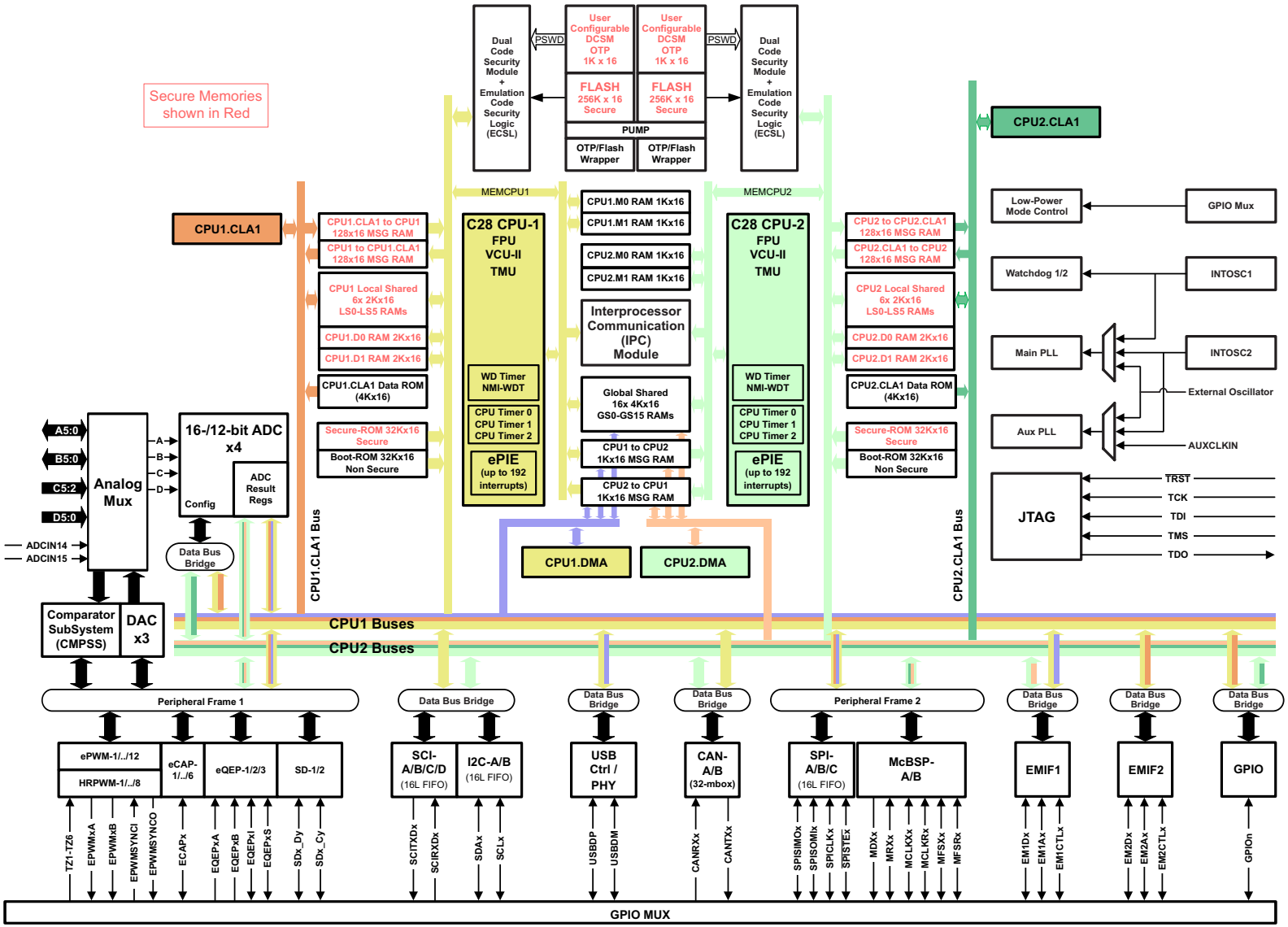

Figure 6-1. Functional Block Diagram

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6.3 Memory

6.3.1 C28x Memory Map

Both C28x CPUs on the device have the same memory map except where noted in Table 6-1. Note the GSx_RAM (Global Shared RAM) should be assigned to either CPU by the GSxMSEL register. Memories accessible by the CLA or DMA (direct memory access) are noted as well.

Table 6-1. C28x Memory Map

MEMORY	SIZE	START ADDRESS	END ADDRESS	CLA ACCESS	DMA ACCESS
M0 RAM	1K x 16	0x0000 0000	0x0000 03FF		
M1 RAM	1K x 16	0x0000 0400	0x0000 07FF		
PieVectTable	512 x 16	0x0000 0D00	0x0000 0EFF		
CPUx.CLA1 to CPUx MSGRAM	128 x 16	0x0000 1480	0x0000 14FF	Yes	
CPUx to CPUx.CLA1 MSGRAM	128 x 16	0x0000 1500	0x0000 157F	Yes	
UPP TX MSG RAM	512 x 16	0x0000 6C00	0x0000 6DFF	Yes	
UPP RX MSG RAM	512 x 16	0x0000 6E00	0x0000 6FFF	Yes	
LS0 RAM	2K x 16	0x0000 8000	0x0000 87FF	Yes	
LS1 RAM	2K x 16	0x0000 8800	0x0000 8FFF	Yes	
LS2 RAM	2K x 16	0x0000 9000	0x0000 97FF	Yes	
LS3 RAM	2K x 16	0x0000 9800	0x0000 9FFF	Yes	
LS4 RAM	2K x 16	0x0000 A000	0x0000 A7FF	Yes	
LS5 RAM	2K x 16	0x0000 A800	0x0000 AFFF	Yes	
D0 RAM	2K x 16	0x0000 B000	0x0000 B7FF		
D1 RAM	2K x 16	0x0000 B800	0x0000 BFFF		
GS0 RAM(1)	4K x 16	0x0000 C000	0x0000 CFFF		Yes
GS1 RAM(1)	4K x 16	0x0000 D000	0x0000 DFFF		Yes
GS2 RAM(1)	4K x 16	0x0000 E000	0x0000 EFFF		Yes
GS3 RAM(1)	4K x 16	0x0000 F000	0x0000 FFFF		Yes
GS4 RAM(1)	4K x 16	0x0001 0000	0x0001 0FFF		Yes
GS5 RAM(1)	4K x 16	0x0001 1000	0x0001 1FFF		Yes
GS6 RAM(1)	4K x 16	0x0001 2000	0x0001 2FFF		Yes
GS7 RAM(1)	4K x 16	0x0001 3000	0x0001 3FFF		Yes
GS8 RAM(1)	4K x 16	0x0001 4000	0x0001 4FFF		Yes
GS9 RAM(1)	4K x 16	0x0001 5000	0x0001 5FFF		Yes
GS10 RAM(1)	4K x 16	0x0001 6000	0x0001 6FFF		Yes
GS11 RAM(1)	4K x 16	0x0001 7000	0x0001 7FFF		Yes
GS12 RAM(1)(2)	4K x 16	0x0001 8000	0x0001 8FFF		Yes
GS13 RAM(1)(2)	4K x 16	0x0001 9000	0x0001 9FFF		Yes
GS14 RAM(1)(2)	4K x 16	0x0001 A000	0x0001 AFFF		Yes
GS15 RAM(1)(2)	4K x 16	0x0001 B000	0x0001 BFFF		Yes
CPU2 to CPU1 MSGRAM(1)	1K x 16	0x0003 F800	0x0003 FBFF		Yes
CPU1 to CPU2 MSGRAM(1)	1K x 16	0x0003 FC00	0x0003 FFFF		Yes
USB RAM(3)	2K x 16	0x0004 1000	0x0004 17FF		Yes
CAN A Message RAM(1)	2K x 16	0x0004 8800	0x0004 97FF		
CAN B Message RAM(1)	2K x 16	0x0004 A800	0x0004 B7FF		
Flash	256K x 16	0x0008 0000	0x000B FFFF		
Secure ROM	32K x 16	0x003F 0000	0x003F 7FFF		
Boot ROM	32K x 16	0x003F 8000	0x003F FFBF		
Vectors	64 x 16	0x003F FFC0	0x003F FFFF		

(1) Shared between CPU subsystems.
(2) Only available on F28377D and F28375D.
(3) Only on the CPU1 subsystem.

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6.3.2 Flash Memory Map

On the F28377D and F28375D devices, each CPU has its own flash bank (256KW), the total flash for each device is 512KW. Only one bank can be programmed or erased at a time and the code to program the flash should be executed out of RAM. Table 6-2 shows the addresses of flash sectors on CPU1 and CPU2 for F28377D and F28375D.

Table 6-2. Addresses of Flash Sectors on CPU1 and CPU2 for F28377D and F28375D

SECTOR	SIZE	START ADDRESS	END ADDRESS
OTP Sectors			
TI OTP	1K x 16	0x0007 0000	0x0007 03FF
User configurable DCSM OTP	1K x 16	0x0007 8000	0x0007 83FF
Sectors			
Sector A	8K x 16	0x0008 0000	0x0008 1FFF
Sector B	8K x 16	0x0008 2000	0x0008 3FFF
Sector C	8K x 16	0x0008 4000	0x0008 5FFF
Sector D	8K x 16	0x0008 6000	0x0008 7FFF
Sector E	32K x 16	0x0008 8000	0x0008 FFFF
Sector F	32K x 16	0x0009 0000	0x0009 7FFF
Sector G	32K x 16	0x0009 8000	0x0009 FFFF
Sector H	32K x 16	0x000A 0000	0x000A 7FFF
Sector I	32K x 16	0x000A 8000	0x000A FFFF
Sector J	32K x 16	0x000B 0000	0x000B 7FFF
Sector K	8K x 16	0x000B 8000	0x000B 9FFF
Sector L	8K x 16	0x000B A000	0x000B BFFF
Sector M	8K x 16	0x000B C000	0x000B DFFF
Sector N	8K x 16	0x000B E000	0x000B FFFF
Flash ECC Locations			
TI OTP ECC	128 x 16	0x0107 0000	0x0107 007F
User OTP ECC	128 x 16	0x0107 1000	0x0107 107F
Flash ECC	32K x16	0x0108 0000	0x0108 7FFF

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On the F28376D and F28374D devices, each CPU has its own flash bank (128KW), the total flash for each device is 256KW. Only one bank can be programmed or erased at a time and the code to program the flash should be executed out of RAM. Table 6-3 shows the addresses of flash sectors on CPU1 and CPU2 for F28376D and F28374D.

Table 6-3. Addresses of Flash Sectors on CPU1 and CPU2 for F28376D and F28374D

SECTOR	SIZE	START ADDRESS	END ADDRESS
OTP Sectors			
TI OTP	1K x 16	0x0007 0000	0x0007 03FF
User configurable DCSM OTP	1K x 16	0x0007 8000	0x0007 83FF
Sectors			
Sector A	8K x 16	0x0008 0000	0x0008 1FFF
Sector B	8K x 16	0x0008 2000	0x0008 3FFF
Sector C	8K x 16	0x0008 4000	0x0008 5FFF
Sector D	8K x 16	0x0008 6000	0x0008 7FFF
Sector E	32K x 16	0x0008 8000	0x0008 FFFF
Sector F	32K x 16	0x0009 0000	0x0009 7FFF
Sector G	32K x 16	0x0009 8000	0x0009 FFFF
Flash ECC Locations			
TI OTP ECC	128 x 16	0x0107 0000	0x0107 007F
User OTP ECC	128 x 16	0x0107 1000	0x0107 107F
Flash ECC	16K x16	0x0108 0000	0x0108 3FFF

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6.3.3 EMIF Chip Select Memory Map

The EMIF1 memory map is the same for both CPU subsystems. EMIF2 is only available on the CPU1 subsystem.

Table 6-4. EMIF Chip Select Memory Map

EMIF CHIP SELECT	SIZE	START ADDRESS	END ADDRESS	CLA ACCESS	DMA ACCESS
EMIF1_CS0n - Data	256M x 16	0x8000 0000	0x8FFF FFFF		Yes
EMIF1_CS2n - Program + Data	2M x 16	0x0010 0000	0x002F FFFF		Yes
EMIF1_CS3n - Program + Data	512K x 16	0x0030 0000	0x0037 FFFF		Yes
EMIF1_CS4n - Program + Data	393K x 16	0x0038 0000	0x003D FFFF		Yes
EMIF2_CS0n - Data(1)	64M x 16	0x9000 0000	0x93FF FFFF		
EMIF2_CS2n - Program + Data(1)	4K x 16	0x0000 2000	0x0000 2FFF	Yes (Data only)	

(1) Only available on the CPU1 subsystem.

6.3.4 Peripheral Registers Memory Map

The peripheral registers memory map can be found in Table 6-5. The peripheral registers can be assigned to either the CPU1 or CPU2 subsystems except where noted in Table 6-5. Registers in the peripheral frames share a secondary master (CLA or DMA) selection with all other registers within the same peripheral frame. See the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual* (SPRUHM8) for details on the CPU subsystem and secondary master selection.

Table 6-5. Peripheral Registers Memory Map

REGISTERS	STRUCTURE NAME	START ADDRESS	END ADDRESS	CLA ACCESS	DMA ACCESS
AdcaResultRegs	ADC_RESULT_REGS	0x0000 0B00	0x0000 0B1F	Yes	Yes
AdcbResultRegs	ADC_RESULT_REGS	0x0000 0B20	0x0000 0B3F	Yes	Yes
AdccResultRegs	ADC_RESULT_REGS	0x0000 0B40	0x0000 0B5F	Yes	Yes
AdcdResultRegs	ADC_RESULT_REGS	0x0000 0B60	0x0000 0B7F	Yes	Yes
CpuTimer0Regs(1)	CPUTIMER_REGS	0x0000 0C00	0x0000 0C07		
CpuTimer1Regs(1)	CPUTIMER_REGS	0x0000 0C08	0x0000 0C0F		
CpuTimer2Regs(1)	CPUTIMER_REGS	0x0000 0C10	0x0000 0C17		
PieCtrlRegs(1)	PIE_CTRL_REGS	0x0000 0CE0	0x0000 0CFF		
Cla1SoftIntRegs	CLA_SOFTINT_REGS	0x0000 0CE0	0x0000 0CFF	Yes – CLA only, no CPU access	
DmaRegs(1)	DMA_REGS	0x0000 1000	0x0000 11FF		
Cla1Regs(1)	CLA_REGS	0x0000 1400	0x0000 147F		
Peripheral Frame 1					
EPwm1Regs	EPWM_REGS	0x0000 4000	0x0000 40FF	Yes	Yes
EPwm2Regs	EPWM_REGS	0x0000 4100	0x0000 41FF	Yes	Yes
EPwm3Regs	EPWM_REGS	0x0000 4200	0x0000 42FF	Yes	Yes
EPwm4Regs	EPWM_REGS	0x0000 4300	0x0000 43FF	Yes	Yes
EPwm5Regs	EPWM_REGS	0x0000 4400	0x0000 44FF	Yes	Yes
EPwm6Regs	EPWM_REGS	0x0000 4500	0x0000 45FF	Yes	Yes
EPwm7Regs	EPWM_REGS	0x0000 4600	0x0000 46FF	Yes	Yes
EPwm8Regs	EPWM_REGS	0x0000 4700	0x0000 47FF	Yes	Yes
EPwm9Regs	EPWM_REGS	0x0000 4800	0x0000 48FF	Yes	Yes
EPwm10Regs	EPWM_REGS	0x0000 4900	0x0000 49FF	Yes	Yes
EPwm11Regs	EPWM_REGS	0x0000 4A00	0x0000 4AFF	Yes	Yes

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Table 6-5. Peripheral Registers Memory Map (continued)

REGISTERS	STRUCTURE NAME	START ADDRESS	END ADDRESS	CLA ACCESS	DMA ACCESS
EPwm12Regs	EPWM_REGS	0x0000 4B00	0x0000 4BFF	Yes	Yes
ECap1Regs	ECAP_REGS	0x0000 5000	0x0000 501F	Yes	Yes
ECap2Regs	ECAP_REGS	0x0000 5020	0x0000 503F	Yes	Yes
ECap3Regs	ECAP_REGS	0x0000 5040	0x0000 505F	Yes	Yes
ECap4Regs	ECAP_REGS	0x0000 5060	0x0000 507F	Yes	Yes
ECap5Regs	ECAP_REGS	0x0000 5080	0x0000 509F	Yes	Yes
ECap6Regs	ECAP_REGS	0x0000 50A0	0x0000 50BF	Yes	Yes
EQep1Regs	EQEP_REGS	0x0000 5100	0x0000 513F	Yes	Yes
EQep2Regs	EQEP_REGS	0x0000 5140	0x0000 517F	Yes	Yes
EQep3Regs	EQEP_REGS	0x0000 5180	0x0000 51BF	Yes	Yes
DacaRegs	DAC_REGS	0x0000 5C00	0x0000 5C0F	Yes	Yes
DacbRegs	DAC_REGS	0x0000 5C10	0x0000 5C1F	Yes	Yes
DaccRegs	DAC_REGS	0x0000 5C20	0x0000 5C2F	Yes	Yes
Cmpss1Regs	CMPSS_REGS	0x0000 5C80	0x0000 5C9F	Yes	Yes
Cmpss2Regs	CMPSS_REGS	0x0000 5CA0	0x0000 5CBF	Yes	Yes
Cmpss3Regs	CMPSS_REGS	0x0000 5CC0	0x0000 5CDF	Yes	Yes
Cmpss4Regs	CMPSS_REGS	0x0000 5CE0	0x0000 5CFF	Yes	Yes
Cmpss5Regs	CMPSS_REGS	0x0000 5D00	0x0000 5D1F	Yes	Yes
Cmpss6Regs	CMPSS_REGS	0x0000 5D20	0x0000 5D3F	Yes	Yes
Cmpss7Regs	CMPSS_REGS	0x0000 5D40	0x0000 5D5F	Yes	Yes
Cmpss8Regs	CMPSS_REGS	0x0000 5D60	0x0000 5D7F	Yes	Yes
Sdfm1Regs	SDFM_REGS	0x0000 5E00	0x0000 5E7F	Yes	Yes
Sdfm2Regs	SDFM_REGS	0x0000 5E80	0x0000 5EFF	Yes	Yes
Peripheral Frame 2					
McbspaRegs	MCBSP_REGS	0x0000 6000	0x0000 603F	Yes	Yes
McbspbRegs	MCBSP_REGS	0x0000 6040	0x0000 607F	Yes	Yes
SpiaRegs	SPI_REGS	0x0000 6100	0x0000 610F	Yes	Yes
SpibRegs	SPI_REGS	0x0000 6110	0x0000 611F	Yes	Yes
SpicRegs	SPI_REGS	0x0000 6120	0x0000 612F	Yes	Yes
UppRegs(2)	UPP_REGS	0x0000 6200	0x0000 62FF	Yes	Yes
WdRegs(1)	WD_REGS	0x0000 7000	0x0000 703F		
NmiIntruptRegs(1)	NMI_INTRUPT_REGS	0x0000 7060	0x0000 706F		
XintRegs(1)	XINT_REGS	0x0000 7070	0x0000 707F		
SciaRegs	SCI_REGS	0x0000 7200	0x0000 720F		
ScibRegs	SCI_REGS	0x0000 7210	0x0000 721F		
ScicRegs	SCI_REGS	0x0000 7220	0x0000 722F		
ScidRegs	SCI_REGS	0x0000 7230	0x0000 723F		
I2caRegs	I2C_REGS	0x0000 7300	0x0000 733F		
I2cbRegs	I2C_REGS	0x0000 7340	0x0000 737F		
AdcaRegs	ADC_REGS	0x0000 7400	0x0000 747F	Yes	
AdcbRegs	ADC_REGS	0x0000 7480	0x0000 74FF	Yes	
AdccRegs	ADC_REGS	0x0000 7500	0x0000 757F	Yes	
AdcdRegs	ADC_REGS	0x0000 7580	0x0000 75FF	Yes	
InputXbarRegs(2)	INPUT_XBAR_REGS	0x0000 7900	0x0000 791F		
XbarRegs(2)	XBAR_REGS	0x0000 7920	0x0000 793F		
TrigRegs(2)	TRIG_REGS	0x0000 7940	0x0000 794F		

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Table 6-5. Peripheral Registers Memory Map (continued)

REGISTERS	STRUCTURE NAME	START ADDRESS	END ADDRESS	CLA ACCESS	DMA ACCESS
DmaClaSrcSelRegs(1)	DMA_CLA_SRC_SEL_REGS	0x0000 7980	0x0000 798F		
EPwmXbarRegs(2)	EPWM_XBAR_REGS	0x0000 7A00	0x0000 7A3F		
OutputXbarRegs(2)	OUTPUT_XBAR_REGS	0x0000 7A80	0x0000 7ABF		
GpioCtrlRegs(2)	GPIO_CTRL_REGS	0x0000 7C00	0x0000 7D7F		
GpioDataRegs(1)	GPIO_DATA_REGS	0x0000 7F00	0x0000 7F2F	Yes	
UsbaRegs(2)	USB_REGS	0x0004 0000	0x0004 0FFF		
Emif1Regs	EMIF_REGS	0x0004 7000	0x0004 77FF		
Emif2Regs(2)	EMIF_REGS	0x0004 7800	0x0004 7FFF		
CanaRegs	CAN_REGS	0x0004 8000	0x0004 87FF		
CanbRegs	CAN_REGS	0x0004 A000	0x0004 A7FF		
IpcRegs(1)	IPC_REGS_CPU1 IPC_REGS_CPU2	0x0005 0000	0x0005 0FFF		
DevCfgRegs(2)	DEV_CFG_REGS	0x0005 D000	0x0005 D17F		
AnalogSubsysRegs(2)	ANALOG_SUBSYS_REGS	0x0005 D180	0x0005 D1FF		
ClkCfgRegs(3)	CLK_CFG_REGS	0x0005 D200	0x0005 D2FF		
CpuSysRegs(1)	CPU_SYS_REGS	0x0005 D300	0x0005 D3FF		
RomPrefetchRegs(2)	ROM_PREFETCH_REGS	0x0005 E608	0x0005 E60B		
DcsmZ1Regs(1)	DCSM_Z1_REGS	0x0005 F000	0x0005 F02F		
DcsmZ2Regs(1)	DCSM_Z2_REGS	0x0005 F040	0x0005 F05F		
DcsmCommonRegs(1)	DCSM_COMMON_REGS	0x0005 F070	0x0005 F07F		
MemCfgRegs(1)	MEM_CFG_REGS	0x0005 F400	0x0005 F47F		
Emif1ConfigRegs(1)	EMIF1_CONFIG_REGS	0x0005 F480	0x0005 F49F		
Emif2ConfigRegs(2)	EMIF2_CONFIG_REGS	0x0005 F4A0	0x0005 F4BF		
AccessProtectionRegs(1)	ACCESS_PROTECTION_REGS	0x0005 F4C0	0x0005 F4FF		
MemoryErrorRegs(1)	MEMORY_ERROR_REGS	0x0005 F500	0x0005 F53F		
RomWaitStateRegs(2)	ROM_WAIT_STATE_REGS	0x0005 F540	0x0005 F541		
Flash0CtrlRegs(1)	FLASH_CTRL_REGS	0x0005 F800	0x0005 FAFF		
Flash0EccRegs(1)	FLASH_ECC_REGS	0x0005 FB00	0x0005 FB3F		

(1) A unique copy of these registers exist on each CPU subsystem.

(2) These registers are only available on the CPU1 subsystem.

(3) These registers are mapped to either CPU1 or CPU2 based on a semaphore.

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6.4 Identification

Table 6-6. Device Identification Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION	
PARTIDH	0x0005 D00A	2	Device part identification number	
			TMS320F28377D	0x00FF 0300
			TMS320F28376D	0x00FE 0300
			TMS320F28375D	0x00FD 0300
			TMS320F28374D	0x00FC 0300
REVID	0x0005 D00C	2	Silicon revision number	
			Revision 0	0x0000 0000
			Revision A	0x0000 0000
			Revision B	0x0000 0002

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6.5 Bus Architecture – Peripheral Connectivity

Table 6-7 shows a broad view of the peripheral and configuration register accessibility from each bus master. Peripherals can be individually assigned to the CPU1 or CPU2 subsystem (for example, ePWM can be assigned to CPU1 and eQEP assigned to CPU2). Peripherals within peripheral frames 1 or 2 will all be mapped to the respective secondary master as a group (if SPI is assigned to CPUx.DMA, then McBSP is also assigned to CPUx.DMA).

Table 6-7. Bus Master Peripheral Access

PERIPHERALS (BY BUS ACCESS TYPE)	CPU1.DMA	CPU1.CLA1	CPU1	CPU2	CPU2.CLA1	CPU2.DMA
Peripherals that can be assigned to CPU1 or CPU2 and have common selectable Secondary Masters						
Peripheral Frame 1: • ePWM/HRPWM • SDFM • eCAP(1) • eQEP(1) • CMPSS(1) • DAC(1)	Y	Y	Y	Y	Y	Y
Peripheral Frame 2: • SPI • McBSP	Y	Y	Y	Y	Y	Y
Peripherals that can be assigned to CPU1 or CPU2 subsystems						
SCI			Y	Y		
I^2C			Y	Y		
CAN			Y	Y		
ADC Configuration		Y	Y	Y	Y	
EMIF1	Y		Y	Y		Y
Peripherals and Device Configuration Registers only on CPU1 subsystem						
EMIF2		Y	Y			
USB and USB RAM	Y		Y			
Device Capability, Peripheral Reset, Peripheral CPU Select			Y			
GPIO Pin Mapping and Configuration			Y			
Analog System Control			Y			
Reset Configuration			Y			
Accessible by only one CPU at a time with Semaphore						
Clock and PLL Configuration			Y	Y		
Peripherals and Registers with Unique Copies of Registers for each CPU and CLA Master(2)						
System Configuration (WD, NMIWD, LPM, Peripheral Clock Gating)			Y	Y		
Flash Configuration(3)			Y	Y		
CPU Timers			Y	Y		
DMA and CLA Trigger Source Select			Y	Y		
GPIO Data(4)		Y	Y	Y	Y	
ADC Results	Y	Y	Y	Y	Y	Y

(1) These modules are on a Peripheral Frame with DMA access; however, they cannot trigger a DMA transfer.
(2) Each CPUx and CPUx.CLA1 can only access its own copy of these registers.
(3) At any given time, only one CPU can perform program or erase operations on the Flash.
(4) The GPIO Data Registers are unique for each CPUx and CPUx.CLAx. When the GPIO Pin Mapping Register is configured to assign a GPIO to a particular master, the respective GPIO Data Register will control the GPIO. See the "General-Purpose Input/Output (GPIO)" chapter of the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual* (SPRUHM8) for more details.

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6.6 CPU and System Control

6.6.1 C28x Processor

The CPU is a 32-bit fixed-point processor. This device draws from the best features of digital signal processing; reduced instruction set computing (RISC); and microcontroller architectures, firmware, and tool sets.

The CPU features include a modified Harvard architecture and circular addressing. The RISC features are single-cycle instruction execution, register-to-register operations, and modified Harvard architecture. The microcontroller features include ease of use through an intuitive instruction set, byte packing and unpacking, and bit manipulation. The modified Harvard architecture of the CPU enables instruction and data fetches to be performed in parallel. The CPU can read instructions and data while it writes data simultaneously to maintain the single-cycle instruction operation across the pipeline. The CPU does this over six separate address/data buses.

For more information on CPU architecture and instruction set, see the *TMS320C28x CPU and Instruction Set Reference Guide* (SPRU430).

6.6.1.1 Floating-Point Unit

The C28x plus floating-point (C28x+FPU) processor extends the capabilities of the C28x fixed-point CPU by adding registers and instructions to support IEEE single-precision floating point operations.

Devices with the C28x+FPU include the standard C28x register set plus an additional set of floating-point unit registers. The additional floating-point unit registers are the following:

- Eight floating-point result registers, RnH (where n = 0–7)
- Floating-point Status Register (STF)
- Repeat Block Register (RB)

All of the floating-point registers, except the repeat block register, are shadowed. This shadowing can be used in high-priority interrupts for fast context save and restore of the floating-point registers.

For more information, see the *TMS320C28x Extended Instruction Sets Reference Guide* (SPRUHS1).

6.6.1.2 Trigonometric Math Unit

The TMU extends the capabilities of a C28x+FPU by adding instructions and leveraging existing FPU instructions to speed up the execution of common trigonometric and arithmetic operations listed in Table 6-8.

Table 6-8. TMU Supported Instructions

INSTRUCTIONS	C EQUIVALENT OPERATION	PIPELINE CYCLES
MPY2PIF32 RaH,RbH	a = b * 2pi	2/3
DIV2PIF32 RaH,RbH	a = b / 2pi	2/3
DIVF32 RaH,RbH,RcH	a = b/c	5
SQRTF32 RaH,RbH	a = sqrt(b)	5
SINPUF32 RaH,RbH	a = sin(b*2pi)	4
COSPUF32 RaH,RbH	a = cos(b*2pi)	4
ATANPUF32 RaH,RbH	a = atan(b)/2pi	4
QUADF32 RaH,RbH,RcH,RdH	Operation to assist in calculating ATANPU2	5

No changes have been made to existing instructions, pipeline or memory bus architecture. All TMU instructions use the existing FPU register set (R0H to R7H) to carry out their operations. A detailed explanation of the workings of the FPU can be found in the *TMS320C28x Extended Instruction Sets Reference Guide* (SPRUHS1).

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6.6.1.3 Viterbi, Complex Math, and CRC Unit II (VCU-II)

The VCU-II is the second-generation Viterbi, Complex Math, and CRC extension to the C28x CPU. The VCU-II extends the capabilities of the C28x CPU by adding registers and instructions to accelerate the performance of FFTs and communications-based algorithms. The C28x+VCU-II supports the following algorithm types:

- **Viterbi Decoding**

  Viterbi decoding is commonly used in baseband communications applications. The Viterbi decode algorithm consists of three main parts: branch metric calculations, compare-select (Viterbi butterfly), and a traceback operation. Table 6-9 shows a summary of the VCU performance for each of these operations.

Table 6-9. Viterbi Decode Performance

VITERBI OPERATION	VCU CYCLES
Branch Metric Calculation (code rate = 1/2)	1
Branch Metric Calculation (code rate = 1/3)	2p
Viterbi Butterfly (add-compare-select)	2 (1)
Traceback per Stage	3 (2)

(1) C28x CPU takes 15 cycles per butterfly.
(2) C28x CPU takes 22 cycles per stage.

- **Cyclic Redundancy Check**

  Cyclic redundancy check (CRC) algorithms provide a straightforward method for verifying data integrity over large data blocks, communication packets, or code sections. The C28x+VCU can perform 8-bit, 16-bit, 24-bit, and 32-bit CRCs. For example, the VCU can compute the CRC for a block length of 10 bytes in 10 cycles. A CRC result register contains the current CRC, which is updated whenever a CRC instruction is executed.

- **Complex Math**

  Complex math is used in many applications, a few of which are:

  – Fast Fourier Transform (FFT)

    The complex FFT is used in spread spectrum communications, as well as in many signal processing algorithms.

  – Complex filters

    Complex filters improve data reliability, transmission distance, and power efficiency. The C28x+VCU can perform a complex I and Q multiply with coefficients (four multiplies) in a single cycle. In addition, the C28x+VCU can read/write the real and imaginary parts of 16-bit complex data to memory in a single cycle.

  Table 6-10 shows a summary of the VCU operations enabled by the VCU.

Table 6-10. Complex Math Performance

COMPLEX MATH OPERATION	VCU CYCLES	NOTES
Add or Subtract	1	32 +/- 32 = 32-bit (Useful for filters)
Add or Subtract	1	16 +/- 32 = 15-bit (Useful for FFT)
Multiply	2p	16 x 16 = 32-bit
Multiply and Accumulate (MAC)	2p	32 + 32 = 32-bit, 16 x 16 = 32-bit
RPT MAC	2p+N	Repeat MAC. Single cycle after the first operation.

For more information, see the *TMS320C28x Extended Instruction Sets Reference Guide* (SPRUHS1).

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6.6.2 Control Law Accelerator

The CLA is an independent single-precision (32-bit) floating-point unit processor with its own bus structure, fetch mechanism, and pipeline. Eight individual CLA tasks can be specified. Each task is started by software or a peripheral such as the ADC, ePWM, eCAP, eQEP, or CPU Timer 0. The CLA executes one task at a time to completion. When a task completes, the main CPU is notified by an interrupt to the PIE and the CLA automatically begins the next highest-priority pending task. The CLA can directly access the ADC Result registers, ePWM, eCAP, eQEP, Comparator and DAC registers. Dedicated message RAMs provide a method to pass additional data between the main CPU and the CLA.

Figure 6-2 shows the CLA block diagram.

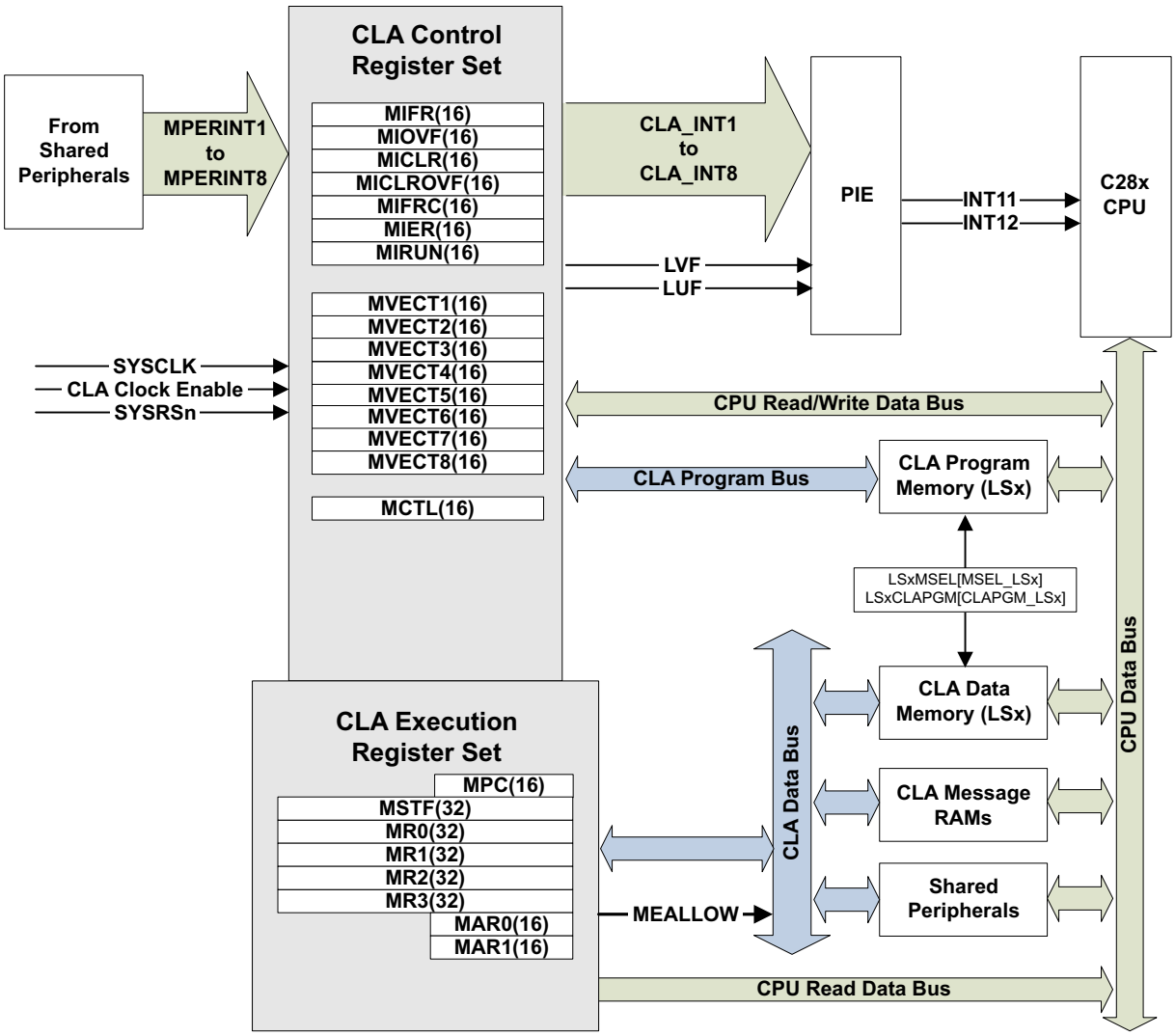

Figure 6-2. CLA Block Diagram

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6.6.3 Direct Memory Access

Each CPU has its own 6-channel DMA module. The DMA module provides a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Additionally, the DMA has the capability to orthogonally rearrange the data as it is transferred as well as “ping-pong” data between buffers. These features are useful for structuring data into blocks for optimal CPU processing.

The DMA module is an event-based machine, meaning it requires a peripheral or software trigger to start a DMA transfer. Although it can be made into a periodic time-driven machine by configuring a timer as the interrupt trigger source, there is no mechanism within the module itself to start memory transfers periodically. The interrupt trigger source for each of the six DMA channels can be configured separately and each channel contains its own independent PIE interrupt to let the CPU know when a DMA transfer has either started or completed. Five of the six channels are exactly the same, while Channel 1 has the ability to be configured at a higher priority than the others.

DMA features include:

- 6 channels with independent PIE interrupts
- Peripheral interrupt trigger sources
  - ADC interrupts and EVT signals
  - Multichannel buffered serial port transmit and receive
  - External interrupts
  - CPU timers
  - EPWMxSOC signals
  - SPIx transmit and receive
  - USBx transmit and receive
  - SDFM
  - Software trigger
- Data sources and destinations:
  - GSx RAM
  - CPU message RAM (IPC RAM)
  - USB RAM
  - ADC result registers
  - ePWMx
  - SPI
  - McBSP
  - EMIF
- Word Size: 16-bit or 32-bit (SPI and McBSP limited to 16-bit)
- Throughput: 4 cycles/word (without arbitration)

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Figure 6-3 shows a device-level block diagram of the DMA.

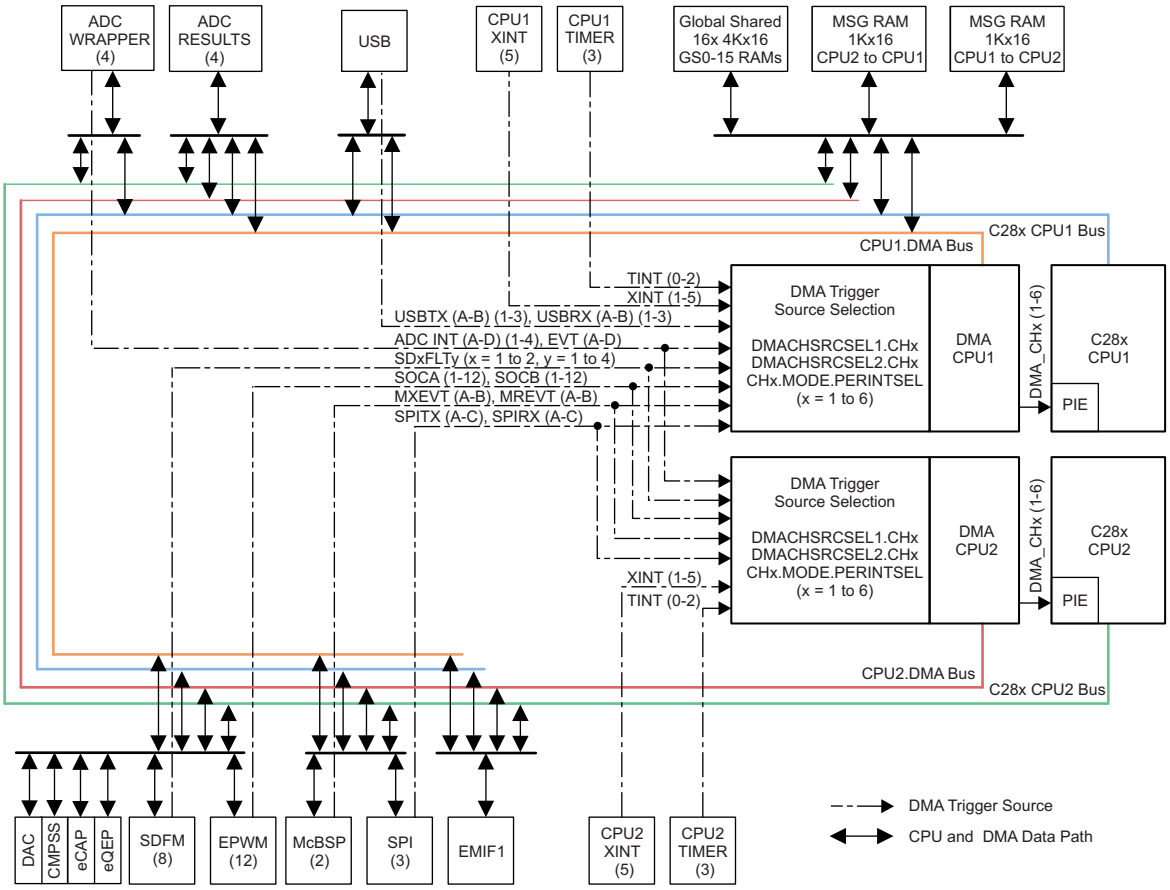

Figure 6-3. DMA Block Diagram

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6.6.4 Interprocessor Communication Module

The IPC module supports several methods of interprocessor communication:

- Thirty-two IPC flags per CPU, which can be used to signal events or indicate status via software polling. Four flags per CPU can generate interrupts.
- Shared data registers, which can be used to send commands or other small pieces of information between CPUs. Although the register names were chosen to support a command/response system, they can be used for any purpose as defined in software.
- Boot mode and status registers, which allow CPU1 to control the CPU2 boot process.
- A general-purpose free-running 64-bit counter.
- Two shared message RAMs, which can be used to transfer bulk data. Each RAM can be read by both CPUs. CPU1 can write to one RAM and CPU2 can write to the other.

Figure 6-4 shows the IPC architecture.

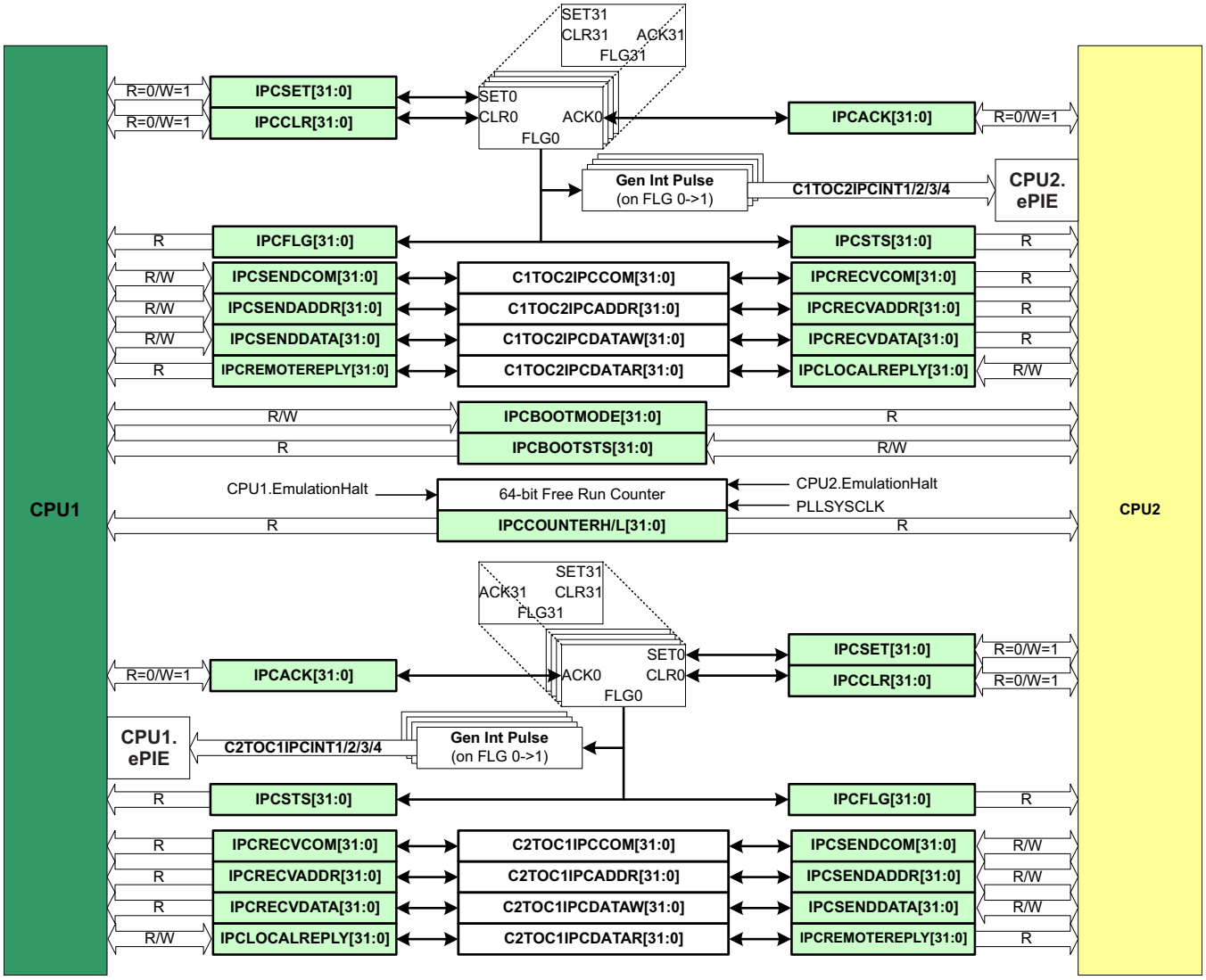

Figure 6-4. IPC Architecture

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6.6.5 Boot ROM and Peripheral Booting

The device boot ROM (on both the CPUs) contains bootloading software. The CPU1 boot ROM does the system initialization before bringing CPU2 out of reset. The device boot ROM is executed each time the device comes out of reset. The device boot ROM is executed each time the device comes out of reset. Users can configure the device to boot to flash (using GET mode) or choose to boot the device through one of the bootable peripherals by configuring the boot mode GPIO pins.

The CPU1 boot ROM, being master, owns the boot mode GPIO and boot configurations. The CPU2 boot ROM either boots to flash (if configured to do so via user configurable DCSM OTP) or enters a WAIT BOOT mode if no OTP is programmed. In WAIT BOOT mode, the CPU1 application instructs the CPU2 boot ROM on how to boot further using boot mode IPC commands supported by CPU2 boot ROM.

Table 6-11 shows the possible boot modes supported on the device. The default boot mode pins are GPIO72 (boot mode pin 1) and GPIO 84 (boot mode pin 0). Users may choose to have weak pullups for boot mode pins if they use a peripheral on these pins as well, so the pullups can be overdriven. On this device, customers can change the factory default boot mode pins by programming user configurable DCSM OTP locations. This is recommended only for cases in which the factory default boot mode pins do not fit into the customer design. More details on the locations to be programmed is available in the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual* (SPRUHM8).

Table 6-11. Device Boot Mode

MODE NO.	CPU1 BOOT MODE	CPU2 BOOT MODE	$\overline{\text{TRST}}$	GPIO72 (BOOT MODE PIN 1)	GPIO84 (BOOT MODE PIN 0)
0	Parallel IO	Boot from Master	0	0	0
1	SCI Mode	Boot from Master	0	0	1
2	Wait Boot Mode	Boot from master	0	1	0
3	Get Mode	Boot from Master	0	1	1
4-7	EMU Boot Mode (Emulator Connected)	Boot from Master	1	X	X

NOTE

The default behavior of Get mode is boot-to-flash. On un-programmed devices, using Get mode will result in repeated watchdog resets, which may prevent proper JTAG connection and device initialization. Use Wait mode or another boot mode for un-programmed devices.

6.6.5.1 EMU Boot or Emulation Boot

The CPU enters this boot when it detects that $\overline{\text{TRST}}$ is HIGH (in other words, when an emulator/debugger is connected). In this mode, the user can program the EMUBOOTCTRL register (at location 0xD00) to instruct the device on how to boot. If the contents of the EMUBOOTCTRL locations are invalid, then the device would default into WAIT Boot mode. The emulation boot allows users to verify the device boot before programming the boot mode into OTP.

6.6.5.2 WAIT Boot Mode

The device in this boot mode loops in the boot ROM. This mode is useful if users want to connect a debugger on a secure device or if users do not want the device to execute an application in flash yet.

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6.6.5.3 Get Mode

The default behavior of Get mode is boot-to-flash. This behavior can be changed by programming the Zx-OTPBOOTCTRL locations in user configurable DCSM OTP. The user configurable DCSM OTP on this device is divided in to two secure zones: Z1 and Z2. The Get mode function in boot ROM first checks if a valid OTPBOOTCTRL value is programmed in Z1. If the answer is yes, then the device boots as per the Z1-OTPBOOTCTRL location. The Z2-OTPBOOTCTRL location is read and decodes only if Z1-OTPBOOTCTRL is invalid or not programmed. If either Zx-OTPBOOTCTRL location is not programmed, then the device defaults to factory default operation, which is to use factory default boot mode pins to boot to flash if the boot mode pins are set to GET MODE. Users can choose the device through which to boot—SPI, I2C, CAN, and USB—by programming proper values into the user configurable DCSM OTP. More details on this can be found in the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual* (SPRUHM8).

6.6.5.4 Peripheral Pins Used by Bootloaders

Table 6-12 shows the GPIO pins used by each peripheral bootloader. This device supports two sets of GPIOs for each mode, as shown in Table 6-12.

Table 6-12. GPIO Pins Used by Each Peripheral Bootloader

BOOTLOADER	GPIO PINS	NOTES
SCI-Boot0	SCITXDA: GPIO84 SCIRXDA: GPIO85	SCIA Boot IO option 1 (default SCI option when chosen through Boot Mode GPIOs)
SCI-Boot1	SCITXDA: GPIO28 SCIRXDA: GPIO29	SCIA Boot option 2 – with alternate IOs.
Parallel Boot	D0 – GPIO65 D1 – GPIO64 D2 – GPIO58 D3 – GPIO59 D4 – GPIO60 D5 – GPIO61 D6 – GPIO62 D7 – GPIO63 HOST_CTRL – GPIO70 DSP_CTRL – GPIO69	
CAN-Boot0	CANRXA: GPIO70 CANTXA: GPIO71	CAN-A Boot -IO Option 1
CAN-Boot1	CANRXA: GPIO62 CANTXA: GPIO63	CAN-A Boot -IO option 2
I2C-Boot0	SDAA: GPIO91 SCLA: GPIO92	I2CA Boot- IO option 1
I2C-Boot1	SDAA: GPIO32 SCLA: GPIO33	I2CA Boot- IO option 2
SPI-Boot0	SPISIMOA - GPIO58 SPISOMIA - GPIO59 SPICLKA - GPIO60 SPISTEA - GPIO61	SPIA Boot- IO Option 1
SPI-Boot1	SPISIMOA – GPIO16 SPISOMIA – GPIO17 SPICLKA – GPIO18 SPISTEA – GPIO19	SPIA Boot - IO Option 2
USB Boot	USB0DM - GPIO42 USB0DP - GPIO43	The USB Bootloader will switch the clock source to the external crystal oscillator (X1 and X2 pins). A 20-MHz crystal should be present on the board if this boot mode is selected.

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6.6.6 Memory

Table 6-13 provides more information about each memory type.

Table 6-13. Memory Types

MEMORY TYPE	ECC-CAPABLE	PARITY	SECURITY	HIBERNATE RETENTION	ACCESS PROTECTION
M0, M1	Yes	–	–	Yes	–
D0, D1	Yes	–	Yes	–	Yes
LSx	–	Yes	Yes	–	Yes
GSx	–	Yes	–	–	Yes
CPU/CLA MSGRAM	–	Yes	Yes	–	Yes
CPU1/CPU2 MSGRAM	–	Yes	–	–	Yes
Flash	Yes	–	Yes	–	N/A
User OTP	Yes	–	Yes	–	N/A

6.6.6.1 Dedicated RAM (Mx and Dx RAM)

The CPU subsystem has four dedicated ECC-capable RAM blocks: M0, M1, D0, and D1. M0/M1 memories are small non-secure blocks that are tightly coupled with the CPU (that is, only the CPU has access to them). D0/D1 memories are secure blocks and also have the access-protection feature (CPU write/CPU fetch protection).

6.6.6.2 Local Shared RAM (LSx RAM)

RAM blocks which are dedicated to each subsystem and are accessible to its CPU and CLA only, are called local shared RAMs (LSx RAMs).

All LSx RAM blocks have parity. These memories are secure and have the access protection (CPU write/CPU fetch) feature.

By default, these memories are dedicated to the CPU only, and the user could choose to share these memories with the CLA by configuring the MSEL_LSx bit field in the LSxMSEL registers appropriately.

Table 6-14. Master Access for LSx RAM (With Assumption That all Other Access Protections are Disabled)

MSEL_LSx	CLAPGM_LSx	CPU ALLOWED ACCESS	CLA1 ALLOWED ACCESS	COMMENT
00	X	All	–	LSx memory is configured as CPU dedicated RAM.
01	0	All	Data Read Data Write	LSx memory is shared between CPU and CLA1.
01	1	Emulation Read Emulation Write	Fetch Only	LSx memory is CLA1 program memory.

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6.6.6.3 Global Shared RAM (GSx RAM)

RAM blocks which are accessible from both the CPU and DMA are called global shared RAMs (GSx RAMs). Each shared RAM block can be owned by either CPU subsystem based on the configuration of respective bits in the GSxMSEL register.

All GSx RAM blocks have parity.

When a GSx RAM block is owned by a CPU subsystem, the CPUx and CPUx.DMA will have full access to that RAM block whereas the other CPUy and CPUy.DMA will only have read access (no fetch/write access).

Table 6-15. Master Access for GSx RAM (With Assumption That all Other Access Protections are Disabled)

GSxMSEL	CPU1 FETCH	CPU1 READ	CPU1 WRITE	CPU1.DMA READ	CPU1.DMA WRITE	CPU2 FETCH	CPU2 READ	CPU2 WRITE	CPU2.DMA READ	CPU2.DMA WRITE
0	Yes	Yes	Yes	Yes	Yes	No	Yes	No	Yes	No
1	No	Yes	No	Yes	No	Yes	Yes	Yes	Yes	Yes

The GSx RAMs have access protection (CPU write/CPU fetch/DMA write).

6.6.6.4 CPU Message RAM (CPU MSGRAM)

These RAM blocks can be used to share data between CPU1 and CPU2. Since these RAMs are used for interprocessor communication, they are also called IPC RAMs. The CPU MSGRAMs have CPU/DMA read/write access from its own CPU subsystem, and CPU/DMA read only access from the other subsystem.

This RAM has parity.

6.6.6.5 CLA Message RAM (CLA MSGRAM)

These RAM blocks are be used to share data between the CPU and CLA. The CLA has read and write access to the "CLA to CPU MSGRAM". The CPU has read and write access to the "CPU to CLA MSGRAM". The CPU and CLA both have read access to both MSGRAMs.

This RAM has parity.

6.6.7 Dual Code Security Module

The dual code security module (DCSM) prevents access to on-chip secure memories. The term “secure” means access to secure memories and resources is blocked. The term “unsecure” means access is allowed; for example, through a debugging tool such as Code Composer Studio.

The code security mechanism offers protection for two zones, Zone 1 (Z1) and Zone 2 (Z2). The security implementation for both the zones is identical. Each zone has its own dedicated secure resource and allocated secure resource.

The security of each zone is ensured by its own 128-bit password (CSM password). The password for each zone is stored in an OTP memory location based on a zone-specific link pointer. The link pointer value can be changed to program a different set of security settings (including passwords) in OTP. The secure resources available are: OTP memory, CLA, LSx RAM, flash sectors, and secure ROM.

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6.6.8 Timers

CPU-Timers 0, 1, and 2 are identical 32-bit timers with presettable periods and with 16-bit clock prescaling. The timers have a 32-bit count-down register that generates an interrupt when the counter reaches zero. The counter is decremented at the CPU clock speed divided by the prescale value setting. When the counter reaches zero, it is automatically reloaded with a 32-bit period value.

CPU-Timer 0 is for general use and is connected to the PIE block. CPU-Timer 1 is also for general use and is connected to INT13 of the CPU. CPU-Timer 2 is reserved for SYS/BIOS. It is connected to INT14 of the CPU. If SYS/BIOS is not being used, CPU-Timer 2 is available for general use.

CPU-Timer 2 can be clocked by any one of the following:

- SYSCLK (default)
- Internal zero-pin oscillator 1 (INTOSC1)
- Internal zero-pin oscillator 2 (INTOSC2)
- External clock source

6.6.9 Nonmaskable Interrupt Watchdog

The NMI is used to monitor erroneous conditions in the system. There is a NMIWD module for each CPU. The conditions monitored are:

- A missing clock condition
- Uncorrectable memory errors on C28x access to Flash
- Uncorrectable memory errors on C28x, CLA, or DMA access to RAM
- Vector fetch ERROR on the other CPU

If the software does not respond to the enabled latched FAIL condition, then the NMI watchdog will trigger a reset after a preprogrammed time interval.

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6.6.10 Watchdog

The watchdog module is the same as the one on previous TMS320C2000™ devices, but with an optional lower limit on the time between software resets of the counter. This windowed countdown is disabled by default, so the watchdog is fully backwards-compatible.

The watchdog is capable of generating either a reset or an interrupt. It is clocked from the internal oscillator with a selectable frequency divider.

Figure 6-5 shows the various functional blocks within the watchdog module.

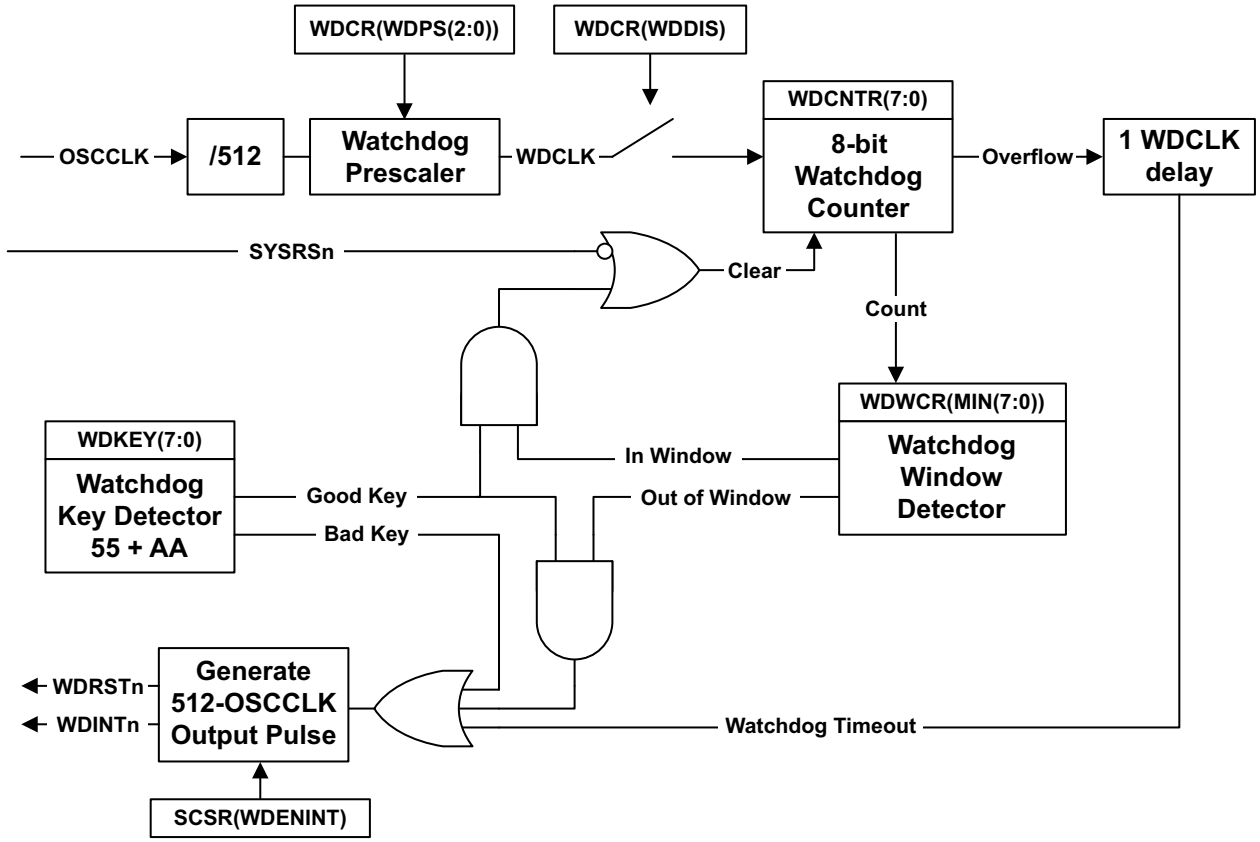

Figure 6-5. Windowed Watchdog

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6.7 Emulation/JTAG

The JTAG port has five dedicated pins: $\overline{\text{TRST}}$, TMS, TDI, TDO, and TCK. The $\overline{\text{TRST}}$ signal should always be pulled down via a 2.2-kΩ pulldown resistor on the board. This MCU does not support the EMU0 and EMU1 signals that are present on 14-pin and 20-pin emulation headers. These signals should always be pulled up at the emulation header through a pair of board pullup resistors ranging from 2.2 kΩ to 4.7 kΩ (depending on the drive strength of the debugger ports). Typically, a 2.2-kΩ value is used.

See Figure 6-6 to see how the 14-pin JTAG header connects to the MCU's JTAG port signals. Figure 6-7 shows how to connect to the 20-pin header. The 20-pin JTAG header terminals EMU2, EMU3, and EMU4 are not used and should be grounded.

The PD (Power Detect) terminal of the emulator header should be connected to the board 3.3-V supply. Header GND terminals should be connected to board ground. TDIS (Cable Disconnect Sense) should also be connected to board ground. The JTAG clock should be looped from the header TCK output terminal back to the RTCK input terminal of the header (to sense clock continuity by the emulator). Header terminal $\overline{\text{RESET}}$ is an open-drain output from the emulator header that enables board components to be reset via emulator commands (only available through the 20-pin header).

Typically, no buffers are needed on the JTAG signals when the distance between the MCU target and the JTAG header is smaller than 6 inches (15.24 cm), and no other devices are present on the JTAG chain. Otherwise, each signal should be buffered. Additionally, for most emulator operations at 10 MHz, no series resistors are needed on the JTAG signals. However, if high emulation speeds are expected (35 MHz or so), 22-Ω resistors should be placed in series on each JTAG signal.

See the XDS Target Connection Guide for more information about JTAG emulation.

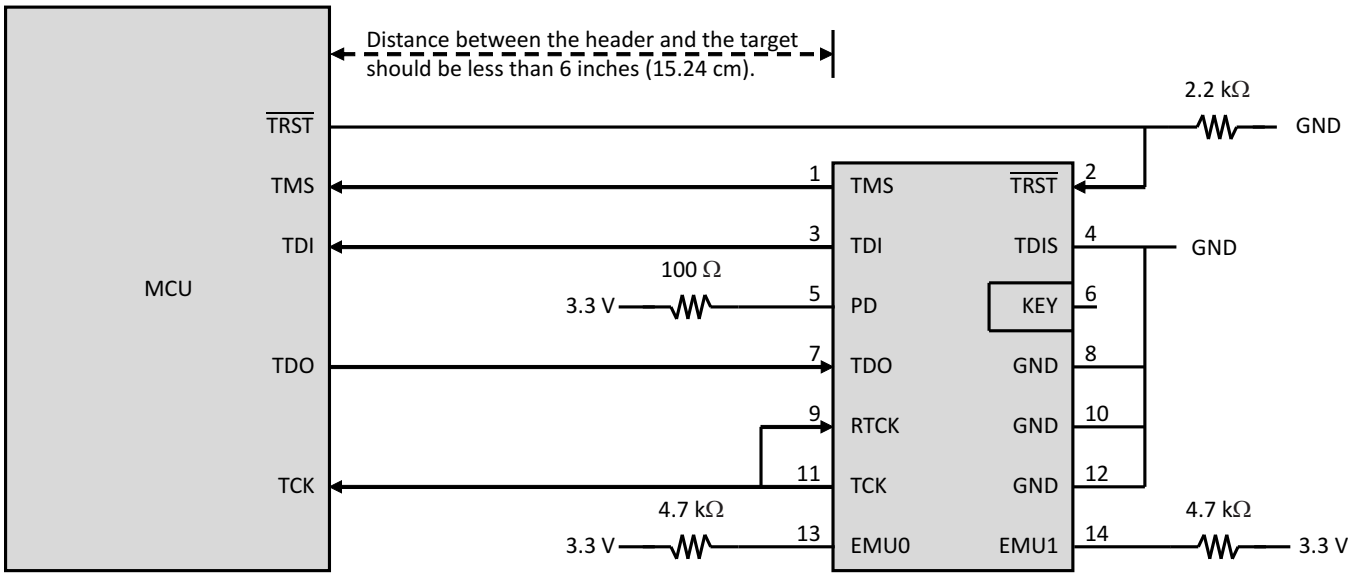

Figure 6-6. Connecting to the 14-Pin JTAG Header

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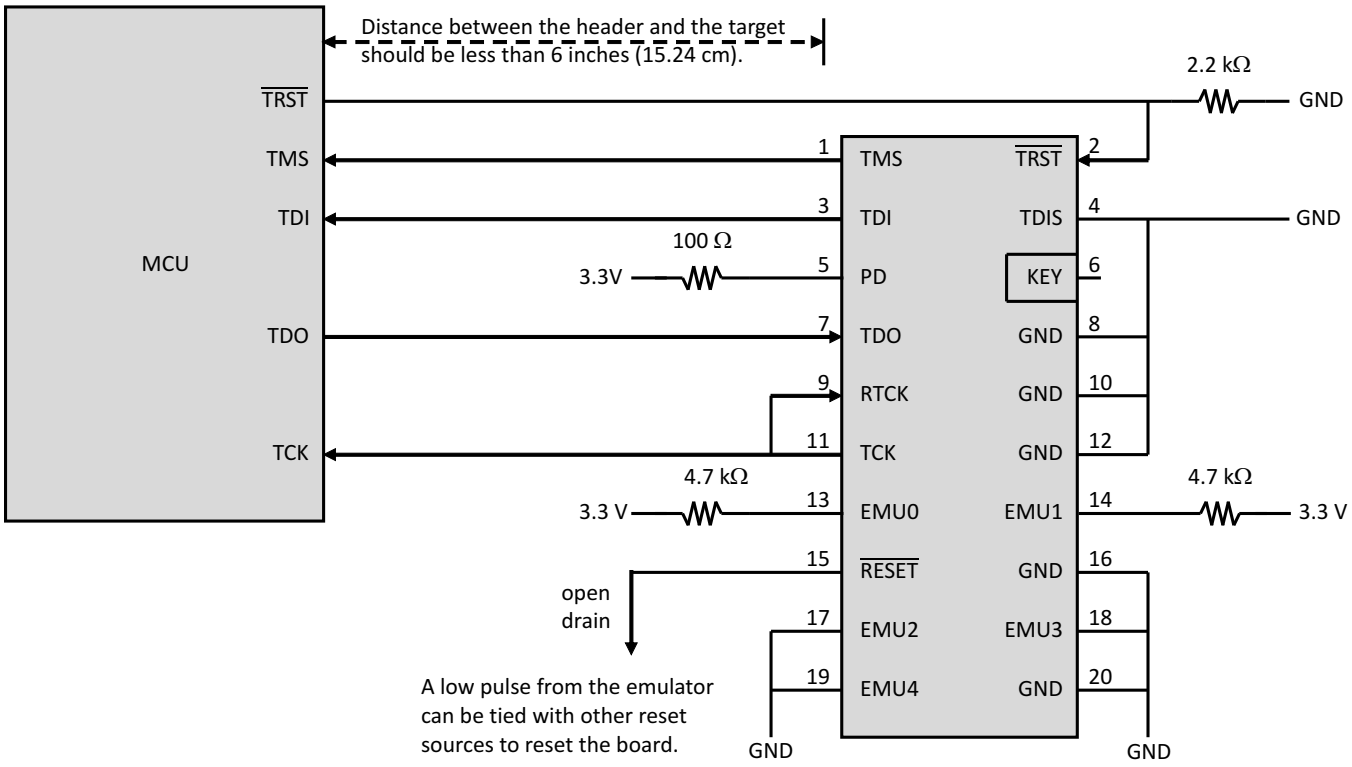

Figure 6-7. Connecting to the 20-Pin JTAG Header

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6.8 Analog Peripherals

NOTE

For the actual number of each peripheral on a specific device, see Table 3-1.

The analog subsystem consists of:

- Four ADCs with selectable resolution of 16 bits or 12 bits
- Eight comparator subsystems, each containing two 12-bit reference DACs, two comparators, and a digital deglitching filter
- Three 12-bit buffered output DACs

Figure 6-8 shows the Analog Subsystem Block Diagram for the 337-ball ZWT package. Figure 6-9 shows the Analog Subsystem Block Diagram for the 176-pin PTP package.

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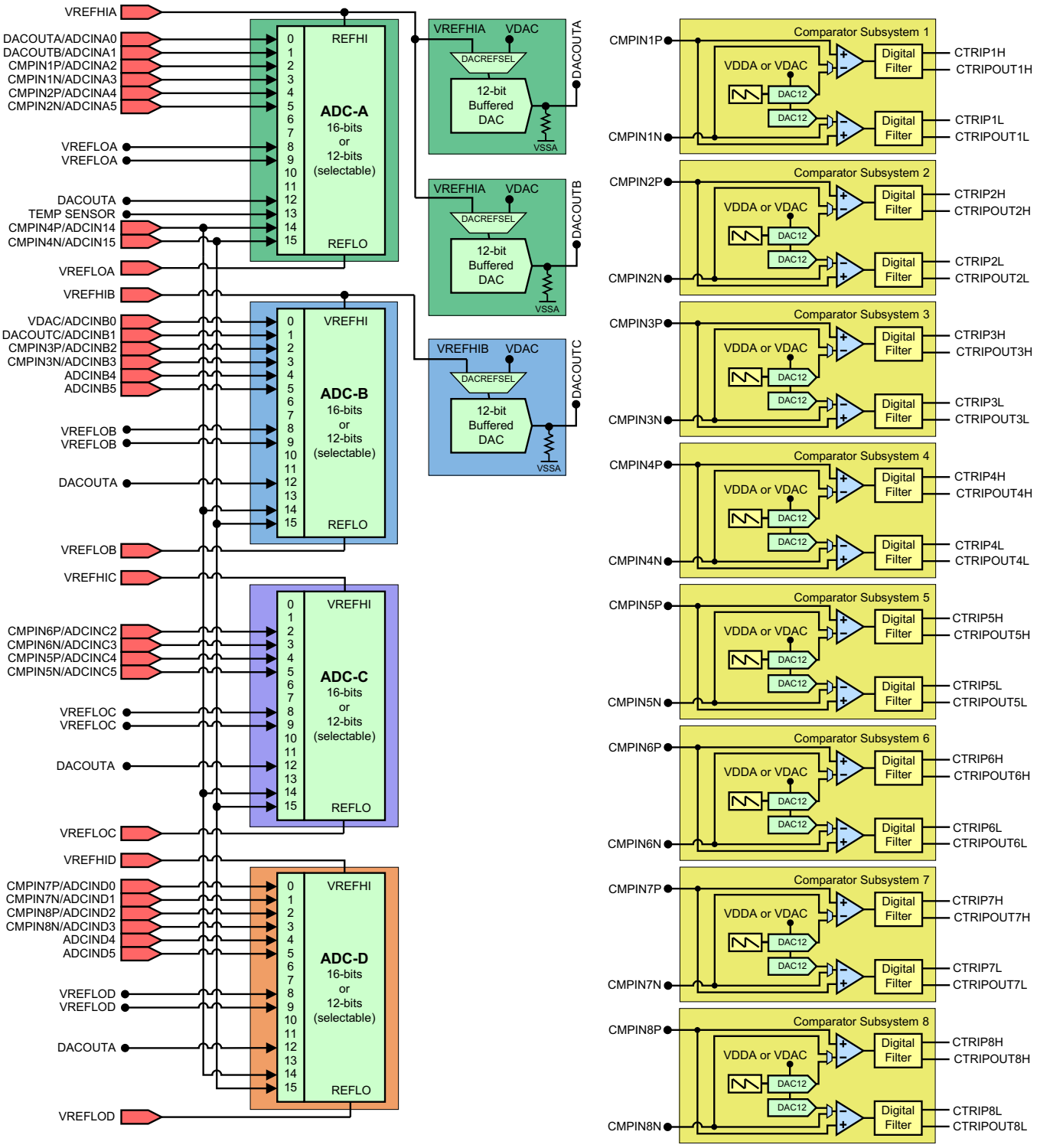

Figure 6-8. Analog Subsystem Block Diagram (337-Ball ZWT)

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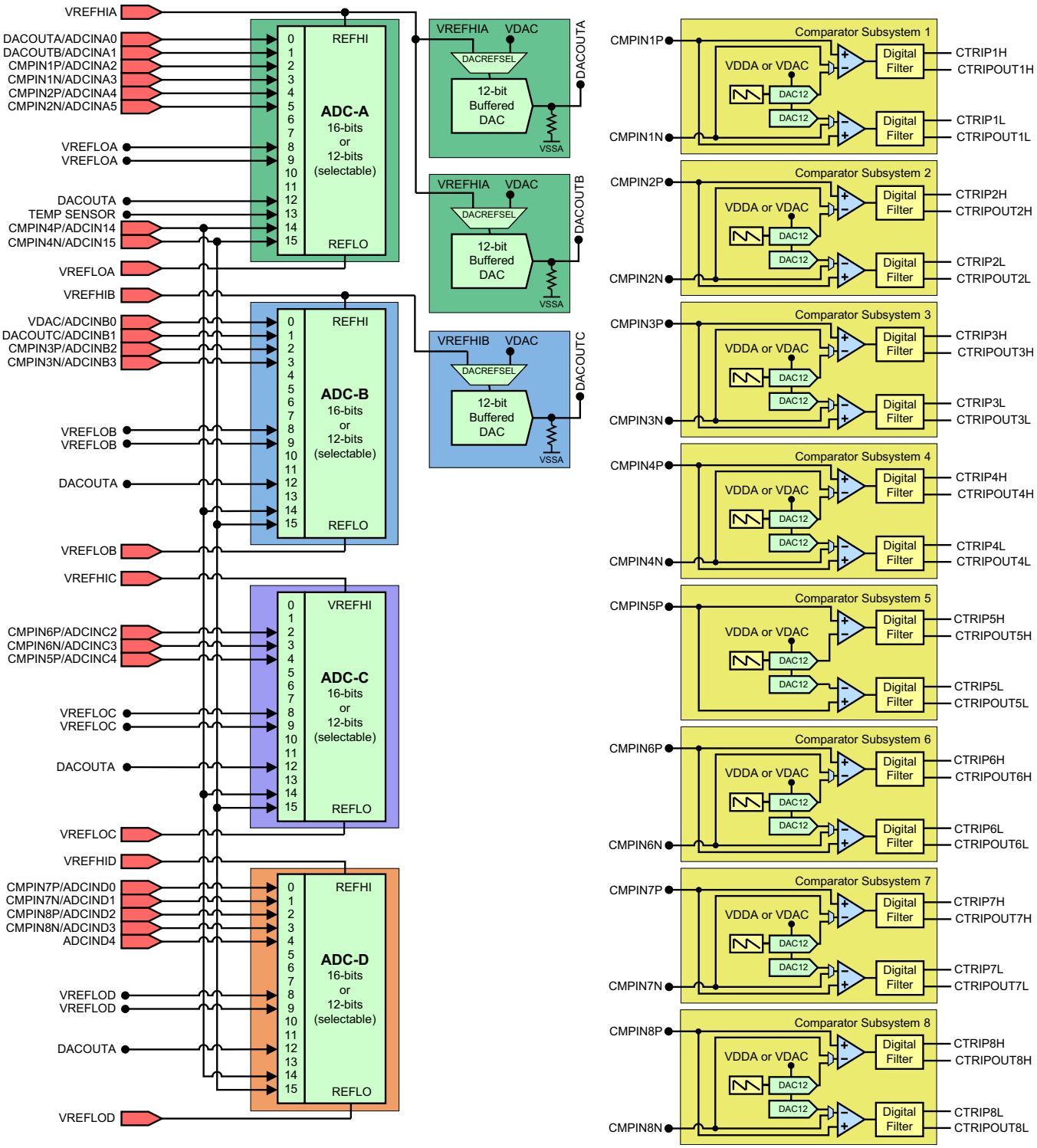

Figure 6-9. Analog Subsystem Block Diagram (176-Pin PTP)

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6.8.1 Analog-to-Digital Converter

The ADCs on this device are successive approximation (SAR) style ADCs with selectable resolution of either 16 bits or 12 bits. There are multiple ADC modules, allowing simultaneous sampling or independent operation. The ADC wrapper is start-of-conversion (SOC) based [see the "SOC Principle of Operation" section of the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual* (SPRUHM8)].

Each ADC has the following features:

- Selectable resolution of 16 bits or 12 bits
- Ratiometric external reference set by V_{REFHI} and V_{REFLO}
- Differential signal conversions (16-bit mode only)
- Single-ended signal conversions (12-bit mode only)
- Input multiplexer with up to 16 channels (single-ended) or 8 channels (differential)
- 16 configurable SOCs
- 16 individually addressable result registers
- Multiple trigger sources
  - Software immediate start
  - All ePWMs
  - GPIO XINT2
  - CPU timers
  - ADCINT1 or 2
- Four flexible PIE interrupts
- Burst mode
- Four post-processing blocks, each with:
  - Saturating offset calibration
  - Error from setpoint calculation
  - High, low, and zero-crossing compare, with interrupt and ePWM trip capability
  - Trigger-to-sample delay capture

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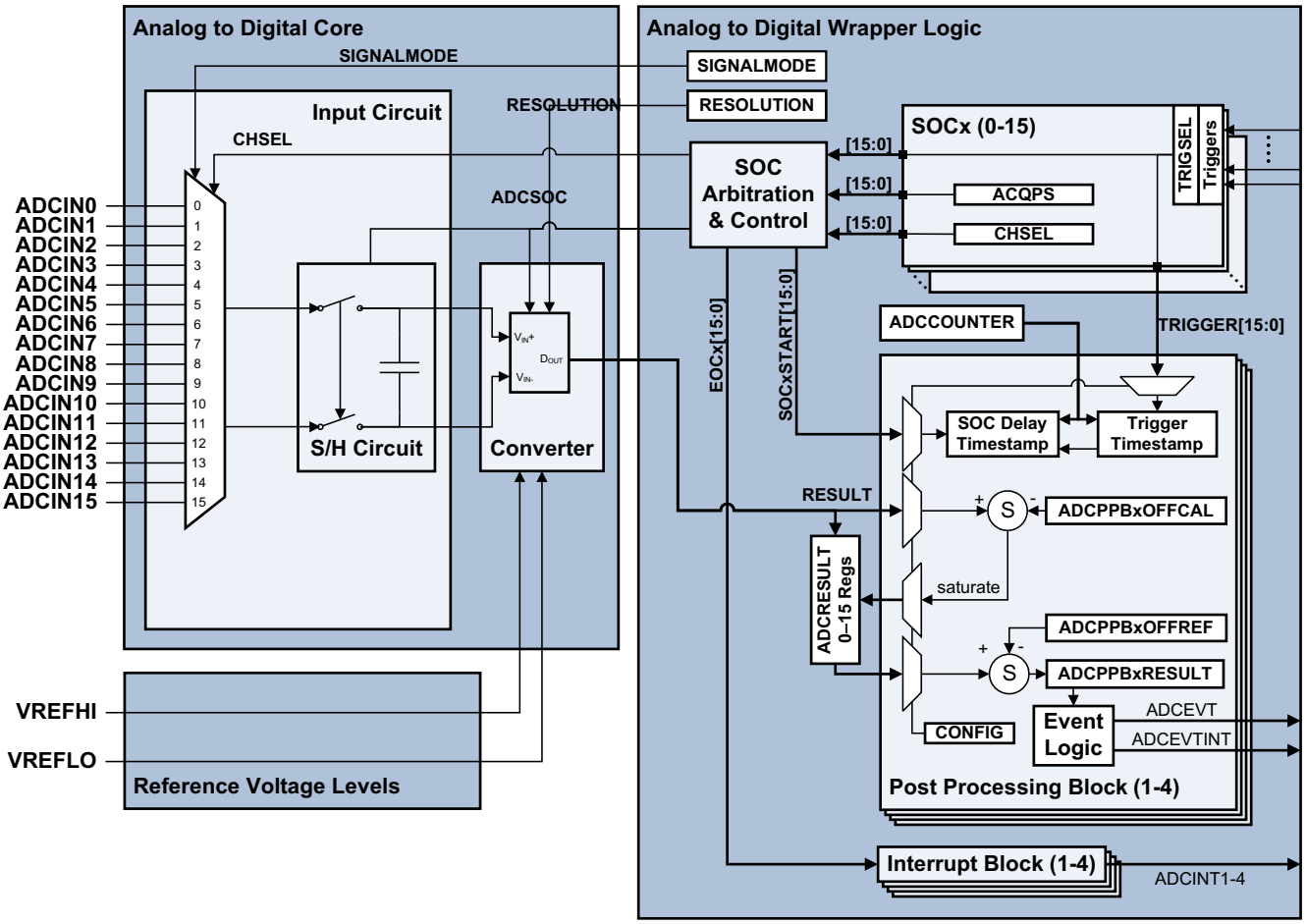

Figure 6-10. ADC Module Block Diagram

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6.8.1.1 ADC Electrical Data and Timing

Table 6-16. ADC Operating Conditions (16-Bit Differential Mode)

over recommended operating conditions (unless otherwise noted)

	MIN	TYP	MAX	UNIT
Input clock	5		50	MHz
Sample window duration	320			ns
Conversion range	V_{REFLO}		V_{REFHI}	V
V_{REFHI}	2.4	2.5 or 3.0	V_{DDA}	V
V_{REFLO}	V_{SSA}	0	V_{SSA}	V
Input common mode voltage(1)	V_{REFCM} – 50		V_{REFCM} + 50	mV

(1) $V_{REFCM} = (V_{REFHI} + V_{REFLO})/2$

Table 6-17. ADC Characteristics (16-Bit Differential Mode)

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC conversion cycles(1)		29.6		31	ADCCLKs
Power-up time				500	µs
Gain error		–64	±9	64	LSBs
Offset error(2)		–16	±9	16	LSBs
Channel-to-channel gain error			±6		LSBs
Channel-to-channel offset error			±3		LSBs
ADC-to-ADC gain error	Identical V_{REFHI} and V_{REFLO} for all ADCs		±TBD		LSBs
ADC-to-ADC offset error	Identical V_{REFHI} and V_{REFLO} for all ADCs		±TBD		LSBs
DNL(3)		> –1	±0.5	1	LSBs
INL		–3	±1.5	3	LSBs
SNR	V_{REFHI} = 2.5 V, f_{in} = 10 kHz		86.9		dB
THD	V_{REFHI} = 2.5 V, f_{in} = 10 kHz		–93.5		dB
SFDR	V_{REFHI} = 2.5 V, f_{in} = 10 kHz		95.4		dB
SINAD	V_{REFHI} = 2.5 V, f_{in} = 10 kHz		86.6		dB
ENOB	V_{REFHI} = 2.5 V, f_{in} = 10 kHz		14.1		bits
PSRR	V_{DDA} = 3.3-V DC + 200 mV Sine at 1 kHz		77		dB
PSRR	V_{DDA} = 3.3-V DC + 200 mV Sine at 800 kHz		74		dB
ADC-to-ADC isolation (synchronous)(4)(5)			±4		LSBs
ADC-to-ADC isolation (asynchronous)(4)(6)			±TBD		LSBs

(1) See Section 6.8.1.1.2.
(2) Difference from conversion result 32768 when ADCINp = ADCINn = V_{REFCM}.
(3) No missing codes.
(4) Code deviation due to operation of multiple ADCs simultaneously.
(5) All ADCs operating with identical ADCCLK, S+H duration, and triggers.
(6) All ADCs operating with heterogenous ADCCLK, S+H duration, or triggers.

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Table 6-18. ADC Operating Conditions (12-Bit Single-Ended Mode)

over recommended operating conditions (unless otherwise noted)

	MIN	TYP	MAX	UNIT
Input clock	5		50	MHz
Sample window duration	75			ns
Conversion range	V_{REFLO}		V_{REFHI}	V
V_{REFHI}	2.4	2.5 or 3.0	V_{DDA}	V
V_{REFLO}	V_{SSA}	0	V_{SSA}	V

Table 6-19. ADC Characteristics (12-Bit Single-Ended Mode)

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC conversion cycles (1)		10.1		11	ADCCLKs
Power-up time				500	µs
Gain error		–8	±6	8	LSBs
Offset error		–4	±2	4	LSBs
Channel-to-channel gain error			±4		LSBs
Channel-to-channel offset error			±2		LSBs
ADC-to-ADC gain error	Identical V_{REFHI} and V_{REFLO} for all ADCs		±TBD		LSBs
ADC-to-ADC offset error	Identical V_{REFHI} and V_{REFLO} for all ADCs		±TBD		LSBs
DNL (2)		> –1	±0.5	1	LSBs
INL		–2	±1.0	2	LSBs
SNR	V_{REFHI} = 2.5 V, f_{in} = 100 kHz		67.8		dB
THD	V_{REFHI} = 2.5 V, f_{in} = 100 kHz		–78.4		dB
SFDR	V_{REFHI} = 2.5 V, f_{in} = 100 kHz		79.2		dB
SINAD	V_{REFHI} = 2.5 V, f_{in} = 100 kHz		67.7		dB
ENOB	V_{REFHI} = 2.5 V, f_{in} = 100 kHz		11.0		bits
PSRR	V_{DDA} = 3.3-V DC + 200 mV Sine at 1 kHz		60		dB
PSRR	V_{DDA} = 3.3-V DC + 200 mV Sine at 800 kHz		57		dB
ADC-to-ADC isolation (synchronous) (3) (4)			±1		LSBs
ADC-to-ADC isolation (asynchronous) (3) (5)			±TBD		LSBs

(1) See Section 6.8.1.1.2.
(2) No missing codes.
(3) Code deviation due to operation of multiple ADCs simultaneously.
(4) All ADCs operating with identical ADCCLK, S+H duration, and triggers.
(5) All ADCs operating with heterogenous ADCCLK, S+H duration, or triggers.

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6.8.1.1.1 ADC Input Models

NOTE

ADC channels ADCINA0, ADCINA1, and ADCINB0 have a 50-kΩ pulldown resistor to V_{SSA}.

For single-ended operation, the ADC input characteristics are given by Table 6-20 and Figure 6-11.

Table 6-20. Single-Ended Input Model Parameters

	DESCRIPTION	VALUE (12-BIT MODE)
C_p	Parasitic input capacitance	See Table 6-22
R_{on}	Sampling switch resistance	500 Ω
C_h	Sampling capacitor	14.5 pF
R_s	Nominal source impedance	50 Ω

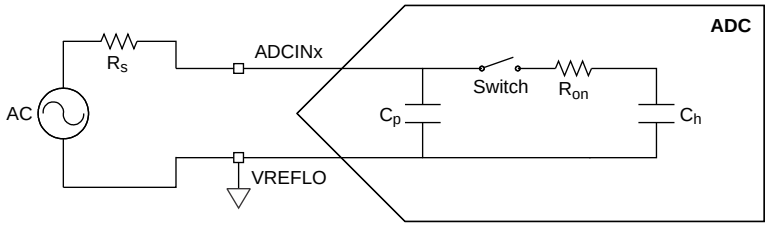

Figure 6-11. Single-Ended Input Model

For differential operation, the ADC input characteristics are given by Table 6-21 and Figure 6-12.

Table 6-21. Differential Input Model Parameters

	DESCRIPTION	VALUE (16-BIT MODE)
C_p	Parasitic input capacitance	See Table 6-22
R_{on}	Sampling switch resistance	700 Ω
C_h	Sampling capacitor	16.5 pF
R_s	Nominal source impedance	50 Ω

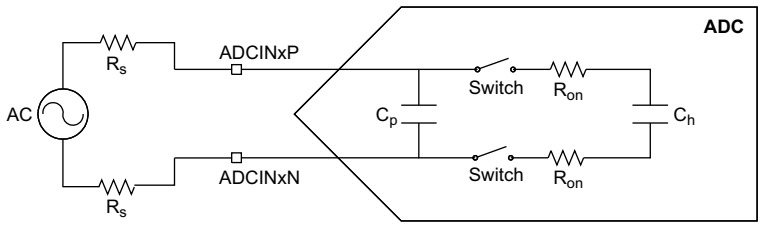

Figure 6-12. Differential Input Model

Table 6-22 shows the parasitic capacitance on each channel. Also note that enabling a comparator will add approximately 1.4 pF of capacitance on positive comparator inputs and 2.5 pF of capacitance on negative comparator inputs.

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Table 6-22. Per-Channel Parasitic Capacitance

ADC CHANNEL	C_p (pF)	
	COMPARATOR DISABLED	COMPARATOR ENABLED
ADCINA0	12.9	N/A
ADCINA1	10.3	N/A
ADCINA2	5.9	7.3
ADCINA3	6.3	8.8
ADCINA4	5.9	7.3
ADCINA5	6.3	8.8
ADCINB0	117.0	N/A
ADCINB1	10.6	N/A
ADCINB2	5.9	7.3
ADCINB3	6.2	8.7
ADCINB4	5.2	N/A
ADCINB5	5.1	N/A
ADCINC2	5.5	6.9
ADCINC3	5.8	8.3
ADCINC4	5.0	6.4
ADCINC5	5.3	7.8
ADCIND0	5.3	6.7
ADCIND1	5.7	8.2
ADCIND2	5.3	6.7
ADCIND3	5.6	8.1
ADCIND4	4.3	N/A
ADCIND5	4.3	N/A
ADCIN14	8.6	10.0
ADCIN15	9.0	11.5

These input models should be used along with actual signal source impedance to determine the acquisition window duration. See the "Choosing an Acquisition Window Duration" section of the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual* (SPRUHM8) for more information.

The user should analyze the ADC input setting assuming worst-case initial conditions on C_h. This will require assuming that C_h could start the S+H window completely charged to V_{REFHI} or completely discharged to V_{REFLO}. When the ADC transitions from an odd-numbered channel to an even-numbered channel, or vice-versa, the actual initial voltage on C_h will be close to being completely discharged to V_{REFLO}. For other transitions, the actually initial voltage on C_h will be close to the voltage of the previously converted channel.

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6.8.1.1.2 ADC Timing Diagrams

Figure 6-13 through Figure 6-16 show the ADC conversion timings for two SOCs given the following assumptions:

- SOC0 and SOC1 are configured to use the same trigger.
- No other SOCs are converting or pending when the trigger occurs.
- The round robin pointer is in a state that causes SOC0 to convert first.
- ADCINTSEL is configured to set an ADCINT flag upon end of conversion for SOC0 (whether this flag propagates through to the CPU to cause an interrupt is determined by the configurations in the PIE module).

The following parameters are identified in the timing diagrams:

- The parameter t_{SH} is the duration of the S+H window. At the end of this window, the value on the S+H capacitor becomes the voltage to be converted into a digital value. The duration is given by (ACQPS + 1) SYSCLK cycles. ACQPS can be configured individually for each SOC, so t_{SH} will not necessarily be the same for different SOCs.
- The parameter t_{LAT} is the time from the end of the S+H window until the ADC conversion results latch in the ADCRESULTx register. If the ADCRESULTx register is read before this time, the previous conversion results will be returned.
- The parameter t_{EOC} is the time from the end of the S+H window until the next ADC conversion S+H window can begin. In 16-bit mode, this will coincide with the latching of the conversion results, while in 12-bit mode, the subsequent sample can start before the conversion results are latched.
- The parameter t_{INT} is the time from the end of the S+H window until an ADCINT flag is set (if configured). If the INTPULSEPOS bit in the ADCCTL1 register is set, this will coincide with the conversion results being latched into the result register. If the bit is cleared, this will coincide with the end of the S+H window.

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Table 6-23. ADC Timings in 12-bit Mode (SYSCLK Cycles)

ADCCTL2.PRESCALE	PRESCALE RATIO	t_{EOC}	t_{LAT}	t_{INT} (EARLY)	t_{INT} (LATE)	ADC CONVERSION CYCLES (ADCCLKs)
0	1	11	12	0	12	11.0
2	2	21	22	0	22	10.5
3	2.5	26	27	0	27	10.4
4	3	31	33	0	33	10.3
5	3.5	36	38	0	38	10.3
6	4	41	43	0	43	10.3
7	4.5	46	48	0	48	10.2
8	5	51	54	0	54	10.2
9	5.5	56	59	0	59	10.2
10	6	61	64	0	64	10.2
11	6.5	66	69	0	69	10.2
12	7	71	75	0	75	10.1
13	7.5	76	80	0	80	10.1
14	8	81	85	0	85	10.1
15	8.5	86	90	0	90	10.1

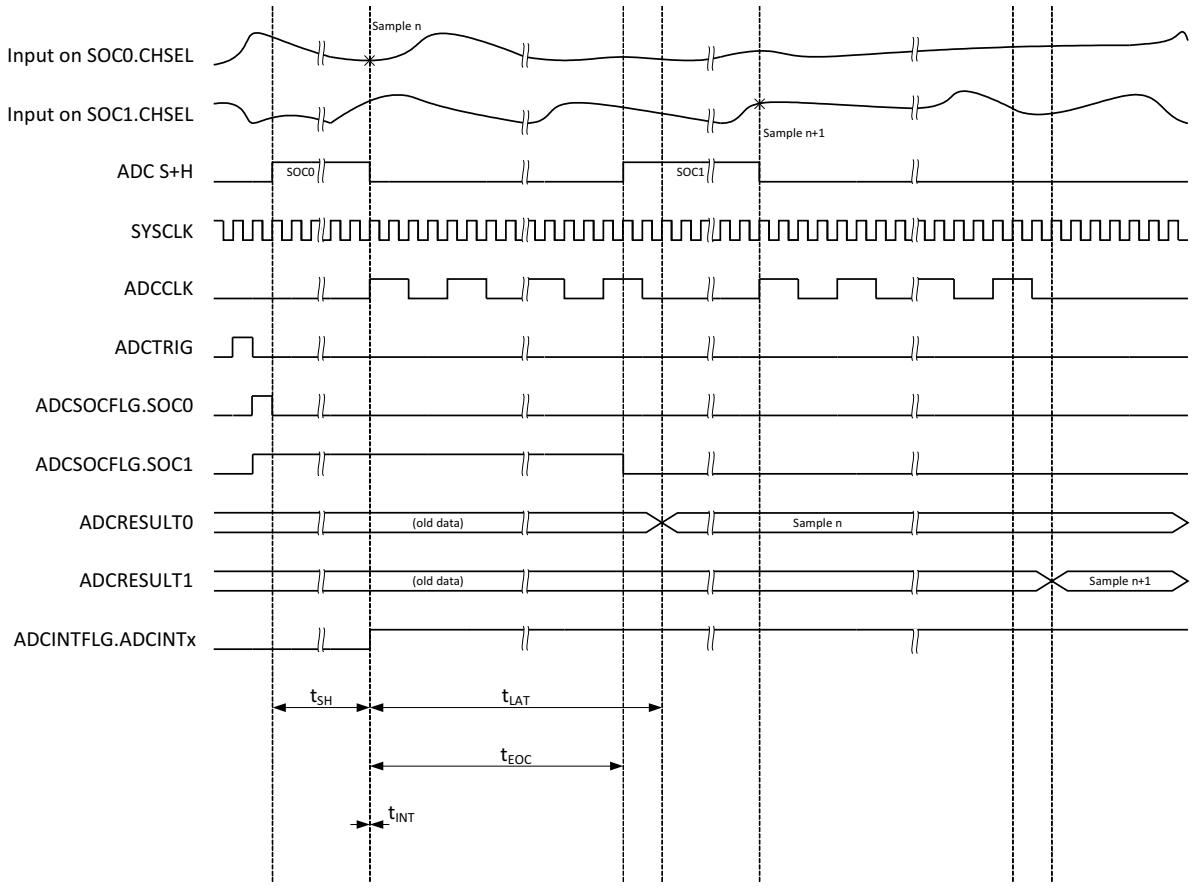

Figure 6-13. ADC Timings for 12-bit Mode in Early Interrupt Mode

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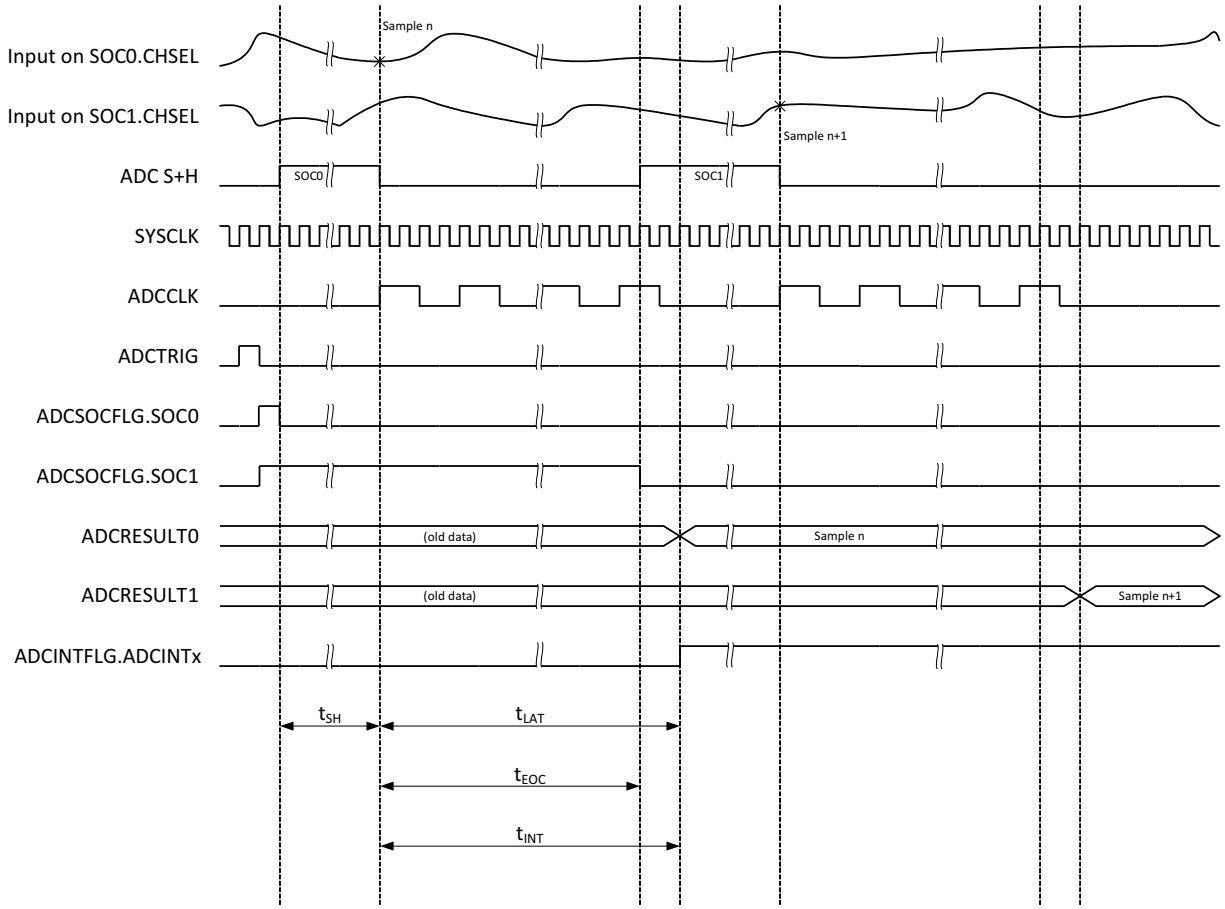

Figure 6-14. ADC Timings for 12-bit Mode in Late Interrupt Mode

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Table 6-24. ADC Timings in 16-bit Mode

ADCCTL2.PRESCALE	PRESCALE RATIO	t_{EOC}	t_{LAT}	t_{INT} (EARLY)	t_{INT} (LATE)	ADC CONVERSION CYCLES (ADCCLKs)
0	1	31	31	0	31	31.0
2	2	60	60	0	60	30.0
3	2.5	75	75	0	75	30.0
4	3	90	90	0	90	30.0
5	3.5	104	104	0	104	29.7
6	4	119	119	0	119	29.8
7	4.5	134	134	0	134	29.8
8	5	149	149	0	149	29.8
9	5.5	163	163	0	163	29.6
10	6	178	178	0	178	29.7
11	6.5	193	193	0	193	29.7
12	7	208	208	0	208	29.7
13	7.5	222	222	0	222	29.6
14	8	237	237	0	237	29.6
15	8.5	252	252	0	252	29.6

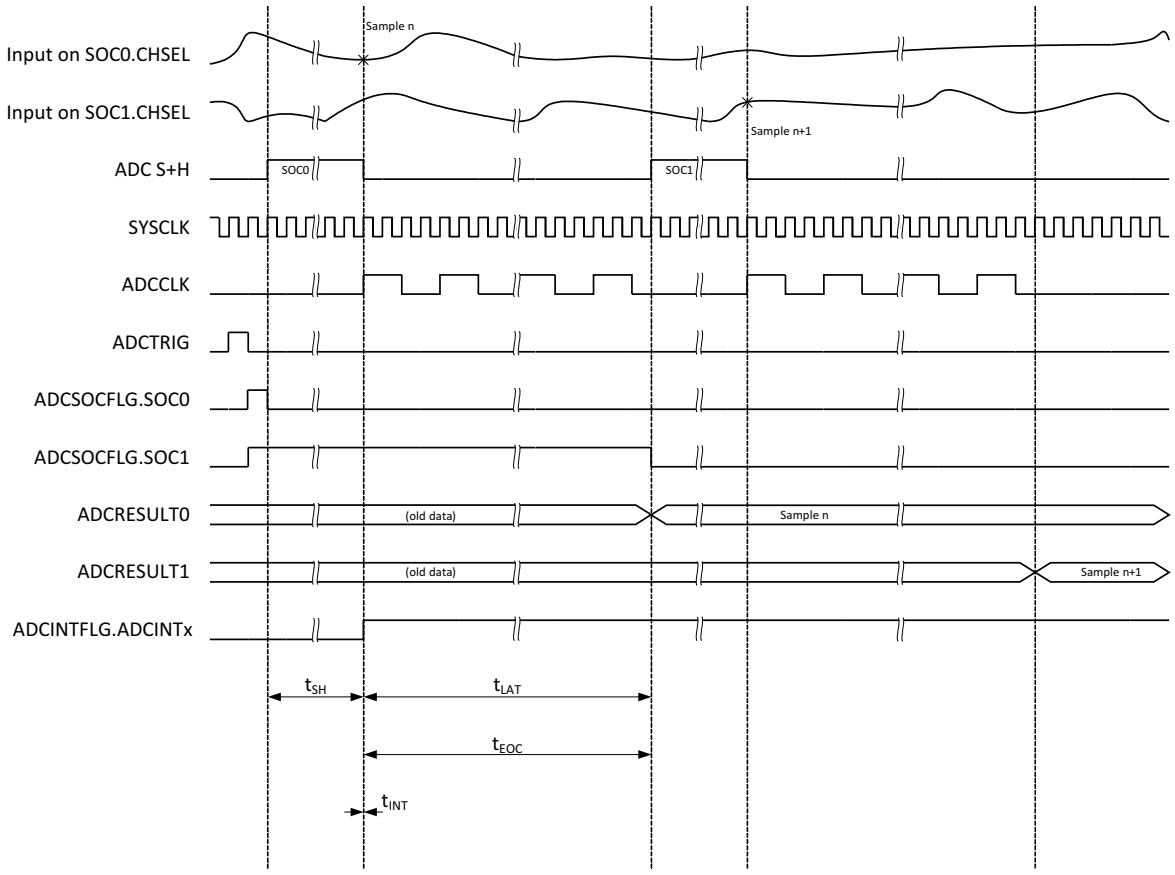

Figure 6-15. ADC Timings for 16-bit Mode in Early Interrupt Mode

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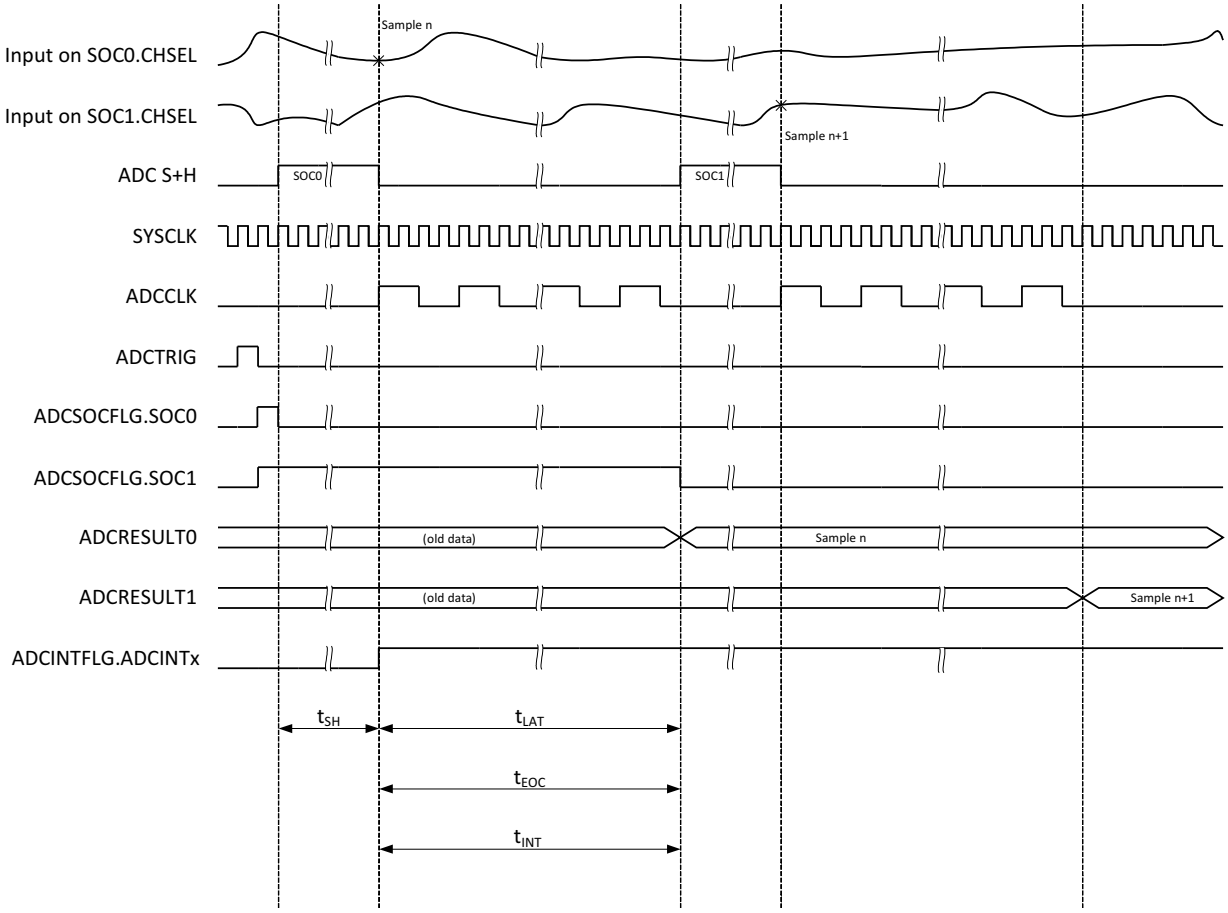

Figure 6-16. ADC Timings for 16-bit Mode in Late Interrupt Mode (SYSCLK Cycles)

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6.8.1.2 Temperature Sensor Electrical Data and Timing

Table 6-25. Temperature Sensor Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Temperature accuracy			±15		°C
Startup time			500		µs
ADC acquisition time		700			ns

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6.8.2 Buffered Digital-to-Analog Converter

The buffered DAC module consists of an internal reference DAC and an analog output buffer that is capable of driving an external load. An integrated pulldown resistor on the DAC output helps to provide a known pin voltage when the output buffer is disabled. This pulldown resistor cannot be disabled and remains as a passive component on the pin, even for other shared pin mux functions. Software writes to the DAC value register can take effect immediately or can be synchronized with PWMSYNC events.

Each Buffered DAC has the following features:

- 12-bit programmable internal DAC
- Selectable reference voltage
- Pulldown resistor on output
- Ability to synchronize with PWMSYNC

The block diagram for the buffered DAC is shown in Figure 6-17.

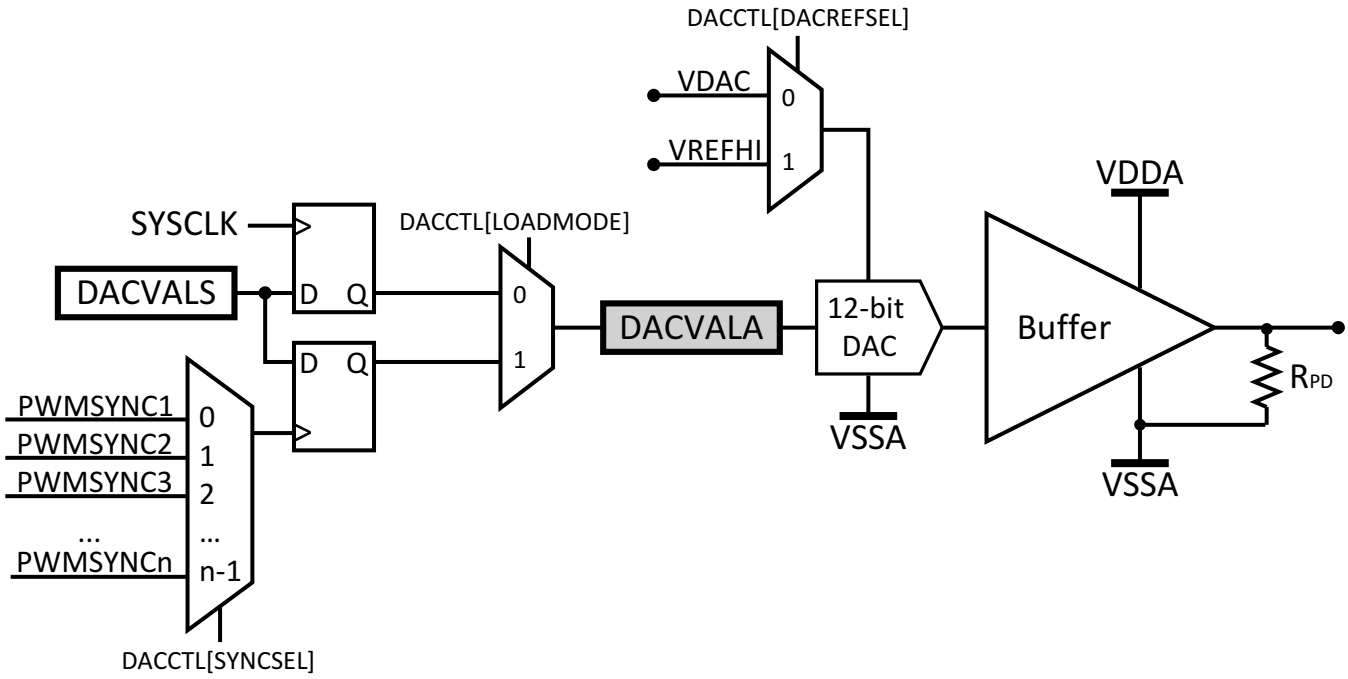

Figure 6-17. DAC Module Block Diagram

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6.8.2.1 Buffered DAC Electrical Data and Timing

Table 6-26. Reference DAC Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Trimmed offset error	Midpoint	–40		40	mV
Gain error		–2.5		2.5	% of FSR
DNL(1)	Endpoint corrected	> –1		1	LSB
INL	Endpoint corrected	–5		5	LSB
Voltage output settling time	Settling to 1 LSB after full-scale output change		2		µs
Resolution			12		Bits
Voltage output range(2)		0.6		V_{DDA} – 0.6	V
Capacitive load	Output drive capability			100	pF
Resistive load	Output drive capability	5			kΩ
RPD			50		kΩ
Reference voltage	VDAC or V_{REFHI}	2.4		V_{DDA}	V
Reference load	VDAC or V_{REFHI}		213		kΩ
Noise			1		mV
Glitch energy			1		V-ns
PSR	1 kHz		70		dB
	100 kHz		30		

(1) The DAC output is monotonic.
(2) The DAC can generate voltages outside of this range, but the output voltage will not be linear.

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6.8.3 Comparator Subsystem

Each CMPSS module includes two comparators, two internal voltage reference DACs, two digital glitch filters, and one ramp generator. There are two inputs, CMPINxP and CMPINxN. Each of these will be internally connected to an ADCIN pin. The CMPINxP pin is always connected to the positive input of the CMPSS comparators. CMPINxN can be used instead of the DAC output to drive the negative comparator inputs. There are two comparators, and therefore two outputs from the CMPSS module, which are connected to the input of a digital filter module before being passed on to the Comparator TRIP crossbar and either PWM modules or directly to a GPIO pin. Figure 6-18 shows the CMPSS connectivity on the 337-ball ZWT and 176-pin PTP packages.

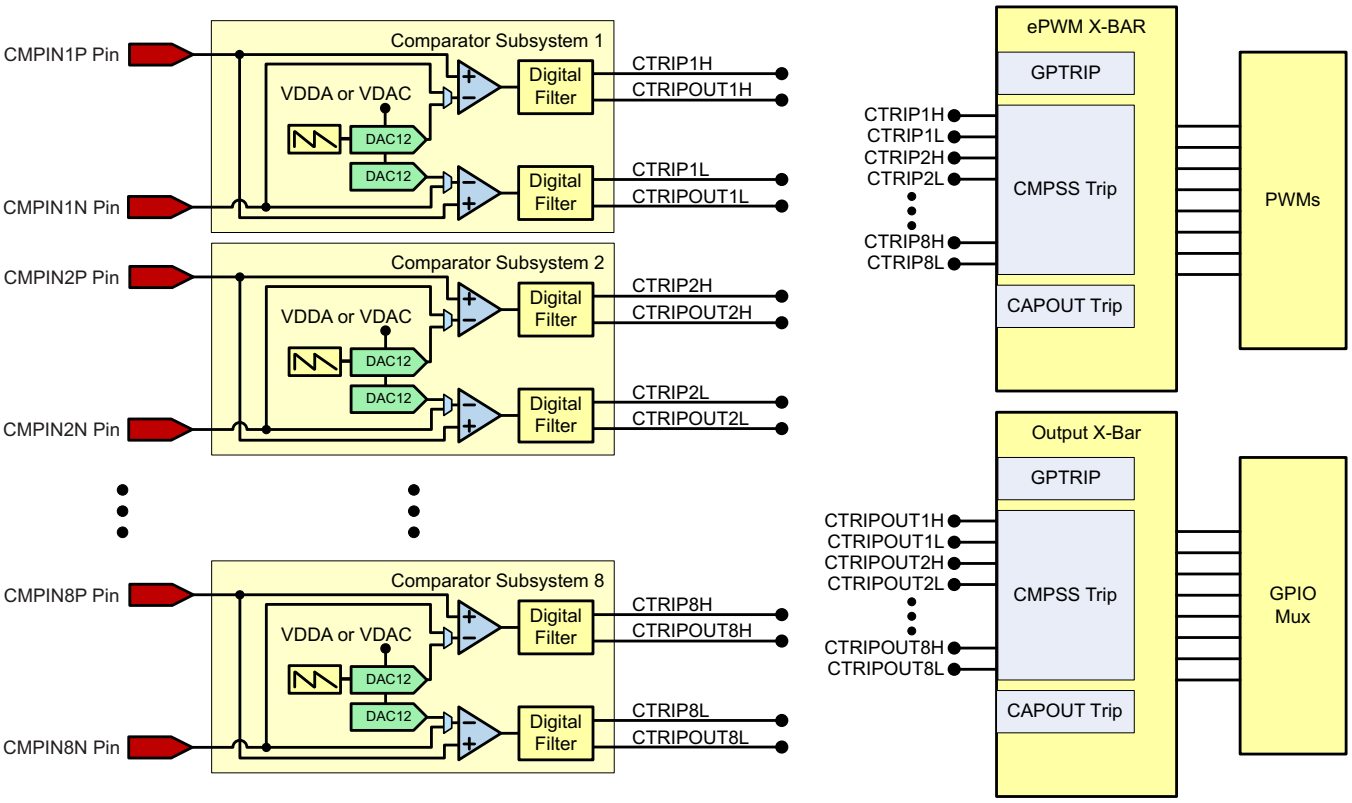

Figure 6-18. CMPSS Connectivity (337-Ball ZWT and 176-Pin PTP)

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6.8.3.1 CMPSS Electrical Data and Timing

Table 6-27. Comparator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Offset error	Input referred	–20		20	mV
Hysteresis(1)	1x	TBD	8		LSB
	2x	TBD	22		
	3x	TBD	33		
	4x	TBD	44		
Response time	Input step response to ePWM or GPIO X-BAR (asynchronous)		50		ns

(1) Hysteresis will scale with the CMPSS reference voltage.

Table 6-28. Reference DAC Static Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static offset error(1)		–25		25	mV
Static gain error(1)		–2		2	% of FSR
Static DNL	Endpoint corrected	–0.99		4	LSB
Static INL	Endpoint corrected	–16		16	LSB
Settling time	Settling to 1 LSB after full-scale output change			1000	ns
Resolution			12		Bits
DACH disturbance error(2)	Induced by COMPH or COMPL trip	–512		512	LSB
DACL disturbance error(2)	Induced by COMPH or COMPL trip	–512		512	LSB
DAC disturbance time(2)	Induced by COMP trip		200		ns
VDAC reference voltage	When VDAC is reference	2.4		V_{DDA}	V
VDAC load	When VDAC is reference		8		kΩ

(1) Includes comparator input referred offset.
(2) Disturbance error may be present on the reference DAC output for a certain amount of time after a comparator trip.

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6.9 Control Peripherals

NOTE

For the actual number of each peripheral on a specific device, see Table 3-1.

6.9.1 Sigma-Delta Filter Module

The SDFM is a four-channel digital filter designed specifically for current measurement and resolver position decoding in motor control applications. Each channel can receive an independent sigma-delta (ΣΔ) modulated bit stream. The bit streams are processed by four individually programmable digital decimation filters. The filter set includes a fast comparator for immediate digital threshold comparisons for over-current and under-current monitoring. The flexible SDFM also offers a filter-bypass mode to enable data logging, analysis, and customized filtering. Figure 6-19 shows a block diagram of the SDFMs.

SDFM features include:

- Four external pins per SDFM module:
  - Four sigma-delta data input pins per SDFM module (SDx_Dy, where x = 1 to 2 and y = 1 to 4)
  - Four sigma-delta clock input pins per SDFM module (SDx_Cy, where x = 1 to 2 and y = 1 to 4)
- Four different configurable modulator clock modes:
  - Modulator clock rate equals modulator data rate
  - Modulator clock rate running at half the modulator data rate
  - Modulator data is Manchester encoded. Modulator clock not required.
  - Modulator clock rate is double that of modulator data rate
- Four independent configurable comparator units:
  - Four different filter type selection (Sinc1/Sinc2/Sincfast/Sinc3) options available
  - Ability to detect over-value and under-value conditions
  - OSR value for comparator programmable from 1 to 32
- Four independent configurable sinc filter units:
  - Four different filter type selection (Sinc1/Sinc2/Sincfast/Sinc3) options available
  - Ability to bypass filter module
  - OSR value for filter unit programmable from 1 to 256
  - Ability to enable or disable individual filter module
  - Ability to synchronize all four independent filters of a SDFM module using the Master Filter Enable (MFE) bit or the PWM signals.
- Filter data can be 16-bit or 32-bit representation
- PWMs can be used to generate modulator clock for sigma-delta modulators

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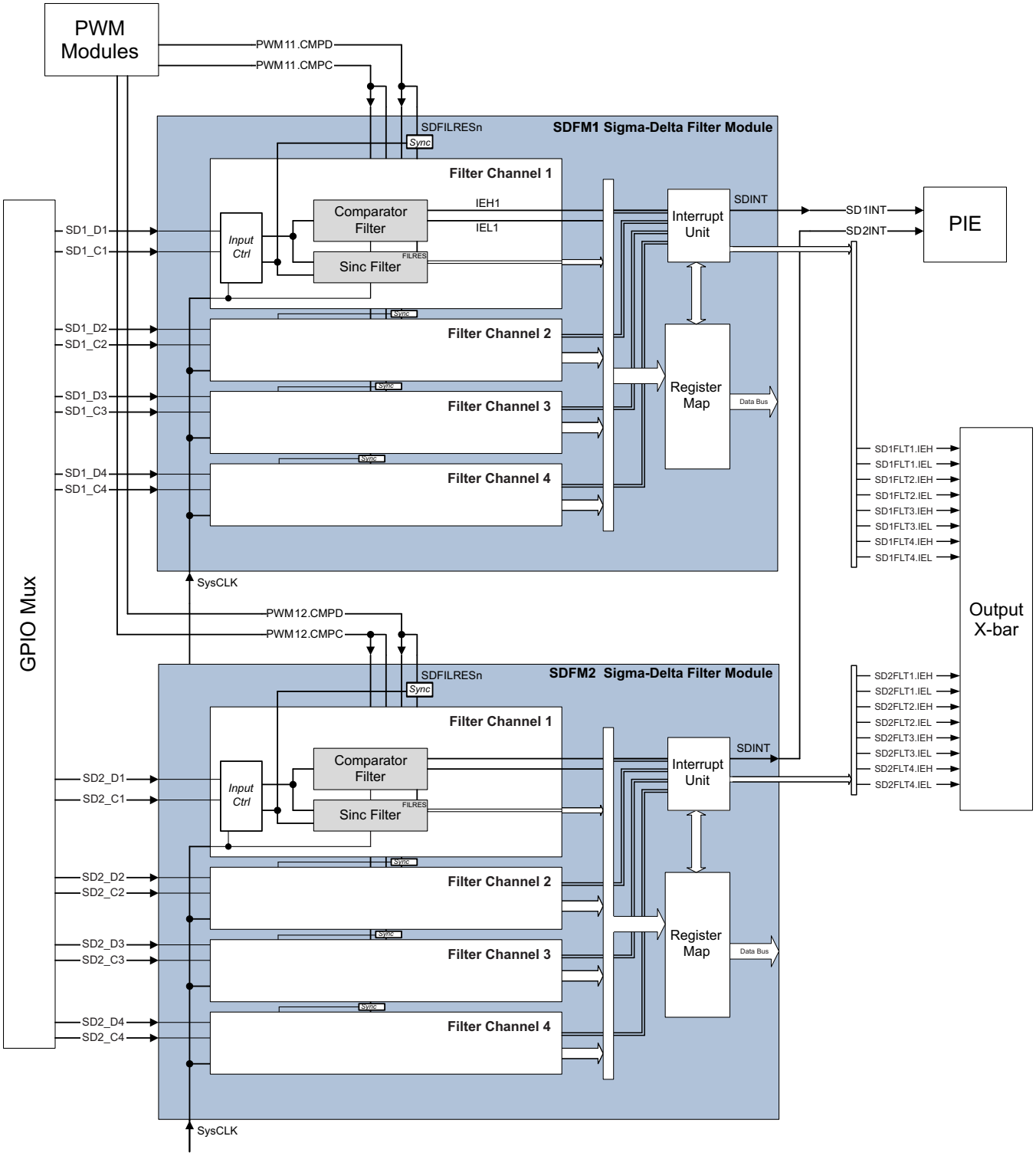

Figure 6-19. SDFM

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6.9.1.1 SDFM Electrical Data and Timing

Table 6-29. SDFM Timing Requirements

		MIN	MAX	UNIT
Mode 0				
$t_{c(SDC)M0}$	Cycle time, SDx_Cy	45	256 * SYSCLK period	ns
$t_{w(SDCH)M0}$	Pulse duration, SDx_Cy high	10	$t_{c(SDC)M0}$ – 10	ns
$t_{su(SDDV-SDCH)M0}$	Setup time, SDx_Dy valid before SDx_Cy goes high	5		ns
$t_{h(SDCH-SDD)M0}$	Hold time, SDx_Dy wait after SDx_Cy goes high	5		ns
Mode 1				
$t_{c(SDC)M1}$	Cycle time, SDx_Cy	90	256 * SYSCLK period	ns
$t_{w(SDCH)M1}$	Pulse duration, SDx_Cy high	20	$t_{c(SDC)M1}$ – 10	ns
$t_{su(SDDV-SDCL)M1}$	Setup time, SDx_Dy valid before SDx_Cy goes low	5		ns
$t_{su(SDDV-SDCH)M1}$	Setup time, SDx_Dy valid before SDx_Cy goes high	5		ns
$t_{h(SDCL-SDD)M1}$	Hold time, SDx_Dy wait after SDx_Cy goes low	5		ns
$t_{h(SDCH-SDD)M1}$	Hold time, SDx_Dy wait after SDx_Cy goes high	5		ns
Mode 2				
$t_{c(SDD)M2}$	Cycle time, SDx_Dy	90	256 * SYSCLK period	ns
$t_{w(SDDH)M2}$	Pulse duration, SDx_Dy high	20		ns
Mode 3				
$t_{c(SDC)M3}$	Cycle time, SDx_Cy	25	256 * SYSCLK period	ns
$t_{w(SDCH)M3}$	Pulse duration, SDx_Cy high	10	$t_{c(SDC)M3}$ – 5	ns
$t_{su(SDDV-SDCH)M3}$	Setup time, SDx_Dy valid before SDx_Cy goes high	5		ns
$t_{h(SDCH-SDD)M3}$	Hold time, SDx_Dy wait after SDx_Cy goes high	5		ns

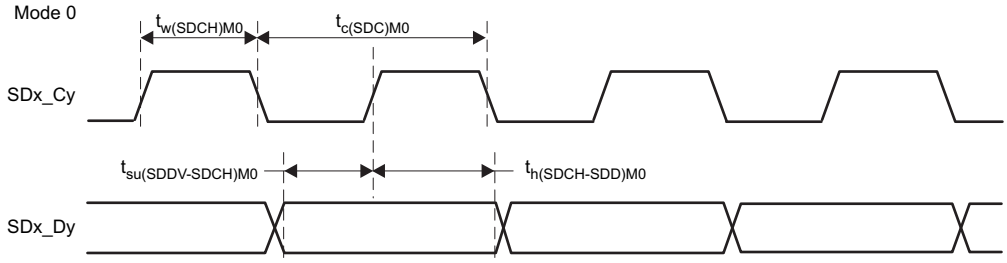

Figure 6-20. SDFM Timing Diagram – Mode 0

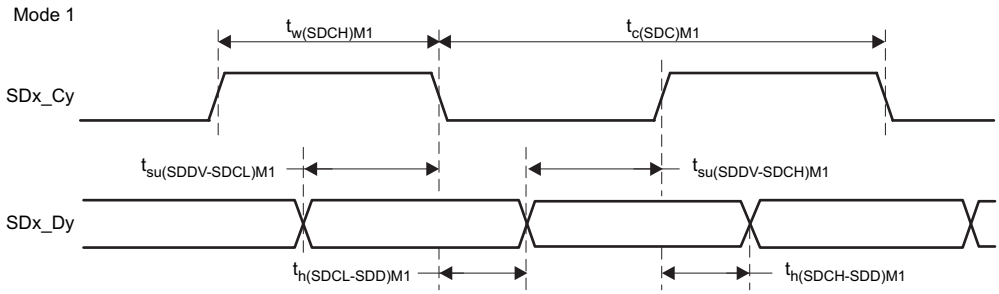

Figure 6-21. SDFM Timing Diagram – Mode 1

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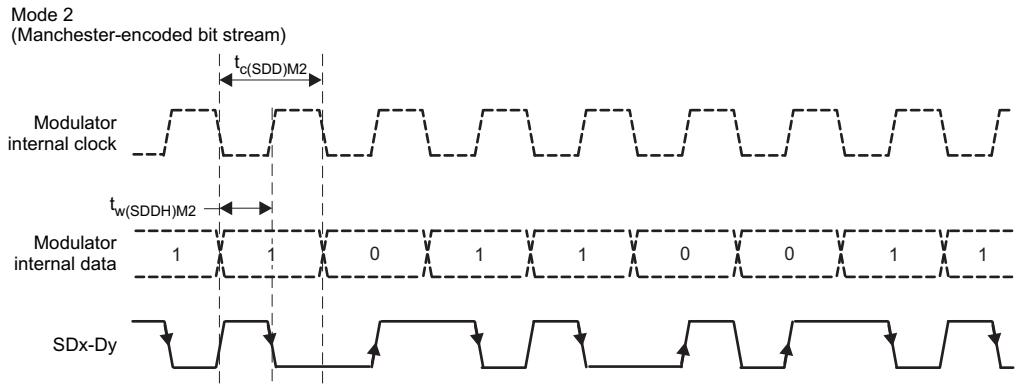

Figure 6-22. SDFM Timing Diagram – Mode 2

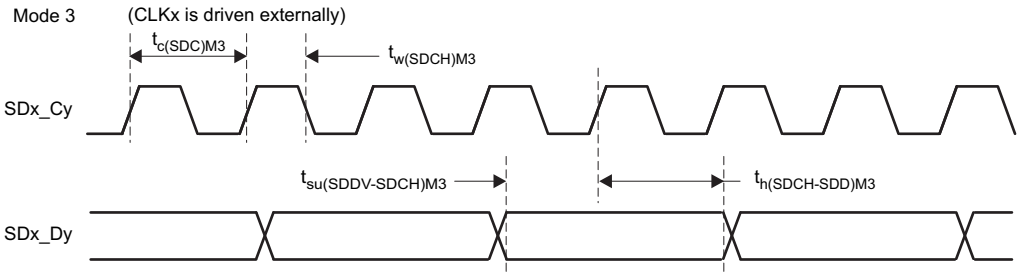

Figure 6-23. SDFM Timing Diagram – Mode 3

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6.9.2 Enhanced Pulse Width Modulator

The ePWM peripheral is a key element in controlling many of the power electronic systems found in both commercial and industrial equipment. The ePWM type-4 module is able to generate complex pulse width waveforms with minimal CPU overhead by building the peripheral up from smaller modules with separate resources that can operate together to form a system. Some of the highlights of the ePWM type-4 module include complex waveform generation, dead-band generation, a flexible synchronization scheme, advanced trip-zone functionality, and global register reload capabilities.

Figure 6-24 shows the signal interconnections with the ePWM.

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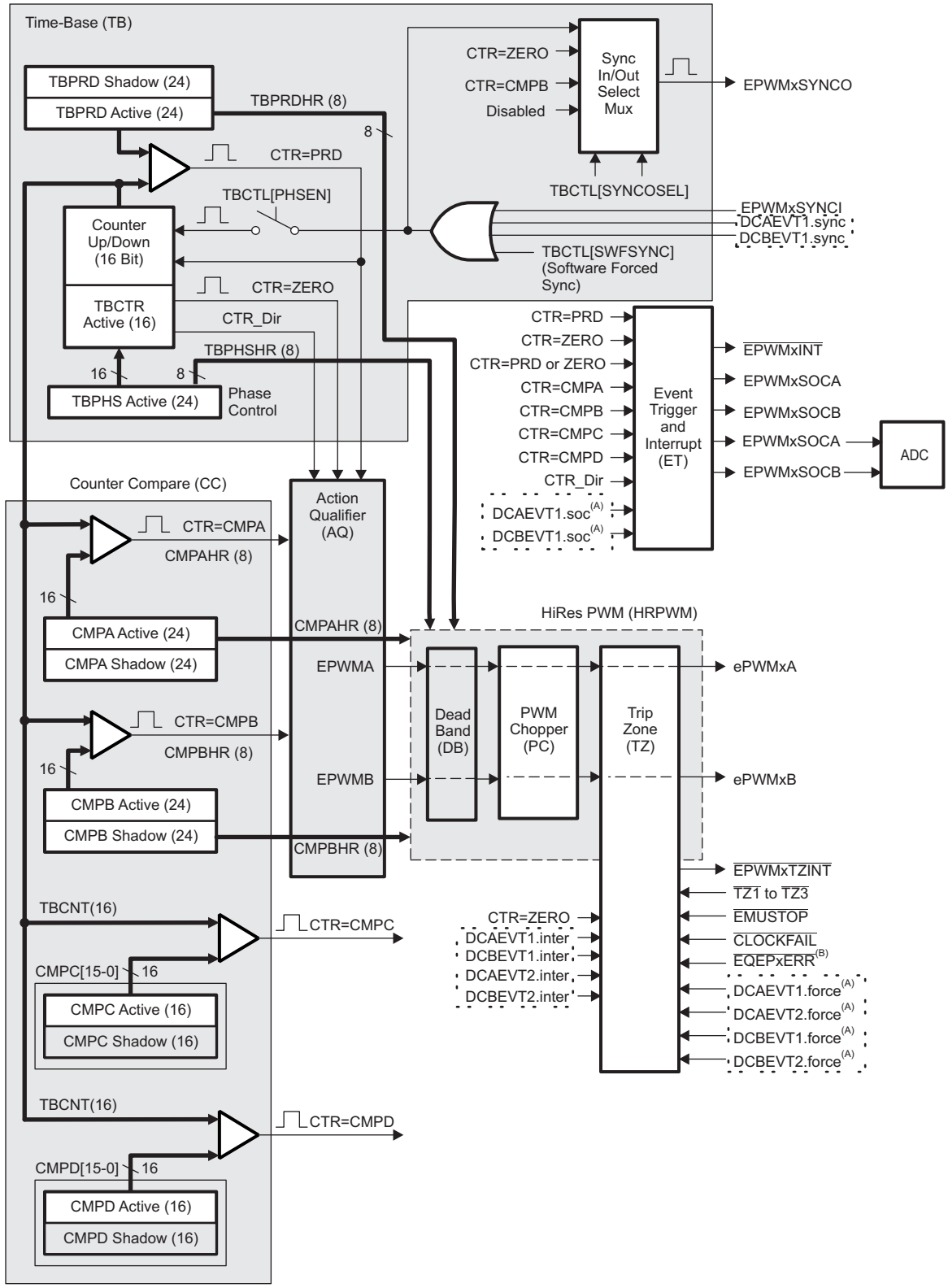

A. These events are generated by the type-4 ePWM digital compare (DC) submodule.

Figure 6-24. ePWM Sub-Modules Showing Critical Internal Signal Interconnections

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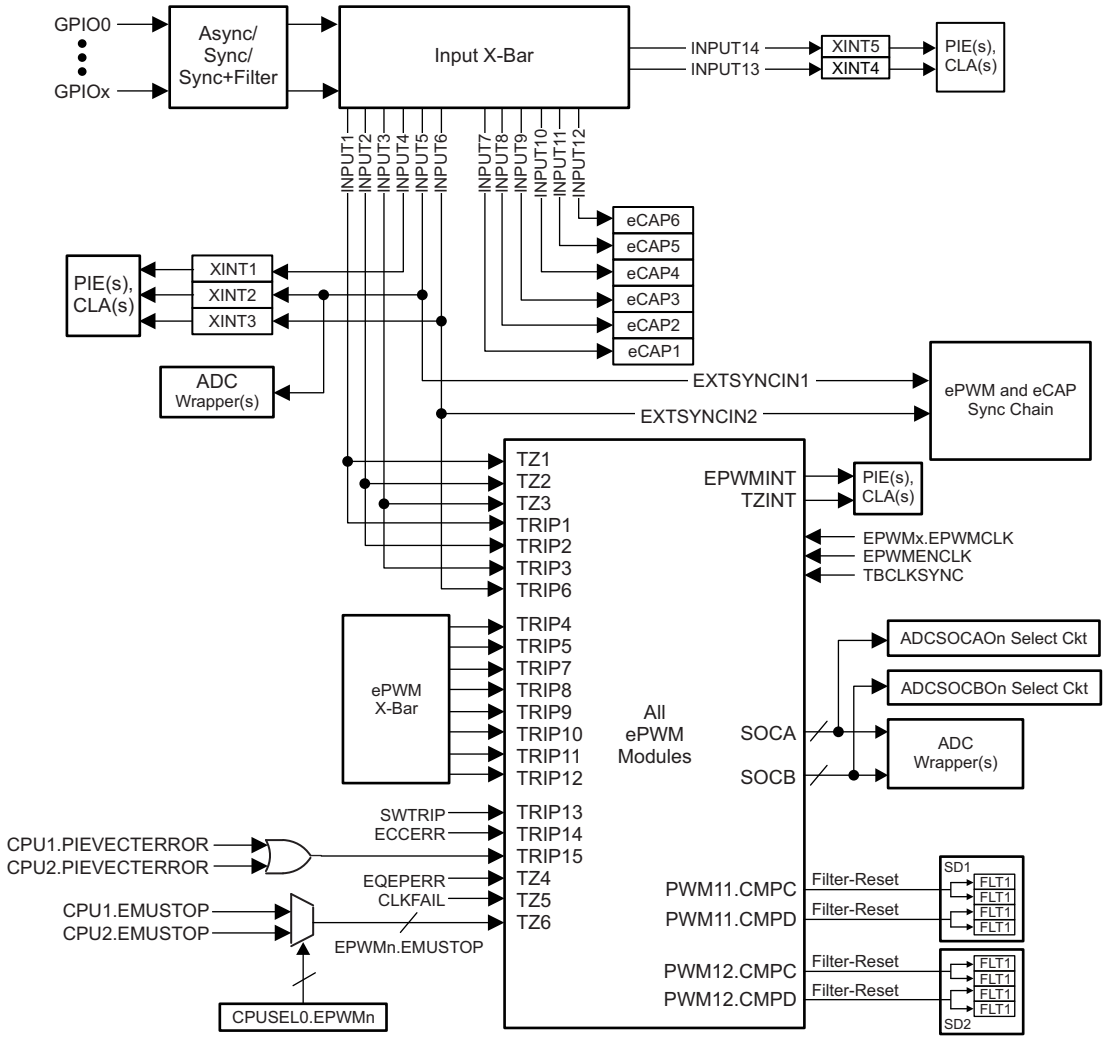

Figure 6-25. ePWM

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6.9.2.1 Control Peripherals Synchronization

The ePWM and eCAP Synchronization Chain on the device provides flexibility in partitioning the ePWM and eCAP modules between CPU1 and CPU2 and allows localized synchronization within the modules belonging to the same CPU. Like the other peripherals, the partitioning of the ePWM and eCAP modules needs to be done using the CPUSELx registers. Figure 6-26 shows the Synchronization Chain Architecture.

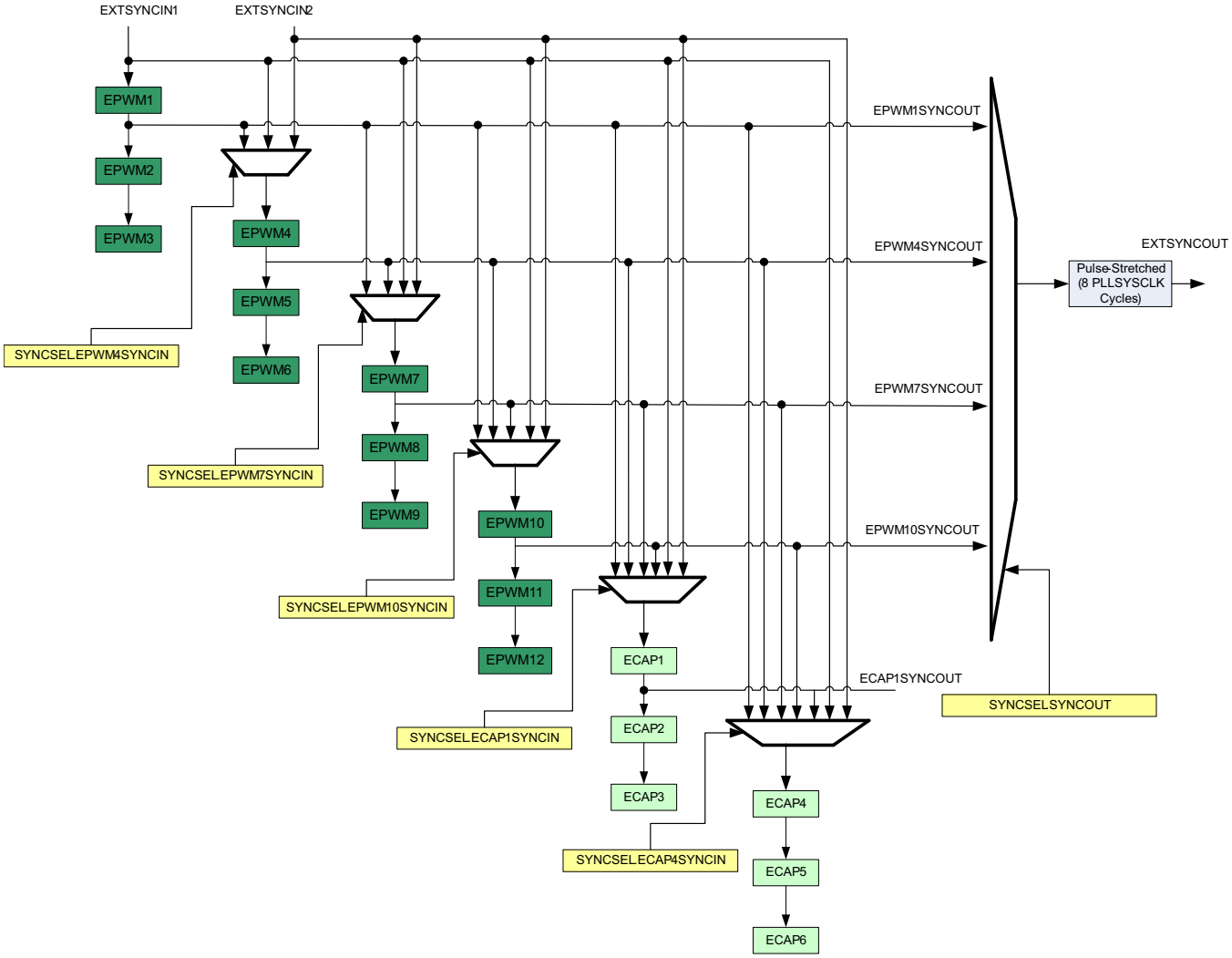

Figure 6-26. Synchronization Chain Architecture

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6.9.2.2 ePWM Electrical Data and Timing

Table 6-30 shows the PWM timing requirements and Table 6-31 shows the PWM switching characteristics.

Table 6-30. ePWM Timing Requirements(1)

			MIN	MAX	UNIT
$t_{w(SYNCIN)}$	Sync input pulse width	Asynchronous	$2t_{c(EPWMCLK)}$		cycles
		Synchronous	$2t_{c(EPWMCLK)}$		cycles
		With input qualifier	$1t_{c(EPWMCLK)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 5-20.

Table 6-31. ePWM Switching Characteristics

over recommended operating conditions (unless otherwise noted)

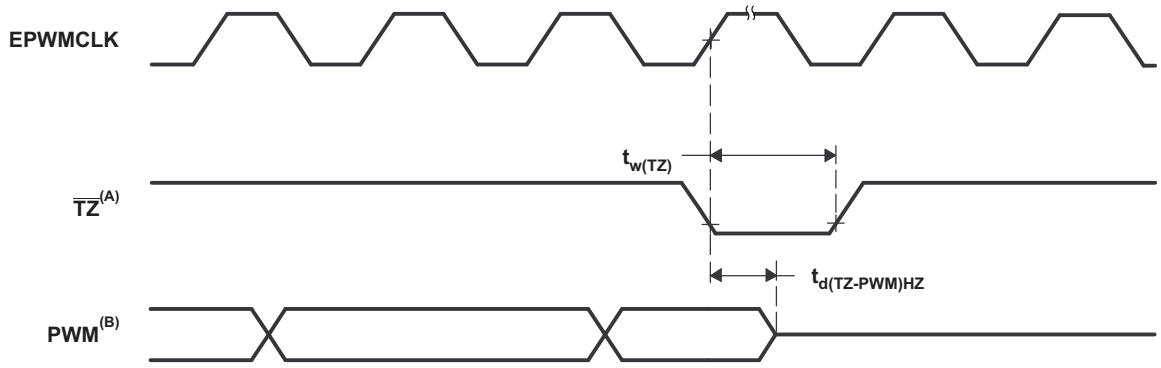
PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(PWM)}$	Pulse duration, PWMx output high/low		20		ns
$t_{w(SYNCOUT)}$	Sync output pulse width		$8t_{c(SYSCLK)}$		cycles
$t_{d(PWM)tza}$	Delay time, trip input active to PWM forced high Delay time, trip input active to PWM forced low Delay time, trip input active to PWM Hi-Z			25	ns

6.9.2.2.1 Trip-Zone Input Timing

Table 6-32. Trip-Zone Input Timing Requirements(1)

			MIN	MAX	UNIT
$t_{w(TZ)}$	Pulse duration, $\overline{TZ}x$ input low	Asynchronous	$1t_{c(EPWMCLK)}$		cycles
		Synchronous	$2t_{c(EPWMCLK)}$		cycles
		With input qualifier	$1t_{c(EPWMCLK)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 5-20.



A. $\overline{TZ}$: $\overline{TZ1}$, $\overline{TZ2}$, $\overline{TZ3}$, TRIP1–TRIP12

B. PWM refers to all the PWM pins in the device. The state of the PWM pins after $\overline{TZ}$ is taken high depends on the PWM recovery software.

Figure 6-27. PWM Hi-Z Characteristics

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6.9.3 High-Resolution Pulse Width Modulator

The HRPWM combines multiple delay lines in a single module and a simplified calibration system by using a dedicated calibration delay line. For each ePWM module there is one HR delay line.

The HRPWM module offers PWM resolution (time granularity) that is significantly better than what can be achieved using conventionally derived digital PWM methods. The key points for the HRPWM module are:

- Significantly extends the time resolution capabilities of conventionally derived digital PWM
- This capability can be utilized in both single edge (duty cycle and phase-shift control) as well as dual edge control for frequency/period modulation.
- Finer time granularity control or edge positioning is controlled via extensions to the Compare A, phase, and period registers of the ePWM module.

NOTE

The minimum HRPWMCLK frequency allowed for HRPWM is 60 MHz.

NOTE

When dual-edge high-resolution is enabled (high-resolution period mode), the PWMxB output is not available for use.

6.9.3.1 HRPWM Electrical Data and Timing

Table 6-33 shows the high-resolution PWM switching characteristics.

Table 6-33. High-Resolution PWM Characteristics at SYSCLK = (60–150 MHz)

PARAMETER	MIN	TYP	MAX	UNIT
Micro Edge Positioning (MEP) step size(1)		150	310	ps

(1) Maximum MEP step size is based on worst-case process, maximum temperature and minimum voltage. MEP step size will increase with low voltage and high temperature and decrease with voltage and cold temperature.
Applications that use the HRPWM feature should use MEP Scale Factor Optimizer (SFO) estimation software functions. See the TI software libraries for details of using SFO function in end applications. SFO functions help to estimate the number of MEP steps per SYSCLK period dynamically while the HRPWM is in operation.

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6.9.4 Enhanced Capture

Figure 6-28 shows the block diagram of an eCAP module.

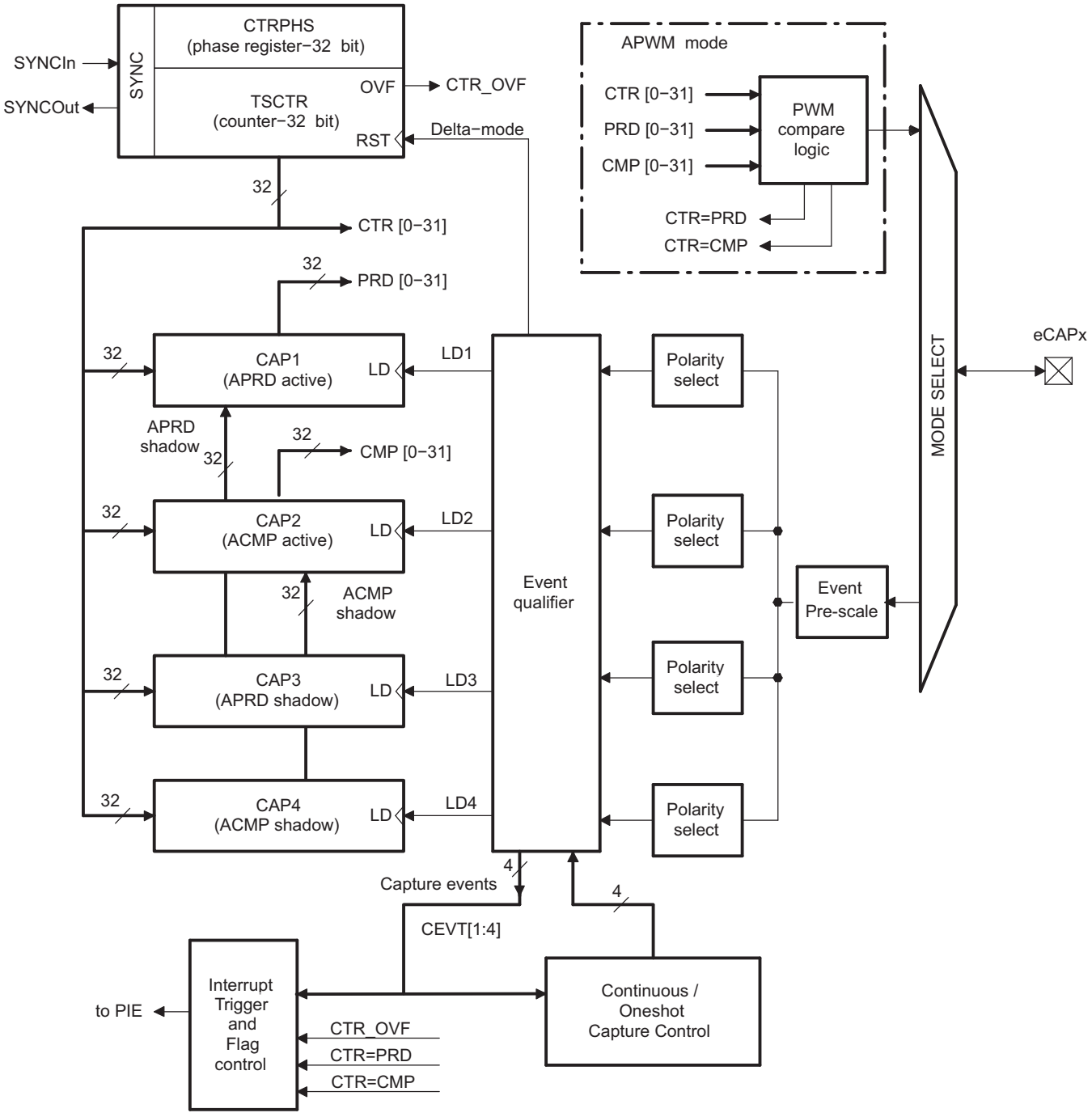

Figure 6-28. eCAP Block Diagram

The eCAP module is clocked at the SYSCLK rate.

The clock enable bits (ECAP1–ECAP6) in the PCLKCR3 register turn off the eCAP module individually (for low-power operation). Upon reset, ECAP1ENCLK is set to low, indicating that the peripheral clock is off.

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6.9.4.1 eCAP Electrical Data and Timing

Table 6-34 shows the eCAP timing requirement and Table 6-35 shows the eCAP switching characteristics.

Table 6-34. eCAP Timing Requirement(1)

		MIN	MAX	UNIT
$t_{w(CAP)}$ Capture input pulse width	Asynchronous	$2t_{c(SYSCLK)}$		cycles
	Synchronous	$2t_{c(SYSCLK)}$		cycles
	With input qualifier	$1t_{c(SYSCLK)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 5-20.

Table 6-35. eCAP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(APWM)}$	Pulse duration, APWMx output high/low		20		ns

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6.9.5 Enhanced Quadrature Encoder Pulse

Figure 6-29 shows the eQEP block diagram.

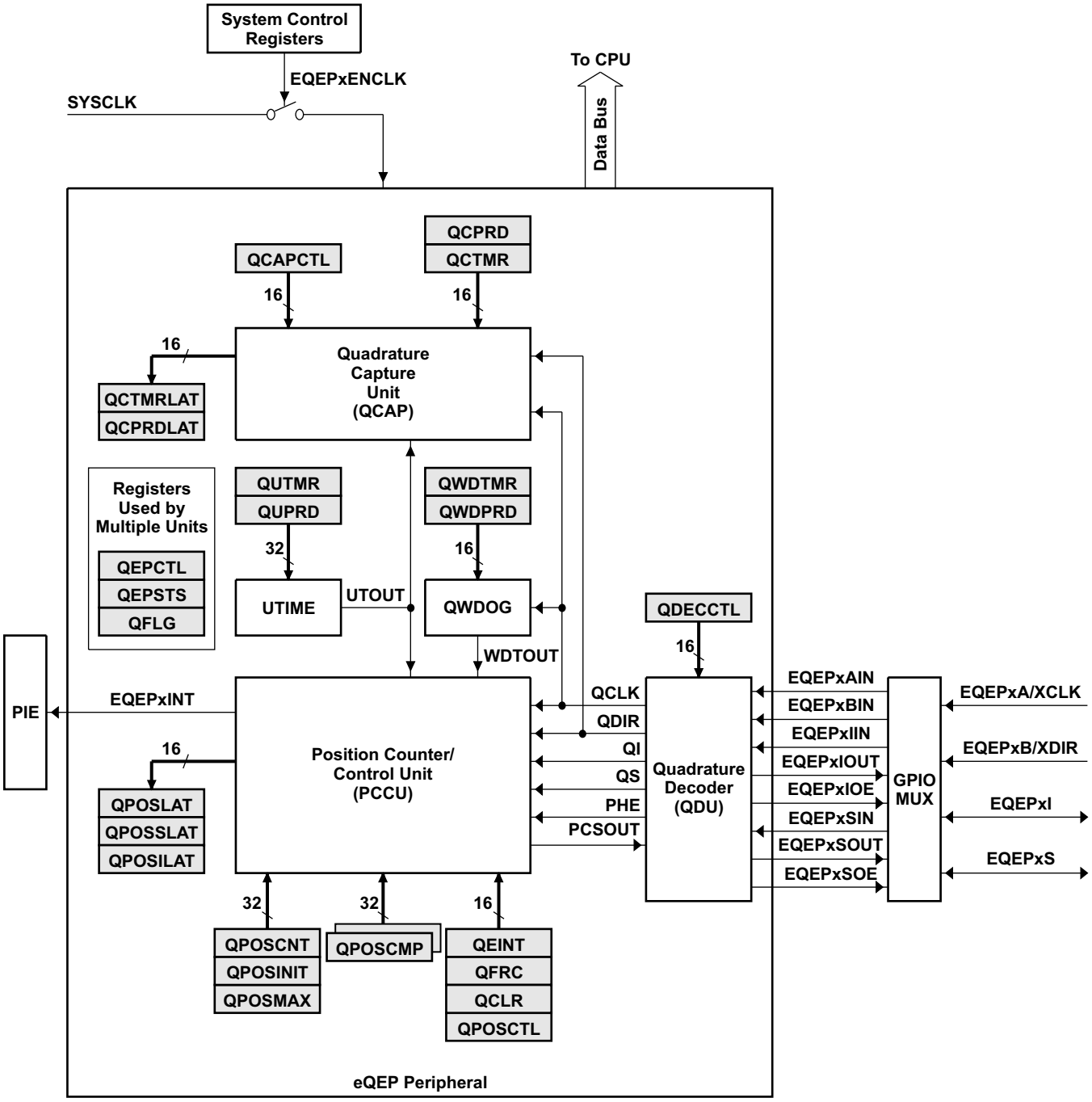

Figure 6-29. eQEP Block Diagram

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6.9.5.1 eQEP Electrical Data and Timing

Table 6-36 shows the eQEP timing requirement and Table 6-37 shows the eQEP switching characteristics.

Table 6-36. eQEP Timing Requirements(1)

			MIN	MAX	UNIT
$t_{w(QEPP)}$	QEP input period	Synchronous	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$2[1t_{c(SYSCLK)} + t_{w(IQSW)}]$		cycles
$t_{w(INDEXH)}$	QEP Index Input High time	Synchronous	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		cycles
$t_{w(INDEXL)}$	QEP Index Input Low time	Synchronous	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		cycles
$t_{w(STROBH)}$	QEP Strobe High time	Synchronous	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		cycles
$t_{w(STROBL)}$	QEP Strobe Input Low time	Synchronous	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 5-20.

Table 6-37. eQEP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(CNTR)xin}$	Delay time, external clock to counter increment			$4t_{c(SYSCLK)}$	cycles
$t_{d(PCS-OUT)QEP}$	Delay time, QEP input edge to position compare sync output			$6t_{c(SYSCLK)}$	cycles

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6.10 Communications Peripherals

NOTE

For the actual number of each peripheral on a specific device, see Table 3-1.

6.10.1 Serial Peripheral Interface

The SPI is a high-speed synchronous serial input/output (I/O) port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communications between the microcontroller and external peripherals or another controller. Typical applications include external I/O or peripheral expansion via devices such as shift registers, display drivers, and ADCs. Multi-device communications are supported by the master/slave operation of the SPI. The port supports 16-level receive and transmit FIFOs for reducing CPU servicing overhead.

The SPI module features include:

- SPISOMI: SPI slave-output/master-input pin
- SPISIMO: SPI slave-input/master-output pin
- $\overline{\text{SPISTE}}$: SPI slave transmit-enable pin
- SPICLK: SPI serial-clock pin
- Two operational modes: master and slave
- Baud rate: 125 different programmable rates
- Data word length: 1 to 16 data bits
- Four clocking schemes (controlled by clock polarity and clock phase bits) include:
  - Falling edge without phase delay: SPICLK active-high. SPI transmits data on the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
  - Falling edge with phase delay: SPICLK active-high. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge without phase delay: SPICLK inactive-low. SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge with phase delay: SPICLK inactive-low. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
- Simultaneous receive-and-transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithms.
- 16-level transmit and receive FIFO
- Delayed transmit control
- 3-wire SPI mode
- $\overline{\text{SPISTE}}$ inversion for digital audio interface receive mode on devices with two SPI modules
- DMA support
- High-speed mode for up to 40-MHz full-duplex communication

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The SPI operates in master or slave mode. The master initiates data transfer by sending the SPICLK signal. For both the slave and the master, data is shifted out of the shift registers on one edge of the SPICLK and latched into the shift register on the opposite SPICLK clock edge. If the CLOCK PHASE bit (SPICTL.3) is high, data is transmitted and received a half-cycle before the SPICLK transition. As a result, both controllers send and receive data simultaneously. The application software determines whether the data is meaningful or dummy data. There are three possible methods for data transmission:

- Master sends data; slave sends dummy data
- Master sends data; slave sends data
- Master sends dummy data; slave sends data

The master can initiate a data transfer at any time because it controls the SPICLK signal. The software, however, determines how the master detects when the slave is ready to broadcast data.

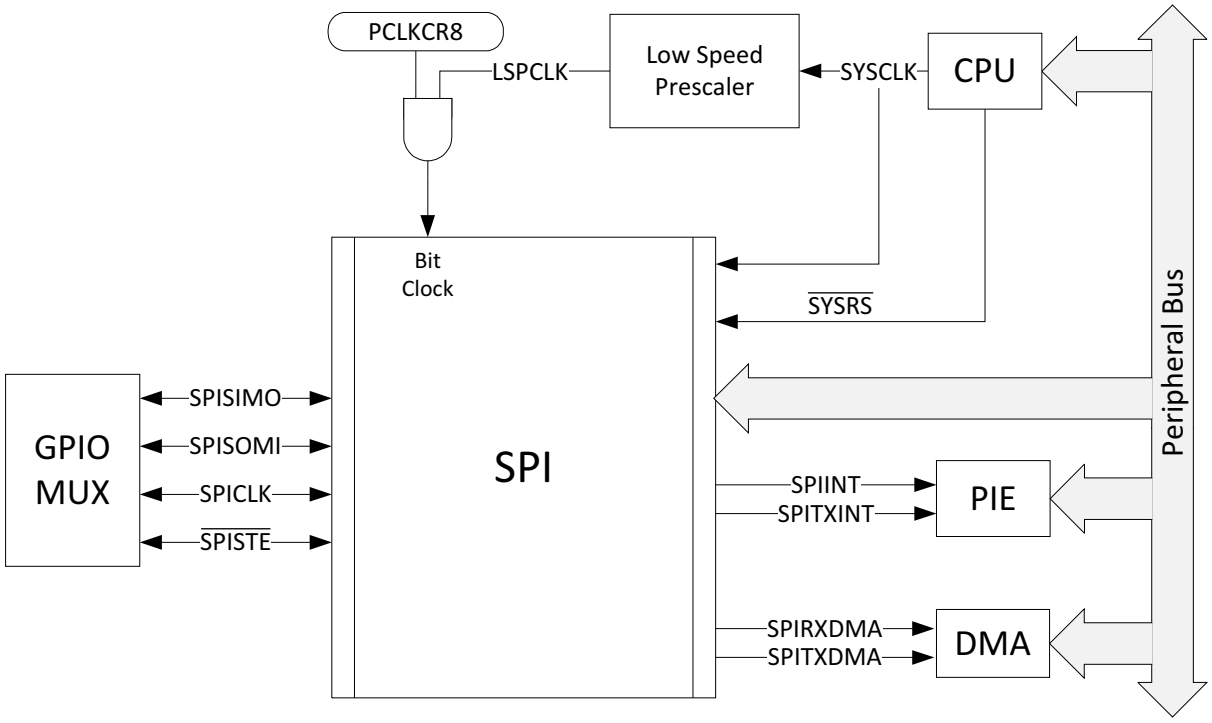

Figure 6-30. SPI

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6.10.1.1 SPI Electrical Data and Timing

The following sections contain the SPI External Timings in Non-High-Speed Mode:

Section 6.10.1.1.1 Master Mode External Timings Where Clock Phase = 0
Section 6.10.1.1.2 Master Mode External Timings Where Clock Phase = 1
Section 6.10.1.1.3 Slave Mode External Timings Where Clock Phase = 0
Section 6.10.1.1.4 Slave Mode External Timings Where Clock Phase = 1

The following sections contain the SPI External Timings in High-Speed Mode:

Section 6.10.1.1.5 High-Speed Master Mode External Timings Where Clock Phase = 0
Section 6.10.1.1.6 High-Speed Master Mode External Timings Where Clock Phase = 1
Section 6.10.1.1.7 High-Speed Slave Mode External Timings Where Clock Phase = 0
Section 6.10.1.1.8 High-Speed Slave Mode External Timings Where Clock Phase = 1

NOTE

All timing parameters for SPI High-Speed Mode assume a load capacitance of 5 pF on SPICLK, SPISIMO, and SPISOMI.

For more information about the SPI in High-Speed mode, see the "Serial Peripheral Interface (SPI)" chapter of the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual* (SPRUHM8).

In order to use the SPI in High-Speed mode, the application must use the high-speed enabled GPIOs (see Section 4.3.3).

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6.10.1.1.1 Master Mode External Timings Where Clock Phase = 0

Table 6-38. SPI Master Mode External Timings Where (SPIBRR + 1) is Even or SPIBRR = 0 or 2

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	ns
2	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	
3	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - 1$	$0.5_{tc(SPC)M} + 1$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5_{tc(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	
4	$t_{d(SPCH-SIMO)M}$	Delay time, SPICLK high to SPISIMO valid (clock polarity = 0)		3	ns
	$t_{d(SPCL-SIMO)M}$	Delay time, SPICLK low to SPISIMO valid (clock polarity = 1)		3	
5	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - 3$		ns
	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - 3$		
8	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 0)	20		ns
	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 1)	20		
9	$t_{h(SPCL-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0)	0		ns
	$t_{h(SPCH-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1)	0		
23	$t_{d(STE-SPCH)M}$	Delay time, $\overline{\text{SPISTE}}$ low to SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)} - 3$		ns
	$t_{d(STE-SPCL)M}$	Delay time, $\overline{\text{SPISTE}}$ low to SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)} - 3$		
24	$t_{d(SPCL-STE)M}$	Delay time, SPICLK low to $\overline{\text{SPISTE}}$ invalid (clock polarity = 0)	$0.5t_{c(SPC)} - 3$		ns
	$t_{d(SPCH-STE)M}$	Delay time, SPICLK high to $\overline{\text{SPISTE}}$ invalid (clock polarity = 1)	$0.5t_{c(SPC)} - 3$		

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Table 6-39. SPI Master Mode External Timings Where (SPIBRR + 1) is Odd and SPIBRR > 3

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	ns
2	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 1$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 1$	
3	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 1$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 1$	
4	$t_{d(SPCH-SIMO)M}$	Delay time, SPICLK high to SPISIMO valid (clock polarity = 0)		3	ns
	$t_{d(SPCL-SIMO)M}$	Delay time, SPICLK low to SPISIMO valid (clock polarity = 1)		3	
5	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 3$		ns
	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 3$		
8	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 0)	20		ns
	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 1)	20		
9	$t_{h(SPCL-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0)	0		ns
	$t_{h(SPCH-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1)	0		
23	$t_{d(STE-SPCH)M}$	Delay time, $\overline{\text{SPISTE}}$ low to SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)} - 3$		ns
	$t_{d(STE-SPCL)M}$	Delay time, $\overline{\text{SPISTE}}$ low to SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)} - 3$		
24	$t_{d(SPCL-STE)M}$	Delay time, SPICLK low to $\overline{\text{SPISTE}}$ invalid (clock polarity = 0)	$0.5t_{c(SPC)} - 3$		ns
	$t_{d(SPCH-STE)M}$	Delay time, SPICLK high to $\overline{\text{SPISTE}}$ invalid (clock polarity = 1)	$0.5t_{c(SPC)} - 3$		

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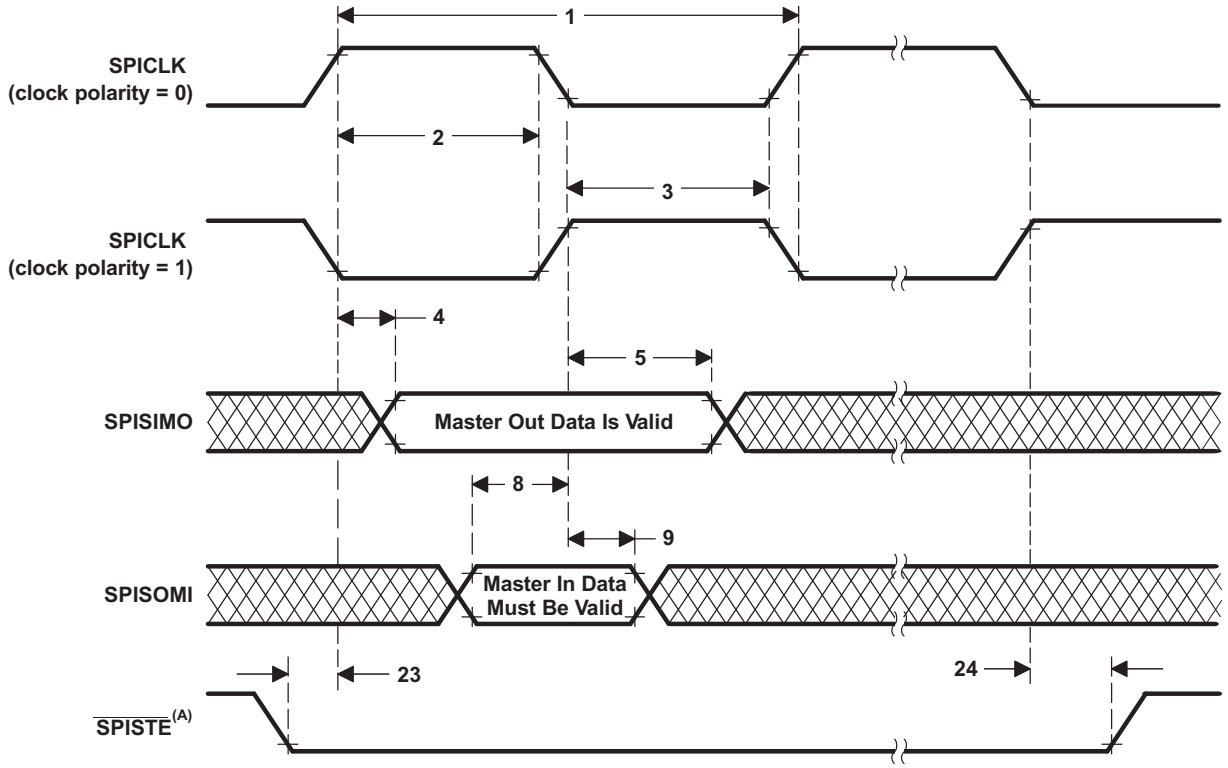

A. On the trailing end of the word, $\overline{\text{SPISTE}}$ will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

Figure 6-31. SPI Master Mode External Timing (Clock Phase = 0)

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6.10.1.1.2 Master Mode External Timings Where Clock Phase = 1

Table 6-40. SPI Master Mode External Timings Where (SPIBRR + 1) is Even or SPIBRR = 0 or 2

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	ns
2	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
	$t_{w(SPCL))M}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	
3	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	
6	$t_{d(SIMO-SPCH)M}$	Delay time, SPISIMO data valid to SPICLK high (clock polarity = 0)		$0.5t_{c(SPC)M} - 3$	ns
	$t_{d(SIMO-SPCL)M}$	Delay time, SPISIMO data valid to SPICLK low (clock polarity = 1)		$0.5t_{c(SPC)M} - 3$	
7	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - 3$		ns
	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 3$		
10	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 0)	20		ns
	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 1)	20		
11	$t_{h(SPCH-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 0)	0		ns
	$t_{h(SPCL-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 1)	0		
23	$t_{d(STE-SPCH)M}$	Delay time, $\overline{\text{SPISTE}}$ low to SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)} - 3$		ns
	$t_{d(STE-SPCL)M}$	Delay time, $\overline{\text{SPISTE}}$ low to SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)} - 3$		
24	$t_{d(SPCL-STE)M}$	Delay time, SPICLK low to $\overline{\text{SPISTE}}$ invalid (clock polarity = 0)	$0.5t_{c(SPC)} - 3$		ns
	$t_{d(SPCH-STE)M}$	Delay time, SPICLK high to $\overline{\text{SPISTE}}$ invalid (clock polarity = 1)	$0.5t_{c(SPC)} - 3$		

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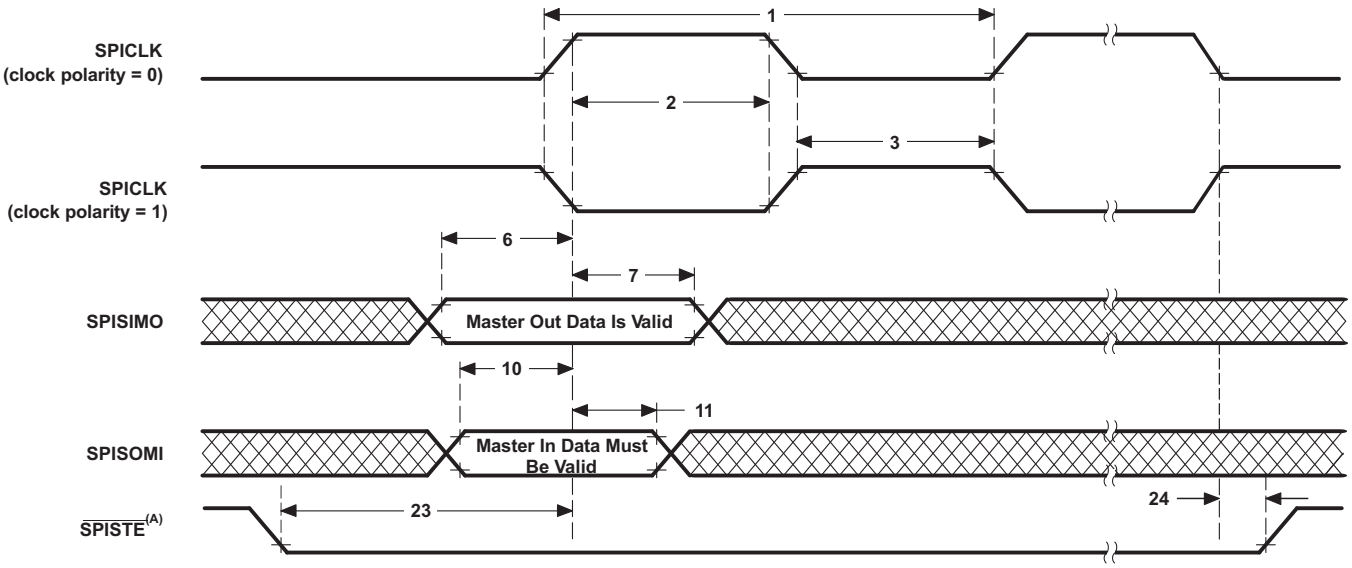
Table 6-41. SPI Master Mode External Timings Where (SPIBRR + 1) is Odd or SPIBRR > 3

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	ns
2	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 1$	ns
	$t_{w(SPCL))M}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 1$	
3	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 1$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5_{tc(SPC)M} + 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 1$	
6	$t_{d(SIMO-SPCH)M}$	Delay time, SPISIMO data valid to SPICLK high (clock polarity = 0)		$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$	ns
	$t_{d(SIMO-SPCL)M}$	Delay time, SPISIMO data valid to SPICLK low (clock polarity = 1)		$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 3$	
7	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 3$		ns
	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$		
10	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 0)	20		ns
	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 1)	20		
11	$t_{h(SPCH-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 0)	0		ns
	$t_{h(SPCL-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 1)	0		
23	$t_{d(STE-SPCH)M}$	Delay time, $\overline{\text{SPISTE}}$ low to SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)} - 3$		ns
	$t_{d(STE-SPCL)M}$	Delay time, $\overline{\text{SPISTE}}$ low to SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)} - 3$		
24	$t_{d(SPCL-STE)M}$	Delay time, SPICLK low to $\overline{\text{SPISTE}}$ invalid (clock polarity = 0)	$0.5t_{c(SPC)} - 3$		ns
	$t_{d(SPCH-STE)M}$	Delay time, SPICLK high to $\overline{\text{SPISTE}}$ invalid (clock polarity = 1)	$0.5t_{c(SPC)} - 3$		



A. On the trailing end of the word, $\overline{\text{SPISTE}}$ will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

Figure 6-32. SPI Master Mode External Timing (Clock Phase = 1)

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6.10.1.1.3 Slave Mode External Timings Where Clock Phase = 0

Table 6-42. SPI Slave Mode External Timings Where Clock Phase = 0

NO.			MIN	MAX	UNIT
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$4t_{c(SYSCLK)}$		ns
13	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	$2t_{c(SYSCLK)} - 1$		ns
	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 1)	$2t_{c(SYSCLK)} - 1$		
14	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	$2t_{c(SYSCLK)} - 1$		ns
	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 1)	$2t_{c(SYSCLK)} - 1$		
15	$t_{d(SPCH-SOMI)S}$	Delay time, SPICLK high to SPISOMI valid (clock polarity = 0)		20	ns
	$t_{d(SPCL-SOMI)S}$	Delay time, SPICLK low to SPISOMI valid (clock polarity = 1)		20	
16	$t_{v(SPCH-SOMI)S}$	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 0)	0		ns
	$t_{v(SPCL-SOMI)S}$	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 1)	0		
19	$t_{su(SIMO-SPCL)S}$	Setup time, SPISIMO before SPICLK low (clock polarity = 0)	5		ns
	$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO before SPICLK high (clock polarity = 1)	5		
20	$t_{h(SPCL-SIMO)S}$	Hold time, SPISIMO data valid after SPICLK low (clock polarity = 0)	5		ns
	$t_{h(SPCH-SIMO)S}$	Hold time, SPISIMO data valid after SPICLK high (clock polarity = 1)	5		
25	$t_{su(STE-SPCH)S}$	Setup time, $\overline{\text{SPISTE}}$ valid before SPICLK high (clock polarity = 0)	$2t_{c(SYSCLK)}$		ns
	$t_{su(STE-SPCL)S}$	Setup time, $\overline{\text{SPISTE}}$ valid before SPICLK low (clock polarity = 1)	$2t_{c(SYSCLK)}$		
26	$t_{h(SPCL-STE)S}$	Hold time, $\overline{\text{SPISTE}}$ invalid after SPICLK low (clock polarity = 0)	$2t_{c(SYSCLK)}$		ns
	$t_{h(SPCH-STE)S}$	Hold time, $\overline{\text{SPISTE}}$ invalid after SPICLK high (clock polarity = 1)	$2t_{c(SYSCLK)}$		

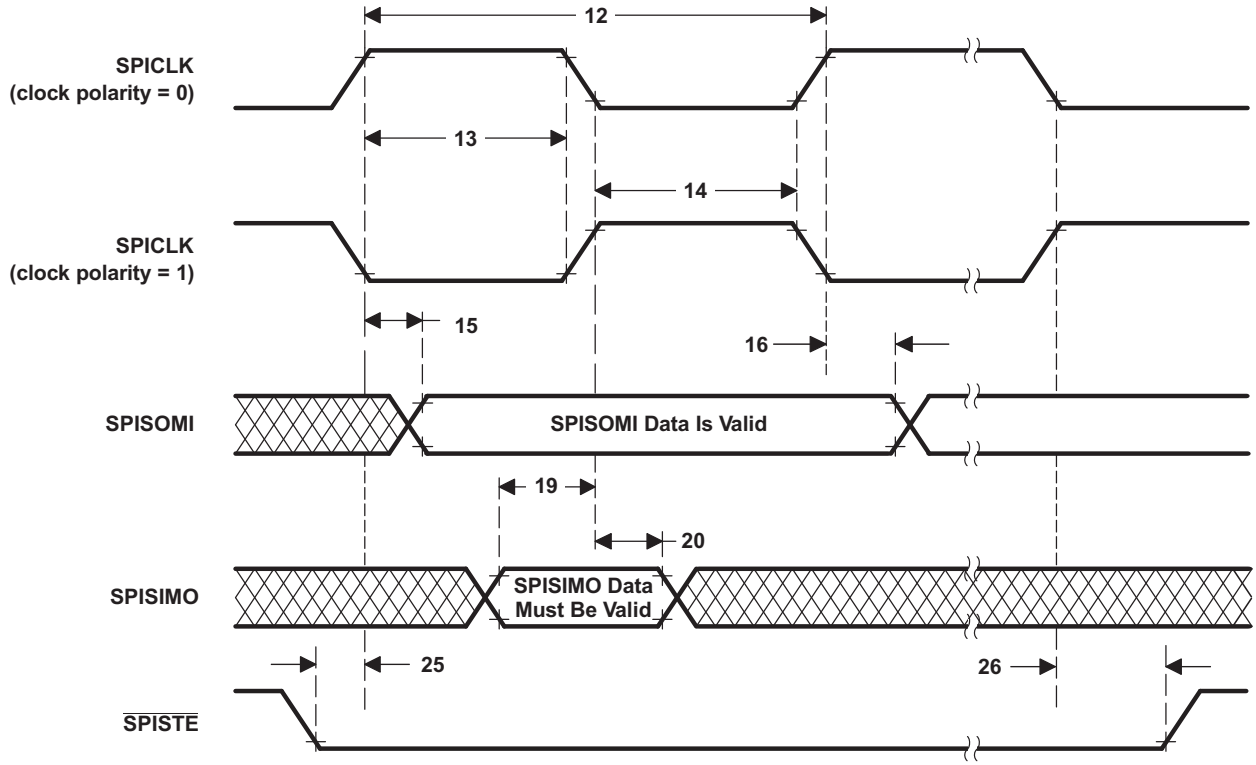

Figure 6-33. SPI Slave Mode External Timing (Clock Phase = 0)

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6.10.1.1.4 Slave Mode External Timings Where Clock Phase = 1

Table 6-43. SPI Slave Mode External Timings Where Clock Phase = 1

NO.			MIN	MAX	UNIT
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$8t_{c(SYSCLK)}$		ns
13	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	$4t_{c(SYSCLK)} - 1$		ns
	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 1)	$4t_{c(SYSCLK)} - 1$		
14	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	$4t_{c(SYSCLK)} - 1$		ns
	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 1)	$4t_{c(SYSCLK)} - 1$		
17	$t_{d(SPCL-SOMI)S}$	Delay time, SPICLK low to SPISOMI (clock polarity = 0)		20	ns
	$t_{d(SPCH-SOMI)S}$	Delay time, SPICLK high to SPISOMI (clock polarity = 1)		20	
18	$t_{v(SPCL-SOMI)S}$	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 0)	0		ns
	$t_{v(SPCH-SOMI)S}$	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 1)	0		
21	$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO before SPICLK high (clock polarity = 0)	5		ns
	$t_{su(SIMO-SPCL)S}$	Setup time, SPISIMO before SPICLK low (clock polarity = 1)	5		
22	$t_{h(SPCH-SIMO)S}$	Hold time, SPISIMO data valid after SPICLK high (clock polarity = 0)	5		ns
	$t_{h(SPCL-SIMO)S}$	Hold time, SPISIMO data valid after SPICLK low (clock polarity = 1)	5		
25	$t_{su(STE-SPCH)S}$	Setup time, $\overline{\text{SPISTE}}$ valid before SPICLK high (clock polarity = 0)	$2t_{c(SYSCLK)}$		ns
	$t_{su(STE-SPCL)S}$	Setup time, $\overline{\text{SPISTE}}$ valid before SPICLK low (clock polarity = 1)	$2t_{c(SYSCLK)}$		
26	$t_{h(STE-SPCL)S}$	Hold time, $\overline{\text{SPISTE}}$ invalid after SPICLK low (clock polarity = 0)	$2t_{c(SYSCLK)}$		ns
	$t_{h(STE-SPCH)S}$	Hold time, $\overline{\text{SPISTE}}$ invalid after SPICLK high (clock polarity = 1)	$2t_{c(SYSCLK)}$		

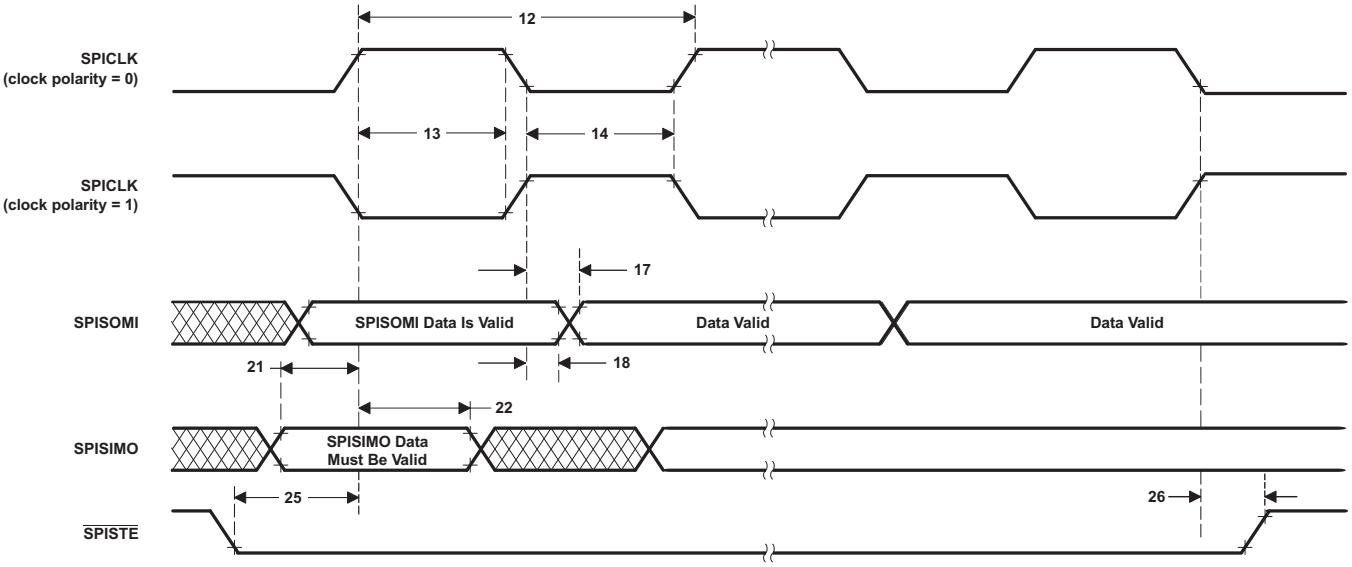

Figure 6-34. SPI Slave Mode External Timing (Clock Phase = 1)

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6.10.1.1.5 High-Speed Master Mode External Timings Where Clock Phase = 0

Table 6-44. High-Speed SPI Master Mode External Timings Where (SPIBRR + 1) is Even or SPIBRR = 0 or 2

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	ns
2	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	
3	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - 1$	$0.5_{tc(SPC)M} + 1$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5_{tc(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	
4	$t_{d(SPCH-SIMO)M}$	Delay time, SPICLK high to SPISIMO valid (clock polarity = 0)		1	ns
	$t_{d(SPCL-SIMO)M}$	Delay time, SPICLK low to SPISIMO valid (clock polarity = 1)		1	
5	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - 1$		ns
	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - 1$		
8	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 0)	1		ns
	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 1)	1		
9	$t_{h(SPCL-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0)	5		ns
	$t_{h(SPCH-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1)	5		
23	$t_{d(STE-SPCH)M}$	Delay time, $\overline{\text{SPISTE}}$ low to SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)} - 1$		ns
	$t_{d(STE-SPCL)M}$	Delay time, $\overline{\text{SPISTE}}$ low to SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)} - 1$		
24	$t_{d(SPCL-STE)M}$	Delay time, SPICLK low to $\overline{\text{SPISTE}}$ invalid (clock polarity = 0)	$0.5t_{c(SPC)} - 1$		ns
	$t_{d(SPCH-STE)M}$	Delay time, SPICLK high to $\overline{\text{SPISTE}}$ invalid (clock polarity = 1)	$0.5t_{c(SPC)} - 1$		

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Table 6-45. High-Speed SPI Master Mode External Timings Where (SPIBRR + 1) is Odd and SPIBRR > 3

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	ns
2	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 1$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 1$	
3	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 1$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 1$	
4	$t_{d(SPCH-SIMO)M}$	Delay time, SPICLK high to SPISIMO valid (clock polarity = 0)		1	ns
	$t_{d(SPCL-SIMO)M}$	Delay time, SPICLK low to SPISIMO valid (clock polarity = 1)		1	
5	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$		ns
	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$		
8	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 0)	6		ns
	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 1)	6		
9	$t_{h(SPCL-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0)	7		ns
	$t_{h(SPCH-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1)	7		
23	$t_{d(STE-SPCH)M}$	Delay time, $\overline{\text{SPISTE}}$ low to SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)} - 1$		ns
	$t_{d(STE-SPCL)M}$	Delay time, $\overline{\text{SPISTE}}$ low to SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)} - 1$		
24	$t_{d(SPCL-STE)M}$	Delay time, SPICLK low to $\overline{\text{SPISTE}}$ invalid (clock polarity = 0)	$0.5t_{c(SPC)} - 1$		ns
	$t_{d(SPCH-STE)M}$	Delay time, SPICLK high to $\overline{\text{SPISTE}}$ invalid (clock polarity = 1)	$0.5t_{c(SPC)} - 1$		

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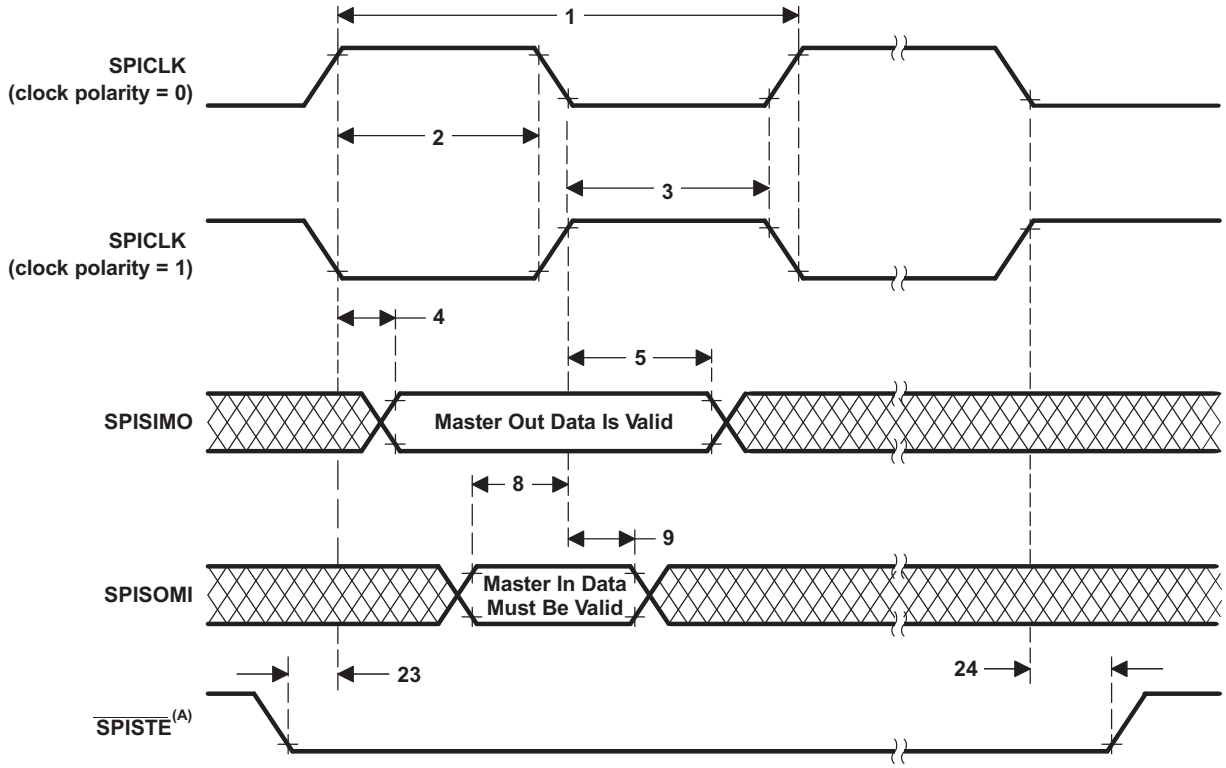

A. On the trailing end of the word, SPISTE will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

Figure 6-35. High-Speed SPI Master Mode External Timing (Clock Phase = 0)

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6.10.1.1.6 High-Speed Master Mode External Timings Where Clock Phase = 1

Table 6-46. High-Speed SPI Master Mode External Timings Where (SPIBRR + 1) is Even or SPIBRR = 0 or 2

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	ns
2	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
	$t_{w(SPCL))M}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	
3	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	
6	$t_{d(SIMO-SPCH)M}$	Delay time, SPISIMO data valid to SPICLK high (clock polarity = 0)		$0.5t_{c(SPC)M} - 1$	ns
	$t_{d(SIMO-SPCL)M}$	Delay time, SPISIMO data valid to SPICLK low (clock polarity = 1)		$0.5t_{c(SPC)M} - 1$	
7	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - 1$		ns
	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 1$		
10	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 0)	1		ns
	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 1)	1		
11	$t_{h(SPCH-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 0)	7		ns
	$t_{h(SPCL-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 1)	7		
23	$t_{d(STE-SPCH)M}$	Delay time, $\overline{\text{SPISTE}}$ low to SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)} - 1$		ns
	$t_{d(STE-SPCL)M}$	Delay time, $\overline{\text{SPISTE}}$ low to SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)} - 1$		
24	$t_{d(SPCL-STE)M}$	Delay time, SPICLK low to $\overline{\text{SPISTE}}$ invalid (clock polarity = 0)	$0.5t_{c(SPC)} - 1$		ns
	$t_{d(SPCH-STE)M}$	Delay time, SPICLK high to $\overline{\text{SPISTE}}$ invalid (clock polarity = 1)	$0.5t_{c(SPC)} - 1$		

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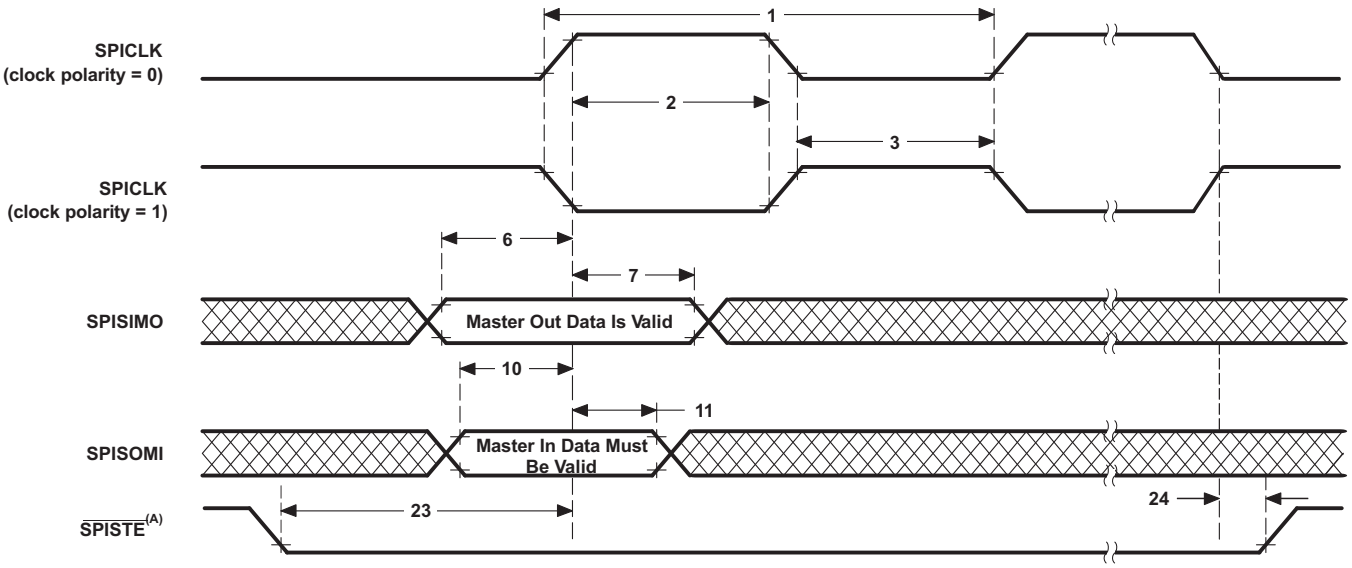
Table 6-47. High-Speed SPI Master Mode External Timings Where (SPIBRR + 1) is Odd or SPIBRR > 3

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	ns
2	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 1$	ns
	$t_{w(SPCL))M}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 1$	
3	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 1$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5_{tc(SPC)M} + 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 1$	
6	$t_{d(SIMO-SPCH)M}$	Delay time, SPISIMO data valid to SPICLK high (clock polarity = 0)		$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$	ns
	$t_{d(SIMO-SPCL)M}$	Delay time, SPISIMO data valid to SPICLK low (clock polarity = 1)		$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$	
7	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$		ns
	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$		
10	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 0)	1		ns
	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 1)	1		
11	$t_{h(SPCH-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 0)	5		ns
	$t_{h(SPCL-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 1)	5		
23	$t_{d(STE-SPCH)M}$	Delay time, $\overline{SPISTE}$ low to SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)} - 1$		ns
	$t_{d(STE-SPCL)M}$	Delay time, $\overline{SPISTE}$ low to SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)} - 1$		
24	$t_{d(SPCL-STE)M}$	Delay time, SPICLK low to $\overline{SPISTE}$ invalid (clock polarity = 0)	$0.5t_{c(SPC)} - 1$		ns
	$t_{d(SPCH-STE)M}$	Delay time, SPICLK high to $\overline{SPISTE}$ invalid (clock polarity = 1)	$0.5t_{c(SPC)} - 1$		



A. On the trailing end of the word, $\overline{SPISTE}$ will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

Figure 6-36. High-Speed SPI Master Mode External Timing (Clock Phase = 1)

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6.10.1.1.7 High-Speed Slave Mode External Timings Where Clock Phase = 0

Table 6-48. High-Speed SPI Slave Mode External Timings Where Clock Phase = 0

NO.			MIN	MAX	UNIT
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$4t_{c(SYSCLK)}$		ns
13	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	$2t_{c(SYSCLK)} - 1$		ns
	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 1)	$2t_{c(SYSCLK)} - 1$		
14	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	$2t_{c(SYSCLK)} - 1$		ns
	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 1)	$2t_{c(SYSCLK)} - 1$		
15	$t_{d(SPCH-SOMI)S}$	Delay time, SPICLK high to SPISOMI valid (clock polarity = 0)		9	ns
	$t_{d(SPCL-SOMI)S}$	Delay time, SPICLK low to SPISOMI valid (clock polarity = 1)		9	
16	$t_{v(SPCH-SOMI)S}$	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 0)	0		ns
	$t_{v(SPCL-SOMI)S}$	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 1)	0		
19	$t_{su(SIMO-SPCL)S}$	Setup time, SPISIMO before SPICLK low (clock polarity = 0)	5		ns
	$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO before SPICLK high (clock polarity = 1)	5		
20	$t_{h(SPCL-SIMO)S}$	Hold time, SPISIMO data valid after SPICLK low (clock polarity = 0)	5		ns
	$t_{h(SPCH-SIMO)S}$	Hold time, SPISIMO data valid after SPICLK high (clock polarity = 1)	5		
25	$t_{su(STE-SPCH)S}$	Setup time, $\overline{\text{SPISTE}}$ valid before SPICLK high (clock polarity = 0)	$2t_{c(SYSCLK)}$		ns
	$t_{su(STE-SPCL)S}$	Setup time, $\overline{\text{SPISTE}}$ valid before SPICLK low (clock polarity = 1)	$2t_{c(SYSCLK)}$		
26	$t_{h(SPCL-STE)S}$	Hold time, $\overline{\text{SPISTE}}$ invalid after SPICLK low (clock polarity = 0)	$2t_{c(SYSCLK)}$		ns
	$t_{h(SPCH-STE)S}$	Hold time, $\overline{\text{SPISTE}}$ invalid after SPICLK high (clock polarity = 1)	$2t_{c(SYSCLK)}$		

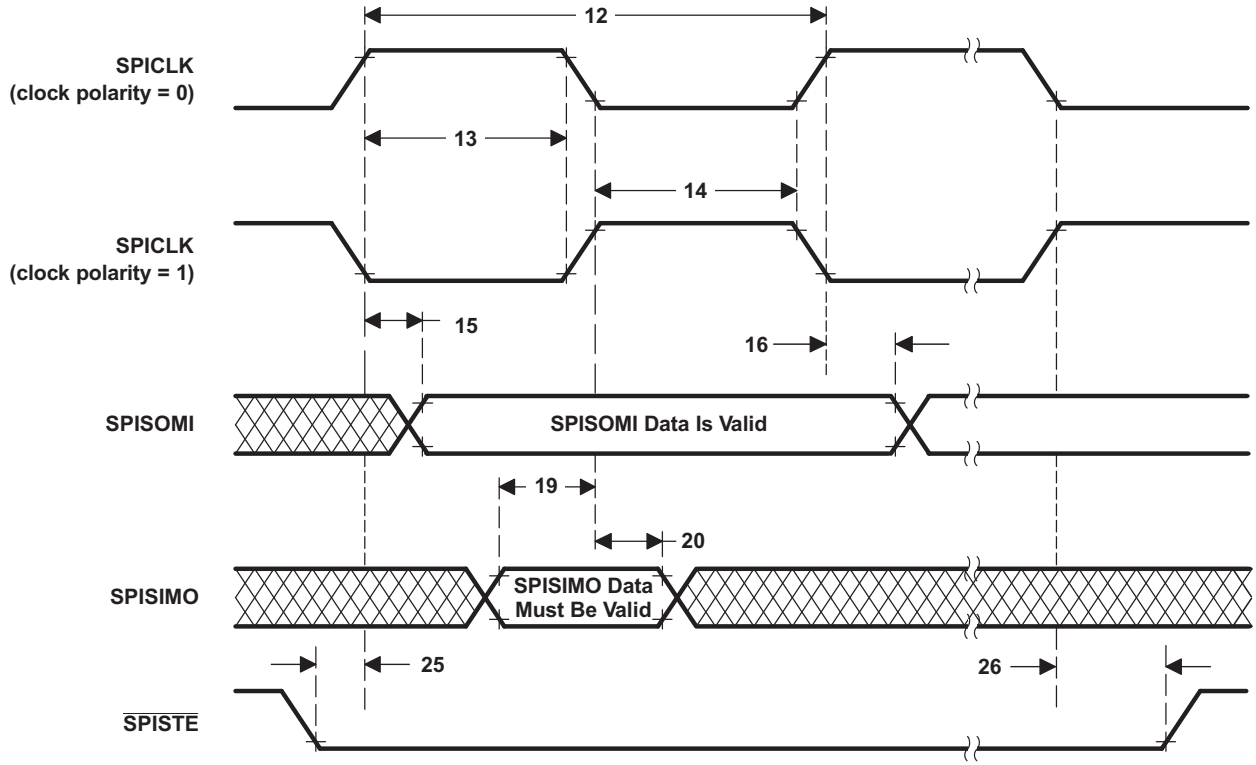

Figure 6-37. High-Speed SPI Slave Mode External Timing (Clock Phase = 0)

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6.10.1.1.8 High-Speed Slave Mode External Timings Where Clock Phase = 1

Table 6-49. High-Speed SPI Slave Mode External Timings Where Clock Phase = 1

NO.			MIN	MAX	UNIT
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$8t_{c(SYSCLK)}$		ns
13	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	$4t_{c(SYSCLK)} - 1$		ns
	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 1)	$4t_{c(SYSCLK)} - 1$		
14	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	$4t_{c(SYSCLK)} - 1$		ns
	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 1)	$4t_{c(SYSCLK)} - 1$		
17	$t_{d(SPCL-SOMI)S}$	Delay time, SPICLK low to SPISOMI (clock polarity = 0)		9	ns
	$t_{d(SPCH-SOMI)S}$	Delay time, SPICLK high to SPISOMI (clock polarity = 1)		9	
18	$t_{v(SPCL-SOMI)S}$	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 0)	0		ns
	$t_{v(SPCH-SOMI)S}$	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 1)	0		
21	$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO before SPICLK high (clock polarity = 0)	5		ns
	$t_{su(SIMO-SPCL)S}$	Setup time, SPISIMO before SPICLK low (clock polarity = 1)	5		
22	$t_{h(SPCH-SIMO)S}$	Hold time, SPISIMO data valid after SPICLK high (clock polarity = 0)	5		ns
	$t_{h(SPCL-SIMO)S}$	Hold time, SPISIMO data valid after SPICLK low (clock polarity = 1)	5		
25	$t_{su(STE-SPCH)S}$	Setup time, $\overline{\text{SPISTE}}$ valid before SPICLK high (clock polarity = 0)	$2t_{c(SYSCLK)}$		ns
	$t_{su(STE-SPCL)S}$	Setup time, $\overline{\text{SPISTE}}$ valid before SPICLK low (clock polarity = 1)	$2t_{c(SYSCLK)}$		
26	$t_{h(STE-SPCL)S}$	Hold time, $\overline{\text{SPISTE}}$ invalid after SPICLK low (clock polarity = 0)	$2t_{c(SYSCLK)}$		ns
	$t_{h(STE-SPCH)S}$	Hold time, $\overline{\text{SPISTE}}$ invalid after SPICLK high (clock polarity = 1)	$2t_{c(SYSCLK)}$		

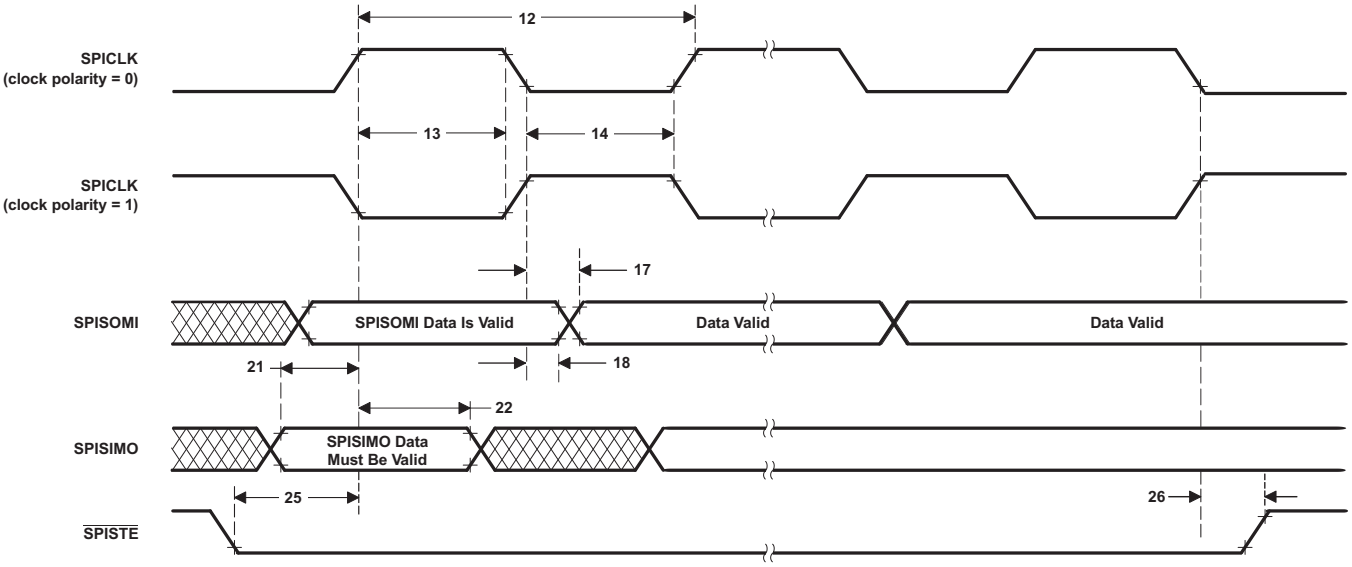

Figure 6-38. High-Speed SPI Slave Mode External Timing (Clock Phase = 1)

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6.10.2 Serial Communications Interface

The SCI is a two-wire asynchronous serial port, commonly known as a UART. The SCI module supports digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format

The SCI receiver and transmitter each have a 16-level-deep FIFO for reducing servicing overhead, and each has its own separate enable and interrupt bits. Both can be operated independently for half-duplex communication, or simultaneously for full-duplex communication. To specify data integrity, the SCI checks received data for break detection, parity, overrun, and framing errors. The bit rate is programmable to different speeds through a 16-bit baud-select register.

Features of the SCI module include:

- Two external pins:
  - SCITXD: SCI transmit-output pin
  - SCIRXD: SCI receive-input pin

    NOTE: Both pins can be used as GPIO if not used for SCI.
  - Baud rate programmable to 64K different rates
- Data-word format
  - One start bit
  - Data-word length programmable from one to eight bits
  - Optional even/odd/no parity bit
  - One or two stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: idle-line and address bit
- Half- or full-duplex operation
- Double-buffered receive and transmit functions
- Transmitter and receiver operations can be accomplished through interrupt-driven or polled algorithms with status flags.
  - Transmitter: TXRDY flag (transmitter-buffer register is ready to receive another character) and TX EMPTY flag (transmitter-shift register is empty)
  - Receiver: RXRDY flag (receiver-buffer register is ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR flag (monitoring four interrupt conditions)
- Separate enable bits for transmitter and receiver interrupts (except BRKDT)
- NRZ (non-return-to-zero) format
- Auto baud-detect hardware logic
- 16-level transmit and receive FIFO

NOTE

All registers in this module are 8-bit registers. When a register is accessed, the register data is in the lower byte (bits 7–0), and the upper byte (bits 15–8) is read as zeros. Writing to the upper byte has no effect.

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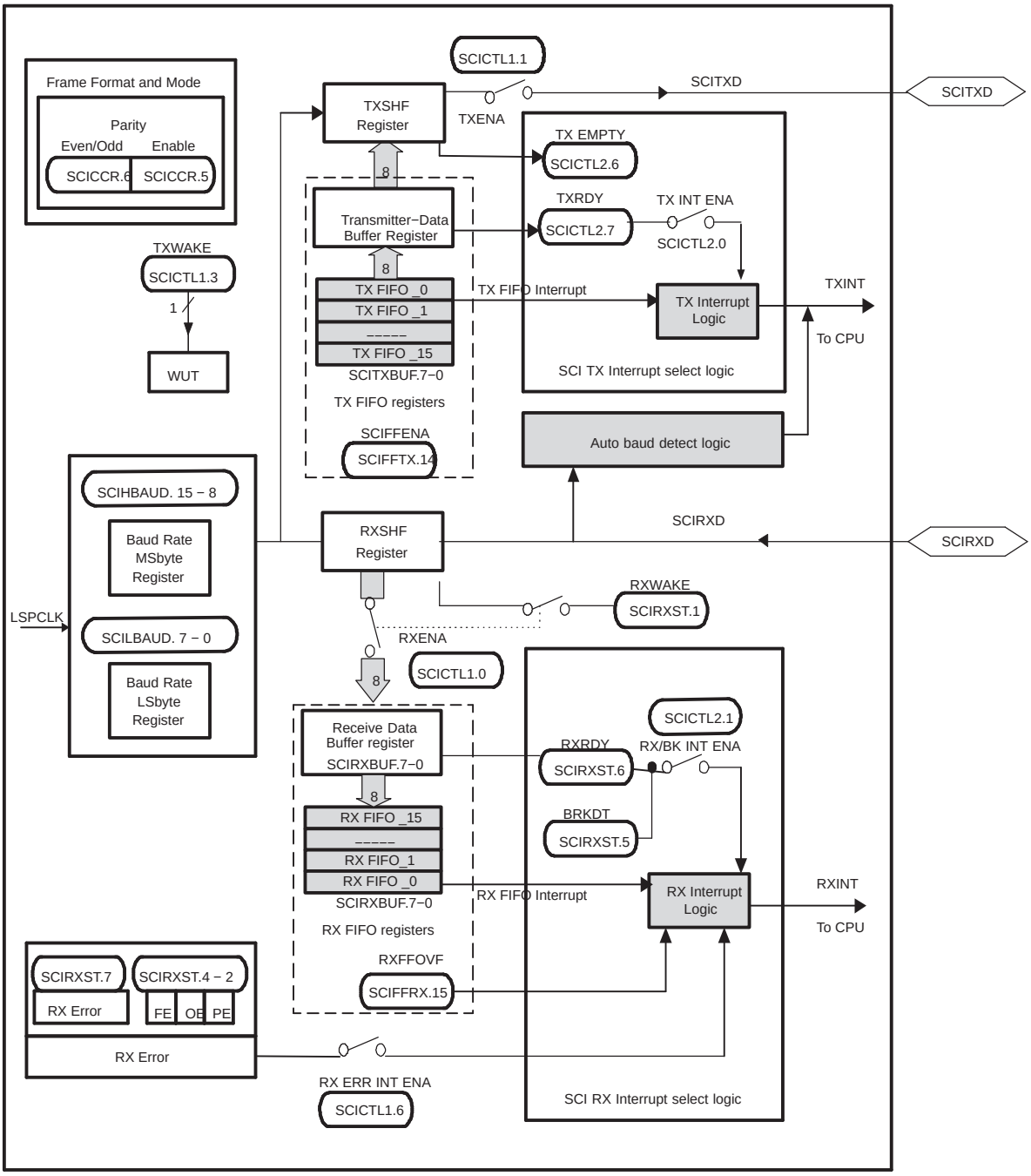

Figure 6-39. SCI Block Diagram

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The major elements used in full-duplex operation include:

- A transmitter (TX) and its major registers:
  - SCITXBUF register – Transmitter Data Buffer register. Contains data (loaded by the CPU) to be transmitted
  - TXSHF register – Transmitter Shift register. Accepts data from the SCITXBUF register and shifts data onto the SCITXD pin, one bit at a time
- A receiver (RX) and its major registers:
  - RXSHF register – Receiver Shift register. Shifts data in from the SCIRXD pin, one bit at a time
  - SCIRXBUF register – Receiver Data Buffer register. Contains data to be read by the CPU. Data from a remote processor is loaded into the RXSHF register and then into the SCIRXBUF and SCIRXEMU registers
- A programmable baud generator
- Data-memory-mapped control and status registers enable the CPU to access the I^2C module registers and FIFOs.

The SCI receiver and transmitter operate independently.

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6.10.3 Inter-Integrated Circuit

The I^2C module has the following features:

- Compliance with the Philips Semiconductors I^2C-bus specification (version 2.1):
  - Support for 1-bit to 8-bit format transfers
  - 7-bit and 10-bit addressing modes
  - General call
  - START byte mode
  - Support for multiple master-transmitters and slave-receivers
  - Support for multiple slave-transmitters and master-receivers
  - Combined master transmit/receive and receive/transmit mode
  - Data transfer rate of from 10 kbps up to 400 kbps (I^2C Fast-mode rate)
- One 16-word receive FIFO and one 16-word transmit FIFO
- One interrupt that can be used by the CPU. This interrupt can be generated as a result of one of the following conditions:
  - Transmit-data ready
  - Receive-data ready
  - Register-access ready
  - No-acknowledgment received
  - Arbitration lost
  - Stop condition detected
  - Addressed as slave
- An additional interrupt that can be used by the CPU when in FIFO mode
- Module enable/disable capability
- Free data format mode

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Figure 6-40 shows how the I²C peripheral module interfaces within the device.

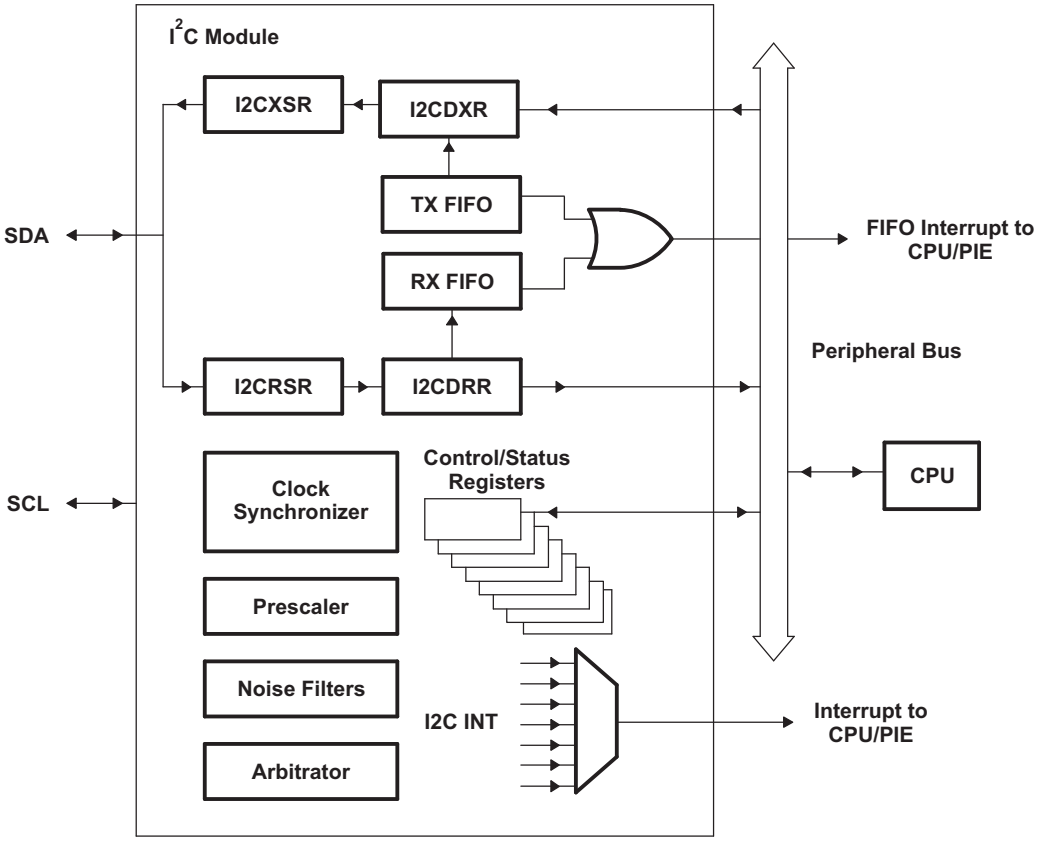

Figure 6-40. I²C Peripheral Module Interfaces

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6.10.3.1 I²C Electrical Data and Timing

Table 6-50. I²C Timing Requirement

			MIN	MAX	UNIT
$t_{h(SDA-SCL)START}$	Hold time, START condition, SCL fall delay after SDA fall		0.6		µs
$t_{su(SCL-SDA)START}$	Setup time, Repeated START, SCL rise before SDA fall delay		0.6		µs
$t_{h(SCL-DAT)}$	Hold time, data after SCL fall		0		µs
$t_{su(DAT-SCL)}$	Setup time, data before SCL rise		100		ns
$t_{r(SDA)}$	Rise time, SDA	Input tolerance	20	300	ns
$t_{r(SCL)}$	Rise time, SCL	Input tolerance	20	300	ns
$t_{f(SDA)}$	Fall time, SDA	Input tolerance	11.4	300	ns
$t_{f(SCL)}$	Fall time, SCL	Input tolerance	11.4	300	ns
$t_{su(SCL-SDA)STOP}$	Setup time, STOP condition, SCL rise before SDA rise delay		0.6		µs

Table 6-51. I²C Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{SCL}	SCL clock frequency		0	400	kHz
$t_{w(SCLL)}$	Pulse duration, SCL clock low		1.3		µs
$t_{w(SCLH)}$	Pulse duration, SCL clock high		0.6		µs
$t_{w(SP)}$	Pulse duration of spikes that will be suppressed by the input filter		0	50	ns
t_{BUF}	Bus free time between STOP and START conditions		1.3		µs
$t_{v(SCL-DAT)}$	Valid time, data after SCL fall			0.9	µs
$t_{v(SCL-ACK)}$	Valid time, Acknowledge after SCL fall			0.9	µs
V_{IL}	Valid low-level input voltage		–0.3	$0.3 * V_{DDIO}$	V
V_{IH}	Valid high-level input voltage		$0.7 * V_{DDIO}$	$V_{DDIO} + 0.3$	V
V_{OL}	Low-level output voltage	Sinking 3 mA	0	0.4	V
I_I	Input current on pins	$0.1 V_{bus} < V_i < 0.9 V_{bus}$	–10	10	µA

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6.10.4 Multichannel Buffered Serial Port

The McBSP module has the following features:

- Compatible to McBSP in TMS320C28x/TMS320F28x DSP devices
- Full-duplex communication
- Double-buffered data registers that allow a continuous data stream
- Independent framing and clocking for receive and transmit
- External shift clock generation or an internal programmable frequency shift clock
- 8-bit data transfer mode can be configured to transmit with LSB or MSB first
- Programmable polarity for both frame synchronization and data clocks
- Highly programmable internal clock and frame generation
- Direct interface to industry-standard CODECs, Analog Interface Chips (AICs), and other serially connected A/D and D/A devices
- Works with SPI-compatible devices
- The following application interfaces can be supported on the McBSP:
  - T1/E1 framers
  - IOM-2 compliant devices
  - AC97-compliant devices (the necessary multiphase frame synchronization capability is provided.)
  - IIS-compliant devices
  - SPI
- McBSP clock rate,

$$CLKG = \frac{CLKSRG}{(1 + CLKGDV)}$$

where CLKSRG source could be LSPCLK, CLKX, or CLKR. Serial port performance is limited by I/O buffer switching speed. Internal prescalers must be adjusted such that the peripheral speed is less than the I/O buffer speed limit.

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Figure 6-41 shows the block diagram of the McBSP module.

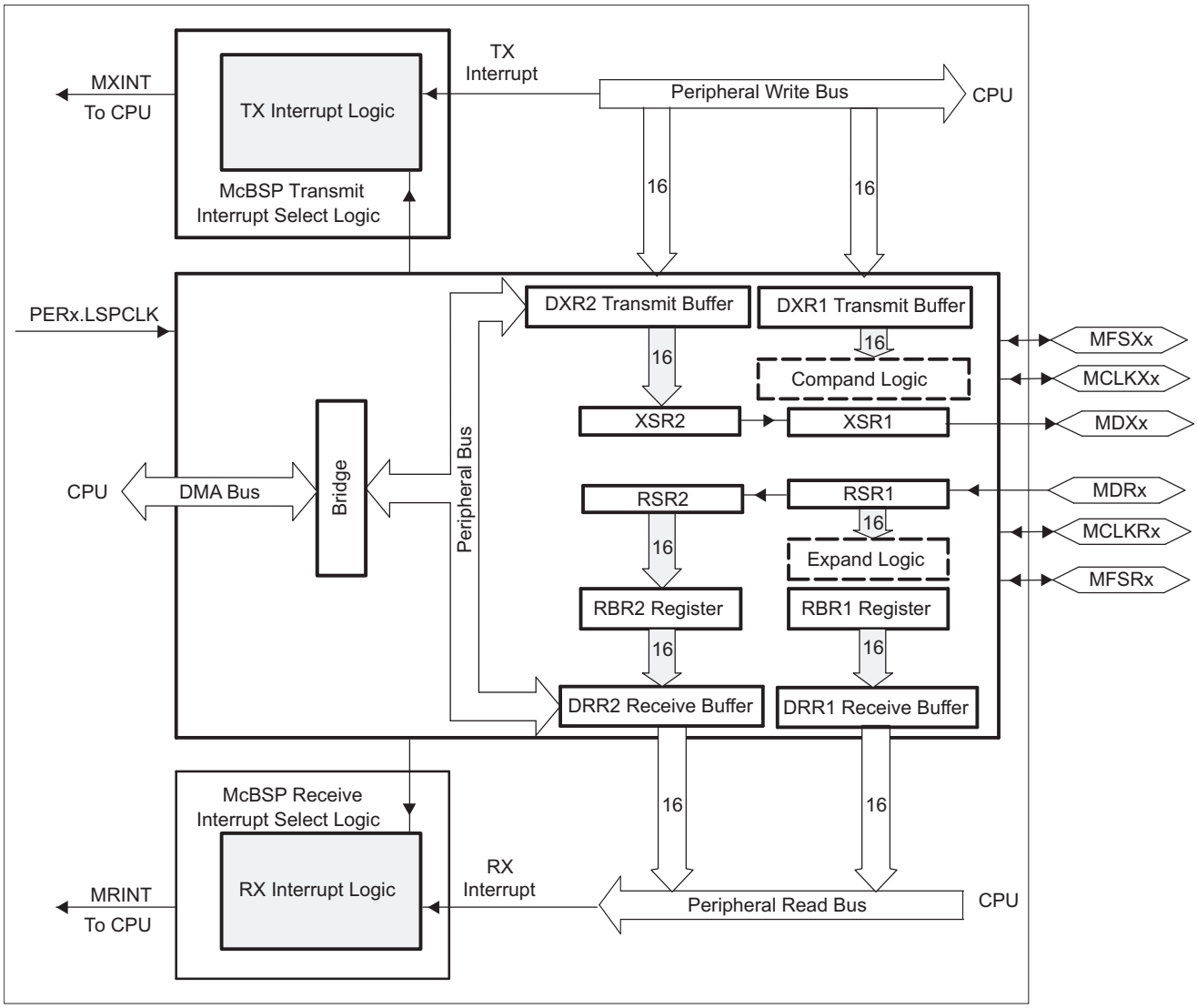

Figure 6-41. McBSP Block Diagram

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6.10.4.1 McBSP Electrical Data and Timing

6.10.4.1.1 McBSP Transmit and Receive Timing

Table 6-52. McBSP Timing Requirements(1) (2)

NO.				MIN	MAX	UNIT
		McBSP module clock (CLKG, CLKX, CLKR) range		1		kHz
					25 (3)	MHz
		McBSP module cycle time (CLKG, CLKX, CLKR) range		40		ns
					1	ms
M11	$t_{c(CKRX)}$	Cycle time, CLKR/X	CLKR/X ext	2P		ns
M12	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X ext	P – 7		ns
M13	$t_{r(CKRX)}$	Rise time, CLKR/X	CLKR/X ext		7	ns
M14	$t_{f(CKRX)}$	Fall time, CLKR/X	CLKR/X ext		7	ns
M15	$t_{su(FRH-CKRL)}$	Setup time, external FSR high before CLKR low	CLKR int	18		ns
			CLKR ext	2		
M16	$t_{h(CKRL-FRH)}$	Hold time, external FSR high after CLKR low	CLKR int	0		ns
			CLKR ext	6		
M17	$t_{su(DRV-CKRL)}$	Setup time, DR valid before CLKR low	CLKR int	18		ns
			CLKR ext	5		
M18	$t_{h(CKRL-DRV)}$	Hold time, DR valid after CLKR low	CLKR int	0		ns
			CLKR ext	3		
M19	$t_{su(FXH-CKXL)}$	Setup time, external FSX high before CLKX low	CLKX int	18		ns
			CLKX ext	2		
M20	$t_{h(CKXL-FXH)}$	Hold time, external FSX high after CLKX low	CLKX int	0		ns
			CLKX ext	6		

(1) Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) 2P = 1/CLKG in ns. CLKG is the output of sample rate generator mux. CLKG = CLKSRG / (1 + CLKGDV). CLKSRG can be LSPCLK, CLKX, CLKR as source. CLKSRG ≤ (SYSCLK/2). McBSP performance is limited by I/O buffer switching speed.
(3) Internal clock prescalers must be adjusted such that the McBSP clock (CLKG, CLKX, CLKR) speeds are not greater than the I/O buffer speed limit (30 MHz).

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Table 6-53. McBSP Switching Characteristics(1) (2)

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER				MIN	MAX	UNIT
M1	$t_{c(CKRX)}$	Cycle time, CLKR/X		CLKR/X int	2P		ns
M2	$t_{w(CKRXH)}$	Pulse duration, CLKR/X high		CLKR/X int	D – 5 (3)	D + 5 (3)	ns
M3	$t_{w(CKRXL)}$	Pulse duration, CLKR/X low		CLKR/X int	C – 5 (3)	C + 5 (3)	ns
M4	$t_{d(CKRH-FRV)}$	Delay time, CLKR high to internal FSR valid		CLKR int	0	4	ns
				CLKR ext	3	27	
M5	$t_{d(CKXH-FXV)}$	Delay time, CLKX high to internal FSX valid		CLKX int	0	4	ns
				CLKX ext	3	27	
M6	$t_{dis(CKXH-DXHZ)}$	Disable time, CLKX high to DX high impedance following last data bit		CLKX int		8	ns
				CLKX ext		14	
M7	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid. This applies to all bits except the first bit transmitted.		CLKX int		9	ns
				CLKX ext		28	
		Delay time, CLKX high to DX valid. Only applies to first bit transmitted when in Data Delay 1 or 2 (XDATDLY=01b or 10b) modes	DXENA = 0	CLKX int		8	
				CLKX ext		14	
			DXENA = 1	CLKX int		P + 8	
				CLKX ext		P + 14	
M8	$t_{en(CKXH-DX)}$	Enable time, CLKX high to DX driven. Only applies to first bit transmitted when in Data Delay 1 or 2 (XDATDLY=01b or 10b) modes	DXENA = 0	CLKX int	0		ns
				CLKX ext	6		
			DXENA = 1	CLKX int	P		
				CLKX ext	P + 6		
M9	$t_{d(FXH-DXV)}$	Delay time, FSX high to DX valid. Only applies to first bit transmitted when in Data Delay 0 (XDATDLY=00b) mode.	DXENA = 0	FSX int		8	ns
				FSX ext		14	
			DXENA = 1	FSX int		P + 8	
				FSX ext		P + 14	
M10	$t_{en(FXH-DX)}$	Enable time, FSX high to DX driven. Only applies to first bit transmitted when in Data Delay 0 (XDATDLY=00b) mode	DXENA = 0	FSX int	0		ns
				FSX ext	6		
			DXENA = 1	FSX int	P		
				FSX ext	P + 6		

(1) Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) 2P = 1/CLKG in ns.
(3) C = CLKRX low pulse width = P
D = CLKRX high pulse width = P

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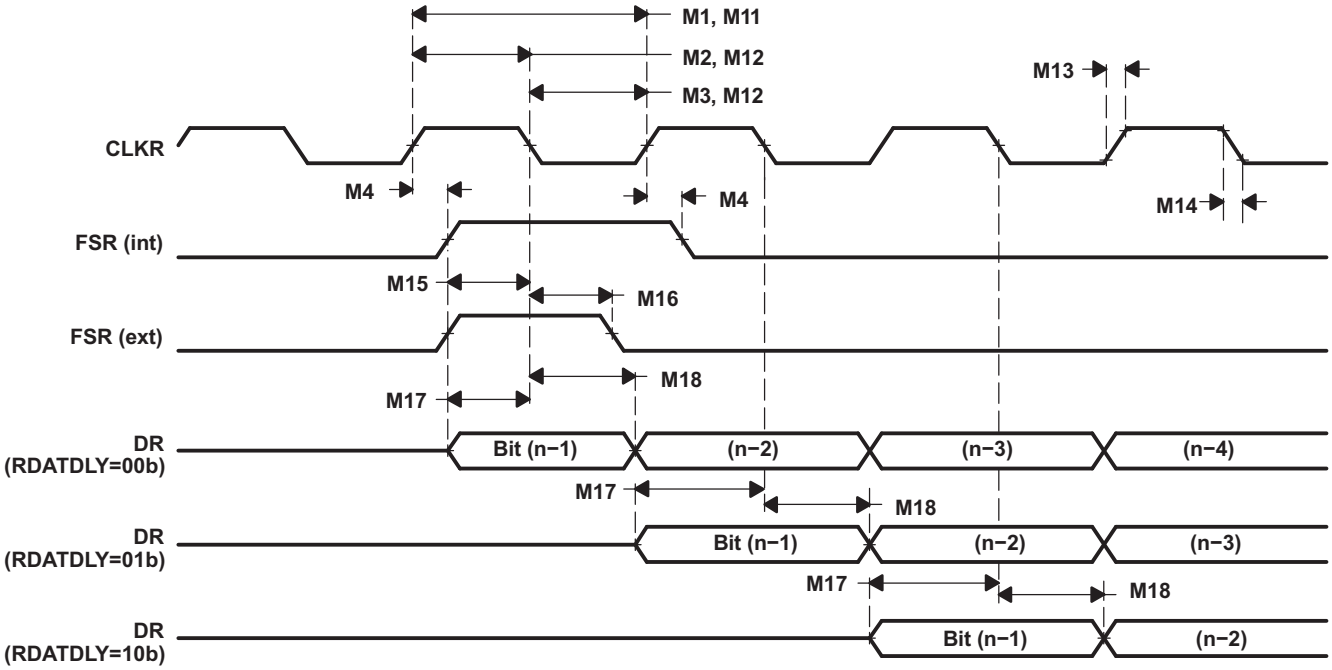

Figure 6-42. McBSP Receive Timing

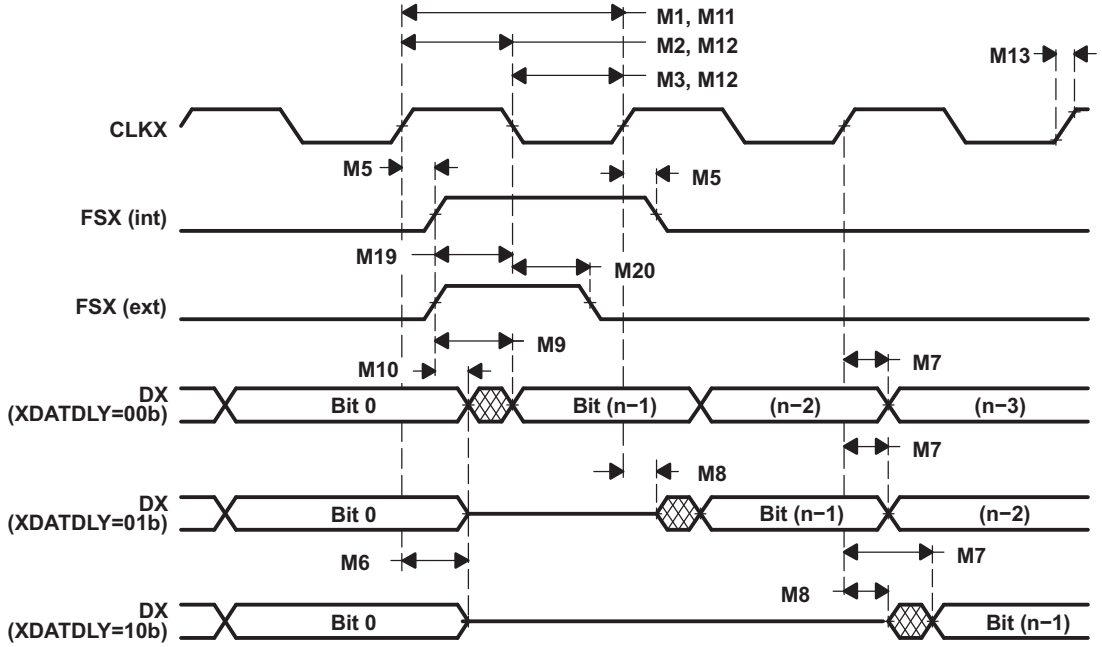

Figure 6-43. McBSP Transmit Timing

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6.10.4.1.2 McBSP as SPI Master or Slave Timing

Table 6-54. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 0)

NO.			MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M30	$t_{su(DRV-CKXL)}$	Setup time, DR valid before CLKX low	30		8P – 10		ns
M31	$t_{h(CKXL-DRV)}$	Hold time, DR valid after CLKX low	1		8P – 10		ns
M32	$t_{su(BFXL-CKXH)}$	Setup time, FSX low before CLKX high			8P + 10		ns
M33	$t_{c(CKX)}$	Cycle time, CLKX	2P (1)		16P		ns

(1) 2P = 1/CLKG

Table 6-55. McBSP as SPI Master or Slave Switching Characteristics Over Recommended Operating Conditions (Unless Otherwise Noted) (CLKSTP = 10b, CLKXP = 0)

NO.	PARAMETER		MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M24	$t_{h(CKXL-FXL)}$	Hold time, FSX low after CLKX low	2P (1)				ns
M25	$t_{d(FXL-CKXH)}$	Delay time, FSX low to CLKX high	P				ns
M28	$t_{dis(FXH-DXHZ)}$	Disable time, DX high impedance following last data bit from FSX high	6		6P + 6		ns
M29	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	6		4P + 6		ns

(1) 2P = 1/CLKG

For all SPI slave modes, CLKX has to be minimum 8 CLKG cycles. Also CLKG should be LSPCLK/2 by setting CLKSM = CLKGDV = 1. With maximum LSPCLK speed of 75 MHz, CLKX maximum frequency will be LSPCLK/16 , that is 4.6875 MHz and P = 13.3 ns.

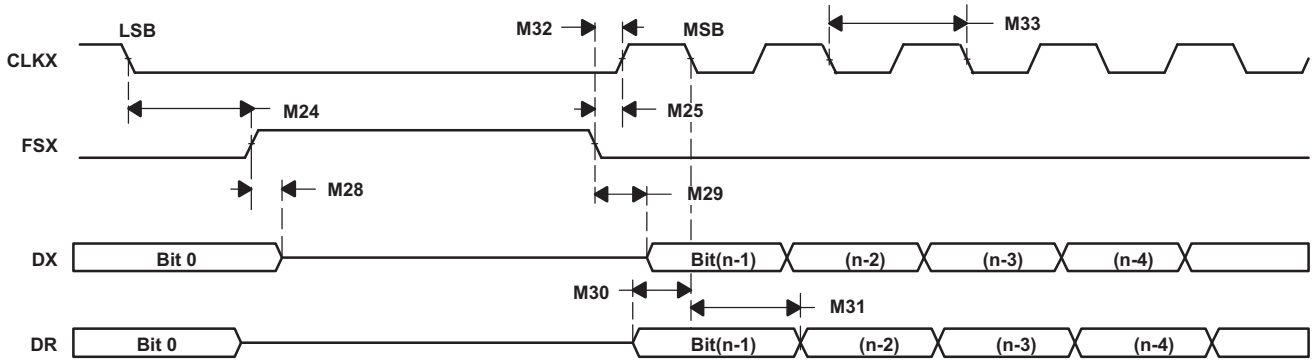

Figure 6-44. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0

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Table 6-56. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 0)

NO.			MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M39	$t_{su(DRV-CKXH)}$	Setup time, DR valid before CLKX high	30		8P – 10		ns
M40	$t_{h(CKXH-DRV)}$	Hold time, DR valid after CLKX high	1		8P – 10		ns
M41	$t_{su(FXL-CKXH)}$	Setup time, FSX low before CLKX high			16P + 10		ns
M42	$t_{c(CKX)}$	Cycle time, CLKX	2P (1)		16P		ns

(1) 2P = 1/CLKG

Table 6-57. McBSP as SPI Master or Slave Switching Characteristics Over Recommended Operating Conditions (Unless Otherwise Noted) (CLKSTP = 11b, CLKXP = 0)

NO.	PARAMETER		MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M34	$t_{h(CKXL-FXL)}$	Hold time, FSX low after CLKX low	P				ns
M35	$t_{d(FXL-CKXH)}$	Delay time, FSX low to CLKX high	2P (1)				ns
M37	$t_{dis(CKXL-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX low	P + 6		7P + 6		ns
M38	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	6		4P + 6		ns

(1) 2P = 1/CLKG

For all SPI slave modes, CLKX must be a minimum of 8 CLKG cycles. Also, CLKG should be LSPCLK/2 by setting CLKSM = CLKGDV = 1. With a maximum LSPCLK speed of 75 MHz, CLKX maximum frequency is LSPCLK/16; that is, 4.6875 MHz and P = 13.3 ns.

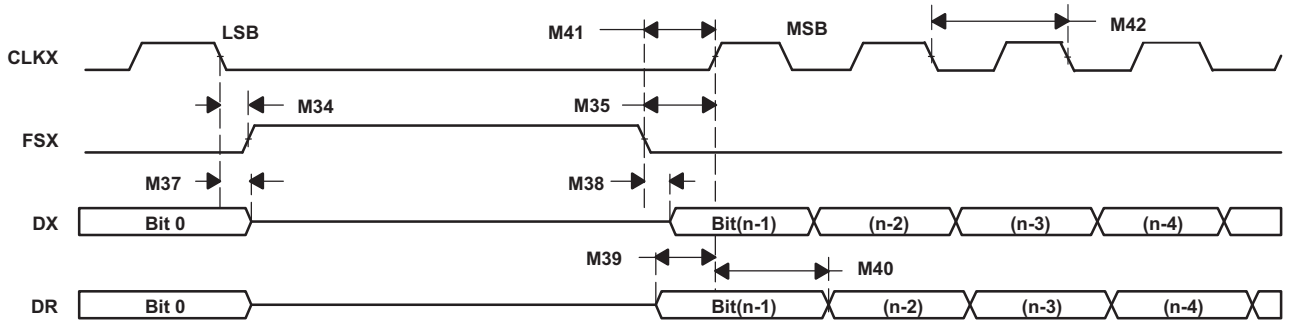

Figure 6-45. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0

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Table 6-58. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 1)

NO.			MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M49	$t_{su(DRV-CKXH)}$	Setup time, DR valid before CLKX high	30		8P – 10		ns
M50	$t_{h(CKXH-DRV)}$	Hold time, DR valid after CLKX high	1		8P – 10		ns
M51	$t_{su(FXL-CKXL)}$	Setup time, FSX low before CLKX low			8P + 10		ns
M52	$t_{c(CKX)}$	Cycle time, CLKX	2P (1)		16P		ns

(1) 2P = 1/CLKG

Table 6-59. McBSP as SPI Master or Slave Switching Characteristics Over Recommended Operating Conditions (Unless Otherwise Noted) (CLKSTP = 10b, CLKXP = 1)

NO.	PARAMETER		MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M43	$t_{h(CKXH-FXL)}$	Hold time, FSX low after CLKX high	2P (1)				ns
M44	$t_{d(FXL-CKXL)}$	Delay time, FSX low to CLKX low	P				ns
M47	$t_{dis(FXH-DXHZ)}$	Disable time, DX high impedance following last data bit from FSX high	6		6P + 6		ns
M48	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	6		4P + 6		ns

(1) 2P = 1/CLKG

For all SPI slave modes, CLKX must be a minimum of 8 CLKG cycles. Also, CLKG should be LSPCLK/2 by setting CLKSM = CLKGDV = 1. With maximum LSPCLK speed of 75 MHz, CLKX maximum frequency will be LSPCLK/16; that is, 4.6875 MHz and P = 13.3 ns.

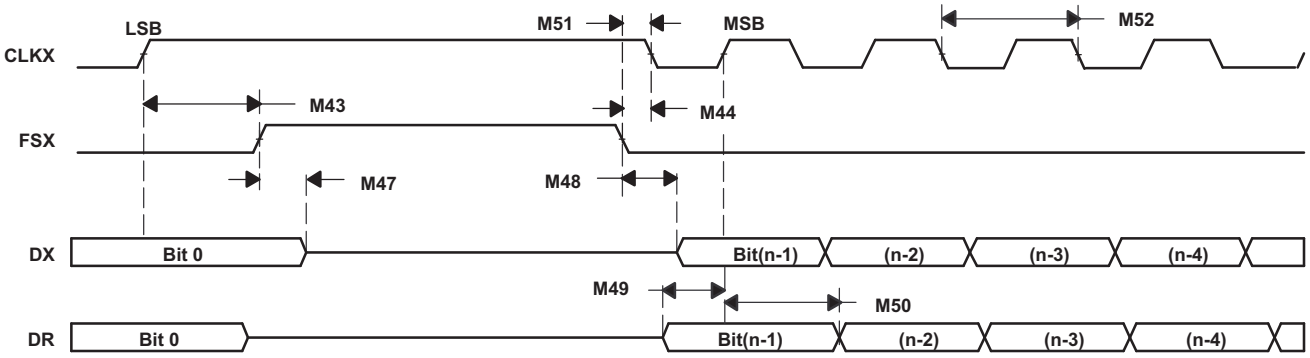

Figure 6-46. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1

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Table 6-60. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 1)

NO.			MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M58	$t_{su(DRV-CKXL)}$	Setup time, DR valid before CLKX low	30		8P – 10		ns
M59	$t_{h(CKXL-DRV)}$	Hold time, DR valid after CLKX low	1		8P – 10		ns
M60	$t_{su(FXL-CKXL)}$	Setup time, FSX low before CLKX low			16P + 10		ns
M61	$t_{c(CKX)}$	Cycle time, CLKX	2P (1)		16P		ns

(1) 2P = 1/CLKG

Table 6-61. McBSP as SPI Master or Slave Switching Characteristics Over Recommended Operating Conditions (Unless Otherwise Noted) (CLKSTP = 11b, CLKXP = 1)(1)

NO.	PARAMETER		MASTER(2)		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M53	$t_{h(CKXH-FXL)}$	Hold time, FSX low after CLKX high	P				ns
M54	$t_{d(FXL-CKXL)}$	Delay time, FSX low to CLKX low	2P (1)				ns
M55	$t_{d(CLKXH-DXV)}$	Delay time, CLKX high to DX valid	–2	0	3P + 6	5P + 20	ns
M56	$t_{dis(CKXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high	P + 6		7P + 6		ns
M57	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	6		4P + 6		ns

(1) 2P = 1/CLKG
(2) C = CLKX low pulse width = P
D = CLKX high pulse width = P

For all SPI slave modes, CLKX must be a minimum of 8 CLKG cycles. Also CLKG should be LSPCLK/2 by setting CLKSM = CLKGDV = 1. With maximum LSPCLK speed of 75 MHz, CLKX maximum frequency is LSPCLK/16 , that is 4.6875 MHz and P = 13.3 ns.

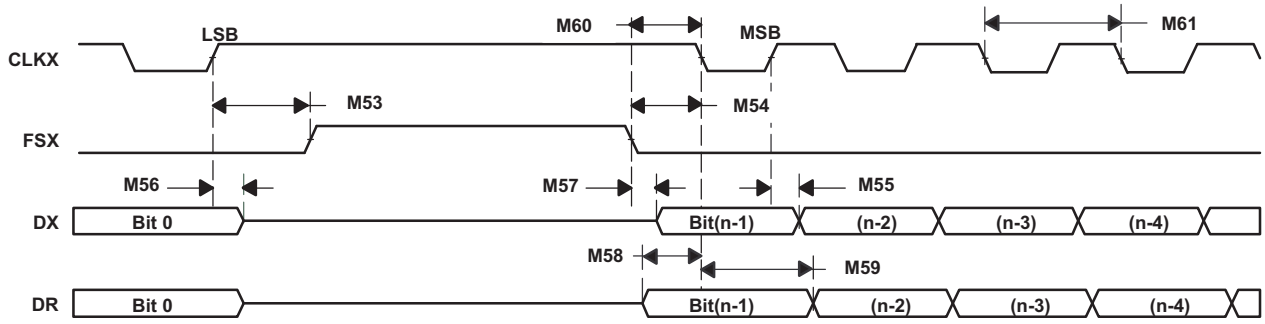

Figure 6-47. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1

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6.10.5 Universal Serial Bus Controller

The USB controller operates as a full-speed or low-speed function controller during point-to-point communications with USB host or device functions.

The USB module has the following features:

- USB 2.0 full-speed (12 Mbps) and low-speed (1.5 Mbps) operation
- Integrated PHY
- Four transfer types: control, interrupt, bulk, and isochronous
- 32 endpoints
  - One dedicated control IN endpoint and one dedicated control OUT endpoint
  - 15 configurable IN endpoints and 15 configurable OUT endpoints
- Four KB dedicated endpoint memory: one endpoint may be defined for double-buffered 1023-byte isochronous packet size
- Efficient transfers using DMA controller
  - Separate channels for transmit and receive for up to three IN endpoints and three OUT endpoints
  - Channel requests asserted when FIFO contains required amount of data

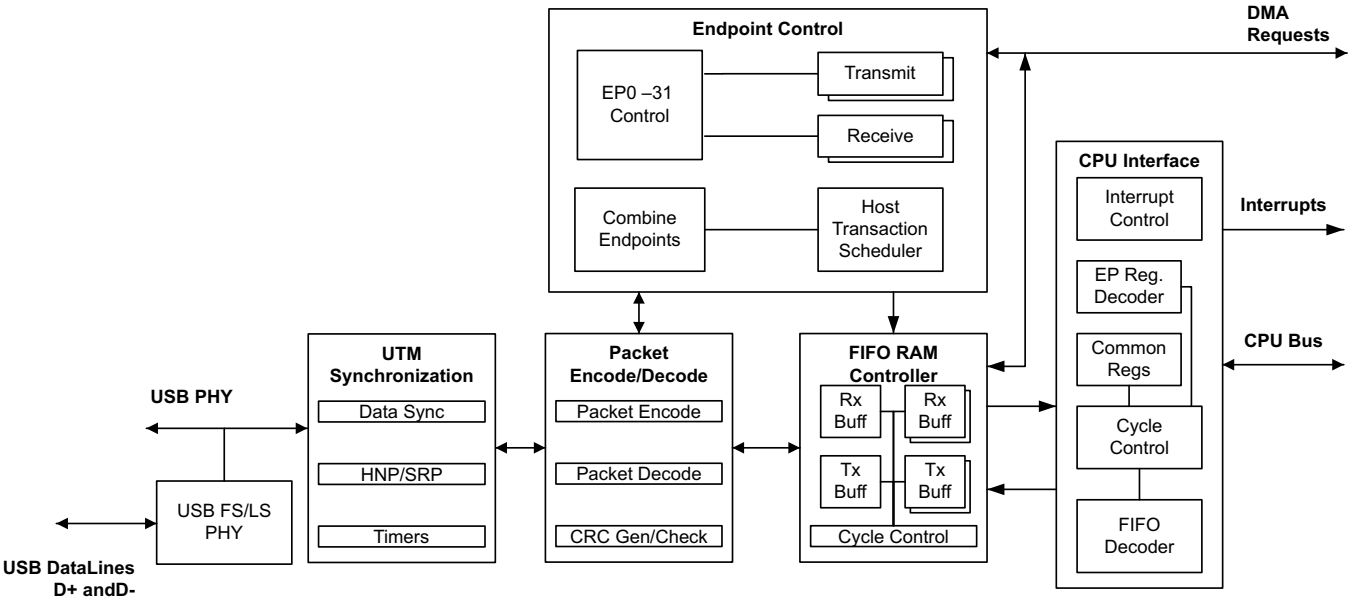

Figure 6-48. USB Block Diagram

NOTE

The accuracy of the on-chip zero-pin oscillator (Table 5-14, Internal Oscillator Electrical Characteristics) will not meet the accuracy requirements of the USB protocol. An external clock source must be used for applications using USB. For applications using the USB boot mode, see Section 6.6.5 (Boot ROM and Peripheral Booting) for clock frequency requirements.

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6.10.5.1 USB Electrical Data and Timing

Table 6-62. USB Input Ports DP and DM Timing Requirements

		MIN	MAX	UNIT
V(CM)	Differential input common mode range	0.8	2.5	V
Z(IN)	Input impedance	300		kΩ
VCRS	Crossover voltage	1.3	2.0	V
V_{IL}	Static SE input logic-low level	0.8		V
V_{IH}	Static SE input logic-high level		2.0	V
VDI	Differential input voltage		0.2	V

Table 6-63. USB Output Ports DP and DM Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	D+, D– single-ended	USB 2.0 load conditions	2.8	3.6	V
V_{OL}	D+, D– single-ended	USB 2.0 load conditions	0	0.3	V
Z(DRV)	D+, D– impedance		28	44	Ω
t_r	Rise time	Full speed, differential, C_L = 50 pF, 10%/90%, Rpu on D+	4	20	ns
t_f	Fall time	Full speed, differential, C_L = 50 pF, 10%/90%, Rpu on D+	4	20	ns

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6.10.6 Controller Area Network

The CAN module implements the following features:

- Complies with ISO11898-1 (Bosch® CAN protocol specification 2.0 A and B)
- Bit rates up to 1 MBit/s
- Multiple clock sources
- 32 message objects, each with the following properties:
  - Configurable as receive or transmit
  - Configurable with standard or extended identifier
  - Programmable receive and identifier masks for each object
  - Supports data and remote frames
  - Holds 0 to 8 bytes of data
  - Parity-checked configuration and data RAM
- Individual identifier mask for each message object
- Programmable FIFO mode for receive message objects
- Programmable loop-back modes for self-test operation
- Suspend mode for debug support
- Software module reset
- Automatic bus on after Bus-Off state by a programmable 32-bit timer
- Message RAM parity check mechanism
- Two interrupt lines
- Global power down and wakeup support

NOTE

For a CANx Bit-CLK of 200 MHz, the smallest bit rate possible is 7.8125 kbps.

NOTE

The accuracy of the on-chip zero-pin oscillator is in Table 5-14, Internal Oscillator Electrical Characteristics. Depending on parameters such as bit rate, bus length, and propagation delay, the accuracy of this oscillator may not meet the requirements of the CAN protocol. In this situation, an external clock source must be used.

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6.10.7 External Memory Interface

The EMIF provides a means of connecting the CPU to various external storage devices like asynchronous memories (SRAM, NOR flash) or synchronous memory (SDRAM).

6.10.7.1 Asynchronous Memory Support

The EMIF supports asynchronous memories:

- SRAMs
- NOR Flash memories

There is an external wait input that allows slower asynchronous memories to extend the memory access. The EMIF module supports up to three chip selects (EMIF_CS[4:2]). Each chip select has the following individually programmable attributes:

- Data bus width
- Read cycle timings: setup, hold, strobe
- Write cycle timings: setup, hold, strobe
- Bus turnaround time
- Extended wait option with programmable timeout
- Select strobe option

6.10.7.2 Synchronous DRAM Support

The EMIF memory controller is compliant with the JESD21-C SDR SDRAMs that use a 32-bit or 16-bit data bus. The EMIF has a single SDRAM chip select (EMIF_CS[0]).

The address space of the EMIF, for the synchronous memory (SDRAM), lies beyond the 22-bit range of the program address bus and can only be accessed through the data bus, which places a restriction on the C compiler being able to work effectively on data in this space. Therefore, when using SDRAM, the user is advised to copy data (using the DMA) from external memory to RAM before working on it. See the examples in controlSUITE™ (CONTROLSUITE) and the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual* (SPRUHM8).

SDRAM configurations supported are:

- One-bank, two-bank, and four-bank SDRAM devices
- Devices with eight, nine, ten, and eleven column addresses
- CAS latency of two or three clock cycles
- 16-bit/32-bit data bus width
- 3.3-V LVCMOS interface

Additionally, the EMIF supports placing the SDRAM in self-refresh and power-down modes. Self-refresh mode allows the SDRAM to be put in a low-power state while still retaining memory contents because the SDRAM will continue to refresh itself even without clocks from the microcontroller. Power-down mode achieves even lower power, except the microcontroller must periodically wake up and issue refreshes if data retention is required. Note that the EMIF module does not support mobile SDRAM devices.

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6.10.7.3 EMIF Electrical Data and Timing

6.10.7.3.1 Asynchronous RAM

Table 6-64. EMIF Asynchronous Memory Timing Requirements

NO.			MIN	MAX	UNIT
Reads and Writes					
	E	EMIF clock period	SYSCLK period		ns
2	$t_{w(EM_WAIT)}$	Pulse duration, EMxWAIT assertion and deassertion	2E		ns
Reads					
12	$t_{su(EMDV-EMOEH)}$	Setup time, EMxD[y:0] valid before $\overline{EMxOE}$ high	15		ns
13	$t_{h(EMOEH-EMDIV)}$	Hold time, EMxD[y:0] valid after $\overline{EMxOE}$ high	0		ns
14	$t_{su(EMOEL-EMWAIT)}$	Setup Time, EMxWAIT asserted before end of Strobe Phase (1)	4E		ns
Writes					
28	$t_{su(EMWEL-EMWAIT)}$	Setup Time, EMxWAIT asserted before end of Strobe Phase (1)	4E		ns

(1) Setup before end of STROBE phase (if no extended wait states are inserted) by which EMxWAIT must be asserted to add extended wait states. Figure 6-50 and Figure 6-52 describe EMIF transactions that include extended wait states inserted during the STROBE phase. However, cycles inserted as part of this extended wait period should not be counted; the 4E requirement is to the start of where the HOLD phase would begin if there were no extended wait cycles.

Table 6-65. EMIF Asynchronous Memory Switching Characteristics (1) (2) (3)

NO.	PARAMETER		MIN	MAX	UNIT
Reads and Writes					
1	$t_{d(TURNAROUND)}$	Turn around time	(TA)*E–3	(TA)*E+2	ns
Reads					
3	$t_{c(EMRCYCLE)}$	EMIF read cycle time (EW = 0)	(RS+RST+RH+2)*E–3	(RS+RST+RH+2)*E+2	ns
		EMIF read cycle time (EW = 1)	(RS+RST+RH+2+ (EWC*16))*E–3	(RS+RST+RH+2+ (EWC*16))*E+2	ns
4	$t_{su(EMCEL-EMOEL)}$	Output setup time, $\overline{EMxCS[y:2]}$ low to $\overline{EMxOE}$ low (SS = 0)	(RS)*E–3	(RS)*E+2	ns
		Output setup time, $\overline{EMxCS[y:2]}$ low to $\overline{EMxOE}$ low (SS = 1)	–3	2	ns
5	$t_{h(EMOEH-EMCEH)}$	Output hold time, $\overline{EMxOE}$ high to $\overline{EMxCS[y:2]}$ high (SS = 0)	(RH)*E–3	(RH)*E	ns
		Output hold time, $\overline{EMxOE}$ high to $\overline{EMxCS[y:2]}$ high (SS = 1)	–3	0	ns
6	$t_{su(EMBAV-EMOEL)}$	Output setup time, EMxBA[y:0] valid to $\overline{EMxOE}$ low	(RS)*E–3	(RS)*E+2	ns
7	$t_{h(EMOEH-EMBAIV)}$	Output hold time, $\overline{EMxOE}$ high to EMxBA[y:0] invalid	(RH)*E–3	(RH)*E	ns
8	$t_{su(EMAV-EMOEL)}$	Output setup time, EMxA[y:0] valid to $\overline{EMxOE}$ low	(RS)*E–3	(RS)*E+2	ns
9	$t_{h(EMOEH-EMAIV)}$	Output hold time, $\overline{EMxOE}$ high to EMxA[y:0] invalid	(RH)*E–3	(RH)*E	ns

(1) TA = Turn around, RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold, MEWC = Maximum external wait cycles. These parameters are programmed via the Asynchronous Bank and Asynchronous Wait Cycle Configuration Registers. These support the following ranges of values: TA[4–1], RS[16–1], RST[64–4], RH[8–1], WS[16–1], WST[64–1], WH[8–1], and MEWC[1–256]. See the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual* (SPRUHM8) for more information.
(2) E = EMxCLK period in ns.
(3) EWC = external wait cycles determined by EMxWAIT input signal. EWC supports the following range of values. EWC[256–1]. Note that the maximum wait time before timeout is specified by bit field MEWC in the Asynchronous Wait Cycle Configuration Register. See the *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual* (SPRUHM8) for more information.

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Table 6-65. EMIF Asynchronous Memory Switching Characteristics[1][2][3] (continued)

NO.	PARAMETER		MIN	MAX	UNIT
10	$t_{w(EMOEL)}$	$\overline{EMxOE}$ active low width (EW = 0)	(RST)*E–1	(RST)*E+1	ns
		$\overline{EMxOE}$ active low width (EW = 1)	(RST+(EWC*16))*E–1	(RST+(EWC*16))*E+1	ns
11	$t_{d(EMWAITH-EMOEH)}$	Delay time from EMxWAIT deasserted to $\overline{EMxOE}$ high	3E+8	4E+10	ns
29	$t_{su(EMDQMV-EMOEL)}$	Output setup time, EMxDQM[y:0] valid to $\overline{EMxOE}$ low	(RS)*E–3	(RS)*E+2	ns
30	$t_{h(EMOEH-EMDQMIV)}$	Output hold time, $\overline{EMxOE}$ high to EMxDQM[y:0] invalid	(RH)*E–3	(RH)*E	ns
Writes					
15	$t_{c(EMWCYCLE)}$	EMIF write cycle time (EW = 0)	(WS+WST+WH+2)*E–3	(WS+WST+WH+2)*E+1	ns
		EMIF write cycle time (EW = 1)	(WS+WST+WH+2+ (EWC*16))*E–3	(WS+WST+WH+2+ (EWC*16))*E+1	ns
16	$t_{su(EMCEL-EMWEL)}$	Output setup time, $\overline{EMxCS[y:2]}$ low to $\overline{EMxWE}$ low (SS = 0)	(WS)*E–3	(WS)*E+1	ns
		Output setup time, $\overline{EMxCS[y:2]}$ low to $\overline{EMxWE}$ low (SS = 1)	–3	1	ns
17	$t_{h(EMWEH-EMCEH)}$	Output hold time, $\overline{EMxWE}$ high to $\overline{EMxCS[y:2]}$ high (SS = 0)	(WH)*E–3	(WH)*E	ns
		Output hold time, $\overline{EMxWE}$ high to $\overline{EMxCS[y:2]}$ high (SS = 1)	–3	0	ns
18	$t_{su(EMDQMV-EMWEL)}$	Output setup time, EMxDQM[y:0] valid to $\overline{EMxWE}$ low	(WS)*E–3	(WS)*E+1	ns
19	$t_{h(EMWEH-EMDQMIV)}$	Output hold time, $\overline{EMxWE}$ high to EMxDQM[y:0] invalid	(WH)*E–3	(WH)*E	ns
20	$t_{su(EMBAV-EMWEL)}$	Output setup time, EMxBA[y:0] valid to $\overline{EMxWE}$ low	(WS)*E–3	(WS)*E+1	ns
21	$t_{h(EMWEH-EMBAIV)}$	Output hold time, $\overline{EMxWE}$ high to EMxBA[y:0] invalid	(WH)*E–3	(WH)*E	ns
22	$t_{su(EMAV-EMWEL)}$	Output setup time, EMxA[y:0] valid to $\overline{EMxWE}$ low	(WS)*E–3	(WS)*E+1	ns
23	$t_{h(EMWEH-EMAIV)}$	Output hold time, $\overline{EMxWE}$ high to EMxA[y:0] invalid	(WH)*E–3	(WH)*E	ns
24	$t_{w(EMWEL)}$	$\overline{EMxWE}$ active low width (EW = 0)	(WST)*E–1	(WST)*E+1	ns
		$\overline{EMxWE}$ active low width (EW = 1)	(WST+(EWC*16))*E–1	(WST+(EWC*16))*E+1	ns
25	$t_{d(EMWAITH-EMWEH)}$	Delay time from EMxWAIT deasserted to $\overline{EMxWE}$ high	3E+8	4E+10	ns
26	$t_{su(EMDV-EMWEL)}$	Output setup time, EMxD[y:0] valid to $\overline{EMxWE}$ low	(WS)*E–3	(WS)*E+1	ns
27	$t_{h(EMWEH-EMDIV)}$	Output hold time, $\overline{EMxWE}$ high to EMxD[y:0] invalid	(WH)*E–3	(WH)*E	ns

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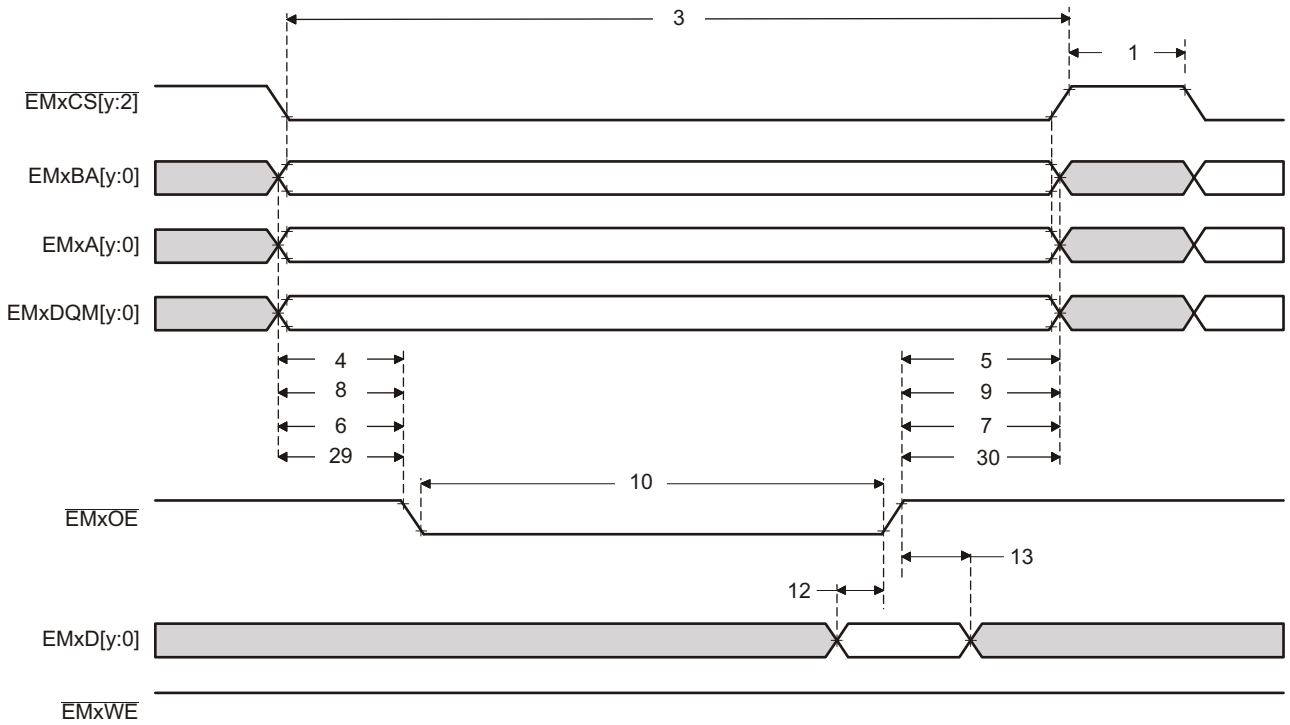

Figure 6-49. Asynchronous Memory Read Timing

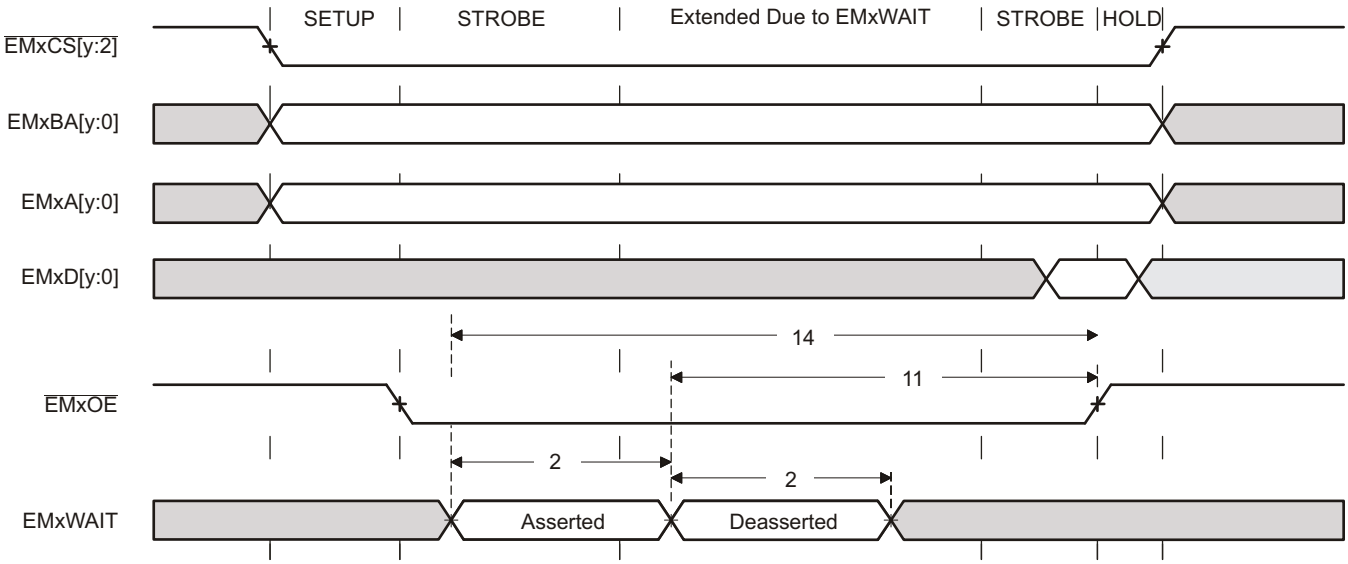

Figure 6-50. EMxWAIT Read Timing Requirements

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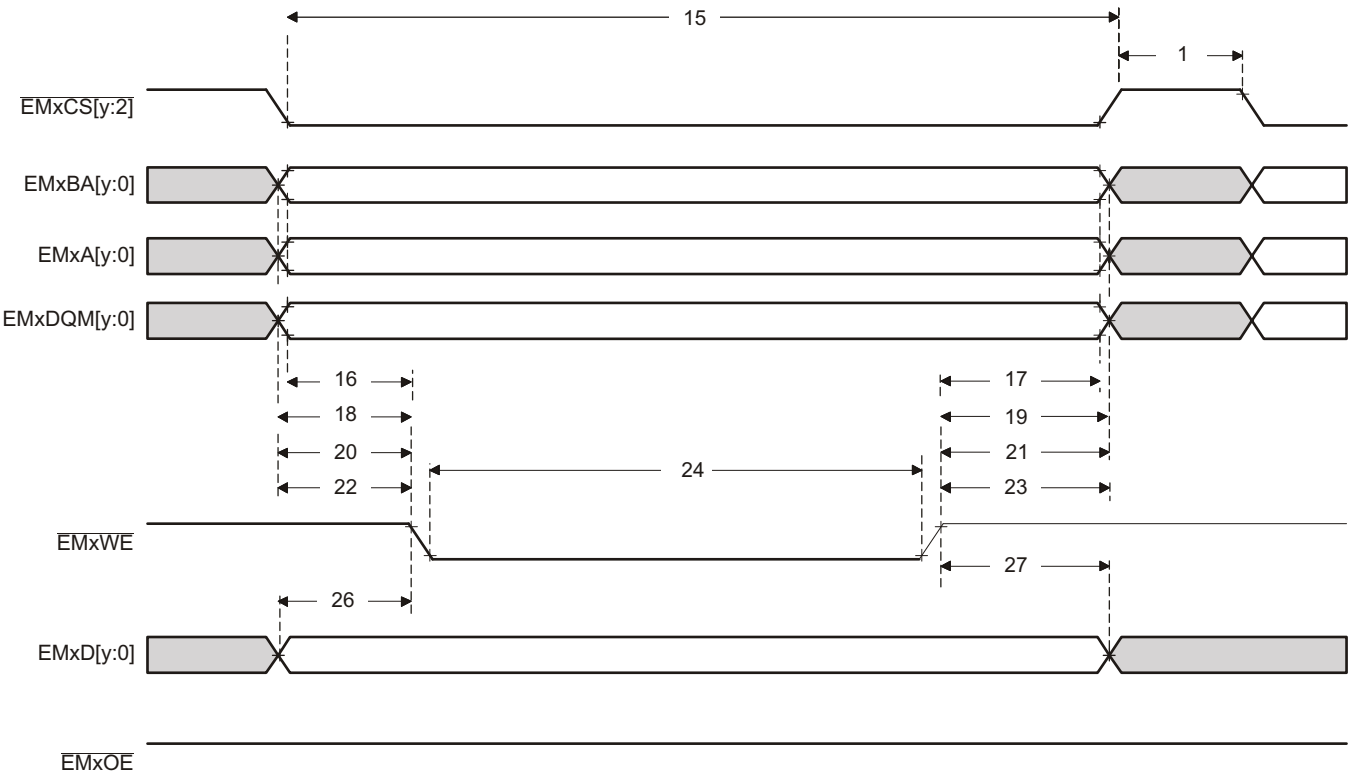

Figure 6-51. Asynchronous Memory Write Timing

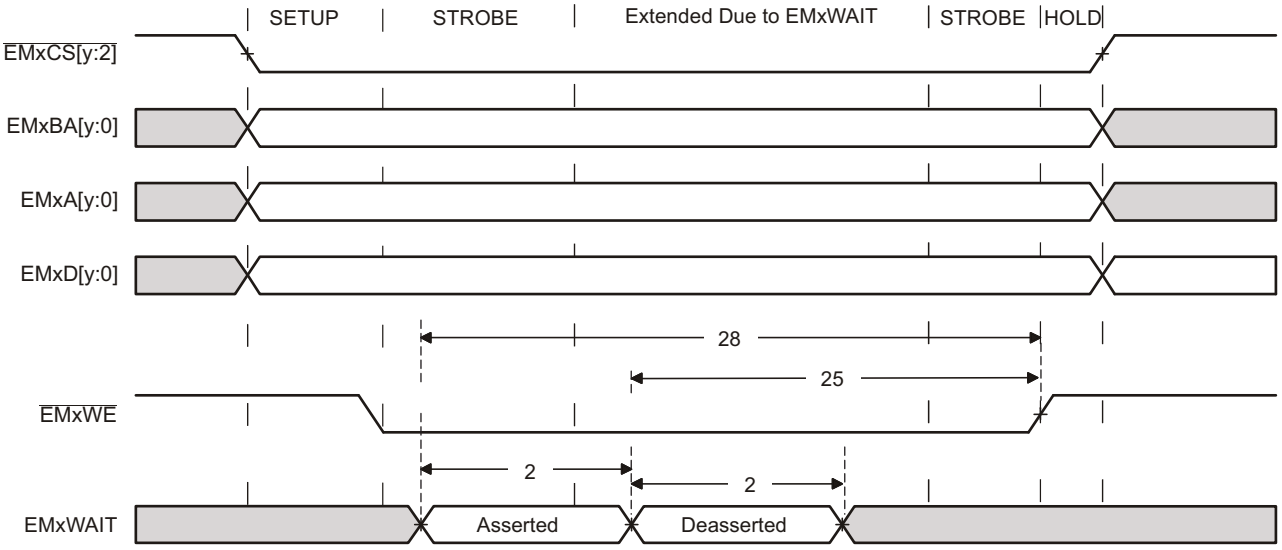

Figure 6-52. EMxWAIT Write Timing Requirements

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6.10.7.3.2 Synchronous RAM

Table 6-66. EMIF Synchronous Memory Timing Requirements

NO.			MIN	MAX	UNIT
19	$t_{su(EMIFDV-EM_CLKH)}$	Input setup time, read data valid on EMxD[y:0] before EMxCLK rising	2		ns
20	$t_{h(CLKH-DIV)}$	Input hold time, read data valid on EMxD[y:0] after EMxCLK rising	1.5		ns

Table 6-67. EMIF Synchronous Memory Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{c(CLK)}$	Cycle time, EMIF clock EMxCLK	10		ns
2	$t_{w(CLK)}$	Pulse width, EMIF clock EMxCLK high or low	3		ns
3	$t_{d(CLKH-CSV)}$	Delay time, EMxCLK rising to $\overline{\text{EMxCS}}$[y:2] valid		8	ns
4	$t_{oh(CLKH-CSIV)}$	Output hold time, EMxCLK rising to $\overline{\text{EMxCS}}$[y:2] invalid	1		ns
5	$t_{d(CLKH-DQMV)}$	Delay time, EMxCLK rising to EMxDQM[y:0] valid		8	ns
6	$t_{oh(CLKH-DQMIV)}$	Output hold time, EMxCLK rising to EMxDQM[y:0] invalid	1		ns
7	$t_{d(CLKH-AV)}$	Delay time, EMxCLK rising to EMxA[y:0] and EMxBA[y:0] valid		8	ns
8	$t_{oh(CLKH-AIV)}$	Output hold time, EMxCLK rising to EMxA[y:0] and EMxBA[y:0] invalid	1		ns
9	$t_{d(CLKH-DV)}$	Delay time, EMxCLK rising to EMxD[y:0] valid		8	ns
10	$t_{oh(CLKH-DIV)}$	Output hold time, EMxCLK rising to EMxD[y:0] invalid	1		ns
11	$t_{d(CLKH-RASV)}$	Delay time, EMxCLK rising to EMxRAS valid		8	ns
12	$t_{oh(CLKH-RASIV)}$	Output hold time, EMxCLK rising to EMxRAS invalid	1		ns
13	$t_{d(CLKH-CASV)}$	Delay time, EMxCLK rising to EMxCAS valid		8	ns
14	$t_{oh(CLKH-CASIV)}$	Output hold time, EMxCLK rising to EMxCAS invalid	1		ns
15	$t_{d(CLKH-WEV)}$	Delay time, EMxCLK rising to $\overline{\text{EMxWE}}$ valid		8	ns
16	$t_{oh(CLKH-WEIV)}$	Output hold time, EMxCLK rising to $\overline{\text{EMxWE}}$ invalid	1		ns
17	$t_{d(CLKH-DHZ)}$	Delay time, EMxCLK rising to EMxD[y:0] tri-stated		8	ns
18	$t_{oh(CLKH-DLZ)}$	Output hold time, EMxCLK rising to EMxD[y:0] driving	1		ns

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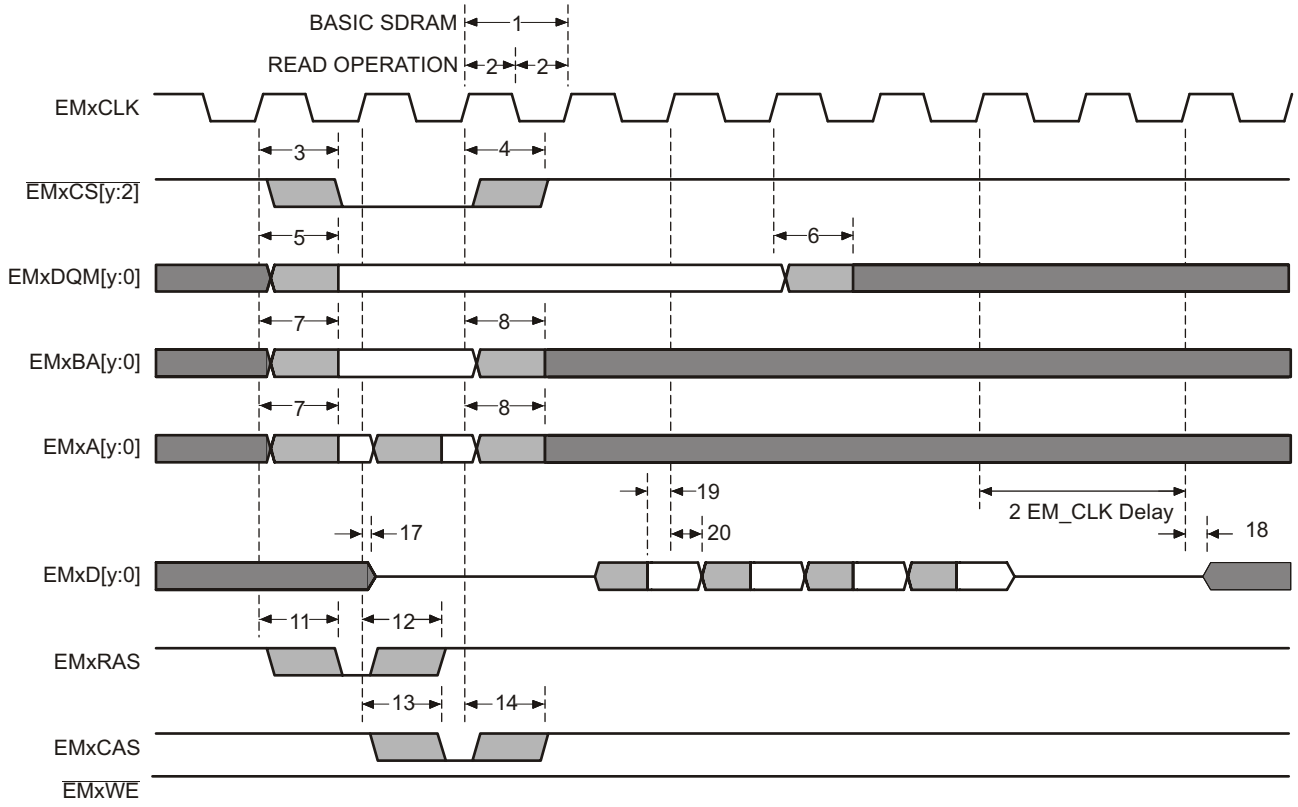

Figure 6-53. Basic SDRAM Read Operation

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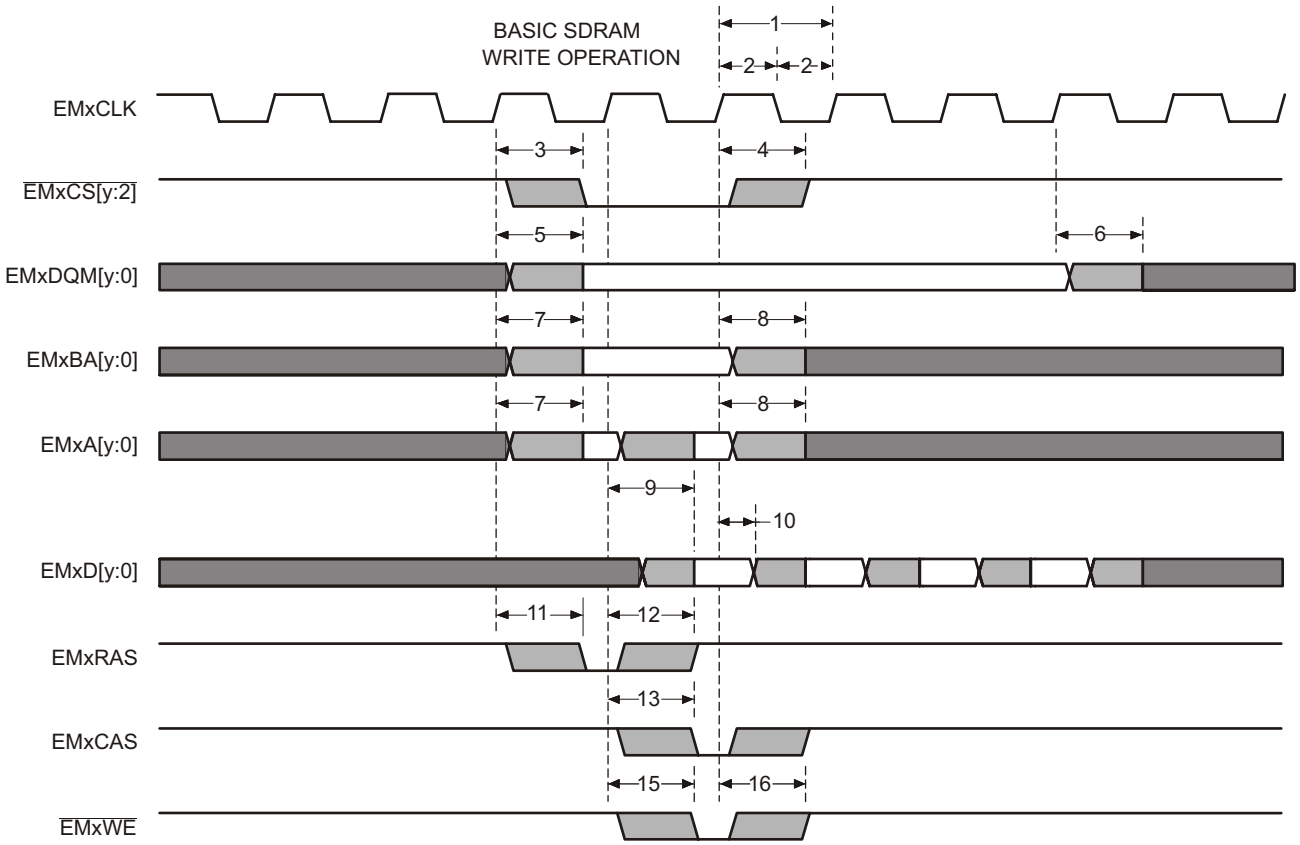

Figure 6-54. Basic SDRAM Write Operation

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7 Device and Documentation Support

7.1 Device Support

7.1.1 Development Support

Texas Instruments (TI) offers an extensive line of development tools for the C28x family of MCUs, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development:

Software Development Tools

- Code Composer Studio™ (CCS) Integrated Development Environment (IDE)
  - C/C++ Compiler
  - Code generation tools
  - Assembler/Linker
  - Cycle Accurate Simulator
  - FPU and VCU Optimized Libraries
  - TMU native compiler support
- Application algorithms
- Sample applications code

Hardware Development Tools

- Development and evaluation boards
- JTAG-based emulators - XDS510™ class, XDS560™ emulator, XDS100v2, XDS200
- Flash programming tools

For a complete listing of development-support tools for the processor platform, visit the Texas Instruments website at www.ti.com. For technical questions, visit http://e2e.ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

7.1.1.1 Getting Started and Next Steps

This section gives a brief overview on how to get started with the TMS320F2837xD devices.

Development tools:

- F28377D Delfino Experimenter Kit (TMDXDOCK28377D)
- F28377D Delfino controlCARD (TMDXCNCD28377D)

Software tools:

- controlSUITE (CONTROLSUITE)
- Code Composer Studio (CCS) Integrated Development Environment (IDE) (CCSTUDIO)
- Pin Mux Utility for ARM® and F2837xD Microcontrollers (PINMUXTOOL)
- F021 Flash API (F021FLASHAPI)

Useful documentation:

- *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual* (SPRUHM8)
- *Getting Started With TMS320C28x Digital Signal Controllers Application Report* (SPRAAM0)

Training:

- F2837xD Workshop

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7.1.2 Device and Development Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320™ MCU devices and support tools. Each TMS320 MCU commercial family member has one of three prefixes: TMX, TMP, or TMS (for example, **TMS**320F28377D). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (with TMX for devices and TMDX for tools) through fully qualified production devices and tools (with TMS for devices and TMDS for tools).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

TMS Fully qualified production device

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing

TMDS Fully qualified development-support product

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer: "Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PTP) and temperature range (for example, S). Figure 7-1 provides a legend for reading the complete device name for any family member.

For device part numbers and further ordering information, see the TI website (www.ti.com) or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the *TMS320F28377D, TMS320F28376D, TMS320F28375D, TMS320F28374D Dual-Core Delfino Microcontrollers Silicon Errata* (SPRZ412).

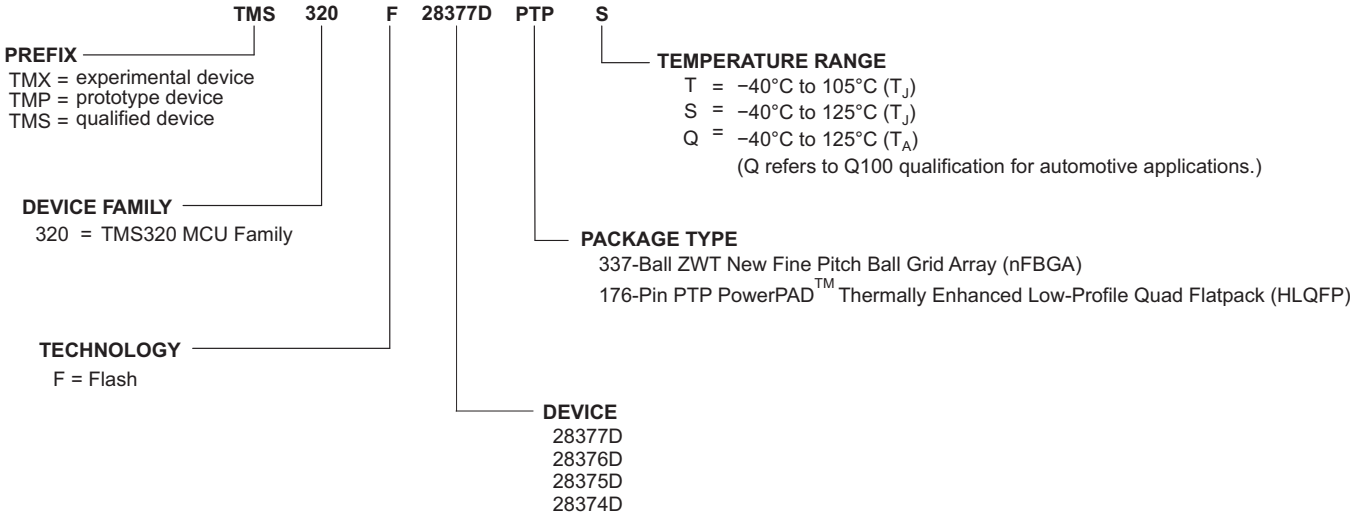

Figure 7-1. Device Nomenclature

ADVANCE INFORMATION

7.2 Documentation Support

Extensive documentation supports all of the TMS320 MCU family generations of devices from product announcement through applications development. The types of documentation available include: data sheets and data manuals, with design specifications; and hardware and software applications.

The following documents can be downloaded from the TI website (www.ti.com):

Data Manual and Errata

SPRS880 **TMS320F28377D, TMS320F28376D, TMS320F28375D, TMS320F28374D Dual-Core Delfino™ Microcontrollers Data Manual** contains the pinout, signal descriptions, as well as electrical and timing specifications.

SPRZ412 **TMS320F28377D, TMS320F28376D, TMS320F28375D, TMS320F28374D Dual-Core Delfino Microcontrollers Silicon Errata** describes known advisories on silicon and provides workarounds.

Technical Reference Manual

SPRUHM8 **TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual** details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the 2837xD microcontrollers.

CPU User's Guides

SPRU430 **TMS320C28x CPU and Instruction Set Reference Guide** describes the central processing unit (CPU) and the assembly language instructions of the TMS320C28x fixed-point digital signal processors (DSPs). This Reference Guide also describes emulation features available on these DSPs.

SPRUHS1 **TMS320C28x Extended Instruction Sets Reference Guide** describes the architecture, pipeline, and instruction set of the TMU, VCU-II, and FPU accelerators.

Peripheral Guides

SPRU566 **TMS320x28xx, 28xxx DSP Peripheral Reference Guide** describes the peripheral reference guides of the 28x DSPs.

Tools Guides

SPRU513 **TMS320C28x Assembly Language Tools v6.2.4 User's Guide** describes the assembly language tools (assembler and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the TMS320C28x device.

SPRU514 **TMS320C28x Optimizing C/C++ Compiler v6.2.4 User's Guide** describes the TMS320C28x C/C++ compiler. This compiler accepts ANSI standard C/C++ source code and produces TMS320 DSP assembly language source code for the TMS320C28x device.

SPRU608 **TMS320C28x Instruction Set Simulator Technical Overview** describes the simulator, available within the Code Composer Studio for TMS320C2000 IDE, that simulates the instruction set of the C28x core.

Application Reports

SZZA021 **Semiconductor Packing Methodology** describes the packing methodologies employed to prepare semiconductor devices for shipment to end users.

ADVANCE INFORMATION

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7.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 7-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TMS320F28377D	Click here	Click here	Click here	Click here	Click here
TMS320F28376D	Click here	Click here	Click here	Click here	Click here
TMS320F28375D	Click here	Click here	Click here	Click here	Click here
TMS320F28374D	Click here	Click here	Click here	Click here	Click here

7.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki ***Texas Instruments Embedded Processors Wiki.*** Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

7.5 Trademarks

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All other trademarks are the property of their respective owners.

7.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

ADVANCE INFORMATION

8 Mechanical Packaging and Orderable Information

8.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

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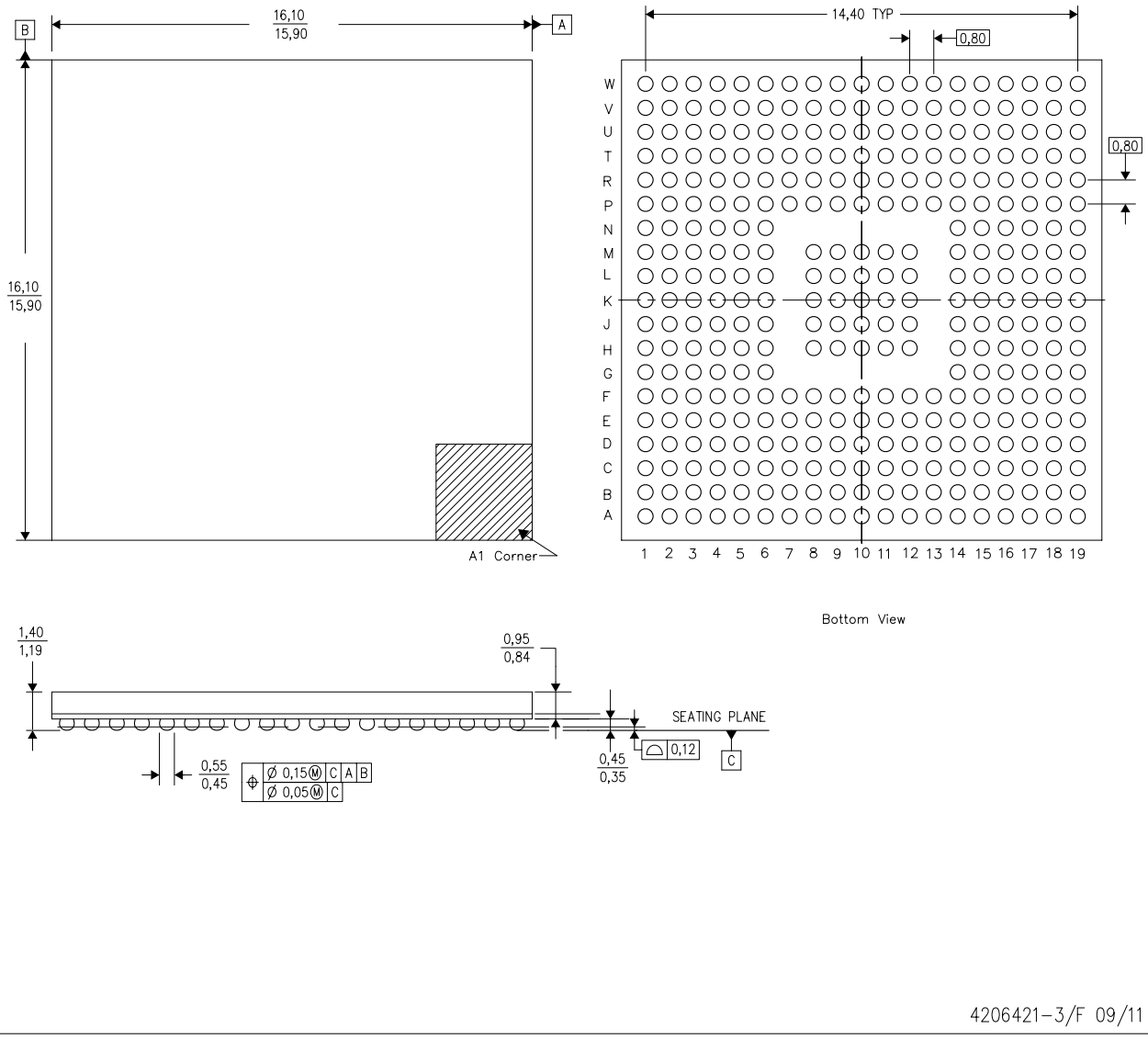
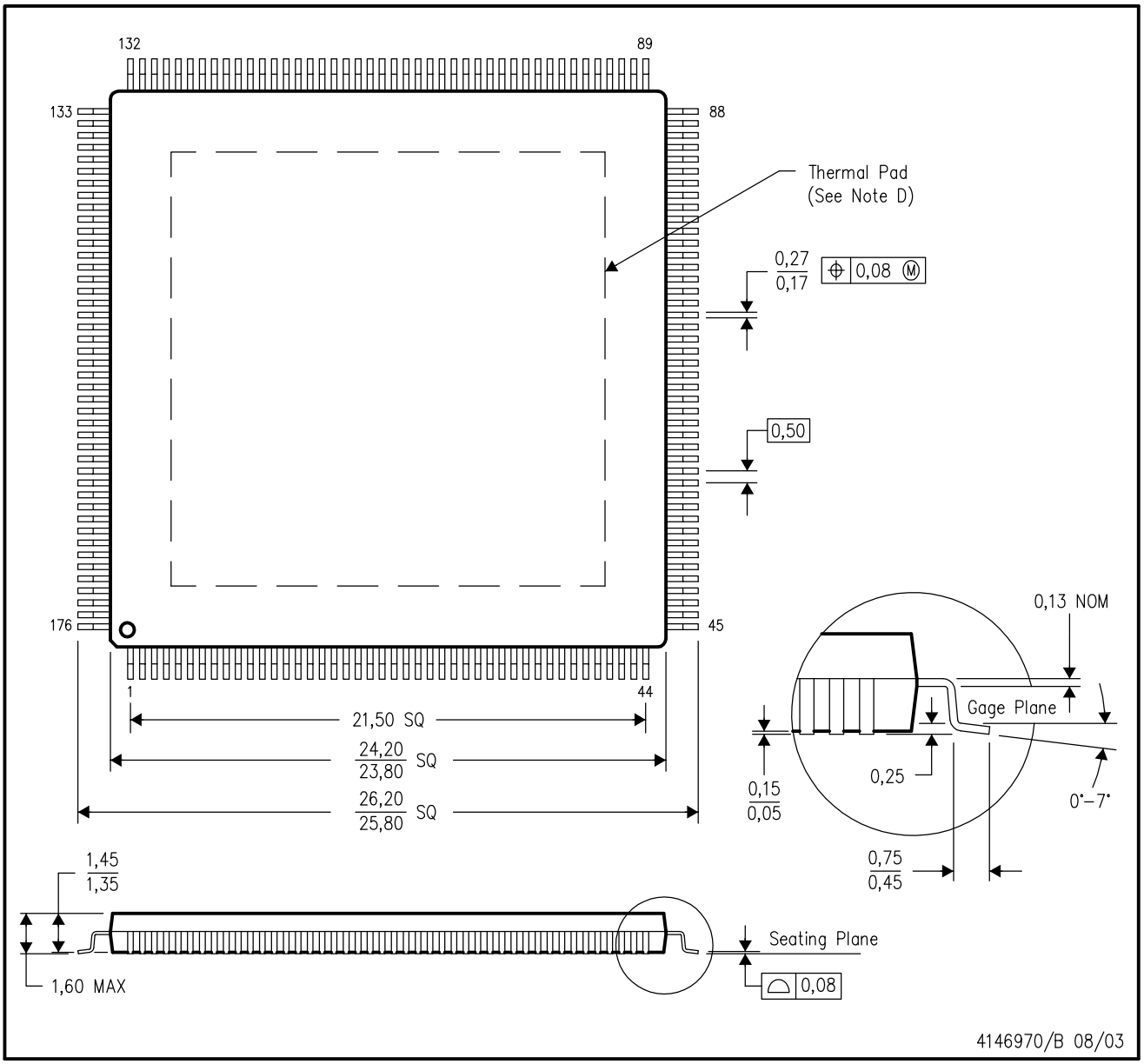
ZWT (S–PBGA–N337) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This is a Pb–free solder ball design.
D. Falls within JEDEC MO–275.

PTP (S–PQFP–G176) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–026

PowerPAD is a trademark of Texas Instruments.

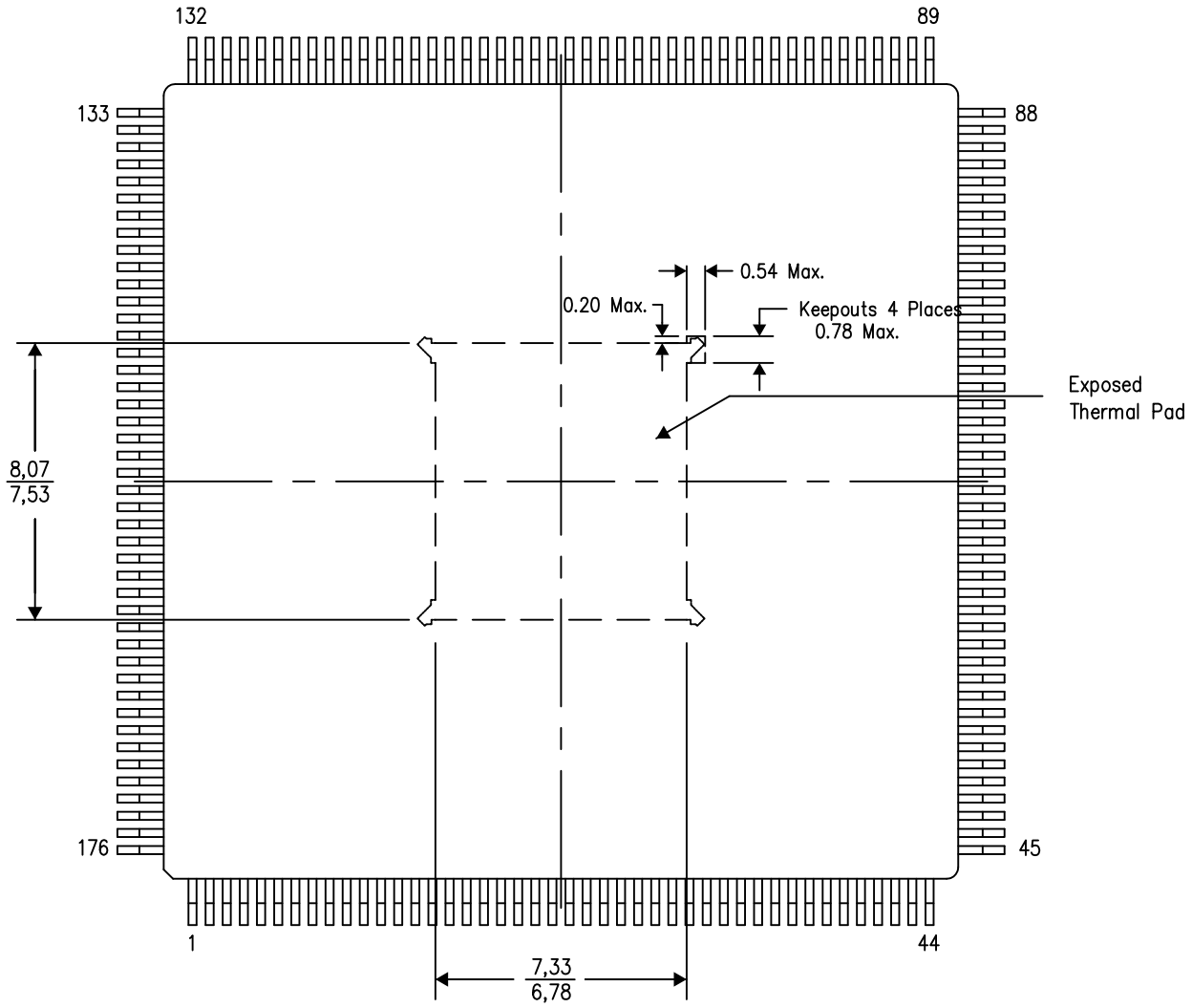
PTP (S–PQFP–G176) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions 4209350–8/F 04/13

NOTE: All linear dimensions are in millimeters

NOTE: Keep–out features are identified to prevent board routing interference. These exposed metal features may vary within the identified area or be completely absent on some devices.

PowerPAD is a trademark of Texas Instruments

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMS320F28374DPTPT	PREVIEW	HLQFP	PTP	176	40	TBD	Call TI	Call TI	-40 to 105		
TMS320F28375DPTPT	PREVIEW	HLQFP	PTP	176	40	TBD	Call TI	Call TI	-40 to 105		
TMS320F28376DPTPS	PREVIEW	HLQFP	PTP	176	40	TBD	Call TI	Call TI	-40 to 125		
TMS320F28376DPTPT	PREVIEW	HLQFP	PTP	176	40	TBD	Call TI	Call TI	-40 to 105		
TMS320F28376DZWTS	PREVIEW	NFBGA	ZWT	337	90	TBD	Call TI	Call TI	-40 to 125		
TMS320F28376DZWTT	PREVIEW	NFBGA	ZWT	337	90	TBD	Call TI	Call TI	-40 to 105		
TMS320F28377DPTPQ	PREVIEW	HLQFP	PTP	176	40	TBD	Call TI	Call TI	-40 to 125		
TMS320F28377DPTPS	PREVIEW	HLQFP	PTP	176	40	TBD	Call TI	Call TI	-40 to 125		
TMS320F28377DPTPT	PREVIEW	HLQFP	PTP	176	40	TBD	Call TI	Call TI	-40 to 105		
TMS320F28377DZWTQ	PREVIEW	NFBGA	ZWT	337	90	TBD	Call TI	Call TI	-40 to 125		
TMS320F28377DZWTS	PREVIEW	NFBGA	ZWT	337	90	TBD	Call TI	Call TI	-40 to 105		
TMS320F28377DZWTT	PREVIEW	NFBGA	ZWT	337	90	TBD	Call TI	Call TI	-40 to 105		
TMX320F28377DPTPT	ACTIVE	HLQFP	PTP	176	1	TBD	Call TI	Call TI	-40 to 105		Samples
TMX320F28377DZWTT	ACTIVE	NFBGA	ZWT	337	1	TBD	Call TI	Call TI	-40 to 105		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
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