

## TMS320F2837xD Dual-Core Delfino™ Microcontrollers

Check for Samples: [TMS320F28377D](#), [TMS320F28376D](#)

### 1 TMS320F2837xD Dual-Core Delfino MCUs

#### 1.1 Features

- **Dual-Core Architecture**
  - Two TMS320C28x™ 32-Bit CPUs
  - 200 MHz (5-ns Cycle Time)
  - IEEE 754 Single-Precision Floating-Point Unit (FPU)
  - Trigonometric Math Unit (TMU)
  - Viterbi/Complex Math Unit (VCU-II)
  - 16 x 16 and 32 x 32 MAC Operations
  - 16 x 16 Dual MAC
  - Three 32-Bit CPU Timers per Core
  - Harvard Bus Architecture
  - Fast Interrupt Response and Processing
  - Unified Memory Programming Model
- **Two Programmable Control Law Accelerators**
  - 200 MHz (5-ns Cycle Time)
  - 32-Bit Floating-Point Math Accelerator (IEEE 754 Single Precision)
  - Executes Code Independently of Main CPU
- **On-Chip Memory**
  - Up to 1MB Flash, Up to 204KB RAM
  - Boot ROM (64KB)
    - SPI, I<sup>2</sup>C, CAN, and Parallel I/O Software Boot Modes
    - Standard Math Tables
- **System Peripherals**
  - Dual 32- and 16-Bit EMIF With ASRAM and SDRAM Support
  - Dual 6-Channel DMA Controller
  - Up to 169 Individually Programmable, Multiplexed GPIO Pins With Input Filtering
- **Communications Peripherals**
  - USB 2.0 + PHY Port
  - Support for 12-Pin 3.3 V-Compatible Universal Parallel Port (uPP) Interface
  - Two CAN-Bus Ports (32 Mailboxes Each)
  - Three High-Speed (40-MHz) SPI Ports With 16-Level FIFO, DMA Support, and CLA-Accessible
  - Two Multichannel Buffered Serial Ports
  - Four Serial Communications Interfaces
  - Two Inter-Integrated Circuit (I<sup>2</sup>C) Interfaces
- **Analog Subsystem**
  - Four Dual-Mode Analog-to-Digital Converters
    - 16-Bit Mode
      - 1.1 MSPS Each (Up to 4.4-MSPS System)
      - Differential
      - External Reference
      - Up to 12 External Channels
    - 12-Bit Mode
      - 3.5 MSPS Each (Up to 14-MSPS System)
      - Single-Ended or Differential
      - External Reference
      - Up to 24 External Channels
  - Single Sample-and-Hold (S/H) (Four-Simultaneous-S/H System)
  - Integrated Post-Processing of ADC Conversions
    - Saturating Offset Calibration
    - Error From Setpoint Calculation
    - High, Low, and Zero-Crossing Compare, With Interrupt Capability
    - Trigger-to-Sample Delay Capture
  - Analog Comparator/Digital-to-Analog Converter (DAC) Subsystem With Glitch Filter, for Windowed Trip Monitor and PCMC Interfaces
    - Eight Windowed Comparators With 12-Bit DAC References
  - Three 12-Bit Buffered DAC Outputs
- **Enhanced Control Peripherals**
  - 24 PWM Channels With Enhanced Features
  - 16 High-Resolution PWM Channels
    - High-Resolution on Both A and B Channels of 8 PWM Modules
    - Dead-Band Support (on Both Standard and High-Resolution)
  - Six Capture Modules
  - Three Quadrature Encoder Pulse (QEP) Modules
  - Two Sigma-Delta Filter Modules (SDFMs) With up to 8 Input Channels, Plus PWM Synchronization



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- **Expanded Peripheral Interrupt (ePIE) Block**
    - Supports up to 192 Peripheral Interrupts
    - GPIO Pins can be Connected to 5 Core Interrupts
  - **JTAG Boundary Scan Support** <sup>(1)</sup>
  - **Advanced Emulation Features**
    - Analysis and Breakpoint Functions
    - Two Hardware Breakpoints per CPU
    - Real-Time Debug via Hardware
  - **Independent Dual-Zone Security per CPU**
    - 128-Bit Security Key and Lock
    - Protects Flash, OTP, and RAM Blocks
  - **Safety and Reliability Features**
    - ECC on Flash, ECC or Parity on RAMs
    - Missing Clock Detection
    - Self-Test and Real-Time Self-Test BIST
  - **Low-Power Modes and Power Savings**
    - IDLE, STANDBY, HALT, and HIBERNATE Modes Supported
    - Disable Individual Peripheral Clocks
  - **Clock and System Control**
    - Two Internal Zero-Pin 10-MHz Oscillators
    - On-Chip Crystal Oscillator/External Clock Input
  - **Dynamic PLL Ratio Changes Supported**
  - **Watchdog Timer Module**
  - **Missing Clock Detection Circuitry**
  - **1.2-V Core, 3.3-V I/O Design**
  - **Development Support Includes**
    - ANSI C/C++ Compiler/Assembler/Linker
    - Code Composer Studio™ IDE
    - DSP/BIOS™ and SYS/BIOS™
    - Digital Motor Control and Digital Power Libraries
  - **Package Options:**
    - Lead-Free, Green Packaging
    - 337-Ball New Fine Pitch Ball Grid Array (nFBGA) [ZWT Suffix]
    - 176-Pin PowerPAD™ Thermally Enhanced Low-Profile Quad Flatpack (HLQFP) [PTP Suffix]
  - **Temperature Options:**
    - T: –40°C to 105°C
    - S: –40°C to 125°C
    - Q: –40°C to 125°C (Q100 Qualification for Automotive Applications)
- (1) IEEE Standard 1149.1-1990 Standard Test Access Port and Boundary Scan Architecture

## 1.2 Applications

- Industrial Drives
- Solar Micro Inverters and Converters
- Radar
- Digital Power
- Smart Metering
- Automotive Transportation
- Power Line Communications
- Software-Defined Radio

## 1.3 Description

The Delfino TMS320F2837xD device is a dual-core microcontroller with integrated analog features and communications interfaces. The dual real-time control subsystems are based on TI's industry-leading 32-bit TMS320C28x Floating-Point CPUs and feature two control law accelerators (CLAs) that provide additional flexibility to designers who are interested in doing applications such as running parallel control algorithms and much more. Designers can realize up to 800 MIPS of total system performance.

The TMS320F2837xD series introduces the trigonometric math unit (TMU), which is an accelerator that greatly reduces the number of cycles required to perform common trigonometric functions. The TMS320F2837xD device also has a second-generation Viterbi Complex Math Unit (VCU II) with improved acceleration on Viterbi operations, complex multiplies, and the CRC engine.

The TMS320F2837xD device supports up to 1MB of ECC-protected on-board flash memory and up to 204KB of SRAM with parity. Two independent security zones are also available for 128-bit code protection. High-precision control peripherals such as Enhanced Pulse Width Modulators (ePWMs) with fault protection, encoders, and captures are also included.

The analog subsystem boasts up to four 16-bit analog-to-digital converters (ADCs) as well as eight comparator subsystems. Each comparator subsystem contains two comparators and a built-in 12-bit DAC reference. Each comparator subsystem can be used as peak-current-mode comparators or as windowed comparators. In addition, the device has three 12-bit digital-to-analog converters (DACs).

Connectivity peripherals such as dual External Memory Interfaces (EMIFs), dual CAN 2.0 interfaces, and a new Universal Parallel Port (uPP) are also available. The uPP is a high-speed, parallel data bus that allows direct connection to FPGAs or other devices with similar interfaces. A USB 2.0 OTG port with MAC and PHY lets users add USB connectivity to their application.

### 1.4 Functional Block Diagram

Figure 1-1 shows the CPU system and associated peripherals comprising the F2837xD device.

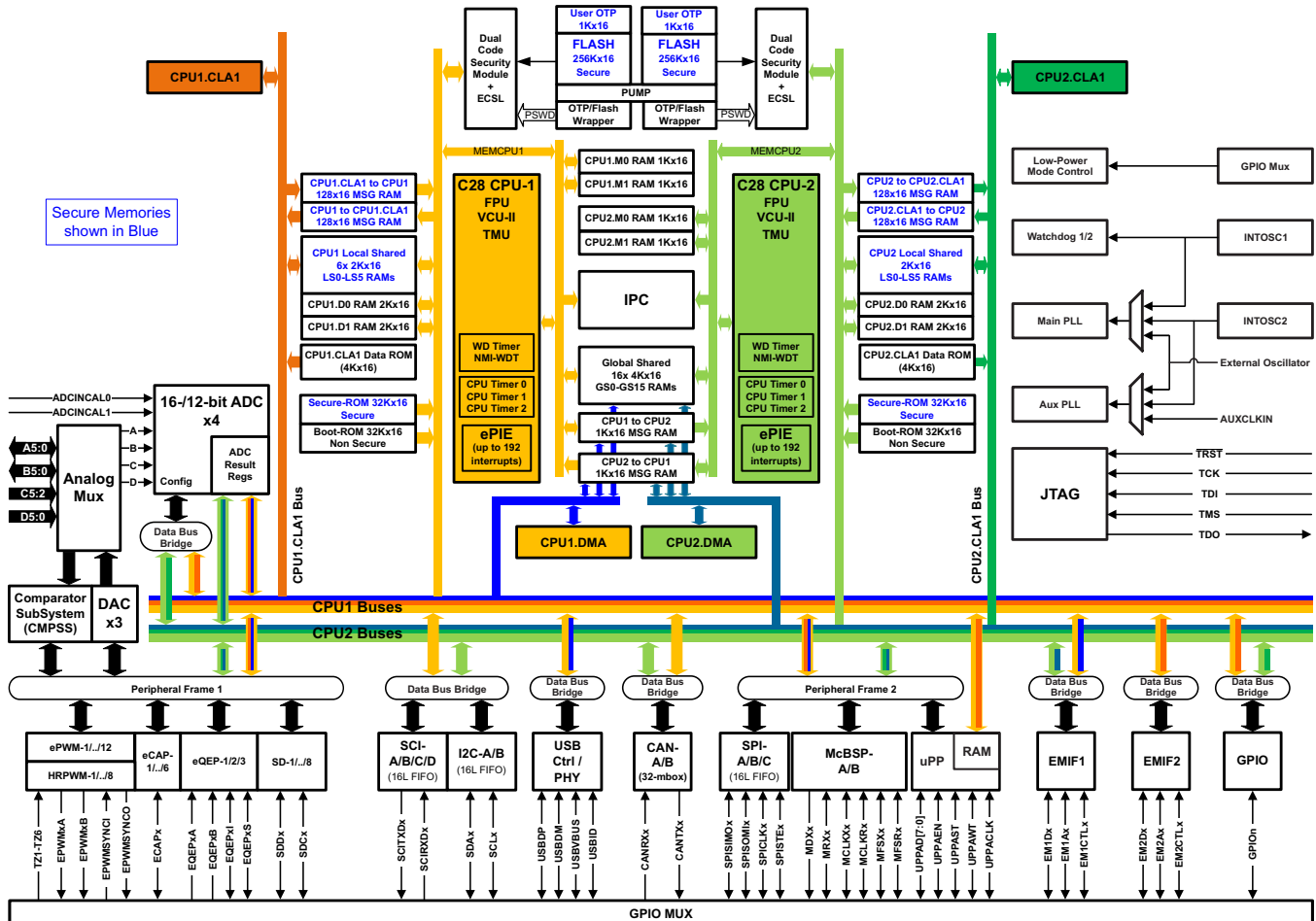


Figure 1-1. Functional Block Diagram

ADVANCE INFORMATION

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## 2 Device Overview

### 2.1 Device Characteristics

Table 2-1 lists the features of the TMS320F2837xD devices.

**Table 2-1. TMS320F2837xD Hardware Features**

FEATURE <sup>(1)</sup>		28377D		28376D	
		337-Ball ZWT	176-Pin PTP	337-Ball ZWT	176-Pin PTP
Package Type (ZWT is an nFBGA package. PTP is an HLQFP package.)					
Processor speed (MHz)		200			
Instruction cycle (ns)		5			
Floating-Point Unit (FPU)		Yes			
Viterbi, Complex Math, and CRC Unit II (VCU-II)		Yes			
Trigonometric Math Unit (TMU) – Type 0		Yes			
Control Law Accelerator (CLA) – Type 1		2 (1 per CPU)			
6-Channel DMA – Type 0		2 (1 per CPU)			
Flash (16-bit words)		512KW (256KW per CPU)		256KW (128KW per CPU)	
RAM (16-bit words)	Dedicated and Local Shared RAM	36KW (18KW per CPU)			
	Global Shared RAM	64KW		44KW	
	Message RAM	2KW (1KW per CPU)			
	<b>Total RAM</b>	<b>102KW</b>		<b>82KW</b>	
Code security for on-chip Flash, RAM, and OTP blocks		Yes			
Boot ROM		Yes			
One-time programmable (OTP) memory (16-bit words)		2KW			
ePWM Type-4 channels		24			
High-resolution ePWM Type- 4 channels		16			
eCAP inputs – Type 0		6			
eQEP modules – Type 0		3			
32-Bit CPU timers		6 (3 per CPU)			
Watchdog timers		2 (1 per CPU)			
Nonmaskable Interrupt Watchdog (NMIWD) timers		2 (1 per CPU)			
16-/12-Bit Analog-to-Digital Converter (ADC)	MSPS	1.1/3.5			
	Conversion Time (ns)	910 /286			
	Input pins	24	20	24	20
	Channels (differential/single-ended)	12/24	9/20	12/24	9/20
Number of 16-/12-Bit ADCs		4			
Temperature sensor		1			
Comparator Subsystems (CMPSS) [each CMPSS has two Comparators and one internal DAC]		8			
Buffered Digital-to-Analog Converter (DAC)		3			
Sigma-Delta Filter Module (SDFM) channels		8			
Inter-integrated circuit (I <sup>2</sup> C) – Type 0		2			
Multichannel Buffered Serial Port (McBSP) – Type 1		2			
Universal Parallel Port (uPP)		1			
Controller Area Network (CAN) – Type 0		2			
Serial Peripheral Interface (SPI) – Type 1		3			
Serial Communications Interface (SCI) – Type 0		4			
Universal Serial Bus (USB) – Type 0		1			

**Table 2-1. TMS320F2837xD Hardware Features (continued)**

FEATURE <sup>(1)</sup>		28377D		28376D	
		337-Ball ZWT	176-Pin PTP	337-Ball ZWT	176-Pin PTP
<b>Package Type</b> (ZWT is an nFBGA package. PTP is an HLQFP package.)					
External Memory Bus (EMIF)	16/32-bit	1			
	16-bit	1	–	1	–
On-chip crystal oscillator/External clock input		1			
0-pin internal oscillator		2			
I/O pins (shared)	GPIO	169	97	169	97
External interrupts		5			
Power-on reset (POR)		Yes			
I/O supply voltage (nominal)		3.3 V			
Core supply voltage (nominal)		1.2 V			
Temperature options	T: –40°C to 105°C	Yes			
	S: –40°C to 125°C	Yes			
	Q: –40°C to 125°C <sup>(2)</sup>	Yes		–	
Product status <sup>(3)</sup>		TMX			

- (1) A type change represents a major functional feature difference in a peripheral module. Within a peripheral type, there may be minor differences between devices that do not affect the basic functionality of the module.
- (2) "Q" refers to Q100 qualification for automotive applications.
- (3) The "TMX" product status denotes an experimental device that is not necessarily representative of the final device's electrical specifications.

## 2.2 Memory Map

Table 2-2 shows the memory map.

**Table 2-2. Memory Map**

BLOCK START ADDRESS	CPU1.DMA	CPU1.CLA1 (DATA SPACE)	C28x_1	C28x_2	CPU2.CLA1 (DATA SPACE)	CPU2.DMA
0x0000 0000			M0 RAM (with ECC) (2KB) (1KW)			
0x0000 0400			M1 RAM (with ECC) (2KB) (1KW)			
0x0000 0800			C28x Emulation and Test Registers (512 Bytes) (256 Words)			
0x0000 0A00						
0x0000 0B00	ADC-A to ADC-D Result Registers (0-wait access) (64 Bytes each) (32 Words each)					
0x0000 0B80						
0x0000 0C00			CPU Timer 0, 1, 2 Registers (3 x 16 Bytes) (3 x 8 Words)	CPU Timer 0, 1, 2 Registers (3 x 16 Bytes) (3 x 8 Words)		
0x0000 0C18						
0x0000 0CE0			ePIE Registers and Vectors	ePIE Registers and Vectors		
0x0000 0D00						
0x0000 0E00						
0x0000 0F00			FPU Registers (512 Bytes) (256 Words)	FPU Registers (512 Bytes) (256 Words)		
0x0000 1000			DMA Registers (1KB) (0.5KW)	DMA Registers (1KB) (0.5KW)		
0x0000 1200			VCU Registers (512 Bytes) (256 Words)	VCU Registers (512 Bytes) (256 Words)		
0x0000 1300						
0x0000 2000	EMIF-2 (8KB) (4KW)					
0x0000 3000						
0x0000 4000	Control Peripheral Registers (16KB) (8KW)					
0x0000 6000	High-Speed Serial Port Registers (8KB) (4KW)					
0x0000 7000	Reserved					
0x0000 8000		LS0–LS5 RAM (with Parity) (4KB each) (2KW each)		LS0–LS5 RAM (with Parity) (4KB each) (2KW each)		
0x0000 B000			D0 RAM (ECC) (4KB) (2KW)	D0 RAM (ECC) (4KB) (2KW)		
0x0000 B800			D1 RAM (ECC) (4KB) (2KW)	D1 RAM (ECC) (4KB) (2KW)		
0x0000 C000	GS0–GS2 RAM		GS0–GS2 RAM (with Parity) (8KB each) (4KW each)			GS0–GS2 RAM
0x0000 F000	GS3 RAM	CPU1.CLA1 Data ROM	GS3 RAM (with Parity) (8KB) (4KW)		CPU2.CLA1 Data ROM	GS3 RAM
0x0001 0000	GS4–GS15 RAM		GS4–GS15 RAM (with Parity) (8KB each) (4KW each)			GS4–GS15 RAM
0x0001 C000						
0x0003 F800	CPU2–CPU1 IPC MSG RAM		CPU2–CPU1 IPC MSG RAM (2KB) (1KW)			CPU2–CPU1 IPC MSG RAM
0x0003 FC00	CPU1–CPU2 IPC MSG RAM		CPU1–CPU2 IPC MSG RAM (2KB) (1KW)			CPU1–CPU2 IPC MSG RAM
0x0004 0000			USB Registers (8KB) (4KW)			

**Table 2-2. Memory Map (continued)**

BLOCK START ADDRESS	CPU1.DMA	CPU1.CLA1 (DATA SPACE)	C28x_1	C28x_2	CPU2.CLA1 (DATA SPACE)	CPU2.DMA
0x0004 1000	USB RAM (4KB) (2KW)					
0x0004 1800						
0x0004 7000			EMIF-1 and EMIF-2			
0x0004 8000			CAN-A/B Registers and Msg RAM (4KB each) (2KW each)			
0x0004 F800						
0x0005 0000			IPC Registers (8KB) (4KW)	IPC Registers (8KB) (4KW)		
0x0005 1000						
0x0005 D000			Reserved			
0x0007 8000			USER OTP (2KB) (1K x 16)			
0x0007 8D00						
0x0008 0000			CPU1 FLASH BANK (512KB) (256K x 16)	CPU2 FLASH BANK (512KB) (256K x 16)		
0x0010 0000	EMIF-1 (Data)		EMIF-1 (Prog + Data) (4MB) (2MW)			EMIF-1 (Data)
0x0030 0000	EMIF-1 (Data)		EMIF-1 (Prog + Data) (1MB) (0.5MW)			EMIF-1 (Data)
0x0038 0000	EMIF-1 (Data)		EMIF-1 (Prog + Data) (1MB–128KB ROM sizes) (0.5MW–64KW ROM sizes)			EMIF-1 (Data)
0x003F 0000			Secure ROM (64KB) (32KW)			
0x003F 8000			Secure ROM (20KW, 0-wait, Z1/Z2 Secure Zone, EXEONLY + ECSL)			
0x003F D000			Boot ROM (12KW, 0-wait, Non-secure)			
0x003F FFC0			Vectors (32 vectors, enabled if VMAP = 1)			
0x0040 0000						
0x8000 0000	EMIF-1 (Data)		EMIF-1 (Data Only) (0.5GB) (0.25GW)			EMIF-1 (Data)
0x9000 0000			EMIF-2 (Data Only) (0.5GB) (0.25GW)			
0xA000 0000						

**Table 2-3. Addresses of Flash Sectors on CPU1 and CPU2 for F28377D**

ADDRESS RANGE	PROGRAM AND DATA SPACE
0x07 0000 – 0x07 03FF	TI OTP (1K x 16)
0x07 8000 – 0x07 83FF	User OTP (1K x 16)
0x08 0000 – 0x08 1FFF	Sector A - 8K x 16
0x08 2000 – 0x08 3FFF	Sector B - 8K x 16
0x08 4000 – 0x08 5FFF	Sector C - 8K x 16
0x08 6000 – 0x08 7FFF	Sector D - 8K x 16
0x08 8000 – 0x08 FFFF	Sector E - 32K x 16
0x09 0000 – 0x09 7FFF	Sector F - 32K x 16
0x09 8000 – 0x09 FFFF	Sector G - 32K x 16
0x0A 0000 – 0x0A 7FFF	Sector H - 32K x 16
0x0A 8000 – 0x0A FFFF	Sector I - 32K x 16
0x0B 0000 – 0x0B 7FFF	Sector J - 32K x 16
0x0B 8000 – 0x0B 9FFF	Sector K - 8K x 16
0x0B A000 – 0x0B BFFF	Sector L - 8K x 16
0x0B C000 – 0x0B DFFF	Sector M - 8K x 16
0x0B E000 – 0x0B FFFF	Sector N - 8K x 16

**Table 2-4. Addresses of Flash Sectors on CPU1 and CPU2 for F28376D**

ADDRESS RANGE	PROGRAM AND DATA SPACE
0x07 0000 – 0x07 03FF	TI OTP (1K x 16)
0x07 8000 – 0x07 83FF	User OTP (1K x 16)
0x08 0000 – 0x08 1FFF	Sector A - 8K x 16
0x08 2000 – 0x08 3FFF	Sector B - 8K x 16
0x08 4000 – 0x08 5FFF	Sector C - 8K x 16
0x08 6000 – 0x08 7FFF	Sector D - 8K x 16
0x08 8000 – 0x08 FFFF	Sector E - 32K x 16
0x09 0000 – 0x09 7FFF	Sector F - 32K x 16
0x09 8000 – 0x09 FFFF	Sector G - 32K x 16

## 2.3 Device Identification Registers

**Table 2-5. Device Identification Registers**

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
PARTIDH	0x0005 D00A	2	Device part identification number
			TMS320F28377D                      0x00FF 0300
			TMS320F28376D                      TBD
REVID	0x0005 D00C	2	Silicon revision number
			Revision 0                              0x0000 0000
			Revision A                              0x0000 0000

## 2.4 Bus Architecture – Peripheral Connectivity

Table 2-6 shows a broad view of the peripheral and configuration register accessibility from each bus master. Peripherals can be individually assigned to the CPU1 or CPU2 subsystem (for example, ePWM can be assigned to CPU1 and eQEP assigned to CPU2). Peripherals within peripheral frames 1 or 2 will all be mapped to the respective secondary master as a group (if SPI is assigned to CPUx.DMA, then McBSP is also assigned to CPUx.DMA).

**Table 2-6. Bus Master Peripheral Access**

PERIPHERALS (BY BUS ACCESS TYPE)	CPU1.DMA	CPU1.CLA1	CPU1	CPU2	CPU2.CLA1	CPU2.DMA
<b>Peripherals that can be assigned to CPU1 or CPU2 and have common selectable Secondary Masters</b>						
Peripheral Frame 1: • ePWM/HRPWM • Sigma-Delta Filter Module (SDFM) Demodulator • eCAP <sup>(1)</sup> • eQEP <sup>(1)</sup> • CMPSS <sup>(1)</sup> • DAC <sup>(1)</sup>	Y	Y	Y	Y	Y	Y
Peripheral Frame 2: • SPI • McBSP • uPP Configuration <sup>(1)</sup>	Y	Y	Y	Y	Y	Y
<b>Peripherals that can be assigned to CPU1 or CPU2 subsystems</b>						
SCI			Y	Y		
I <sup>2</sup> C			Y	Y		
CAN			Y	Y		
ADC Configuration		Y	Y	Y	Y	
EMIF1	Y		Y	Y		Y
<b>Peripherals and Device Configuration Registers only on CPU1 subsystem</b>						
EMIF2		Y	Y			
USB and USB RAM	Y		Y			
Device Capability, Peripheral Reset, Peripheral CPU Select			Y			
GPIO Pin Mapping and Configuration			Y			
Analog System Control			Y			
uPP Message RAMs		Y	Y			
Reset Configuration			Y			
<b>Accessible by only one CPU at a time with Semaphore</b>						
Clock and PLL Configuration			Y	Y		
<b>Peripherals and Registers with Unique Copies of Registers for each CPU and CLA Master<sup>(2)</sup></b>						
System Configuration (WD, NMIWD, LPM, Peripheral Clock Gating)			Y	Y		
Flash Configuration <sup>(3)</sup>			Y	Y		
CPU Timers			Y	Y		
DMA and CLA Trigger Source Select			Y	Y		
GPIO Data <sup>(4)</sup>		Y	Y	Y	Y	
ADC Results	Y	Y	Y	Y	Y	Y

(1) These modules are on a Peripheral Frame with DMA access; however, they do not support DMA transfers.

(2) Each CPUx and CPUx.CLA1 can only access its own copy of these registers.

(3) At any given time, only one CPU can perform program or erase operations on the Flash.

(4) The GPIO Data Registers are unique for each CPUx and CPUx.CLAx. When the GPIO Pin Mapping Register is configured to assign a GPIO to a particular master, the respective GPIO Data Register will control the GPIO. See the "General-Purpose Input/Output (GPIO)" chapter of the *TMS320F2837xD Technical Reference Manual* (literature number [SPRUHM8](#)) for more details.

### 3 Device Pins

#### 3.1 Pin Assignments

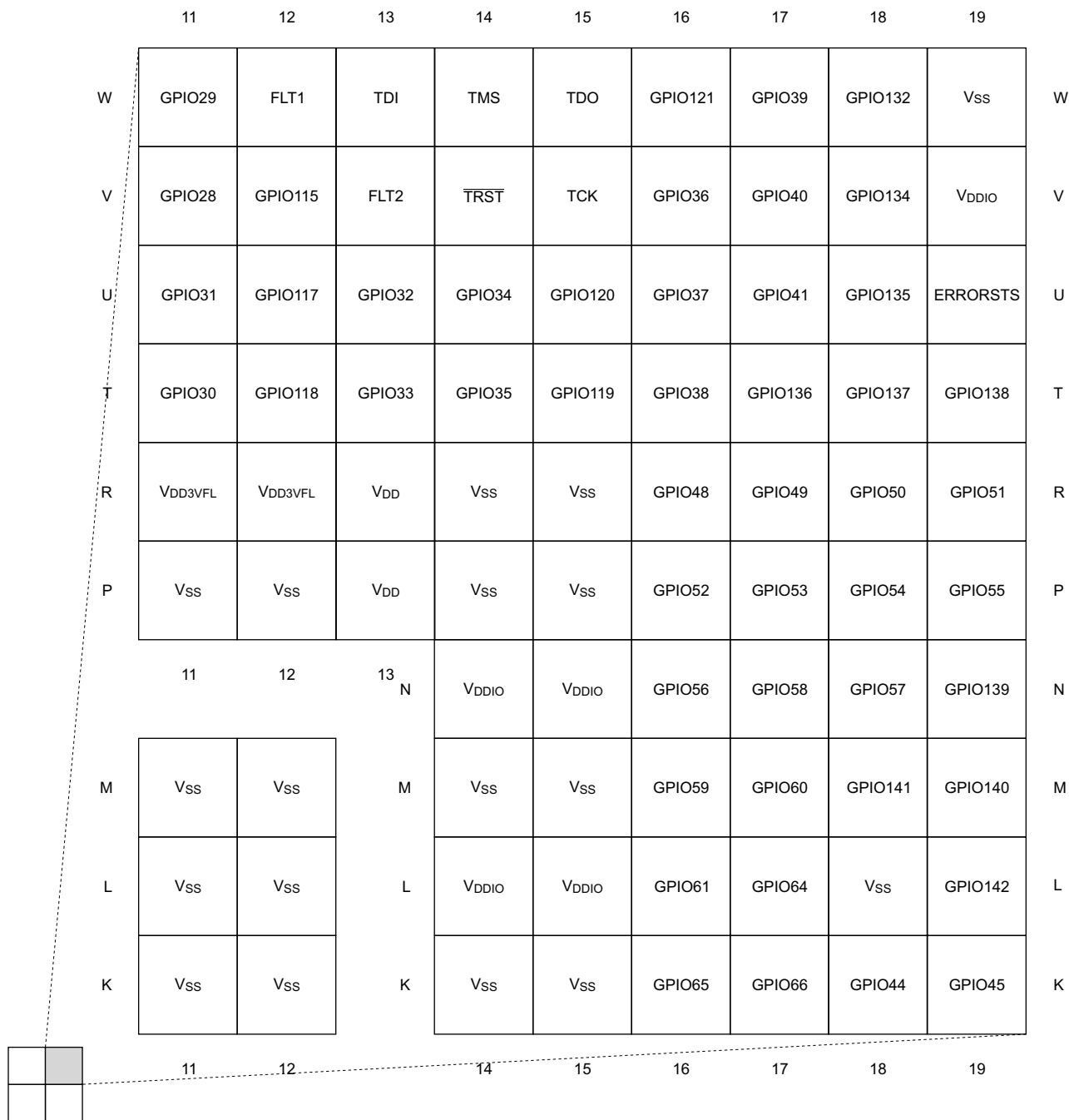
Figure 3-1 to Figure 3-4 show in four quadrants the terminal assignments on the 337-ball ZWT New Fine Pitch Ball Grid Array (nFBGA). Figure 3-5 shows the pin assignments on the 176-pin PTP PowerPAD™ Thermally Enhanced Low-Profile Quad Flatpack (HLQFP).

ADVANCE INFORMATION

	1	2	3	4	5	6	7	8	9	10	
W	V <sub>SSA</sub>	ADCINB1	ADCINB3	ADCINB5	V <sub>REFHIB</sub>	V <sub>REFLOD</sub>	V <sub>SS</sub>	V <sub>DDIO</sub>	GPIO128	GPIO116	W
V	V <sub>REFHIA</sub>	ADCINB0	ADCINB2	ADCINB4	V <sub>REFHID</sub>	V <sub>REFLOB</sub>	V <sub>SSA</sub>	GPIO124	GPIO127	GPIO131	V
U	ADCINA0	ADCINA2	ADCINA4	ADCINCAL1	ADCIND1	ADCIND3	ADCIND5	GPIO123	GPIO126	GPIO130	U
T	ADCINA1	ADCINA3	ADCINA5	ADCINCAL0	ADCIND0	ADCIND2	ADCIND4	GPIO122	GPIO125	GPIO129	T
R	V <sub>REFHIC</sub>	V <sub>REFLOA</sub>	ADCINC2	ADCINC4	V <sub>SSA</sub>	V <sub>DDA</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDIO</sub>	V <sub>DD</sub>	R
P	V <sub>SSA</sub>	V <sub>REFLOC</sub>	ADCINC3	ADCINC5	V <sub>SSA</sub>	V <sub>DDA</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDIO</sub>	V <sub>DD</sub>	P
N	V <sub>SS</sub>	GPIO109	GPIO114	GPIO113	V <sub>SS</sub>	V <sub>SS</sub>	7 N	8	9	10	N
M	V <sub>DDIO</sub>	GPIO110	GPIO112	GPIO111	V <sub>DDIO</sub>	V <sub>DDIO</sub>	M	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	M
L	GPIO27	GPIO106	GPIO107	GPIO108	V <sub>SS</sub>	V <sub>SS</sub>	L	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	L
K	GPIO26	GPIO25	GPIO24	GPIO23	V <sub>DD</sub>	V <sub>DD</sub>	K	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	K
	1	2	3	4	5	6		8	9	10	

A. Only the GPIO function is shown on GPIO terminals. See Table 3-2 for the complete, muxed signal name.

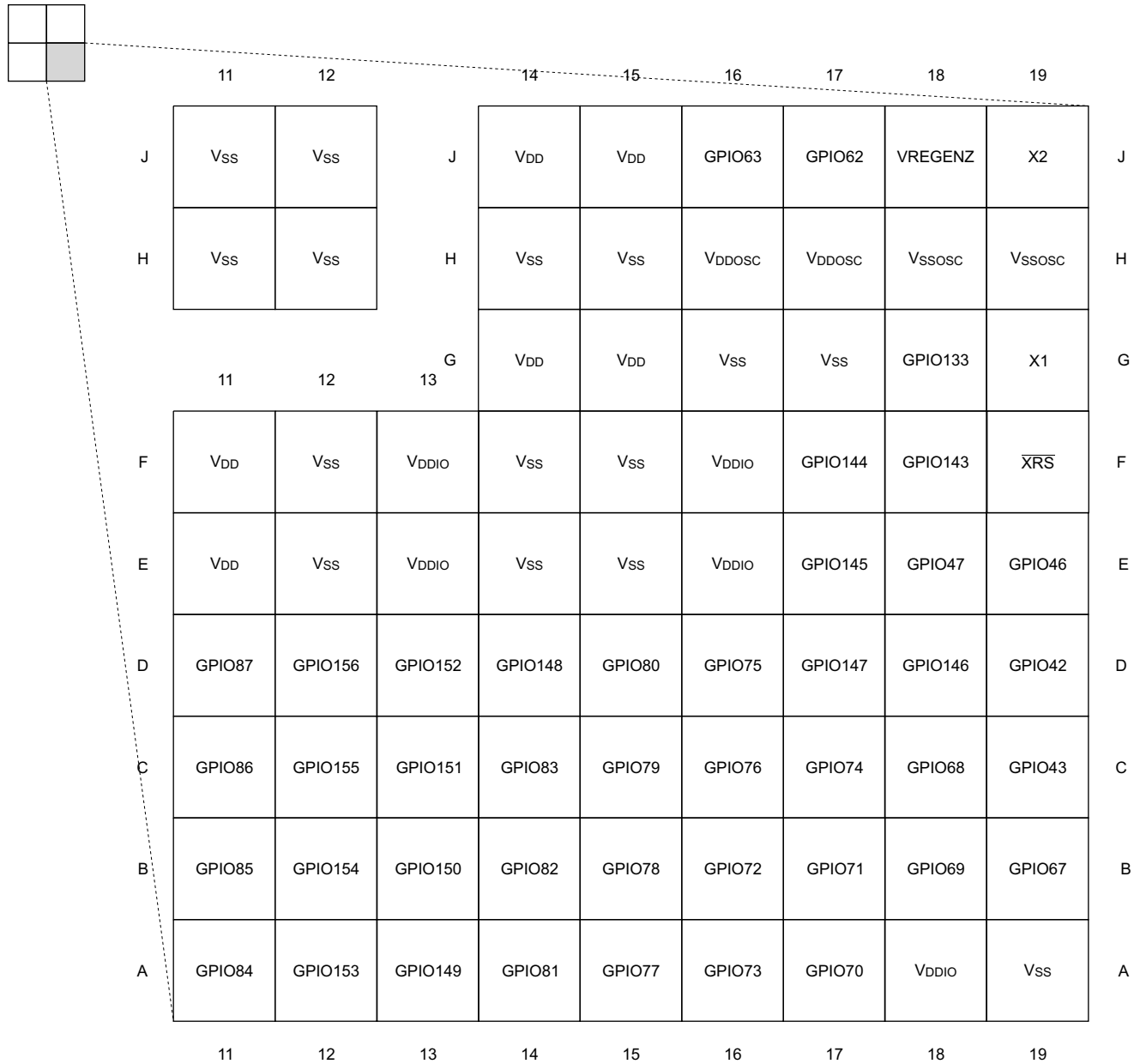
**Figure 3-1. 337-Ball ZWT nFBGA (Bottom View) – [Quadrant A]**



ADVANCE INFORMATION

A. Only the GPIO function is shown on GPIO terminals. See Table 3-2 for the complete, muxed signal name.

Figure 3-2. 337-Ball ZWT nFBGA (Bottom View) – [Quadrant B]



A. Only the GPIO function is shown on GPIO terminals. See [Table 3-2](#) for the complete, muxed signal name.

**Figure 3-3. 337-Ball ZWT nFBGA (Bottom View) – [Quadrant C]**

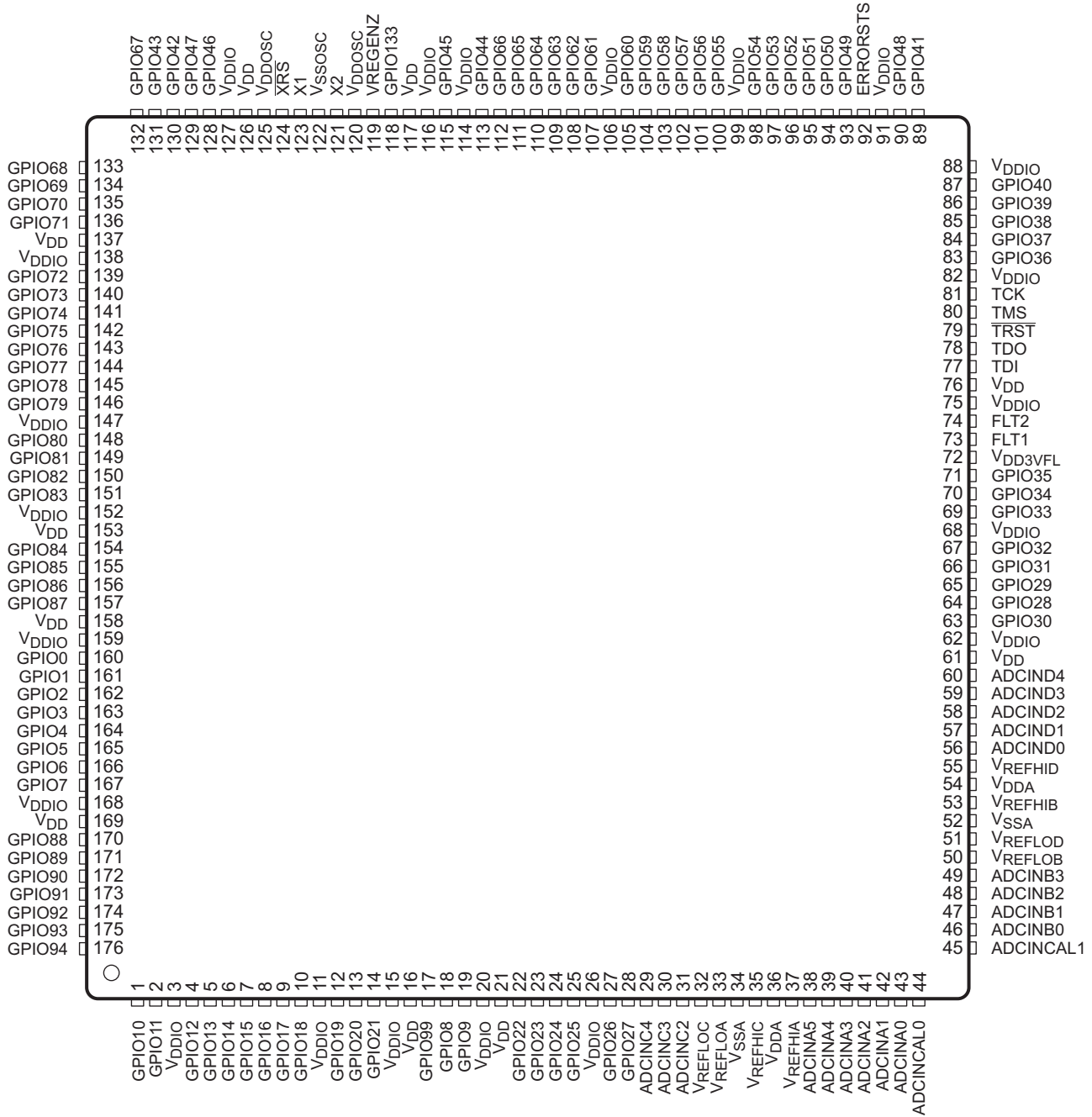
	1	2	3	4	5	6		8	9	10	
J	GPIO103	GPIO104	GPIO105	GPIO22	Vss	Vss	J	Vss	Vss	Vss	J
H	GPIO100	GPIO101	GPIO102	NC	VDDIO	VDDIO	H	Vss	Vss	Vss	H
G	GPIO99	GPIO8	GPIO9	VDDIO	VDDIO	VDDIO	G	7	8	9	10
F	GPIO98	GPIO20	GPIO21	VDDIO	Vss	Vss	VDDIO	Vss	VDD	VDDIO	F
E	GPIO16	GPIO17	GPIO18	GPIO19	Vss	Vss	VDDIO	Vss	VDD	VDDIO	E
D	GPIO13	GPIO14	GPIO15	GPIO168	GPIO166	GPIO89	GPIO5	GPIO1	GPIO162	GPIO159	D
C	GPIO11	GPIO12	GPIO96	GPIO167	GPIO165	GPIO88	GPIO4	GPIO0	GPIO161	GPIO158	C
B	VDDIO	GPIO10	GPIO95	GPIO93	GPIO91	GPIO7	GPIO3	GPIO164	GPIO160	GPIO157	B
A	Vss	GPIO97	GPIO94	GPIO92	GPIO90	GPIO6	GPIO2	GPIO163	VDDIO	Vss	A
	1	2	3	4	5	6	7	8	9	10	

A. Only the GPIO function is shown on GPIO terminals. See [Table 3-2](#) for the complete, muxed signal name.

**Figure 3-4. 337-Ball ZWT nFBGA (Bottom View) – [Quadrant D]**

ADVANCE INFORMATION

**ADVANCE INFORMATION**



A. Only the GPIO function is shown on GPIO pins. See [Table 3-2](#) for the complete, muxed signal name.

**Figure 3-5. 176-Pin PTP PowerPAD™ HLQFP (Top View)**

### 3.1.1 GPIO Muxed Pins

Table 3-1 shows the GPIO muxed pins and their alternate USB functions. The default for each pin is the GPIO function, secondary functions can be selected by setting both the GPyGMUXn.GPIOz and GPyMUXn.GPIOz register bits. The GPyGMUXn register should be configured prior to the GPyMUXn to avoid transient pulses on GPIO's from alternate mux selections. Columns not shown and blank cells are reserved GPIO Mux settings. The alternate USB function is selected by the GPyAMSEL register.

**Table 3-1. GPIO Muxed Pins**

GPIO Index	GPIO Mux Selection								Alternate Function
	0, 4, 8, 12	1	2	3	5	6	7	15	
GPyGMUXn. GPIOz =	00b, 01b, 10b, 11b	00b			01b			11b	GPyAMSEL. GPIOz = 1
GPyMUXn. GPIOz =	00b	01b	10b	11b	01b	10b	11b	11b	GPyAMSEL. GPIOz=1
GPIO0	EPWM1A (O)					SDAA (I/OD)			
GPIO1	EPWM1B (O)			MFSRB (I/O)		SCLA (I/OD)			
GPIO2	EPWM2A (O)				XTRIPOUT1 (O)	SDAB (I/OD)			
GPIO3	EPWM2B (O)	XTRIPOUT2 (O)		MCLKRB (I/O)	XTRIPOUT2 (O)	SCLB (I/OD)			
GPIO4	EPWM3A (O)				XTRIPOUT3 (O)	CANTXA (O)			
GPIO5	EPWM3B (O)	MFSRA (I/O)	XTRIPOUT3 (O)			CANRXA (I)			
GPIO6	EPWM4A (O)	XTRIPOUT4 (O)	EPWMSYNCO (O)		EQEP3A (I)	CANTXB (O)			
GPIO7	EPWM4B (O)	MCLKRA (I/O)			EQEP3B (I)	CANRXB (I)			
GPIO8	EPWM5A (O)	CANTXB (O)		ADCSOCAO (O)	EQEP3S (I/O)	SCITXDA (O)			
GPIO9	EPWM5B (O)	SCITXDB (O)			EQEP3I (I/O)	SCIRXDA (I)			
GPIO10	EPWM6A (O)	CANRXB (I)	ADCSOCBO (O)		EQEP1A (I)	SCITXDB (O)		UPP-WAIT (I/O)	
GPIO11	EPWM6B (O)	SCIRXDB (I)	XTRIPOUT7 (O)		EQEP1B (I)	SCIRXDB (I)		UPP-STRT (I/O)	
GPIO12	EPWM7A (O)	CANTXB (O)	MDXB (O)		EQEP1S (I/O)	SCITXDC (O)		UPP-ENA (I/O)	
GPIO13	EPWM7B (O)	CANRXB (I)	MDRB (I)		EQEP1I (I/O)	SCIRXDC (I)		UPP-D7 (I/O)	
GPIO14	EPWM8A (O)	SCITXDB (O)	MCLKXB (I/O)			XTRIPOUT3 (O)		UPP-D6 (I/O)	
GPIO15	EPWM8B (O)	SCIRXDB (I)	MFSXB (I/O)			XTRIPOUT4 (O)		UPP-D5 (I/O)	
GPIO16	SPISIMOA (I/O)	CANTXB (O)	XTRIPOUT7 (O)		EPWM9A (O)		SD-D1 (I)	UPP-D4 (I/O)	
GPIO17	SPISOMIA (I/O)	CANRXB (I)	XTRIPOUT8 (O)		EPWM9B (O)		SD-C1 (I)	UPP-D3 (I/O)	
GPIO18	SPICLKA (I/O)	SCITXDB (O)	CANRXA (I)		EPWM10A (O)		SD-D2 (I)	UPP-D2 (I/O)	
GPIO19	SPISTEA (I/O)	SCIRXDB (I)	CANTXA (O)		EPWM10B (O)		SD-C2 (I)	UPP-D1 (I/O)	
GPIO20	EQEP1A (I)	MDXA (O)	CANTXB (O)		EPWM11A (O)		SD-D3 (I)	UPP-D0 (I/O)	
GPIO21	EQEP1B (I)	MDRA (I)	CANRXB (I)		EPWM11B (O)		SD-C3 (I)	UPP-CLK (I/O)	
GPIO22	EQEP1S (I/O)	MCLKXA (I/O)	SCITXDB (O)		EPWM12A (O)	SPICLKB (I/O)	SD-D4 (I)		
GPIO23	EQEP1I (I/O)	MFSXA (I/O)	SCIRXDB (I)		EPWM12B (O)	SPISTEB (I/O)	SD-C4 (I)		
GPIO24	XTRIPOUT1 (O)	EQEP2A (I)	MDXB (O)			SPISIMOB (I/O)	SD-D5 (I)		
GPIO25	XTRIPOUT2 (O)	EQEP2B (I)	MDRB (I)			SPISOMIB (I/O)	SD-C5 (I)		
GPIO26	XTRIPOUT3 (O)	EQEP2I (I/O)	MCLKXB (I/O)		XTRIPOUT3 (O)	SPICLKB (I/O)	SD-D6 (I)		
GPIO27	XTRIPOUT4 (O)	EQEP2S (I/O)	MFSXB (I/O)		XTRIPOUT4 (O)	SPISTEB (I/O)	SD-C6 (I)		
GPIO28	SCIRXDA (I)	EM1CS4 (O)				EQEP3A (I)	SD-D7 (I)		
GPIO29	SCITXDA (O)	EM1SDCKE (O)				EQEP3B (I)	SD-C7 (I)		
GPIO30	CANRXA (I)	EM1CLK (O)			XTRIPOUT7 (O)	EQEP3S (I/O)	SD-D8 (I)		
GPIO31	CANTXA (O)	EM1WE (O)			XTRIPOUT8 (O)	EQEP3I (I/O)	SD-C8 (I)		
GPIO32	SDAA (I/OD)	EM1CS0 (O)							
GPIO33	SCLA (I/OD)	EM1RNW (O)							
GPIO34	XTRIPOUT1 (O)	EM1CS2 (O)				SDAB (I/OD)			
GPIO35	SCIRXDA (I)	EM1CS3 (O)				SCLB (I/OD)			
GPIO36	SCITXDA (O)	EM1WAIT (I)				CANRXA (I)			
GPIO37	XTRIPOUT2 (O)	EM1OE (O)				CANTXA (O)			
GPIO38		EM1A0 (O)			SCITXDC (O)	CANTXB (O)			
GPIO39		EM1A1 (O)			SCIRXDC (I)	CANRXB (I)			
GPIO40		EM1A2 (O)				SDAB (I/OD)			
GPIO41		EM1A3 (O)				SCLB (I/OD)			

**Table 3-1. GPIO Muxed Pins (continued)**

GPIO Index	GPIO Mux Selection								Alternate Function
	0, 4, 8, 12	1	2	3	5	6	7	15	N/A
GPyGMUXn. GPIOz =	00b, 01b, 10b, 11b	00b			01b			11b	GPyAMSEL. GPIOz = 1
GPyMUXn. GPIOz =	00b	01b	10b	11b	01b	10b	11b	11b	GPyAMSEL. GPIOz=1
GPIO42						SDAA (I/OD)		SCITXDA (O)	USB0DM
GPIO43						SCLA (I/OD)		SCIRXDA (I)	USB0DP
GPIO44			EM1A4 (O)						
GPIO45			EM1A5 (O)						
GPIO46			EM1A6 (O)			SCIRXDD (I)			USB0VBUS
GPIO47			EM1A7 (O)			SCITXDD (O)			USB0ID
GPIO48	XTRIP0UT3 (O)	EM1A8 (O)				SCITXDA (O)	SD-D1 (I)		
GPIO49	XTRIP0UT4 (O)	EM1A9 (O)				SCIRXDA (I)	SD-C1 (I)		
GPIO50	EQEP1A (I)	EM1A10 (O)				SPISIMOC (I/O)	SD-D2 (I)		
GPIO51	EQEP1B (I)	EM1A11 (O)				SPISOMIC (I/O)	SD-C2 (I)		
GPIO52	EQEP1S (I/O)	EM1A12 (O)				SPICLK (I/O)	SD-D3 (I)		
GPIO53	EQEP1I (I/O)	EM1D31 (I/O)	EM2D15 (I/O)			SPISTEC (I/O)	SD-C3 (I)		
GPIO54	SPISIMOA (I/O)	EM1D30 (I/O)	EM2D14 (I/O)	EQEP2A (I)	SCITXDB (O)	SD-D4 (I)			
GPIO55	SPISOMIA (I/O)	EM1D29 (I/O)	EM2D13 (I/O)	EQEP2B (I)	SCIRXDB (I)	SD-C4 (I)			
GPIO56	SPICLKA (I/O)	EM1D28 (I/O)	EM2D12 (I/O)	EQEP2S (I/O)	SCITXDC (O)	SD-D5 (I)			
GPIO57	SPISTEA (I/O)	EM1D27 (I/O)	EM2D11 (I/O)	EQEP2I (I/O)	SCIRXDC (I)	SD-C5 (I)			
GPIO58	MCLKRA (I/O)	EM1D26 (I/O)	EM2D10 (I/O)	XTRIP0UT1 (O)	SPICLKB (I/O)	SD-D6 (I)	SPISIMOA (I/O)		
GPIO59	MFSRA (I/O)	EM1D25 (I/O)	EM2D9 (I/O)	XTRIP0UT2 (O)	SPISTEB (I/O)	SD-C6 (I)	SPISOMIA (I/O)		
GPIO60	MCLKRB (I/O)	EM1D24 (I/O)	EM2D8 (I/O)	XTRIP0UT3 (O)	SPISIMOB (I/O)	SD-D7 (I)	SPICLKA (I/O)		
GPIO61	MFSRB (I/O)	EM1D23 (I/O)	EM2D7 (I/O)	XTRIP0UT4 (O)	SPISOMIB (I/O)	SD-C7 (I)	SPISTEA (I/O)		
GPIO62	SCIRXDC (I)	EM1D22 (I/O)	EM2D6 (I/O)	EQEP3A (I)	CANRXA (I)	SD-D8 (I)			
GPIO63	SCITXDC (O)	EM1D21 (I/O)	EM2D5 (I/O)	EQEP3B (I)	CANTXA (O)	SD-C8 (I)	SPISIMOB (I/O)		
GPIO64		EM1D20 (I/O)	EM2D4 (I/O)	EQEP3S (I/O)	SCIRXDA (I)		SPISOMIB (I/O)		
GPIO65		EM1D19 (I/O)	EM2D3 (I/O)	EQEP3I (I/O)	SCITXDA (O)		SPICLKB (I/O)		
GPIO66		EM1D18 (I/O)	EM2D2 (I/O)		SDAB (I/OD)		SPISTEB (I/O)		
GPIO67		EM1D17 (I/O)	EM2D1 (I/O)						
GPIO68		EM1D16 (I/O)	EM2D0 (I/O)						
GPIO69		EM1D15 (I/O)				SCLB (I/OD)		SPISIMOC (I/O)	
GPIO70		EM1D14 (I/O)			CANRXA (I)	SCITXDB (O)		SPISOMIC (I/O)	
GPIO71		EM1D13 (I/O)			CANTXA (O)	SCIRXDB (I)		SPICLK (I/O)	
GPIO72		EM1D12 (I/O)			CANTXB (O)	SCITXDC (O)		SPISTEC (I/O)	
GPIO73		EM1D11 (I/O)	XCLKOUT (O)	CANRXB (I)	SCIRXDC (I)				
GPIO74		EM1D10 (I/O)							
GPIO75		EM1D9 (I/O)							
GPIO76		EM1D8 (I/O)				SCITXDD (O)			
GPIO77		EM1D7 (I/O)				SCIRXDD (I)			
GPIO78		EM1D6 (I/O)				EQEP2A (I)			
GPIO79		EM1D5 (I/O)				EQEP2B (I)			
GPIO80		EM1D4 (I/O)				EQEP2S (I/O)			
GPIO81		EM1D3 (I/O)				EQEP2I (I/O)			
GPIO82		EM1D2 (I/O)							
GPIO83		EM1D1 (I/O)							
GPIO84					SCITXDA (O)	MDXB (O)		MDXA (O)	
GPIO85		EM1D0 (I/O)			SCIRXDA (I)	MDRB (I)		MDRA (I)	
GPIO86		EM1A13 (O)	EM1CAS (O)	SCITXDB (O)	MCLKXB (I/O)		MCLKXA (I/O)		
GPIO87		EM1A14 (O)	EM1RAS (O)	SCIRXDB (I)	MFSXB (I/O)		MFSXA (I/O)		
GPIO88		EM1A15 (O)	EM1DQM0 (O)						
GPIO89		EM1A16 (O)	EM1DQM1 (O)			SCITXDC (O)			
GPIO90		EM1A17 (O)	EM1DQM2 (O)			SCIRXDC (I)			
GPIO91		EM1A18 (O)	EM1DQM3 (O)			SDAA (I/OD)			
GPIO92		EM1A19 (O)	EM1BA1 (O)			SCLA (I/OD)			

ADVANCE INFORMATION

**Table 3-1. GPIO Muxed Pins (continued)**

GPIO Index	GPIO Mux Selection								Alternate Function
	0, 4, 8, 12	1	2	3	5	6	7	15	N/A
GPyGMUXn. GPIOz =	00b, 01b, 10b, 11b	00b			01b			11b	GPyAMSEL. GPIOz = 1
GPyMUXn. GPIOz =	00b	01b	10b	11b	01b	10b	11b	11b	GPyAMSEL. GPIOz=1
GPIO93			EM1A20 (O)	EM1BA0 (O)		SCITXDD (O)			
GPIO94			EM1A21 (O)			SCIRXDD (I)			
GPIO95									
GPIO96				EM2DQM1 (O)	EQEP1A (I)				
GPIO97				EM2DQM0 (O)	EQEP1B (I)				
GPIO98				EM2A0 (O)	EQEP1S (I/O)				
GPIO99				EM2A1 (O)	EQEP11 (I/O)				
GPIO100				EM2A2 (O)	EQEP2A (I)	SPISIMOC (I/O)			
GPIO101				EM2A3 (O)	EQEP2B (I)	SPISOMIC (I/O)			
GPIO102				EM2A4 (O)	EQEP2S (I/O)	SPICLK (I/O)			
GPIO103				EM2A5 (O)	EQEP2I (I/O)	SPISTEC (I/O)			
GPIO104		SDAA (I/OD)		EM2A6 (O)	EQEP3A (I)	SCITXDD (O)			
GPIO105		SCLA (I/OD)		EM2A7 (O)	EQEP3B (I)	SCIRXDD (I)			
GPIO106				EM2A8 (O)	EQEP3S (I/O)	SCITXDC (O)			
GPIO107				EM2A9 (O)	EQEP3I (I/O)	SCIRXDC (I)			
GPIO108				EM2A10 (O)					
GPIO109				EM2A11 (O)					
GPIO110									
GPIO111				EM2BA0 (O)					
GPIO112				EM2BA1 (O)					
GPIO113				EM2CAS (O)					
GPIO114				EM2RAS (O)					
GPIO115									
GPIO116									
GPIO117									
GPIO118									
GPIO119				EM2RNW (O)					
GPIO120				EM2WE (O)				USB0PFLT	
GPIO121								USB0EPEN	
GPIO122						SPISIMOC (I/O)	SD-D1 (I)		
GPIO123						SPISOMIC (I/O)	SD-C1 (I)		
GPIO124						SPICLK (I/O)	SD-D2 (I)		
GPIO125						SPISTEC (I/O)	SD-C2 (I)		
GPIO126							SD-D3 (I)		
GPIO127							SD-C3 (I)		
GPIO128							SD-D4 (I)		
GPIO129							SD-C4 (I)		
GPIO130							SD-D5 (I)		
GPIO131							SD-C5 (I)		
GPIO132							SD-D6 (I)		
GPIO133/ AUXCLKIN							SD-C6 (I)		
GPIO134							SD-D7 (I)		
GPIO135						SCITXDA (O)	SD-C7 (I)		
GPIO136						SCIRXDA (I)	SD-D8 (I)		
GPIO137						SCITXDB (O)	SD-C8 (I)		
GPIO138						SCIRXDB (I)			
GPIO139						SCIRXDC (I)			
GPIO140						SCITXDC (O)			
GPIO141						SCIRXDD (I)			
GPIO142						SCITXDD (O)			

**ADVANCE INFORMATION**

**Table 3-1. GPIO Muxed Pins (continued)**

GPIO Index	GPIO Mux Selection								Alternate Function
	0, 4, 8, 12	1	2	3	5	6	7	15	N/A
GPyGMUXn. GPIOz =	00b, 01b, 10b, 11b	00b			01b			11b	GPyAMSEL. GPIOz = 1
GPyMUXn. GPIOz =	00b	01b	10b	11b	01b	10b	11b	11b	GPyAMSEL. GPIOz=1
GPIO143									
GPIO144									
GPIO145	EPWM1A (O)								
GPIO146	EPWM1B (O)								
GPIO147	EPWM2A (O)								
GPIO148	EPWM2B (O)								
GPIO149	EPWM3A (O)								
GPIO150	EPWM3B (O)								
GPIO151	EPWM4A (O)								
GPIO152	EPWM4B (O)								
GPIO153	EPWM5A (O)								
GPIO154	EPWM5B (O)								
GPIO155	EPWM6A (O)								
GPIO156	EPWM6B (O)								
GPIO157	EPWM7A (O)								
GPIO158	EPWM7B (O)								
GPIO159	EPWM8A (O)								
GPIO160	EPWM8B (O)								
GPIO161	EPWM9A (O)								
GPIO162	EPWM9B (O)								
GPIO163	EPWM10A (O)								
GPIO164	EPWM10B (O)								
GPIO165	EPWM11A (O)								
GPIO166	EPWM11B (O)								
GPIO167	EPWM12A (O)								
GPIO168	EPWM12B (O)								

ADVANCE INFORMATION

### 3.2 Terminal Functions

Table 3-2 describes the signals. With the exception of the JTAG pins, the GPIO function is the default at reset, unless otherwise mentioned. The peripheral signals that are listed under them are alternate functions. Some peripheral functions may not be available in all devices. See Table 2-1 for details. Unless otherwise mentioned, inputs are not 5-V tolerant. All GPIO pins are I/O/Z and have an internal pullup, which can be selectively enabled or disabled on a per-pin basis. This feature only applies to the GPIO pins. The pullups are not enabled at reset.

**Table 3-2. Terminal Functions**

TERMINAL			I/O/Z <sup>(1)</sup>	DESCRIPTION
NAME	ZWT BALL NO.	PTP PIN NO.		
<b>ADC INPUTS AND COMPARATOR INPUTS</b>				
V <sub>REFHIA</sub>	V1	37	I	ADC-A high reference. Place at least a 1-μF capacitor on this pin.
V <sub>REFHIB</sub>	W5	53	I	ADC-B high reference. Place at least a 1-μF capacitor on this pin.
V <sub>REFHIC</sub>	R1	35	I	ADC-C high reference. Place at least a 1-μF capacitor on this pin.
V <sub>REFHID</sub>	V5	55	I	ADC-D high reference. Place at least a 1-μF capacitor on this pin.
V <sub>REFLOA</sub>	R2	33	I	ADC-A low reference
V <sub>REFLOB</sub>	V6	50	I	ADC-B low reference
V <sub>REFLOC</sub>	P2	32	I	ADC-C low reference
V <sub>REFLOD</sub>	W6	51	I	ADC-D low reference
ADCINCAL0	T4	44	I	ADC calibration input 0. All ADCs connect to this pin. This pin can be used as a general-purpose ADCIN pin or used to calibrate all ADCs together (either single-ended or differential) from an external reference.
CMPIN4P			I	Comparator 4 positive input
ADCINCAL1	U4	45	I	ADC calibration input 1. All ADCs connect to this pin. This pin can be used as a general-purpose ADCIN pin or used to calibrate all ADCs together (either single-ended or differential) from an external reference.
CMPIN4N			I	Comparator 4 negative input
ADCINA0 DACOUTA	U1	43	I O	ADC-A input 0 DAC-A output <sup>(2)</sup>
ADCINA1 DACOUTB	T1	42	I O	ADC-A input 1 DAC-B output <sup>(2)</sup>
ADCINA2 CMPIN1P	U2	41	I I	ADC-A input 2 Comparator 1 positive input
ADCINA3 CMPIN1N	T2	40	I I	ADC-A input 3 Comparator 1 negative input
ADCINA4 CMPIN2P	U3	39	I I	ADC-A input 4 Comparator 2 positive input
ADCINA5 CMPIN2N	T3	38	I I	ADC-A input 5 Comparator 2 negative input
ADCINB0 VDAC	V2	46	I I	ADC-B input 0 Optional external reference voltage for on-chip DACs
ADCINB1 DACOUTC	W2	47	I O	ADC-B input 1 DAC-C output <sup>(2)</sup>

Table 3-2. Terminal Functions (continued)

TERMINAL			I/O/Z <sup>(1)</sup>	DESCRIPTION
NAME	ZWT BALL NO.	PTP PIN NO.		
ADCINB2 CMPIN3P	V3	48	I I	ADC-B input 2 Comparator 3 positive input
ADCINB3 CMPIN3N	W3	49	I I	ADC-B input 3 Comparator 3 negative input
ADCINB4	V4	–	I	ADC-B input 4
ADCINB5	W4	–	I	ADC-B input 5
ADCINC2 CMPIN6P	R3	31	I I	ADC-C input 2 Comparator 6 positive input
ADCINC3 CMPIN6N	P3	30	I I	ADC-C input 3 Comparator 6 negative input
ADCINC4 CMPIN5P	R4	29	I I	ADC-C input 4 Comparator 5 positive input
ADCINC5 CMPIN5N	P4	–	I I	ADC-C input 5 Comparator 5 negative input
ADCIND0 CMPIN7P	T5	56	I I	ADC-D input 0 Comparator 7 positive input
ADCIND1 CMPIN7N	U5	57	I I	ADC-D input 1 Comparator 7 negative input
ADCIND2 CMPIN8P	T6	58	I I	ADC-D input 2 Comparator 8 positive input
ADCIND3 CMPIN8N	U6	59	I I	ADC-D input 3 Comparator 8 negative input
ADCIND4	T7	60	I	ADC-D input 4
ADCIND5	U7	–	I	ADC-D input 5
<b>GPIO AND PERIPHERAL SIGNALS</b>				
GPIO0 EPWM1A SDAA	C8	160	I/O O I/OD	General-purpose input/output 0. This pin is 5V-tolerant. Enhanced PWM1 output A and HRPWM channel I2C-A data open-drain bidirectional port
GPIO1 EPWM1B MFSRB SCLA	D8	161	I/O O I/O I/OD	General-purpose input/output 1. This pin is 5V-tolerant. Enhanced PWM1 output B and HRPWM channel McBSP-B receive frame synch I2C-A clock open-drain bidirectional port
GPIO2 EPWM2A XTRIPOUT1 SDAB	A7	162	I/O O O I/OD	General-purpose input/output 2. This pin is 5V-tolerant. Enhanced PWM2 output A and HRPWM channel External trigger output 1 I2C-B data open-drain bidirectional port
GPIO3 EPWM2B XTRIPOUT2 MCLKRB XTRIPOUT2 SCLB	B7	163	I/O O O I/O O I/OD	General-purpose input/output 3. This pin is 5V-tolerant. Enhanced PWM2 output B and HRPWM channel External trigger output 2 McBSP-B receive clock External trigger output 2 I2C-B clock open-drain bidirectional port

**Table 3-2. Terminal Functions (continued)**

TERMINAL			I/O/Z <sup>(1)</sup>	DESCRIPTION
NAME	ZWT BALL NO.	PTP PIN NO.		
GPIO4 EPWM3A XTRIPOUT3 CANTXA	C7	164	I/O O O O	General-purpose input/output 4. This pin is 5V-tolerant. Enhanced PWM3 output A and HRPWM channel External trigger output 3 CAN-A transmit
GPIO5 EPWM3B MFSRA XTRIPOUT3 CANRXA	D7	165	I/O O I/O O I	General-purpose input/output 5. This pin is 5V-tolerant. Enhanced PWM3 output B and HRPWM channel McBSP-A receive frame synch External trigger output 3 CAN-A receive
GPIO6 EPWM4A XTRIPOUT4 EPWMSYNCO EQEP3A CANTXB	A6	166	I/O O O O I O	General-purpose input/output 6. This pin is 5V-tolerant. Enhanced PWM4 output A and HRPWM channel External trigger output 4 External ePWM synch pulse output Enhanced QEP3 input A CAN-B transmit
GPIO7 EPWM4B MCLKRA EQEP3B CANRXB	B6	167	I/O O I/O I I	General-purpose input/output 7. This pin is 5V-tolerant. Enhanced PWM4 output B and HRPWM channel McBSP-A receive clock Enhanced QEP3 input B CAN-B receive
GPIO8 EPWM5A CANTXB ADCSOCAO EQEP3S SCITXDA	G2	18	I/O O O O I/O O	General-purpose input/output 8 Enhanced PWM5 output A and HRPWM channel CAN-B transmit ADC start-of-conversion A Enhanced QEP3 strobe SCI-A transmit data
GPIO9 EPWM5B SCITXDB EQEP3I SCIRXDA	G3	19	I/O O O I/O I	General-purpose input/output 9 Enhanced PWM5 output B and HRPWM channel SCI-B transmit data Enhanced QEP3 index SCI-A receive data
GPIO10 EPWM6A CANRXB ADCSOCBO EQEP1A SCITXDB UPP-WAIT	B2	1	I/O O I O I O I/O	General-purpose input/output 10 Enhanced PWM6 output A and HRPWM channel CAN-B receive ADC start-of-conversion B Enhanced QEP1 input A SCI-B transmit data Universal parallel port wait. Receiver asserts to request a pause in transfer.

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Table 3-2. Terminal Functions (continued)

TERMINAL			I/O/Z <sup>(1)</sup>	DESCRIPTION
NAME	ZWT BALL NO.	PTP PIN NO.		
GPIO11	C1	2	I/O	General-purpose input/output 11
EPWM6B			O	Enhanced PWM6 output B and HRPWM channel
SCIRXDB			I	SCI-B receive data
XTRIP0UT7			O	External trigger output 7
EQEP1B			I	Enhanced QEP1 input B
SCIRXDB			I	SCI-B receive data
UPP-STRT			I/O	Universal parallel port start. Transmitter asserts at start of DMA line.
GPIO12	C2	4	I/O	General-purpose input/output 12
EPWM7A			O	Enhanced PWM7 output A and HRPWM channel
CANTXB			O	CAN-B transmit
MDXB			O	McBSP-B transmit serial data
EQEP1S			I/O	Enhanced QEP1 strobe
SCITXDC			O	SCI-C transmit data
UPP-ENA			I/O	Universal parallel port enable. Transmitter asserts while data bus is active.
GPIO13	D1	5	I/O	General-purpose input/output 13
EPWM7B			O	Enhanced PWM7 output B and HRPWM channel
CANRXB			I	CAN-B receive
MDRB			I	McBSP-B receive serial data
EQEP1I			I/O	Enhanced QEP1 index
SCIRXDC			I	SCI-C receive data
UPP-D7			I/O	Universal parallel port data line 7
GPIO14	D2	6	I/O	General-purpose input/output 14
EPWM8A			O	Enhanced PWM8 output A and HRPWM channel
SCITXDB			O	SCI-B transmit data
MCLKXB			I/O	McBSP-B transmit clock
XTRIP0UT3			O	External trigger output 3
UPP-D6			I/O	Universal parallel port data line 6
GPIO15			D3	7
EPWM8B	O	Enhanced PWM8 output B and HRPWM channel		
SCIRXDB	I	SCI-B receive data		
MFSXB	I/O	McBSP-B transmit frame synch		
XTRIP0UT4	O	External trigger output 4		
UPP-D5	I/O	Universal parallel port data line 5		
GPIO16	E1	8		
SPISIMOA			I/O	SPI-A slave in, master out
CANTXB			O	CAN-B transmit
XTRIP0UT7			O	External trigger output 7
EPWM9A			O	Enhanced PWM9 output A and HRPWM channel
SD-D1			I	Sigma-Delta channel 1 data input
UPP-D4			I/O	Universal parallel port data line 4

**Table 3-2. Terminal Functions (continued)**

TERMINAL			I/O/Z <sup>(1)</sup>	DESCRIPTION
NAME	ZWT BALL NO.	PTP PIN NO.		
GPIO17	E2	9	I/O	General-purpose input/output 17
SPISOMIA			I/O	SPI-A slave out, master in
CANRXB			I	CAN-B receive
XTRIPOUT8			O	External trigger output 8
EPWM9B			O	Enhanced PWM9 output B and HRPWM channel
SD-C1			I	Sigma-Delta channel 1 clock input
UPP-D3			I/O	Universal parallel port data line 3
GPIO18	E3	10	I/O	General-purpose input/output 18
SPICLKA			I/O	SPI-A clock
SCITXDB			O	SCI-B transmit data
CANRXA			I	CAN-A receive
EPWM10A			O	Enhanced PWM10 output A and HRPWM channel
SD-D2			I	Sigma-Delta channel 2 data input
UPP-D2			I/O	Universal parallel port data line 2
GPIO19	E4	12	I/O	General-purpose input/output 19
SPISTEA			I/O	SPI-A slave transmit enable
SCIRXDB			I	SCI-B receive data
CANTXA			O	CAN-A transmit
EPWM10B			O	Enhanced PWM10 output B and HRPWM channel
SD-C2			I	Sigma-Delta channel 2 clock input
UPP-D1			I/O	Universal parallel port data line 1
GPIO20	F2	13	I/O	General-purpose input/output 20
EQEP1A			I	Enhanced QEP1 input A
MDXA			O	McBSP-A transmit serial data
CANTXB			O	CAN-B transmit
EPWM11A			O	Enhanced PWM11 output A and HRPWM channel
SD-D3			I	Sigma-Delta channel 3 data input
UPP-D0			I/O	Universal parallel port data line 0
GPIO21	F3	14	I/O	General-purpose input/output 21
EQEP1B			I	Enhanced QEP1 input B
MDRA			I	McBSP-A receive serial data
CANRXB			I	CAN-B receive
EPWM11B			O	Enhanced PWM11 output B and HRPWM channel
SD-C3			I	Sigma-Delta channel 3 clock input
UPP-CLK			I/O	Universal parallel port transmit clock
GPIO22	J4	22	I/O	General-purpose input/output 22
EQEP1S			I/O	Enhanced QEP1 strobe
MCLKXA			I/O	McBSP-A transmit clock
SCITXDB			O	SCI-B transmit data
EPWM12A			O	Enhanced PWM12 output A and HRPWM channel
SPICLKB			I/O	SPI-B clock
SD-D4			I	Sigma-Delta channel 4 data input

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Table 3-2. Terminal Functions (continued)

TERMINAL			I/O/Z <sup>(1)</sup>	DESCRIPTION
NAME	ZWT BALL NO.	PTP PIN NO.		
GPIO23	K4	23	I/O	General-purpose input/output 23
EQEP1I			I/O	Enhanced QEP1 index
MFSXA			I/O	McBSP-A transmit frame synch
SCIRXDB			I	SCI-B receive data
EPWM12B			O	Enhanced PWM12 output B and HRPWM channel
SPISTEB			I/O	SPI-B slave transmit enable
SD-C4			I	Sigma-Delta channel 4 clock input
GPIO24	K3	24	I/O	General-purpose input/output 24
XTRIPOUT1			O	External trigger output 1
EQEP2A			I	Enhanced QEP2 input A
MDXB			O	McBSP-B transmit serial data
SPISIMOB			I/O	SPI-B slave in, master out
SD-D5			I	Sigma-Delta channel 5 data input
GPIO25	K2	25	I/O	General-purpose input/output 25
XTRIPOUT2			O	External trigger output 2
EQEP2B			I	Enhanced QEP2 input B
MDRB			I	McBSP-B receive serial data
SPISOMIB			I/O	SPI-B slave out, master in
SD-C5			I	Sigma-Delta channel 5 clock input
GPIO26	K1	27	I/O	General-purpose input/output 26
XTRIPOUT3			O	External trigger output 3
EQEP2I			I/O	Enhanced QEP2 index
MCLKXB			I/O	McBSP-B transmit clock
XTRIPOUT3			O	External trigger output 3
SPICKB			I/O	SPI-B clock
SD-D6			I	Sigma-Delta channel 6 data input
GPIO27	L1	28	I/O	General-purpose input/output 27
XTRIPOUT4			O	External trigger output 4
EQEP2S			I/O	Enhanced QEP2 strobe
MFSXB			I/O	McBSP-B transmit frame synch
XTRIPOUT4			O	External trigger output 4
SPISTEB			I/O	SPI-B slave transmit enable
SD-C6			I	Sigma-Delta channel 6 clock input
GPIO28	V11	64	I/O	General-purpose input/output 28
SCIRXDA			I	SCI-A receive data
EM1CS4			O	External memory interface 1 chip select 4
EQEP3A			I	Enhanced QEP3 input A
SD-D7			I	Sigma-Delta channel 7 data input
GPIO29	W11	65	I/O	General-purpose input/output 29
SCITXDA			O	SCI-A transmit data
EM1SDCKE			O	External memory interface 1 SDRAM clock enable
EQEP3B			I	Enhanced QEP3 input B
SD-C7			I	Sigma-Delta channel 7 clock input

**Table 3-2. Terminal Functions (continued)**

TERMINAL			I/O/Z <sup>(1)</sup>	DESCRIPTION
NAME	ZWT BALL NO.	PTP PIN NO.		
GPIO30 CANRXA EM1CLK XTRIPOUT7 EQEP3S SD-D8	T11	63	I/O I O O I/O I	General-purpose input/output 30 CAN-A receive External memory interface 1 clock External trigger output 7 Enhanced QEP3 strobe Sigma-Delta channel 8 data input
GPIO31 CANTXA $\overline{\text{EM1WE}}$ XTRIPOUT8 EQEP3I SD-C8	U11	66	I/O O O O I/O I	General-purpose input/output 31 CAN-A transmit External memory interface 1 write enable External trigger output 8 Enhanced QEP3 index Sigma-Delta channel 8 clock input
GPIO32 SDAA $\overline{\text{EM1CS0}}$	U13	67	I/O I/OD O	General-purpose input/output 32 I2C-A data open-drain bidirectional port External memory interface 1 chip select 0
GPIO33 SCLA EM1RNW	T13	69	I/O I/OD O	General-purpose input/output 33 I2C-A clock open-drain bidirectional port External memory interface 1 read not write
GPIO34 XTRIPOUT1 $\overline{\text{EM1CS2}}$ SDAB	U14	70	I/O O O I/OD	General-purpose input/output 34 External trigger output 1 External memory interface 1 chip select 2 I2C-B data open-drain bidirectional port
GPIO35 SCIRXDA $\overline{\text{EM1CS3}}$ SCLB	T14	71	I/O I O I/OD	General-purpose input/output 35 SCI-A receive data External memory interface 1 chip select 3 I2C-B clock open-drain bidirectional port
GPIO36 SCITXDA EM1WAIT CANRXA	V16	83	I/O O I I	General-purpose input/output 36 SCI-A transmit data External memory interface 1 Asynchronous SRAM WAIT CAN-A receive
GPIO37 XTRIPOUT2 $\overline{\text{EM1OE}}$ CANTXA	U16	84	I/O O O O	General-purpose input/output 37 External trigger output 2 External memory interface 1 output enable CAN-A transmit
GPIO38 EM1A0 SCITXDC CANTXB	T16	85	I/O O O O	General-purpose input/output 38 External memory interface 1 address line 0 SCI-C transmit data CAN-B transmit
GPIO39 EM1A1 SCIRXDC CANRXB	W17	86	I/O O I I	General-purpose input/output 39 External memory interface 1 address line 1 SCI-C receive data CAN-B receive
GPIO40 EM1A2 SDAB	V17	87	I/O O I/OD	General-purpose input/output 40 External memory interface 1 address line 2 I2C-B data open-drain bidirectional port

**ADVANCE INFORMATION**

Table 3-2. Terminal Functions (continued)

TERMINAL			I/O/Z <sup>(1)</sup>	DESCRIPTION
NAME	ZWT BALL NO.	PTP PIN NO.		
GPIO41	U17	89	I/O	General-purpose input/output 41
EM1A3			O	External memory interface 1 address line 3
SCLB			I/OD	I2C-B clock open-drain bidirectional port
GPIO42	D19	130	I/O	General-purpose input/output 42. This pin is 5V-tolerant.
SDAA			I/OD	I2C-A data open-drain bidirectional port
SCITXDA			O	SCI-A transmit data
USB0DM			I/O	USB PHY differential data
GPIO43	C19	131	I/O	General-purpose input/output 43. This pin is 5V-tolerant.
SCLA			I/OD	I2C-A clock open-drain bidirectional port
SCIRXDA			I	SCI-A receive data
USB0DP			I/O	USB PHY differential data
GPIO44	K18	113	I/O	General-purpose input/output 44
EM1A4			O	External memory interface 1 address line 4
GPIO45	K19	115	I/O	General-purpose input/output 45
EM1A5			O	External memory interface 1 address line 5
GPIO46	E19	128	I/O	General-purpose input/output 46. This pin is 5V-tolerant.
EM1A6			O	External memory interface 1 address line 6
SCIRXDD			I	SCI-D receive data
USB0VBUS			I/O	USB bus voltage detection
GPIO47	E18	129	I/O	General-purpose input/output 47. This pin is 5V-tolerant.
EM1A7			O	External memory interface 1 address line 7
SCITXDD			O	SCI-D transmit data
USB0ID			I/O	USB OTG host indicator
GPIO48	R16	90	I/O	General-purpose input/output 48
XTRIPOUT3			O	External trigger output 3
EM1A8			O	External memory interface 1 address line 8
SCITXDA			O	SCI-A transmit data
SD-D1			I	Sigma-Delta channel 1 data input
GPIO49	R17	93	I/O	General-purpose input/output 49
XTRIPOUT4			O	External trigger output 4
EM1A9			O	External memory interface 1 address line 9
SCIRXDA			I	SCI-A receive data
SD-C1			I	Sigma-Delta channel 1 clock input
GPIO50	R18	94	I/O	General-purpose input/output 50
EQEP1A			I	Enhanced QEP1 input A
EM1A10			O	External memory interface 1 address line 10
SPISIMOC			I/O	SPI-C slave in, master out
SD-D2			I	Sigma-Delta channel 2 data input
GPIO51	R19	95	I/O	General-purpose input/output 51
EQEP1B			I	Enhanced QEP1 input B
EM1A11			O	External memory interface 1 address line 11
SPISOMIC			I/O	SPI-C slave out, master in
SD-C2			I	Sigma-Delta channel 2 clock input

**Table 3-2. Terminal Functions (continued)**

TERMINAL			I/O/Z <sup>(1)</sup>	DESCRIPTION
NAME	ZWT BALL NO.	PTP PIN NO.		
GPIO52	P16	96	I/O	General-purpose input/output 52
EQEP1S			I/O	Enhanced QEP1 strobe
EM1A12			O	External memory interface 1 address line 12
SPICLK			I/O	SPI-C clock
SD-D3			I	Sigma-Delta channel 3 data input
GPIO53	P17	97	I/O	General-purpose input/output 53
EQEP1I			I/O	Enhanced QEP1 index
EM1D31			I/O	External memory interface 1 data line 31
EM2D15			I/O	External memory interface 2 data line 15
SPISTEC			I/O	SPI-C slave transmit enable
SD-C3	I	Sigma-Delta channel 3 clock input		
GPIO54	P18	98	I/O	General-purpose input/output 54
SPISIMOA			I/O	SPI-A slave in, master out
EM1D30			I/O	External memory interface 1 data line 30
EM2D14			I/O	External memory interface 2 data line 14
EQEP2A			I	Enhanced QEP2 input A
SCITXDB			O	SCI-B transmit data
SD-D4	I	Sigma-Delta channel 4 data input		
GPIO55	P19	100	I/O	General-purpose input/output 55
SPISOMIA			I/O	SPI-A slave out, master in
EM1D29			I/O	External memory interface 1 data line 29
EM2D13			I/O	External memory interface 2 data line 13
EQEP2B			I	Enhanced QEP2 input B
SCIRXDB			I	SCI-B receive data
SD-C4	I	Sigma-Delta channel 4 clock input		
GPIO56	N16	101	I/O	General-purpose input/output 56
SPICLKA			I/O	SPI-A clock
EM1D28			I/O	External memory interface 1 data line 28
EM2D12			I/O	External memory interface 2 data line 12
EQEP2S			I/O	Enhanced QEP2 strobe
SCITXDC			O	SCI-C transmit data
SD-D5	I	Sigma-Delta channel 5 data input		
GPIO57	N18	102	I/O	General-purpose input/output 57
SPISTEA			I/O	SPI-A slave transmit enable
EM1D27			I/O	External memory interface 1 data line 27
EM2D11			I/O	External memory interface 2 data line 11
EQEP2I			I/O	Enhanced QEP2 index
SCIRXDC			I	SCI-C receive data
SD-C5	I	Sigma-Delta channel 5 clock input		

**ADVANCE INFORMATION**

Table 3-2. Terminal Functions (continued)

TERMINAL			I/O/Z <sup>(1)</sup>	DESCRIPTION
NAME	ZWT BALL NO.	PTP PIN NO.		
GPIO58	N17	103	I/O	General-purpose input/output 58
MCLKRA			I/O	McBSP-A receive clock
EM1D26			I/O	External memory interface 1 data line 26
EM2D10			I/O	External memory interface 2 data line 10
XTRIPOUT1			O	External trigger output 1
SPICLKB			I/O	SPI-B clock
SD-D6			I	Sigma-Delta channel 6 data input
SPISIMOA			I/O	SPI-A slave in, master out
GPIO59	M16	104	I/O	General-purpose input/output 59 <sup>(3)</sup>
MFSRA			I/O	McBSP-A receive frame synch
EM1D25			I/O	External memory interface 1 data line 25
EM2D9			I/O	External memory interface 2 data line 9
XTRIPOUT2			O	External trigger output 2
SPISTEB			I/O	SPI-B slave transmit enable
SD-C6			I	Sigma-Delta channel 6 clock input
SPISOMIA			I/O	SPI-A slave out, master in
GPIO60	M17	105	I/O	General-purpose input/output 60
MCLKRB			I/O	McBSP-B receive clock
EM1D24			I/O	External memory interface 1 data line 24
EM2D8			I/O	External memory interface 2 data line 8
XTRIPOUT3			O	External trigger output 3
SPISIMOB			I/O	SPI-B slave in, master out
SD-D7			I	Sigma-Delta channel 7 data input
SPICLKA			I/O	SPI-A clock
GPIO61	L16	107	I/O	General-purpose input/output 61 <sup>(3)</sup>
MFSRB			I/O	McBSP-B receive frame synch
EM1D23			I/O	External memory interface 1 data line 23
EM2D7			I/O	External memory interface 2 data line 7
XTRIPOUT4			O	External trigger output 4
SPISOMIB			I/O	SPI-B slave out, master in
SD-C7			I	Sigma-Delta channel 7 clock input
SPISTEA			I/O	SPI-A slave transmit enable
GPIO62	J17	108	I/O	General-purpose input/output 62
SCIRXDC			I	SCI-C receive data
EM1D22			I/O	External memory interface 1 data line 22
EM2D6			I/O	External memory interface 2 data line 6
EQEP3A			I	Enhanced QEP3 input A
CANRXA			I	CAN-A receive
SD-D8			I	Sigma-Delta channel 8 data input

**Table 3-2. Terminal Functions (continued)**

TERMINAL			I/O/Z <sup>(1)</sup>	DESCRIPTION
NAME	ZWT BALL NO.	PTP PIN NO.		
GPIO63	J16	109	I/O	General-purpose input/output 63
SCITXDC			O	SCI-C transmit data
EM1D21			I/O	External memory interface 1 data line 21
EM2D5			I/O	External memory interface 2 data line 5
EQEP3B			I	Enhanced QEP3 input B
CANTXA			O	CAN-A transmit
SD-C8			I	Sigma-Delta channel 8 clock input
SPISIMOB			I/O	SPI-B slave in, master out
GPIO64	L17	110	I/O	General-purpose input/output 64 <sup>(3)</sup>
EM1D20			I/O	External memory interface 1 data line 20
EM2D4			I/O	External memory interface 2 data line 4
EQEP3S			I/O	Enhanced QEP3 strobe
SCIRXDA			I	SCI-A receive data
SPISOMIB			I/O	SPI-B slave out, master in
GPIO65	K16	111	I/O	General-purpose input/output 65
EM1D19			I/O	External memory interface 1 data line 19
EM2D3			I/O	External memory interface 2 data line 3
EQEP3I			I/O	Enhanced QEP3 index
SCITXDA			O	SCI-A transmit data
SPICLKB			I/O	SPI-B clock
GPIO66	K17	112	I/O	General-purpose input/output 66 <sup>(3)</sup>
EM1D18			I/O	External memory interface 1 data line 18
EM2D2			I/O	External memory interface 2 data line 2
SDAB			I/OD	I2C-B data open-drain bidirectional port
SPISTEB			I/O	SPI-B slave transmit enable
GPIO67	B19	132	I/O	General-purpose input/output 67
EM1D17			I/O	External memory interface 1 data line 17
EM2D1			I/O	External memory interface 2 data line 1
GPIO68	C18	133	I/O	General-purpose input/output 68
EM1D16			I/O	External memory interface 1 data line 16
EM2D0			I/O	External memory interface 2 data line 0
GPIO69	B18	134	I/O	General-purpose input/output 69
EM1D15			I/O	External memory interface 1 data line 15
SCLB			I/OD	I2C-B clock open-drain bidirectional port
SPISIMOC			I/O	SPI-C slave in, master out
GPIO70	A17	135	I/O	General-purpose input/output 70 <sup>(3)</sup>
EM1D14			I/O	External memory interface 1 data line 14
CANRXA			I	CAN-A receive
SCITXDB			O	SCI-B transmit data
SPISOMIC			I/O	SPI-C slave out, master in
GPIO71	B17	136	I/O	General-purpose input/output 71
EM1D13			I/O	External memory interface 1 data line 13
CANTXA			O	CAN-A transmit
SCIRXDB			I	SCI-B receive data
SPICLKC			I/O	SPI-C clock

Table 3-2. Terminal Functions (continued)

TERMINAL			I/O/Z <sup>(1)</sup>	DESCRIPTION
NAME	ZWT BALL NO.	PTP PIN NO.		
GPIO72	B16	139	I/O	General-purpose input/output 72 <sup>(3)</sup>
EM1D12			I/O	External memory interface 1 data line 12
CANTXB			O	CAN-B transmit
SCITXDC			O	SCI-C transmit data
SPISTEC			I/O	SPI-C slave transmit enable
GPIO73	A16	140	I/O	General-purpose input/output 73
EM1D11			I/O	External memory interface 1 data line 11
XCLKOUT			O/Z	External oscillator output. This pin outputs a divided-down version of the internal PLL system clock. The divide ratio is defined in the XCLKOUTDIVSEL register. Unlike other GPIO pins, the XCLKOUT pin is not placed in high-impedance state during a reset.
CANRXB			I	CAN-B receive
SCIRXDC			I	SCI-C receive
GPIO74	C17	141	I/O	General-purpose input/output 74
EM1D10			I/O	External memory interface 1 data line 10
GPIO75	D16	142	I/O	General-purpose input/output 75
EM1D9			I/O	External memory interface 1 data line 9
GPIO76	C16	143	I/O	General-purpose input/output 76
EM1D8			I/O	External memory interface 1 data line 8
SCITXDD			O	SCI-D transmit data
GPIO77	A15	144	I/O	General-purpose input/output 77
EM1D7			I/O	External memory interface 1 data line 7
SCIRXDD			I	SCI-D receive data
GPIO78	B15	145	I/O	General-purpose input/output 78
EM1D6			I/O	External memory interface 1 data line 6
EQEP2A			I	Enhanced QEP2 input A
GPIO79	C15	146	I/O	General-purpose input/output 79
EM1D5			I/O	External memory interface 1 data line 5
EQEP2B			I	Enhanced QEP2 input B
GPIO80	D15	148	I/O	General-purpose input/output 80
EM1D4			I/O	External memory interface 1 data line 4
EQEP2S			I/O	Enhanced QEP2 strobe
GPIO81	A14	149	I/O	General-purpose input/output 81
EM1D3			I/O	External memory interface 1 data line 3
EQEP2I			I/O	Enhanced QEP2 index
GPIO82	B14	150	I/O	General-purpose input/output 82
EM1D2			I/O	External memory interface 1 data line 2
GPIO83	C14	151	I/O	General-purpose input/output 83
EM1D1			I/O	External memory interface 1 data line 1
GPIO84	A11	154	I/O	General-purpose input/output 84
SCITXDA			O	SCI-A transmit data
MDXB			O	McBSP-B transmit serial data
MDXA			O	McBSP-A transmit serial data

**Table 3-2. Terminal Functions (continued)**

TERMINAL			I/O/Z <sup>(1)</sup>	DESCRIPTION
NAME	ZWT BALL NO.	PTP PIN NO.		
GPIO85	B11	155	I/O	General-purpose input/output 85
EM1D0			I/O	External memory interface 1 data line 0
SCIRXDA			I	SCI-A receive data
MDRB			I	McBSP-B receive serial data
MDRA			I	McBSP-A receive serial data
GPIO86	C11	156	I/O	General-purpose input/output 86
EM1A13			O	External memory interface 1 address line 13
EM1CAS			O	External memory interface 1 column address strobe
SCITXDB			O	SCI-B transmit data
MCLKXB			I/O	McBSP-B transmit clock
MCLKXA			I/O	McBSP-A transmit clock
GPIO87	D11	157	I/O	General-purpose input/output 87
EM1A14			O	External memory interface 1 address line 14
EM1RAS			O	External memory interface 1 row address strobe
SCIRXDB			I	SCI-B receive data
MFSXB			I/O	McBSP-B transmit frame synch
MFSXA			I/O	McBSP-A transmit frame synch
GPIO88	C6	170	I/O	General-purpose input/output 88
EM1A15			O	External memory interface 1 address line 15
EM1DQM0			O	External memory interface 1 Input/output mask for byte 0
GPIO89	D6	171	I/O	General-purpose input/output 89
EM1A16			O	External memory interface 1 address line 16
EM1DQM1			O	External memory interface 1 Input/output mask for byte 1
SCITXDC			O	SCI-C transmit data
GPIO90	A5	172	I/O	General-purpose input/output 90
EM1A17			O	External memory interface 1 address line 17
EM1DQM2			O	External memory interface 1 Input/output mask for byte 2
SCIRXDC			I	SCI-C receive data
GPIO91	B5	173	I/O	General-purpose input/output 91
EM1A18			O	External memory interface 1 address line 18
EM1DQM3			O	External memory interface 1 Input/output mask for byte 3
SDAA			I/OD	I2C-A data open-drain bidirectional port
GPIO92	A4	174	I/O	General-purpose input/output 92
EM1A19			O	External memory interface 1 address line 19
EM1BA1			O	External memory interface 1 bank address 1
SCLA			I/OD	I2C-A clock open-drain bidirectional port
GPIO93	B4	175	I/O	General-purpose input/output 93
EM1A20			O	External memory interface 1 address line 20
EM1BA0			O	External memory interface 1 bank address 0
SCITXDD			O	SCI-D transmit data
GPIO94	A3	176	I/O	General-purpose input/output 94
EM1A21			O	External memory interface 1 address line 21
SCIRXDD			I	SCI-D receive data
GPIO95	B3	–	I/O	General-purpose input/output 95

Table 3-2. Terminal Functions (continued)

TERMINAL			I/O/Z <sup>(1)</sup>	DESCRIPTION
NAME	ZWT BALL NO.	PTP PIN NO.		
GPIO96			I/O	General-purpose input/output 96
EM2DQM1	C3	–	O	External memory interface 2 Input/output mask for byte 1
EQEP1A			I	Enhanced QEP1 input A
GPIO97			I/O	General-purpose input/output 97
EM2DQM0	A2	–	O	External memory interface 2 Input/output mask for byte 0
EQEP1B			I	Enhanced QEP1 input B
GPIO98			I/O	General-purpose input/output 98
EM2A0	F1	–	O	External memory interface 2 address line 0
EQEP1S			I/O	Enhanced QEP1 strobe
GPIO99			I/O	General-purpose input/output 99
EM2A1	G1	17	O	External memory interface 2 address line 1
EQEP1I			I/O	Enhanced QEP1 index
GPIO100			I/O	General-purpose input/output 100
EM2A2	H1	–	O	External memory interface 2 address line 2
EQEP2A			I	Enhanced QEP2 input A
SPISIMOC			I/O	SPI-C slave in, master out
GPIO101			I/O	General-purpose input/output 101
EM2A3	H2	–	O	External memory interface 2 address line 3
EQEP2B			I	Enhanced QEP2 input B
SPISOMIC			I/O	SPI-C slave out, master in
GPIO102			I/O	General-purpose input/output 102
EM2A4	H3	–	O	External memory interface 2 address line 4
EQEP2S			I/O	Enhanced QEP2 strobe
SPICLK			I/O	SPI-C clock
GPIO103			I/O	General-purpose input/output 103
EM2A5	J1	–	O	External memory interface 2 address line 5
EQEP2I			I/O	Enhanced QEP2 index
SPISTEC			I/O	SPI-C slave transmit enable
GPIO104			I/O	General-purpose input/output 104
SDAA			I/OD	I2C-A data open-drain bidirectional port
EM2A6	J2	–	O	External memory interface 2 address line 6
EQEP3A			I	Enhanced QEP3 input A
SCITXDD			O	SCI-D transmit data
GPIO105			I/O	General-purpose input/output 105
SCLA			I/OD	I2C-A clock open-drain bidirectional port
EM2A7	J3	–	O	External memory interface 2 address line 7
EQEP3B			I	Enhanced QEP3 input B
SCIRXDD			I	SCI-D receive data
GPIO106			I/O	General-purpose input/output 106
EM2A8	L2	–	O	External memory interface 2 address line 8
EQEP3S			I/O	Enhanced QEP3 strobe
SCITXDC			O	SCI-C transmit data

**Table 3-2. Terminal Functions (continued)**

TERMINAL			I/O/Z <sup>(1)</sup>	DESCRIPTION
NAME	ZWT BALL NO.	PTP PIN NO.		
GPIO107	L3	–	I/O	General-purpose input/output 107
EM2A9			O	External memory interface 2 address line 9
EQEP3I			I/O	Enhanced QEP3 index
SCIRXDC			I	SCI-C receive data
GPIO108	L4	–	I/O	General-purpose input/output 108
EM2A10			O	External memory interface 2 address line 10
GPIO109	N2	–	I/O	General-purpose input/output 109
EM2A11			O	External memory interface 2 address line 11
GPIO110	M2	–	I/O	General-purpose input/output 110
GPIO111	M4	–	I/O	General-purpose input/output 111
EM2BA0			O	External memory interface 2 bank address 0
GPIO112	M3	–	I/O	General-purpose input/output 112
EM2BA1			O	External memory interface 2 bank address 1
GPIO113	N4	–	I/O	General-purpose input/output 113
EM2CAS			O	External memory interface 2 column address strobe
GPIO114	N3	–	I/O	General-purpose input/output 114
EM2RAS			O	External memory interface 2 row address strobe
GPIO115	V12	–	I/O	General-purpose input/output 115
GPIO116	W10	–	I/O	General-purpose input/output 116
GPIO117	U12	–	I/O	General-purpose input/output 117
GPIO118	T12	–	I/O	General-purpose input/output 118
GPIO119	T15	–	I/O	General-purpose input/output 119
EM2RNW			O	External memory interface 2 read not write
GPIO120	U15	–	I/O	General-purpose input/output 120
EM2WE			O	External memory interface 2 write enable
USB0PFLT			I/O	USB external regulator power fault indicator
GPIO121	W16	–	I/O	General-purpose input/output 121
USB0EPEN			I/O	USB external regulator enable
GPIO122	T8	–	I/O	General-purpose input/output 122
SPISIMOC			I/O	SPI-C slave in, master out
SD-D1			I	Sigma-Delta channel 1 data input
GPIO123	U8	–	I/O	General-purpose input/output 123
SPISOMIC			I/O	SPI-C slave out, master in
SD-C1			I	Sigma-Delta channel 1 clock input
GPIO124	V8	–	I/O	General-purpose input/output 124
SPICLK			I/O	SPI-C clock
SD-D2			I	Sigma-Delta channel 2 data input
GPIO125	T9	–	I/O	General-purpose input/output 125
SPISTEC			I/O	SPI-C slave transmit enable
SD-C2			I	Sigma-Delta channel 2 clock input
GPIO126	U9	–	I/O	General-purpose input/output 126
SD-D3			I	Sigma-Delta channel 3 data input
GPIO127	V9	–	I/O	General-purpose input/output 127
SD-C3			I	Sigma-Delta channel 3 clock input

**ADVANCE INFORMATION**

Table 3-2. Terminal Functions (continued)

TERMINAL			I/O/Z <sup>(1)</sup>	DESCRIPTION
NAME	ZWT BALL NO.	PTP PIN NO.		
GPIO128 SD-D4	W9	–	I/O I	General-purpose input/output 128 Sigma-Delta channel 4 data input
GPIO129 SD-C4	T10	–	I/O I	General-purpose input/output 129 Sigma-Delta channel 4 clock input
GPIO130 SD-D5	U10	–	I/O I	General-purpose input/output 130 Sigma-Delta channel 5 data input
GPIO131 SD-C5	V10	–	I/O I	General-purpose input/output 131 Sigma-Delta channel 5 clock input
GPIO132 SD-D6	W18	–	I/O I	General-purpose input/output 132 Sigma-Delta channel 6 data input
GPIO133/AUXCLKIN SD-C6	G18	118	I/O I	General-purpose input/output 133 Sigma-Delta channel 6 clock input
GPIO134 SD-D7	V18	–	I/O I	General-purpose input/output 134 Sigma-Delta channel 7 data input
GPIO135 SCITXDA SD-C7	U18	–	I/O O I	General-purpose input/output 135 SCI-A transmit data Sigma-Delta channel 7 clock input
GPIO136 SCIRXDA SD-D8	T17	–	I/O I I	General-purpose input/output 136 SCI-A receive data Sigma-Delta channel 8 data input
GPIO137 SCITXDB SD-C8	T18	–	I/O O I	General-purpose input/output 137 SCI-B transmit data Sigma-Delta channel 8 clock input
GPIO138 SCIRXDB	T19	–	I/O I	General-purpose input/output 138 SCI-B receive data
GPIO139 SCIRXDC	N19	–	I/O I	General-purpose input/output 139 SCI-C receive data
GPIO140 SCITXDC	M19	–	I/O O	General-purpose input/output 140 SCI-C transmit data
GPIO141 SCIRXDD	M18	–	I/O I	General-purpose input/output 141 SCI-D receive data
GPIO142 SCITXDD	L19	–	I/O O	General-purpose input/output 142 SCI-D transmit data
GPIO143	F18	–	I/O	General-purpose input/output 143
GPIO144	F17	–	I/O	General-purpose input/output 144
GPIO145 EPWM1A	E17	–	I/O O	General-purpose input/output 145 Enhanced PWM1 output A and HRPWM channel
GPIO146 EPWM1B	D18	–	I/O O	General-purpose input/output 146 Enhanced PWM1 output B and HRPWM channel
GPIO147 EPWM2A	D17	–	I/O O	General-purpose input/output 147 Enhanced PWM2 output A and HRPWM channel
GPIO148 EPWM2B	D14	–	I/O O	General-purpose input/output 148 Enhanced PWM2 output B and HRPWM channel
GPIO149 EPWM3A	A13	–	I/O O	General-purpose input/output 149 Enhanced PWM3 output A and HRPWM channel

**Table 3-2. Terminal Functions (continued)**

TERMINAL			I/O/Z <sup>(1)</sup>	DESCRIPTION
NAME	ZWT BALL NO.	PTP PIN NO.		
GPIO150 EPWM3B	B13	–	I/O O	General-purpose input/output 150 Enhanced PWM3 output B and HRPWM channel
GPIO151 EPWM4A	C13	–	I/O O	General-purpose input/output 151 Enhanced PWM4 output A and HRPWM channel
GPIO152 EPWM4B	D13	–	I/O O	General-purpose input/output 152 Enhanced PWM4 output B and HRPWM channel
GPIO153 EPWM5A	A12	–	I/O O	General-purpose input/output 153 Enhanced PWM5 output A and HRPWM channel
GPIO154 EPWM5B	B12	–	I/O O	General-purpose input/output 154 Enhanced PWM5 output B and HRPWM channel
GPIO155 EPWM6A	C12	–	I/O O	General-purpose input/output 155 Enhanced PWM6 output A and HRPWM channel
GPIO156 EPWM6B	D12	–	I/O O	General-purpose input/output 156 Enhanced PWM6 output B and HRPWM channel
GPIO157 EPWM7A	B10	–	I/O O	General-purpose input/output 157 Enhanced PWM7 output A and HRPWM channel
GPIO158 EPWM7B	C10	–	I/O O	General-purpose input/output 158 Enhanced PWM7 output B and HRPWM channel
GPIO159 EPWM8A	D10	–	I/O O	General-purpose input/output 159 Enhanced PWM8 output A and HRPWM channel
GPIO160 EPWM8B	B9	–	I/O O	General-purpose input/output 160 Enhanced PWM8 output B and HRPWM channel
GPIO161 EPWM9A	C9	–	I/O O	General-purpose input/output 161 Enhanced PWM9 output A
GPIO162 EPWM9B	D9	–	I/O O	General-purpose input/output 162 Enhanced PWM9 output B
GPIO163 EPWM10A	A8	–	I/O O	General-purpose input/output 163 Enhanced PWM10 output A
GPIO164 EPWM10B	B8	–	I/O O	General-purpose input/output 164 Enhanced PWM10 output B
GPIO165 EPWM11A	C5	–	I/O O	General-purpose input/output 165 Enhanced PWM11 output A
GPIO166 EPWM11B	D5	–	I/O O	General-purpose input/output 166 Enhanced PWM11 output B
GPIO167 EPWM12A	C4	–	I/O O	General-purpose input/output 167 Enhanced PWM12 output A
GPIO168 EPWM12B	D4	–	I/O O	General-purpose input/output 168 Enhanced PWM12 output B

Table 3-2. Terminal Functions (continued)

TERMINAL			I/O/Z <sup>(1)</sup>	DESCRIPTION
NAME	ZWT BALL NO.	PTP PIN NO.		
<b>RESET</b>				
$\overline{\text{XRS}}$	F19	124	I/OD	Device reset (in) and watchdog reset (out). F2837xD devices have built-in power-on reset (POR) circuitry. During a power-on condition, this pin is driven low by the device. This pin is also driven low by the MCU when a watchdog or NMI watchdog reset occurs. During watchdog reset, the XRS pin is driven low for 512 INTOSC1 cycles. External circuitry may also drive this pin to assert a device reset. In this case, it is recommended that this pin be driven by an open-drain device. An R-C circuit must be connected to this pin for noise immunity reasons. Regardless of the source, a device reset causes the device to terminate execution. When reset is deactivated, execution begins at the reset vector in the boot ROM. The output buffer of this pin is an open-drain with an internal pullup. This pin has an internal 300-ns (nominal) glitch filter.
<b>CLOCKS</b>				
X1	G19	123	I	On-chip crystal-oscillator input. To use this oscillator, a quartz crystal must be connected across X1 and X2. If this pin is not used, it must be tied to GND. This pin can also be used to feed a single-ended 3.3-V level clock (up to 150 MHz, 45/55% duty cycle). In this case, X2 is a No Connect (NC).
X2	J19	121	O	On-chip crystal-oscillator output. A quartz crystal may be connected across X1 and X2. If X2 is not used, it must be left unconnected.
<b>NO CONNECT</b>				
NC	H4	–		No connect. BGA ball is electrically open and not connected to the die.
<b>JTAG</b>				
TCK	V15	81	I	JTAG test clock with a weak internal pullup (see <a href="#">Section 4.3</a> )
TDI	W13	77	I	JTAG test data input (TDI) with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
TDO	W15	78	O/Z	JTAG scan out, test data output (TDO). The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. (6-mA drive). <sup>(3)</sup>
TMS	W14	80	I	JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK.
$\overline{\text{TRST}}$	V14	79	I	JTAG test reset with internal pulldown. $\overline{\text{TRST}}$ , when driven high, gives the scan system control of the operations of the device. If this signal is not connected or driven low, the device operates in its functional mode, and the test reset signals are ignored. NOTE: $\overline{\text{TRST}}$ is an active-low test pin and must be maintained low at all times during normal device operation. An external pulldown resistor is required on this pin. The value of this resistor should be based on drive strength of the debugger pods applicable to the design. A 2.2-k $\Omega$ resistor generally offers adequate protection. Since the value of the resistor is application-specific, TI recommends that each target board be validated for proper operation of the debugger and the application. This pin has an internal 50-ns (nominal) glitch filter.
<b>INTERNAL VOLTAGE REGULATOR CONTROL</b>				
VREGENZ	J18	119	I	Pull high to the V <sub>DDIO</sub> rail with a 2.2-k $\Omega$ external pullup resistor. The VREG is not supported.

**Table 3-2. Terminal Functions (continued)**

TERMINAL			I/O/Z <sup>(1)</sup>	DESCRIPTION
NAME	ZWT BALL NO.	PTP PIN NO.		
<b>ANALOG, DIGITAL, AND I/O POWER</b>				
V <sub>DD</sub>	E9	16		1.2-V digital logic power pins. Place a minimum 422-nF decoupling capacitor on each V <sub>DD</sub> pin. Higher value capacitors may be used but could impact supply rail ramp-up time.
	E11	21		
	F9	61		
	F11	76		
	G14	117		
	G15	126		
	J14	137		
	J15	153		
	K5	158		
	K6	169		
	P10	–		
	P13	–		
	R10	–		
	R13	–		
V <sub>DD3VFL</sub>	R11	72		3.3-V Flash power pin. Place a minimum 0.1-μF decoupling capacitor on each pin.
	R12	–		
V <sub>DDA</sub>	P6	36		3.3-V analog power pins. Place a minimum 2.2-μF decoupling capacitor on each pin.
	R6	54		

**ADVANCE INFORMATION**

Table 3-2. Terminal Functions (continued)

TERMINAL			I/O/Z <sup>(1)</sup>	DESCRIPTION
NAME	ZWT BALL NO.	PTP PIN NO.		
V <sub>DDIO</sub>	A9	3		3.3-V digital I/O power pins. Place a minimum 0.1- $\mu$ F decoupling capacitor on each pin.
	A18	11		
	B1	15		
	E7	20		
	E10	26		
	E13	62		
	E16	68		
	F4	75		
	F7	82		
	F10	88		
	F13	91		
	F16	99		
	G4	106		
	G5	114		
	G6	116		
	H5	127		
	H6	138		
	L14	147		
	L15	152		
	M1	159		
	M5	168		
M6	–			
N14	–			
N15	–			
P9	–			
R9	–			
V19	–			
W8	–			
V <sub>DDOSC</sub>	H16	120		3.3-V on-chip oscillator power pins. Place a minimum 0.1- $\mu$ F decoupling capacitor on each pin.
	H17	125		

**Table 3-2. Terminal Functions (continued)**

TERMINAL			I/O/Z <sup>(1)</sup>	DESCRIPTION
NAME	ZWT BALL NO.	PTP PIN NO.		
V <sub>SS</sub>	A1	PWR PAD		Analog and digital ground. For Quad Flatpacks (QFPs), the PowerPad™ on the bottom of the package must be soldered to the ground plane of the PCB.
	A10			
	A19			
	E5			
	E6			
	E8			
	E12			
	E14			
	E15			
	F5			
	F6			
	F8			
	F12			
	F14			
	F15			
	G16			
	G17			
	H8			
	H9			
	H10			
	H11			
	H12			
	H14			
	H15			
	J5			
	J6			
	J8			
	J9			
	J10			
	J11			
	J12			
	K8			
	K9			
K10				
K11				
K12				
K14				
K15				
L5				
L6				
L8				
L9				

**ADVANCE INFORMATION**

Table 3-2. Terminal Functions (continued)

TERMINAL			I/O/Z <sup>(1)</sup>	DESCRIPTION
NAME	ZWT BALL NO.	PTP PIN NO.		
V <sub>SS</sub>	L10	PWR PAD		Analog and digital ground power pad (located on the bottom of the chip for quad flatpacks).
	L11			
	L12			
	L18			
	M8			
	M9			
	M10			
	M11			
	M12			
	M14			
	M15			
	N1			
	N5			
	N6			
	P7			
	P8			
	P11			
	P12			
	P14			
	P15			
V <sub>SSOSC</sub>	H18	122		Clock oscillator ground pin. When using an external crystal, do not connect this pin to the board ground. Instead, connect it to the ground reference of the external crystal oscillator circuit. If an external crystal is not used, this pin may be connected to the board ground.
	H19	–		
V <sub>SSA</sub>	P1	34		Analog module ground pins
	P5	52		
	R5	–		
	V7	–		
	W1	–		
<b>SPECIAL FUNCTIONS</b>				
ERRORSTS	U19	92	O	Error status output. This pin has a weak pulldown.
<b>TEST PINS</b>				
FLT1	W12	73	I/O	Flash test pin 1. Reserved for TI. Must be left unconnected.
FLT2	V13	74	I/O	Flash test pin 2. Reserved for TI. Must be left unconnected.

(1) I = Input, O = Output, OD = Open Drain, Z = High Impedance

(2) 100 kΩ of pulldown is present on the pin when the DAC output is active; 50 kΩ of pulldown is present on the pin when the DAC output is inactive.

(3) This pin has output impedance that can be as low as 22Ω. This output could have fast edges and ringing depending on the system PCB characteristics. If this is a concern, the user should take precautions such as adding a 39Ω (10% tolerance) series termination resistor or implement some other termination scheme. It is also recommended that a system-level signal integrity analysis be performed with the provided IBIS models. The termination is not required if this pin is used for input function.

## 4 Device Operating Conditions

### 4.1 Absolute Maximum Ratings<sup>(1) (2)</sup>

Supply voltage range, $V_{DDIO}$	with respect to $V_{SS}$	-0.3 V to 4.6 V
Supply voltage range, $V_{DDSFL}$	with respect to $V_{SS}$	-0.3 V to 4.6 V
Supply voltage range, $V_{DDOSC}$	with respect to $V_{SS}$	-0.3 V to 4.6 V
Supply voltage range, $V_{DD}$	with respect to $V_{SS}$	-0.3 V to 1.5 V
Analog voltage range, $V_{DDA}$	with respect to $V_{SSA}$	-0.3 V to 4.6 V
Supply ramp rate ( $V_{DDIO}$ , $V_{DD}$ , $V_{DDA}$ , $V_{DDSFL}$ , $V_{DDOSC}$ )	with respect to $V_{SS}$	$< 10^5$ V/s
Input voltage range, $V_{IN}$ (3.3 V)		-0.3 V to 4.6 V
Input voltage range, $V_{IN}$ (5 V)		-0.3 V to 5.25 V
Output voltage range, $V_O$		-0.3 V to 4.6 V
Input clamp current, $I_{IK}$ ( $V_{IN} < 0$ or $V_{IN} > V_{DDIO}$ ) <sup>(3)</sup>		$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{DDIO}$ )		$\pm 20$ mA
Free-Air temperature, $T_A$		-40°C to 125°C
Storage temperature range, $T_{stg}$ <sup>(4)</sup>		-65°C to 150°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Section 4.2](#) is not implied. Exposure to conditions with absolute maximum ratings for extended periods may affect device reliability.
- (2) All voltage values are with respect to  $V_{SS}$ , unless otherwise noted.
- (3) Continuous clamp current per pin is  $\pm 2$  mA.
- (4) Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see *IC Package Thermal Metrics Application Report* (literature number [SPRA953](#)).

### 4.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Device supply voltage, I/O, $V_{DDIO}$ <sup>(1)</sup>		3.14	3.3	3.47	V
Device supply voltage, $V_{DD}$		1.14	1.2	1.26	V
Supply ground, $V_{SS}$			0		V
Analog supply voltage, $V_{DDA}$ <sup>(1)</sup>		3.14	3.3	3.47	V
Analog ground, $V_{SSA}$			0		V
Device clock frequency (system clock)			2	200	MHz
High-level input voltage, $V_{IH}$ (5V-tolerant IOs)			$V_{DDIO} * 0.7$	5.25	V
High-level input voltage, $V_{IH}$ (3.3 V)			$V_{DDIO} * 0.7$	$V_{DDIO} + 0.3$	V
Low-level input voltage, $V_{IL}$ (3.3 V)			$V_{SS} - 0.3$	$V_{DDIO} * 0.3$	V
High-level output source current, $I_{OH}$ , for all GPIO pins	$V_{OH} = V_{OH(MIN)}$			-4	mA
Low-level output sink current, $I_{OL}$ , for all GPIO pins	$V_{OL} = V_{OL(MAX)}$			4	mA
Free-Air temperature, $T_A$	T version	-40		105	°C
	S version	-40		125	
	Q version (Q100 qualification)	-40		125	

- (1)  $V_{DDIO}$ ,  $V_{DDSFL}$ ,  $V_{DDOSC}$ , and  $V_{DDA}$  should be maintained within approximately 0.3 V of each other.

### 4.3 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = I <sub>OH</sub> MAX		V <sub>DDIO</sub> * 0.8			V
		I <sub>OH</sub> = 50 μA		V <sub>DDIO</sub> - 0.2			
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = I <sub>OL</sub> MAX		V <sub>DDIO</sub> * 0.2			V
I <sub>IL</sub>	Input current (low level)	Pin with pullup enabled	V <sub>DDIO</sub> = 3.3 V, V <sub>IN</sub> = 0 V	All GPIO pins	-140		μA
				$\overline{\text{XRS}}$ pin	-300		
		Pin with pulldown enabled	V <sub>DDIO</sub> = 3.3 V, V <sub>IN</sub> = 0 V	±2			
I <sub>IH</sub>	Input current (high level)	Pin with pullup enabled	V <sub>DDIO</sub> = 3.3 V, V <sub>IN</sub> = V <sub>DDIO</sub>	±2		μA	
		Pin with pulldown enabled	V <sub>DDIO</sub> = 3.3 V, V <sub>IN</sub> = V <sub>DDIO</sub>	50			
I <sub>OZ</sub>	Output current, pullup or pulldown disabled	V <sub>O</sub> = V <sub>DDIO</sub> or 0 V		±2		μA	
C <sub>I</sub>	Input capacitance			2		pF	

## 4.4 Current Consumption

**Table 4-1. Typical Current Consumption at 200 MHz**

MODE	TEST CONDITIONS <sup>(1) (2)</sup>	VREG DISABLED			
		I <sub>DD</sub>	I <sub>DDIO</sub> <sup>(3)</sup>	I <sub>DDA</sub>	I <sub>DD3VFL</sub>
Operational (RAM)	The following peripherals are exercised: <ul style="list-style-type: none"> <li>ePWM1 to ePWM12</li> <li>eCAP1 to eCAP6</li> <li>CAN-A, CAN-B</li> <li>SPI-A to SPI-C</li> <li>SCI-A to SCI-D</li> <li>I<sup>2</sup>C-A, I<sup>2</sup>C-B</li> <li>McBSP-A</li> <li>USB</li> <li>ADC-A to ADC-D</li> <li>DAC-A to DAC-C</li> <li>CMPSS1 to CMPSS8</li> <li>uPP</li> <li>CPU1.CLA1, CPU2.CLA1</li> <li>CPU1.DMA, CPU2.DMA</li> <li>CPU1.TIMER0, CPU1.TIMER1, CPU1.TIMER2</li> <li>CPU2.TIMER0, CPU2.TIMER1, CPU2.TIMER2</li> <li>CPU2.FPU</li> <li>CPU2.TMU</li> <li>CPU2.VCU</li> <li>EMIF-2</li> </ul>	335 mA	70 mA	25 mA	35 mA
IDLE	<ul style="list-style-type: none"> <li>Both CPU1 and CPU2 are in IDLE mode.</li> <li>Flash is enabled.</li> <li>All peripheral clocks are enabled.</li> <li>XCLKOUT is turned off.</li> </ul>	240 mA	10 mA	150 μA	35 mA
STANDBY	<ul style="list-style-type: none"> <li>Both CPU1 and CPU2 are in STANDBY mode.</li> <li>Flash is enabled.</li> <li>All peripheral clocks are gated.</li> <li>XCLKOUT is turned off.</li> </ul>	55 mA	10 mA	150 μA	35 mA
HALT <sup>(4)</sup>	<ul style="list-style-type: none"> <li>CPU1 watchdog is running.</li> <li>XCLKOUT is turned off.</li> </ul>	20 mA	1 mA	150 μA	35 mA
HIBERNATE <sup>(5)</sup>	<ul style="list-style-type: none"> <li>CPU1.M0 and CPU1.M1 RAMs are in low-power data retention mode.</li> <li>CPU2.M0 and CPU2.M1 RAMs are in low-power data retention mode.</li> </ul>	1 mA	1 mA	140 μA	10 μA

- (1) The following is done in a loop on CPU1:
- Code is running out of RAM.
  - All I/O pins are left unconnected.
  - All of the communication peripherals are exercised in loop-back mode.
  - ePWM1–ePWM12 generate 400-kHz PWM output on 24 pins.
  - CPU1.DMA does 32-bit burst transfers.
  - CPU1.CLA1 does multiply-accumulate tasks.
  - ADC performs continuous conversion.
  - DAC ramps voltage up/down at 150 kHz.
  - FLASH is continuously read and in active state.
  - XCLKOUT is enabled.
- (2) The following is done in a loop on CPU2:
- CPU2.CLA1 does multiply-accumulate tasks.
  - CPU2.VCU does complex multiply/accumulate with parallel load.
  - CPU2.TMU calculates a cosine.
  - CPU2.FPU does multiply/accumulate with parallel load.
- (3) I<sub>DDIO</sub> current is dependent on the electrical loading on the I/O pins.
- (4) CPU2 must go into IDLE mode before CPU1 enters HALT mode.
- (5) CPU2 must go into reset/IDLE/STANDBY mode before CPU1 enters HIBERNATE mode.

**NOTE**

The peripheral-I/O multiplexing implemented in the device prevents all available peripherals from being used at the same time because more than one peripheral function may share an I/O pin. Although not useful, it is possible to turn on all peripheral clocks even when the peripheral is not used in the application. If the clocks to all the peripherals are turned on at the same time, the current drawn by the device will be more than the numbers specified in the current consumption table.

**4.5 Flash Timing****Table 4-2. Flash/OTP Access Timing for CPU1 Subsystem and CPU2 Subsystem<sup>(1)</sup>**

PARAMETER		MIN	MAX	UNIT
$t_{a(f)}$	Flash access time	20		ns
$t_{a(OTP)}$	TI OTP access time	40		ns
$t_{a(UOTP)}$	User OTP access time	220		ns

(1) Access time values shown in [Table 4-2](#) are prior to device characterization. Final values will be published in this data manual when the device becomes a fully qualified production device.

**Table 4-3. Minimum Required Flash/OTP Wait-States at Different Frequencies for CPU1 Subsystem and CPU2 Subsystem**

SYSCCLKOUT (MHz)	SYSCCLKOUT (ns)	WAIT-STATE
200	5	3
190	5.26	3
180	5.56	3
170	5.88	3
160	6.25	3
150	6.7	2
140	7.14	2
130	7.7	2
120	8.33	2
110	9.1	2
100	10	1
90	11.11	1
80	12.5	1
70	14.29	1
60	16.67	1
50	20	0
40	25	0
30	33.33	0
20	50	0
10	100	0

The equation to compute Flash wait-state in [Table 4-3](#) is as follows:

$$R_{WAIT} = \left[ \left( \frac{\text{SYSCCLK (MHz)}}{50 \text{ MHz}} \right) - 1 \right] \text{ round up to the next integer, or 1, whichever is larger}$$

## 5 CPU and System Control

### 5.1 C28x Processor

The CPU is a 32-bit fixed-point processor. This device draws from the best features of digital signal processing; reduced instruction set computing (RISC); and microcontroller architectures, firmware, and tool sets.

The CPU features include a modified Harvard architecture and circular addressing. The RISC features are single-cycle instruction execution, register-to-register operations, and modified Harvard architecture. The microcontroller features include ease of use through an intuitive instruction set, byte packing and unpacking, and bit manipulation. The modified Harvard architecture of the CPU enables instruction and data fetches to be performed in parallel. The CPU can read instructions and data while it writes data simultaneously to maintain the single-cycle instruction operation across the pipeline. The CPU does this over six separate address/data buses.

#### 5.1.1 Floating-Point Unit (FPU)

The C28x plus floating-point (C28x+FPU) processor extends the capabilities of the C28x fixed-point CPU by adding registers and instructions to support IEEE single-precision floating point operations.

Devices with the C28x+FPU include the standard C28x register set plus an additional set of floating-point unit registers. The additional floating-point unit registers are the following:

- Eight floating-point result registers, RnH (where n = 0–7)
- Floating-point Status Register (STF)
- Repeat Block Register (RB)

All of the floating-point registers, except the repeat block register, are shadowed. This shadowing can be used in high-priority interrupts for fast context save and restore of the floating-point registers.

#### 5.1.2 Trigonometric Math Unit (TMU)

The TMU extends the capabilities of a C28x+FPU by adding instructions and leveraging existing FPU instructions to speed up the execution of common trigonometric and arithmetic operations listed in [Table 5-1](#).

**Table 5-1. TMU Supported Instructions**

INSTRUCTIONS	C EQUIVALENT OPERATION
MPY2PIF32 RaH,RbH	$a = b * 2\pi$
DIV2PIF32 RaH,RbH	$a = b / 2\pi$
DIVF32 RaH,RbH,RcH	$a = b/c$
SQRTF32 RaH,RbH	$a = \text{sqrt}(b)$
SINPUF32 RaH,RbH	$a = \sin(b*2\pi)$
COSPUF32 RaH,RbH	$a = \cos(b*2\pi)$
ATANPUF32 RaH,RbH	$a = \text{atan}(b)/2\pi$
QUADF32 RaH,RbH,RcH,RdH	Operation to assist in calculating ATANPU2

No changes have been made to existing instructions, pipeline or memory bus architecture. All TMU instructions use the existing FPU register set (R0H to R7H) to carry out their operations. A detailed explanation of the workings of the FPU can be found in the *TMS320C28x Floating Point Unit and Instruction Set Reference Guide* (literature number [SPRUJEO2](#)).

### 5.1.3 Viterbi, Complex Math, and CRC Unit II (VCU-II)

The VCU is a fully-programmable block which accelerates the performance of FFTs and communications-based algorithms.

The C28x with VCU (C28x+VCU) processor extends the capabilities of the C28x CPU by adding registers and instructions to support the following algorithm types:

- **Viterbi decoding**

Viterbi decoding is commonly used in baseband communications applications. The Viterbi decode algorithm consists of three main parts: branch metric calculations, compare-select (Viterbi butterfly), and a traceback operation. [Table 5-2](#) shows a summary of the VCU performance for each of these operations.

**Table 5-2. Viterbi Decode Performance**

VITERBI OPERATION	VCU CYCLES
Branch Metric Calculation (code rate = 1/2)	1
Branch Metric Calculation (code rate = 1/3)	2p
Viterbi Butterfly (add-compare-select)	2 <sup>(1)</sup>
Traceback per Stage	3 <sup>(2)</sup>

- (1) C28x CPU takes 15 cycles per butterfly.  
 (2) C28x CPU takes 22 cycles per stage.

- **Cyclic redundancy check (CRC)**

CRC algorithms provide a straightforward method for verifying data integrity over large data blocks, communication packets, or code sections. The C28x+VCU can perform 8-bit, 16-bit, 24-bit, and 32-bit CRCs. For example, the VCU can compute the CRC for a block length of 10 bytes in 10 cycles. A CRC result register contains the current CRC, which is updated whenever a CRC instruction is executed.

- **Complex math**

Complex math is used in many applications, a few of which are:

- Fast fourier transform (FFT)

The complex FFT is used in spread spectrum communications, as well as in many signal processing algorithms.

- Complex filters

Complex filters improve data reliability, transmission distance, and power efficiency. The C28x+VCU can perform a complex I and Q multiply with coefficients (four multiplies) in a single cycle. In addition, the C28x+VCU can read/write the real and imaginary parts of 16-bit complex data to memory in a single cycle.

[Table 5-3](#) shows a summary of the VCU operations enabled by the VCU.

**Table 5-3. Complex Math Performance**

COMPLEX MATH OPERATION	VCU CYCLES	NOTES
Add or Subtract	1	32 +/- 32 = 32-bit (Useful for filters)
Add or Subtract	1	16 +/- 32 = 15-bit (Useful for FFT)
Multiply	2p	16 x 16 = 32-bit
Multiply and Accumulate (MAC)	2p	32 + 32 = 32-bit, 16 x 16 = 32-bit
RPT MAC	2p+N	Repeat MAC. Single cycle after the first operation.

## 5.2 Control Law Accelerator (CLA)

The CLA is an independent single-precision (32-bit) floating-point unit processor with its own bus structure, fetch mechanism, and pipeline. Eight individual CLA tasks can be specified. Each task is started by software or a peripheral such as the ADC, ePWM, eCAP, eQEP, or CPU Timer 0. The CLA executes one task at a time to completion. When a task completes, the main CPU is notified by an interrupt to the PIE and the CLA automatically begins the next highest-priority pending task. The CLA can directly access the ADC Result registers, ePWM, eCAP, eQEP, Comparator and DAC registers. Dedicated message RAMs provide a method to pass additional data between the main CPU and the CLA.

Figure 5-1 shows the CLA block diagram.

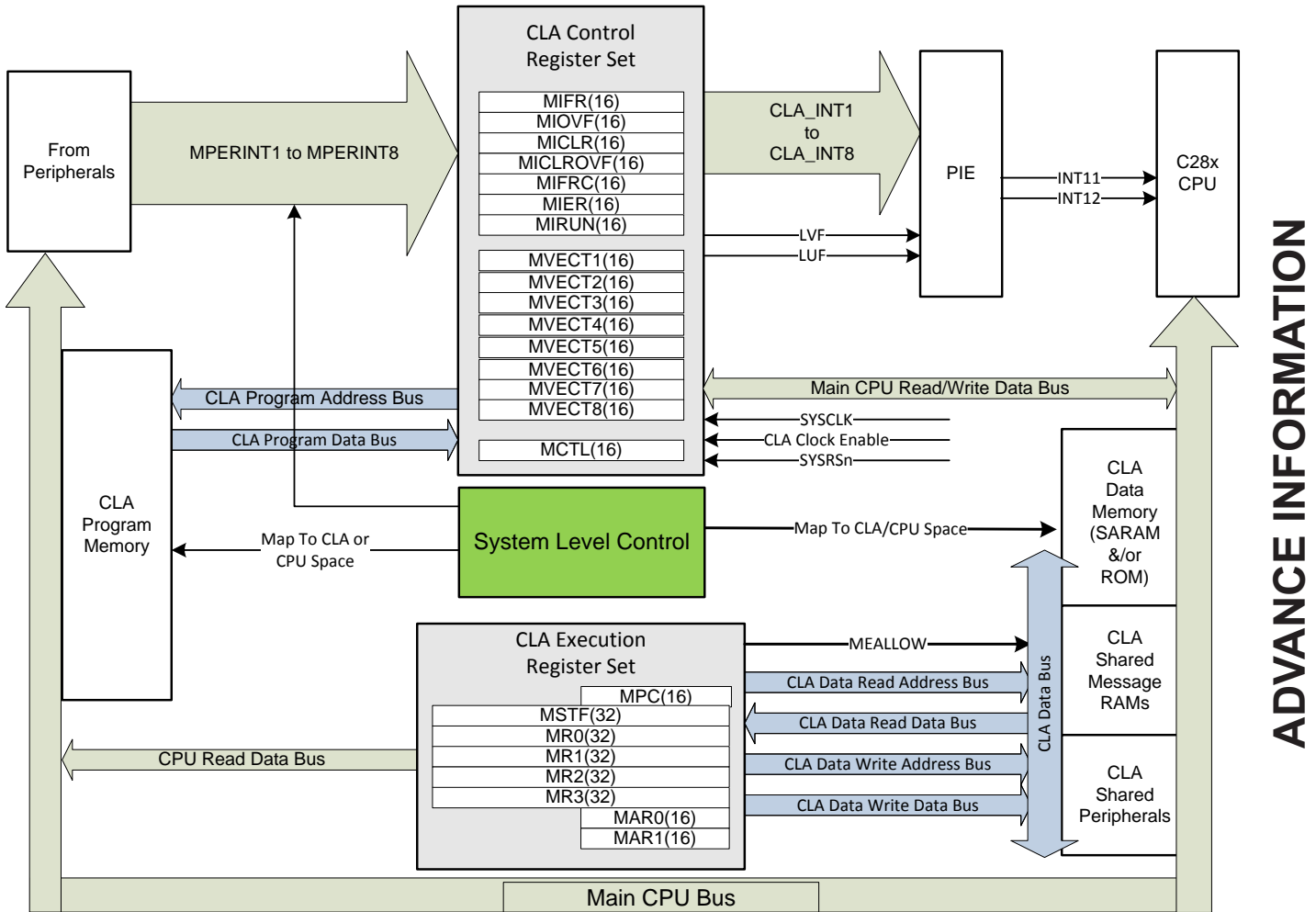


Figure 5-1. CLA Block Diagram

### 5.3 Direct Memory Access (DMA)

The direct memory access (DMA) module provides a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Additionally, the DMA has the capability to orthogonally rearrange the data as it is transferred as well as “ping-pong” data between buffers. These features are useful for structuring data into blocks for optimal CPU processing.

The DMA module is an event-based machine, meaning it requires a peripheral or software trigger to start a DMA transfer. Although it can be made into a periodic time-driven machine by configuring a timer as the interrupt trigger source, there is no mechanism within the module itself to start memory transfers periodically. The interrupt trigger source for each of the six DMA channels can be configured separately and each channel contains its own independent PIE interrupt to let the CPU know when a DMA transfer has either started or completed. Five of the six channels are exactly the same, while Channel 1 has the ability to be configured at a higher priority than the others.

DMA features include:

- 6 channels with independent PIE interrupts
- Peripheral interrupt trigger sources
  - ADC interrupts and EVT signals
  - Multichannel buffered serial port transmit and receive
  - External interrupts
  - CPU timers
  - EPWMxSOC signals
  - SPIx transmit and receive
  - USBx transmit and receive
  - Sigma Delta Filter Module
  - Software trigger
- Data sources and destinations:
  - GSx RAM
  - CPU message RAM (IPC RAM)
  - USB RAM
  - ADC result registers
  - ePWMx
  - SPI
  - McBSP
  - EMIF
- Word Size: 16-bit or 32-bit (SPI and McBSP limited to 16-bit)
- Throughput: 4 cycles/word (without arbitration)

Figure 5-2 shows a device-level block diagram of the DMA for CPU1 and CPU2.

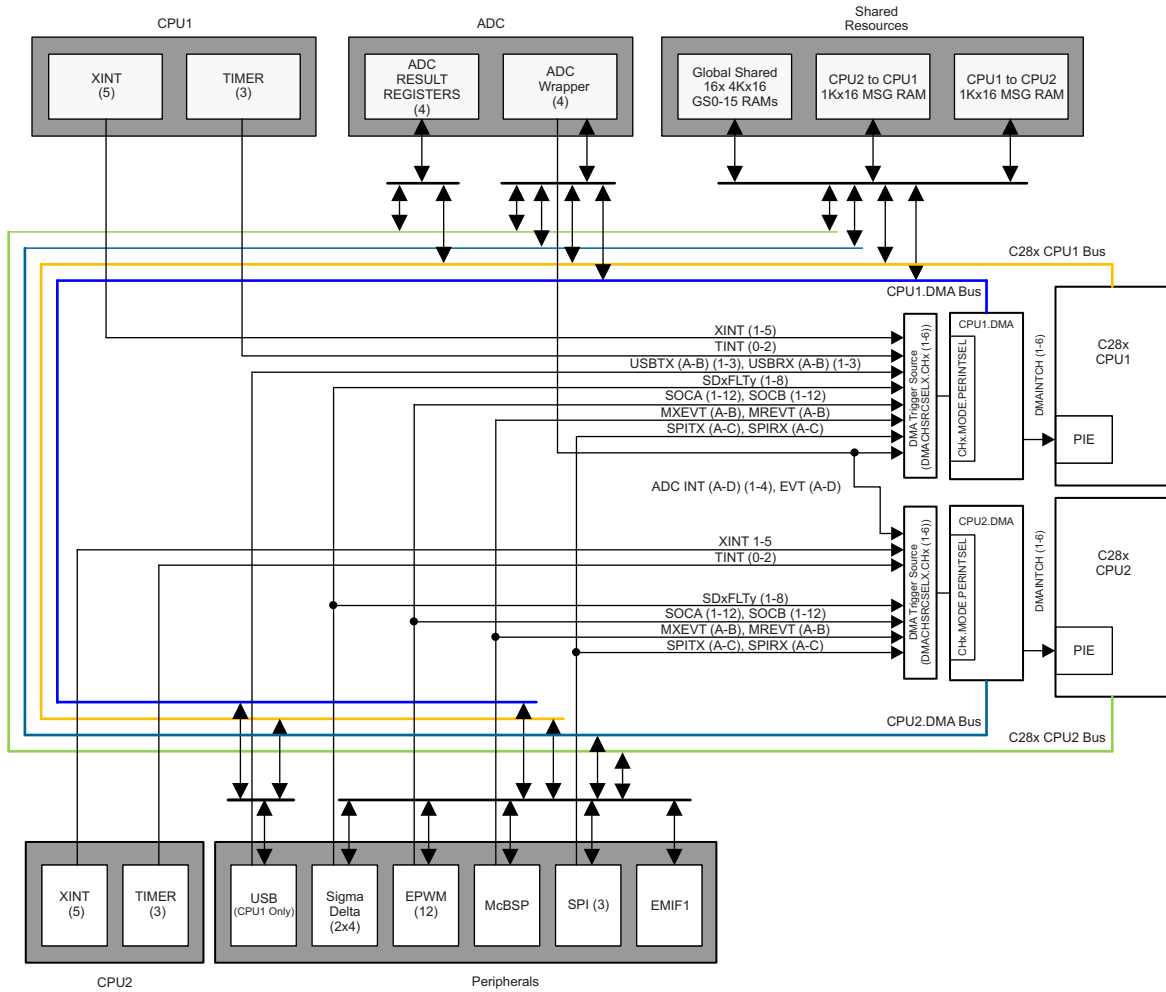


Figure 5-2. DMA Block Diagram

ADVANCE INFORMATION

### 5.4 Interprocessor Communication (IPC) Module

The IPC module supports several methods of inter-processor communication:

- Thirty-two IPC flags per CPU, which can be used to signal events or indicate status via software polling. Four flags per CPU can generate interrupts.
- Shared data registers, which can be used to send commands or other small pieces of information between CPUs. Although the register names were chosen to support a command/response system, they can be used for any purpose as defined in software.
- Boot mode and status registers, which allow CPU1 to control the CPU2 boot process.
- A general-purpose free-running 64-bit counter.
- Two shared message RAMs, which can be used to transfer bulk data. Each RAM can be read by both CPUs. CPU1 can write to one RAM and CPU2 can write to the other.

Figure 5-3 shows the IPC architecture.

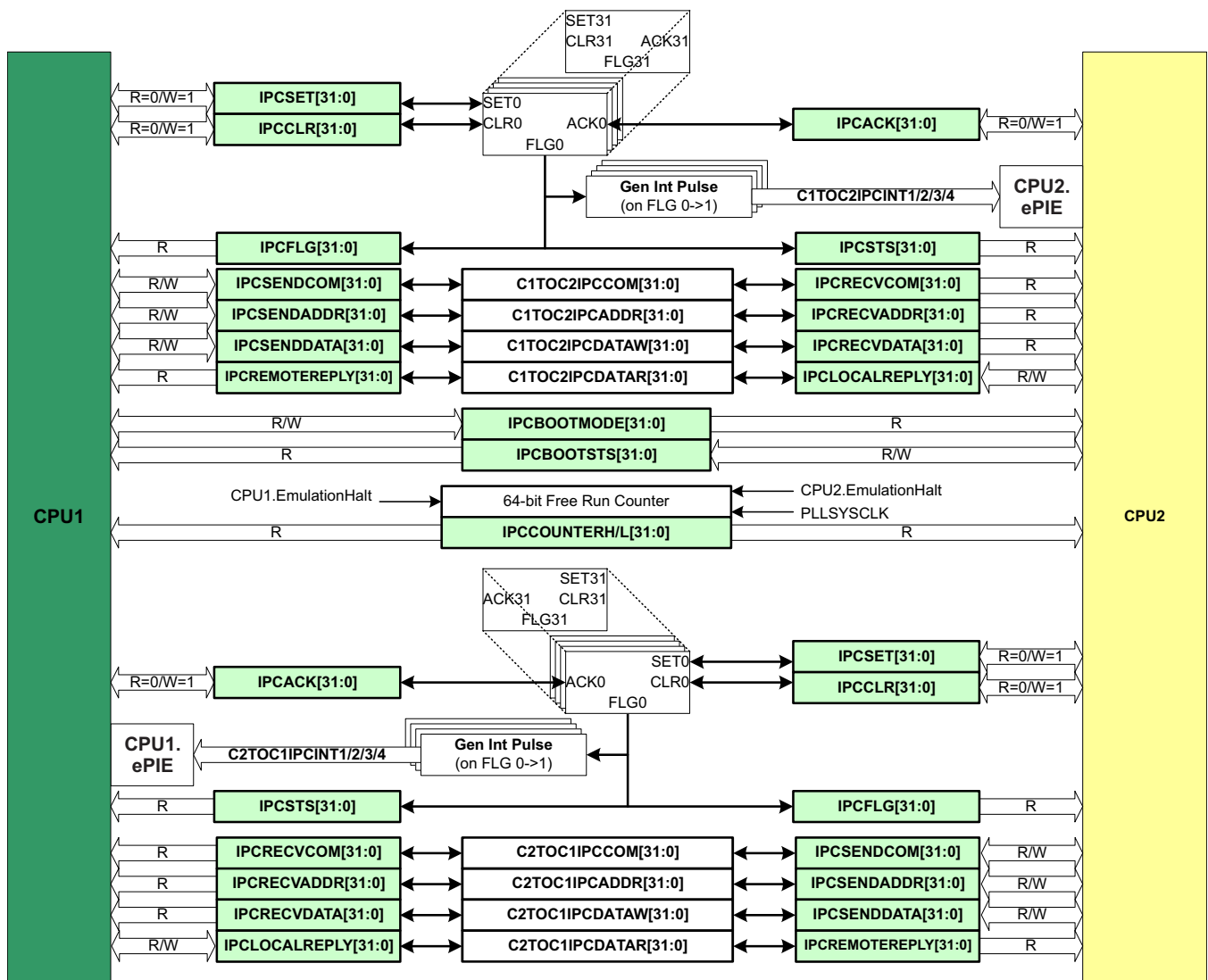


Figure 5-3. IPC Architecture

ADVANCE INFORMATION

## 5.5 Boot ROM and Peripheral Booting

The device boot ROM (on both the CPUs) is factory programmed with bootloading software. The CPU1 boot ROM does the system initialization before bringing CPU2 out of reset. The device boot ROM is executed each time the device comes out of reset. Users can configure the device to boot to flash (using GET mode) or choose to boot the device through one of the bootable peripherals by configuring the boot mode GPIO pins.

The CPU1 boot ROM, being master, owns the boot mode GPIO and boot configurations. The CPU2 boot ROM either boots to flash (if configured to do so via user OTP) or enters a WAIT BOOT mode if no OTP is programmed. In WAIT BOOT mode, the CPU1 application instructs the CPU2 boot ROM on how to boot further using boot mode IPC commands supported by CPU2 boot ROM.

Table 5-4 shows the possible boot modes supported on the device. The default boot mode pins are GPIO72 (boot mode pin 1) and GPIO 84 (boot mode pin 0). Users may choose to have weak pullups for boot mode pins if they use a peripheral on these pins as well, so the pullups can be overdriven. On this device, customers can change the factory default boot mode pins by programming user OTP locations. This is recommended only for cases in which the factory default boot mode pins do not fit into the customer design. More details on the locations to be programmed is available in the *TMS320F2837xD Technical Reference Manual* (literature number [SPRUHM8](#)).

**Table 5-4. Device Boot Mode – Decoded by CPU1**

MODE NO.	CPU1 BOOT MODE	CPU2 BOOT MODE	$\overline{\text{TRST}}$	GPIO72 (BOOT MODE PIN 1)	GPIO84 (BOOT MODE PIN 0)	SUPPORTED IN VERSION 1.0
0	Parallel IO	Boot from Master	0	0	0	Yes
1	SCI Mode	Boot from Master	0	0	1	Yes
2	Wait Boot Mode	Boot from master	0	1	0	Yes
3	Get Mode	Boot from Master	0	1	1	Yes
4-7	EMU Boot Mode (Emulator Connected)	Boot from Master	1	X	X	Yes

### 5.5.1 EMU Boot or Emulation Boot

The CPU enters this boot when it detects that  $\overline{\text{TRST}}$  is HIGH (in other words, when an emulator/debugger is connected). In this mode, the user can program the EMUBOOTCTRL register (at location 0xD00) to instruct the device on how to boot. If the contents of the EMUBOOTCTRL locations are invalid, then the device would default into WAIT Boot mode. The emulation boot allows users to verify the device boot before programming the boot mode into OTP.

### 5.5.2 WAIT Boot Mode

The device in this boot mode loops in the boot ROM. This mode is useful if users want to connect a debugger on a secure device or if users do not want the device to execute an application in flash yet.

### 5.5.3 Get Mode

The default behavior of Get mode is boot-to-flash. This behavior can be changed by programming the Zx-OTPBOOTCTRL locations in user OTP. The user OTP on this device is divided in to two secure zones: Z1 and Z2. The Get mode function in boot ROM first checks if a valid OTPBOOTCTRL value is programmed in Z1. If the answer is yes, then the device boots as per the Z1-OTPBOOTCTRL location. The Z2-OTPBOOTCTRL location is read and decodes only if Z1-OTPBOOTCTRL is invalid or not programmed. If either Zx-OTPBOOTCTRL location is not programmed, then the device defaults to factory default operation, which is to use factory default boot mode pins to boot to flash if the boot mode pins are set to GET MODE. Users can choose the device through which to boot—SPI, I2C, CAN and USB—by programming proper values into the user OTP. More details on this can be found in the *TMS320F2837xD Technical Reference Manual* (literature number [SPRUHM8](#)).

### 5.5.4 Peripheral Pins used by Bootloaders

Table 5-5 shows the GPIO pins used by each peripheral bootloader. This device supports two sets of GPIOs for each mode, as shown in Table 5-5.

**Table 5-5. GPIO Pins Used by Each Peripheral Bootloader**

BOOTLOADER	GPIO PINS	NOTES
SCI-Boot0	SCITXDA: GPIO84 SCIRXDA: GPIO85	SCIA Boot IO option 1 (default SCI option when chosen through Boot Mode GPIOs)
SCI-Boot1	SCITXDA: GPIO28 SCIRXDA: GPIO29	SCIA Boot option 2 – with alternate IOs.
Parallel Boot	D0 – GPIO65 D1 – GPIO64 D2 – GPIO58 D3 – GPIO59 D4 – GPIO60 D5 – GPIO61 D6 – GPIO62 D7 – GPIO63 HOST_CTRL – GPIO70 DSP_CTRL – GPIO69	
CAN-Boot0	CANRXA: GPIO70 CANTXA: GPIO71	CAN-A Boot -IO Option 1
CAN-Boot1	CANRXA: GPIO62 CANTXA: GPIO63	CAN-A Boot -IO option 2
I2C-Boot0	SDAA: GPIO91 SCLA: GPIO92	I2CA Boot- IO option 1
I2C-Boot1	SDAA: GPIO32 SCLA: GPIO33	I2CA Boot- IO option 2
SPI-Boot0	SPISIMOA - GPIO58 SPISOMIA - GPIO59 SPICLKA - GPIO60 SPISTEA - GPIO61	SPIA Boot- IO Option 1
SPI-Boot1	SPISIMOA – GPIO16 SPISOMIA – GPIO17 SPICLKA – GPIO18 SPISTEA – GPIO19	SPIA Boot - IO Option 2
USB Boot	USB0DM - GPIO42 USB0DP - GPIO43	CPU1 Only (USB Boot implements USB custom DFU device type)

## 5.6 Memory

### 5.6.1 Dedicated RAM (Mx and Dx RAM)

Each CPU subsystem has four dedicated RAM blocks, M0, M1, D0 and D1. M0/M1 memories are small blocks of memory which are tightly coupled with CPU. Only the CPU has access to these memories.

All dedicated RAMs have ECC. D0 and D1 are secure and have the access protection (CPU write /CPU fetch) feature.

### 5.6.2 Local Shared RAM (LSx RAM)

RAM blocks which are dedicated to each subsystem and are accessible to its CPU and CLA only, are called local shared RAMs (LSx RAMs).

All LSx RAM blocks have parity. These memories are secure and have the access protection (CPU write/CPU fetch) feature.

By default these memories are dedicated to CPU only and user could choose to share these memories with CLA by configuring MSEL\_LSx bit filed in LSxMSEL registers appropriately.

**Table 5-6. Master Access for LSx RAM  
(With Assumption That all Other Access Protections are Disabled)**

MSEL_LSx	CLAPGM_LSx	CPUx ALLOWED ACCESS	CPUx.CLA1 ALLOWED ACCESS	COMMENT
00	X	All	–	LSx memory is configured as CPU dedicated RAM.
01	0	All	Data Read Data Write	LSx memory is shared between CPU and CLA1.
01	1	Emulation Read Emulation Write	Fetch Only	LSx memory is CLA1 program memory.

### 5.6.3 Global Shared RAM (GSx RAM)

RAM blocks which are accessible from both the CPU and DMA are called global shared RAMs (GSx RAMs). Each shared RAM block can be owned by either of CPU subsystem based on configuration of respective bits in the GSxMSEL register.

When a GSx RAM block is owned by a CPUx subsystem the CPUx and CPUx.DMA will have full access to that RAM block where the other CPUy and CPUy.DMA will have only read access (no fetch/write access).

**Table 5-7. Master Access for GSx RAM  
(With Assumption That all Other Access Protections are Disabled)**

GSxMSEL	CPU1 FETCH	CPU1 READ	CPU1 WRITE	CPU1.DMA READ	CPU1.DMA WRITE	CPU2 FETCH	CPU2 READ	CPU2 WRITE	CPU2.DMA READ	CPU2.DMA WRITE
0	Yes	Yes	Yes	Yes	Yes	No	Yes	No	Yes	No
1	No	Yes	No	Yes	No	Yes	Yes	Yes	Yes	Yes

All these RAMs have access protection (CPU write/CPU fetch/DMA write).

#### 5.6.4 Message RAM (MSGRAM)

These RAM blocks are used to share data between CPU and CLA of same subsystem or between CPU1 and CPU2. Since these RAMs are used for inter-processor communication, these are also called IPC RAMs.

The message RAMs between two CPUs will have CPU/DMA read/write access from one subsystem, and CPU/DMA read only access from the other subsystem. Similarly for message RAMs between CPU and CLA of same subsystem, one of CPU or CLA will have read/write access where as other one will have only read access.

All MSGRAMs have parity.

## 5.7 Dual Code Security Module (DCSM)

The dual code security module (DCSM) prevents access to on-chip secure memories. The term “secure” means access to secure memories and resources is blocked. The term “unsecure” means access is allowed; for example, through a debugging tool such as Code Composer Studio.

The code security mechanism offers protection for two zones, Zone 1 (Z1) and Zone 2 (Z2). The security implementation for both the zones is identical. Each zone has its own dedicated secure resource and allocated secure resource.

The security of each zone is ensured by its own 128-bit password (CSM password). The password for each zone is stored in an OTP memory location based on a zone-specific link pointer. The link pointer value can be changed to program a different set of security settings (including passwords) in OTP. The secure resources available are: OTP memory, CLA, LSx RAM, flash sectors, and secure ROM.

## 5.8 Clocking

### 5.8.1 Clock Sources

Table 5-8 lists four possible reference clock sources on the F2837xD device.

**Table 5-8. Possible Reference Clock Sources on F2837xD Device**

CLOCK SOURCE	POSSIBLE CLOCK SOURCES	COMMENTS
INTOSC1 <sup>(1)</sup>	Can be used to provide clock for: <ul style="list-style-type: none"> <li>• watchdog block</li> <li>• system clock</li> <li>• CPU-Timer 2</li> </ul>	Internal oscillator 1. Zero-pin overhead 10-MHz internal oscillator.
INTOSC2 <sup>(1)(2)</sup>	Can be used to provide clock for: <ul style="list-style-type: none"> <li>• auxiliary clock</li> <li>• system clock</li> <li>• CPU-Timer 2</li> </ul>	Internal oscillator 2. Zero-pin overhead 10-MHz internal oscillator.
XTAL <sup>(1)</sup>	Can be used to provide clock for: <ul style="list-style-type: none"> <li>• auxiliary clock</li> <li>• system clock</li> <li>• CPU-Timer 2</li> </ul>	External oscillator connected between X1 and X2 pins. On-chip crystal oscillator enables the use of external crystal/resonator to provide time base when connected to the device.
GPIO_AUXCLKIN	Can be used to provide clock for: <ul style="list-style-type: none"> <li>• auxiliary clock</li> <li>• CPU-Timer 2</li> </ul>	Single-ended 3.3-V level clock source. GPIO133/AUXCLKIN pin should be used to provide the input clock.

- (1) For power savings, both zero pin internal oscillators and XTAL can be individually powered down if they are not being used by the application.
- (2) On reset, internal oscillator 2 (INTOSC2) is the default clock source for both system PLL (OSCCLK) and auxiliary PLL (AUXOSCCLK).

Figure 5-4 shows the clocking options for system PLL.

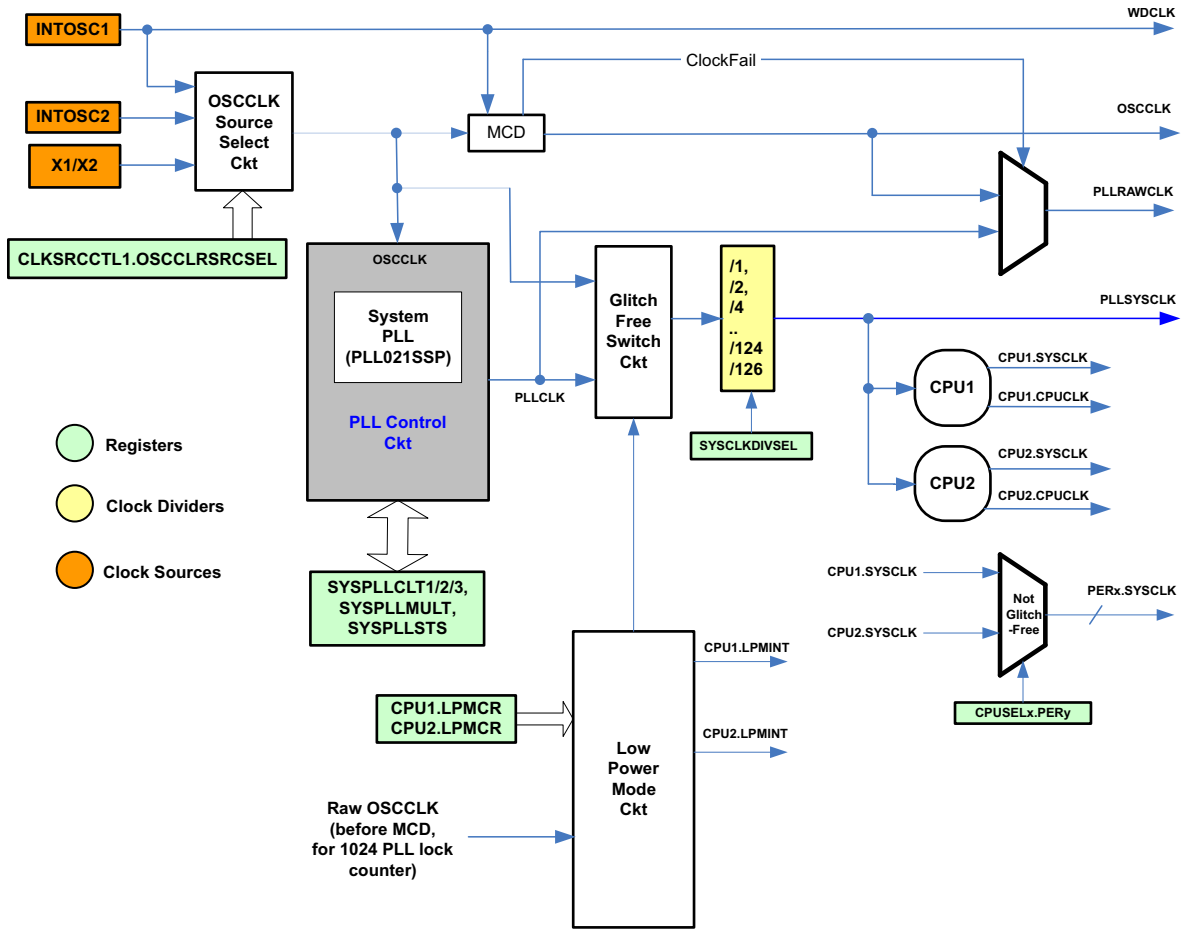


Figure 5-4. Clocking Options for System PLL

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Figure 5-5 shows the clocking options for auxiliary PLL.

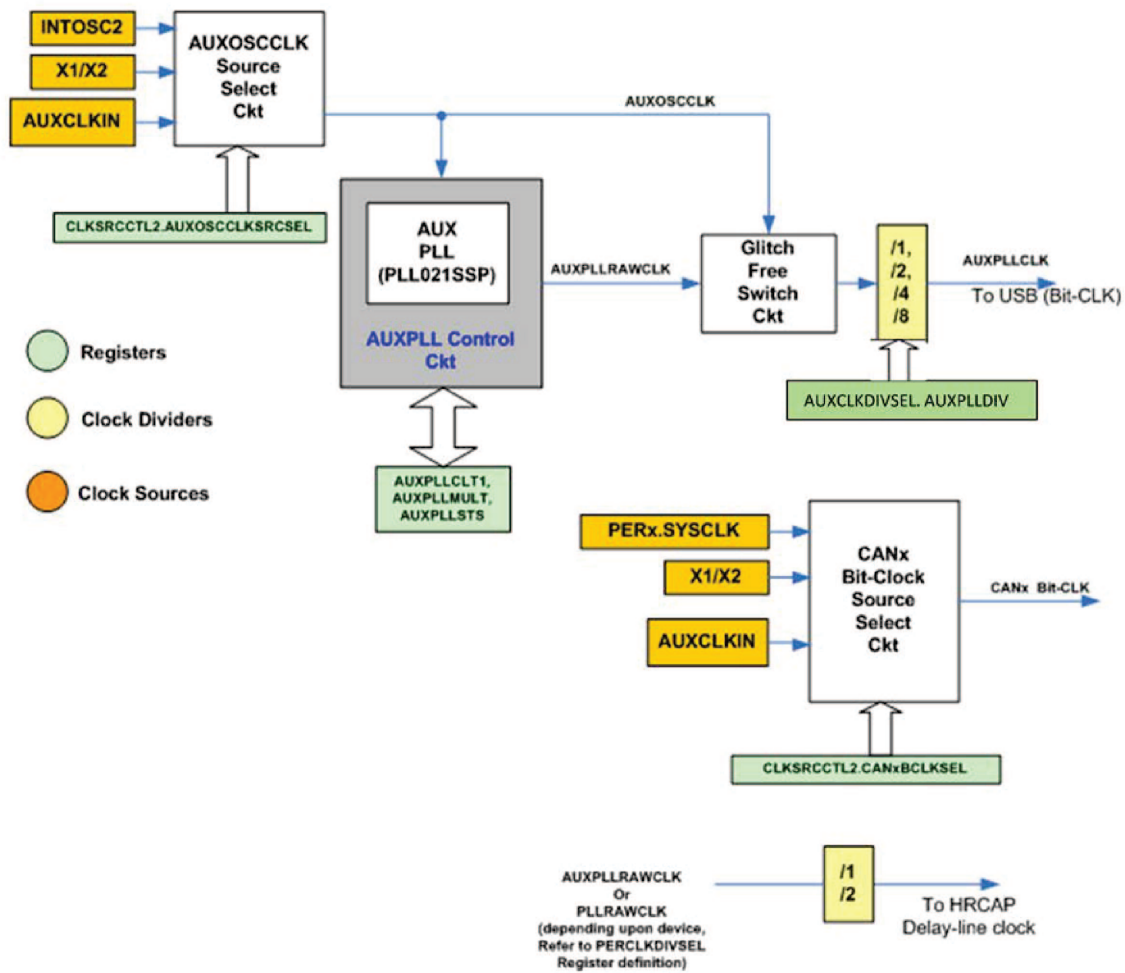


Figure 5-5. Clocking Options for Auxiliary PLL

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Figure 5-6 shows the peripheral clock options.

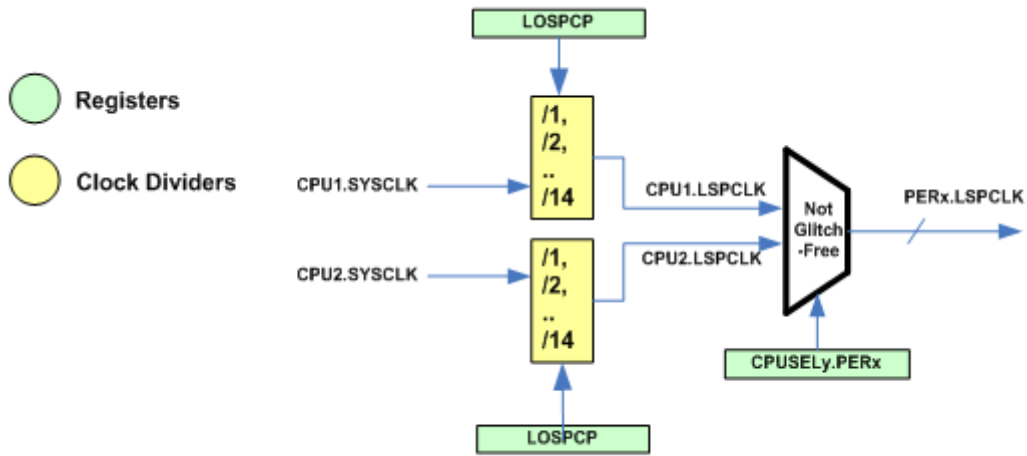


Figure 5-6. Peripheral Clock Options

Figure 5-7 shows the CPU Timer2 clock options.

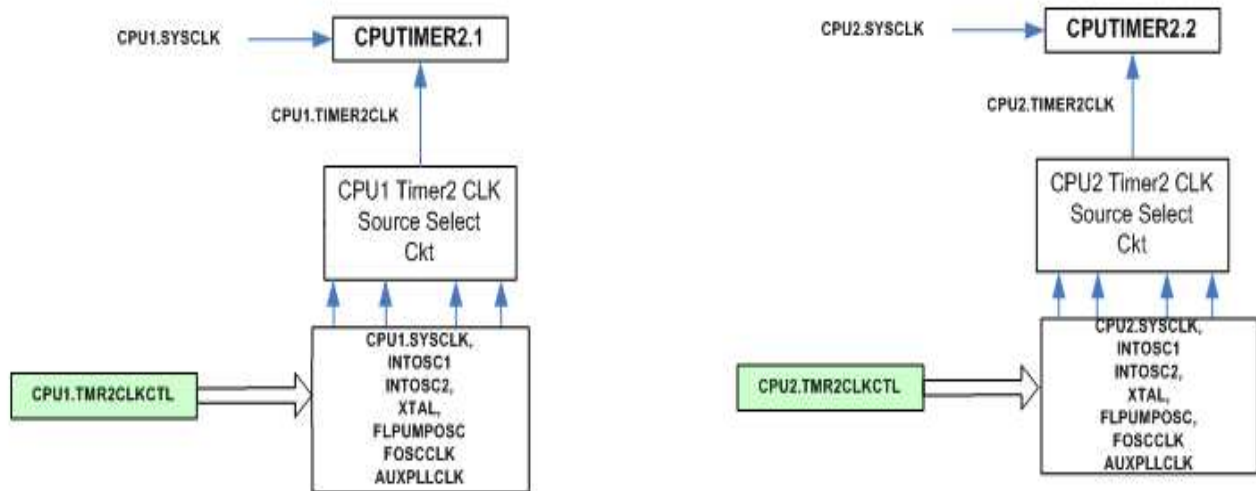


Figure 5-7. CPU Timer2 Clock Options

## 5.8.2 Clock Frequencies, Requirements, and Characteristics

This section provides the frequencies and timing requirements of the input clocks; PLL lock times; frequencies of the internal clocks; and the frequency and switching characteristics of the output clock.

### 5.8.2.1 Input Clock Frequency and Timing Requirements, PLL Lock Times

Table 5-9 shows the frequency requirements for the input clocks to the F2837xD devices. Table 5-10, Table 5-11, Table 5-12, and Table 5-13 show the timing requirements for the input clocks to the F2837xD devices. Table 5-14 shows the PLL lock times for the Main PLL and the USB PLL.

**Table 5-9. Input Clock Frequency**

		MIN	MAX	UNIT
$f_{(OSC)}$	Frequency, X1/X2, from external crystal or resonator	2	20	MHz
$f_{(OCI)}$	Frequency, X1, from external oscillator ( <b>PLL enabled</b> )	2	30	MHz
$f_{(OCI)}$	Frequency, X1, from external oscillator ( <b>PLL disabled</b> )	2	100	MHz
$f_{(XCI)}$	Frequency, XCLKIN, from external oscillator	2	60	MHz

**Table 5-10. X1 Timing Requirements - PLL Enabled**

NO.		MIN	MAX	UNIT
C4	$t_{f(OCI)}$ Fall time, X1		6	ns
C5	$t_{r(OCI)}$ Rise time, X1		6	ns
C6	$t_{w(OCL)}$ Pulse duration, X1 low as a percentage of $t_{c(OCI)}$	45	55	%
C7	$t_{w(OCH)}$ Pulse duration, X1 high as a percentage of $t_{c(OCI)}$	45	55	%

**Table 5-11. X1 Timing Requirements - PLL Disabled**

NO.			MIN	MAX	UNIT
C4	$t_{f(OCI)}$ Fall time, X1	Up to 20 MHz		6	ns
		20 MHz to 100 MHz		2	
C5	$t_{r(OCI)}$ Rise time, X1	Up to 20 MHz		6	ns
		20 MHz to 100 MHz		2	
C6	$t_{w(OCL)}$ Pulse duration, X1 low as a percentage of $t_{c(OCI)}$		45	55	%
C7	$t_{w(OCH)}$ Pulse duration, X1 high as a percentage of $t_{c(OCI)}$		45	55	%

**Table 5-12. XCLKIN Timing Requirements - PLL Enabled**

NO.			MIN	MAX	UNIT
C8	$t_{f(XCI)}$	Fall time, XCLKIN		6	ns
C9	$t_{r(XCI)}$	Rise time, XCLKIN		6	ns
C10	$t_{w(XCL)}$	Pulse duration, XCLKIN low as a percentage of $t_{c(XCI)}$	45	55	%
C11	$t_{w(XCH)}$	Pulse duration, XCLKIN high as a percentage of $t_{c(XCI)}$	45	55	%

**Table 5-13. XCLKIN Timing Requirements - PLL Disabled**

NO.			MIN	MAX	UNIT
C8	$t_{f(XCI)}$	Fall time, XCLKIN	Up to 20 MHz	6	ns
			20 MHz to 100 MHz	2	
C9	$t_{r(XCI)}$	Rise time, XCLKIN	Up to 20 MHz	6	ns
			20 MHz to 100 MHz	2	
C10	$t_{w(XCL)}$	Pulse duration, XCLKIN low as a percentage of $t_{c(XCI)}$	45	55	%
C11	$t_{w(XCH)}$	Pulse duration, XCLKIN high as a percentage of $t_{c(XCI)}$	45	55	%

**Table 5-14. PLL Lock Times**

		MIN	NOM	MAX	UNIT
$t_{(PLL)}$	Lock time, Main PLL (X1, from external oscillator)		2000 <sup>(1)</sup>		input clock cycles
$t_{(USB)}$	Lock time, USB PLL (XCLKIN, from external oscillator)		2000 <sup>(1)</sup>		input clock cycles

(1) For example, if the input clock to the PLL is 10 MHz, then the PLL lock time is 100 ns x 2000 = 200  $\mu$ s.

### 5.8.2.2 Internal Clock Frequencies

Table 5-15 provides the clock frequencies for the internal clocks of the F2837xD devices.

**Table 5-15. Internal Clock Frequencies**

		MIN	NOM	MAX	UNIT
$f_{(AUX)}$	Frequency, AUXPLLCLK		60		MHz
$f_{(PLL)}$	Frequency, PLLSYSCLK	2		200	MHz
$f_{(OCK)}$	Frequency, OSCCLK	2		100	MHz
$f_{(LSP)}$	Frequency, LSPCLK <sup>(1)</sup>	2	50 <sup>(2)</sup>	200	MHz
$f_{(INT)}$	Frequency, INTOSC1/2CLK		10		MHz

(1) Lower LSPCLK will reduce device power consumption.

(2) This is the default reset value if PLLSYSCLK = 200 MHz.

### 5.8.2.3 Output Clock Frequency and Switching Characteristics

Table 5-16 provides the frequency of the output clock from the F2837xD devices. Table 5-17 shows the switching characteristics of the output clock from the F2837xD devices, XCLKOUT.

**Table 5-16. Output Clock Frequency**

NO.		MIN	MAX	UNIT
C14	$f_{(XCO)}$ Frequency, XCLKOUT	2	50	MHz

**Table 5-17. XCLKOUT Switching Characteristics (PLL Bypassed or Enabled)<sup>(1)(2)</sup>**

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER	MIN	MAX	UNIT
C15	$t_{f(XCO)}$ Fall time, XCLKOUT		5	ns
C16	$t_{r(XCO)}$ Rise time, XCLKOUT		5	ns
C17	$t_{w(XCOL)}$ Pulse duration, XCLKOUT low	H – 2	H + 2	ns
C18	$t_{w(XCOH)}$ Pulse duration, XCLKOUT high	H – 2	H + 2	ns

(1) A load of 40 pF is assumed for these parameters.

(2)  $H = 0.5t_{c(XCO)}$

### 5.8.3 Input Clocks and PLLs

F2837xD devices have multiple input clock pins from which all internal clocks and the output clock are derived. Figure 5-8 shows the recommended methods of connecting crystals, resonators, and oscillators to pins X1/X2 and XCLKIN.

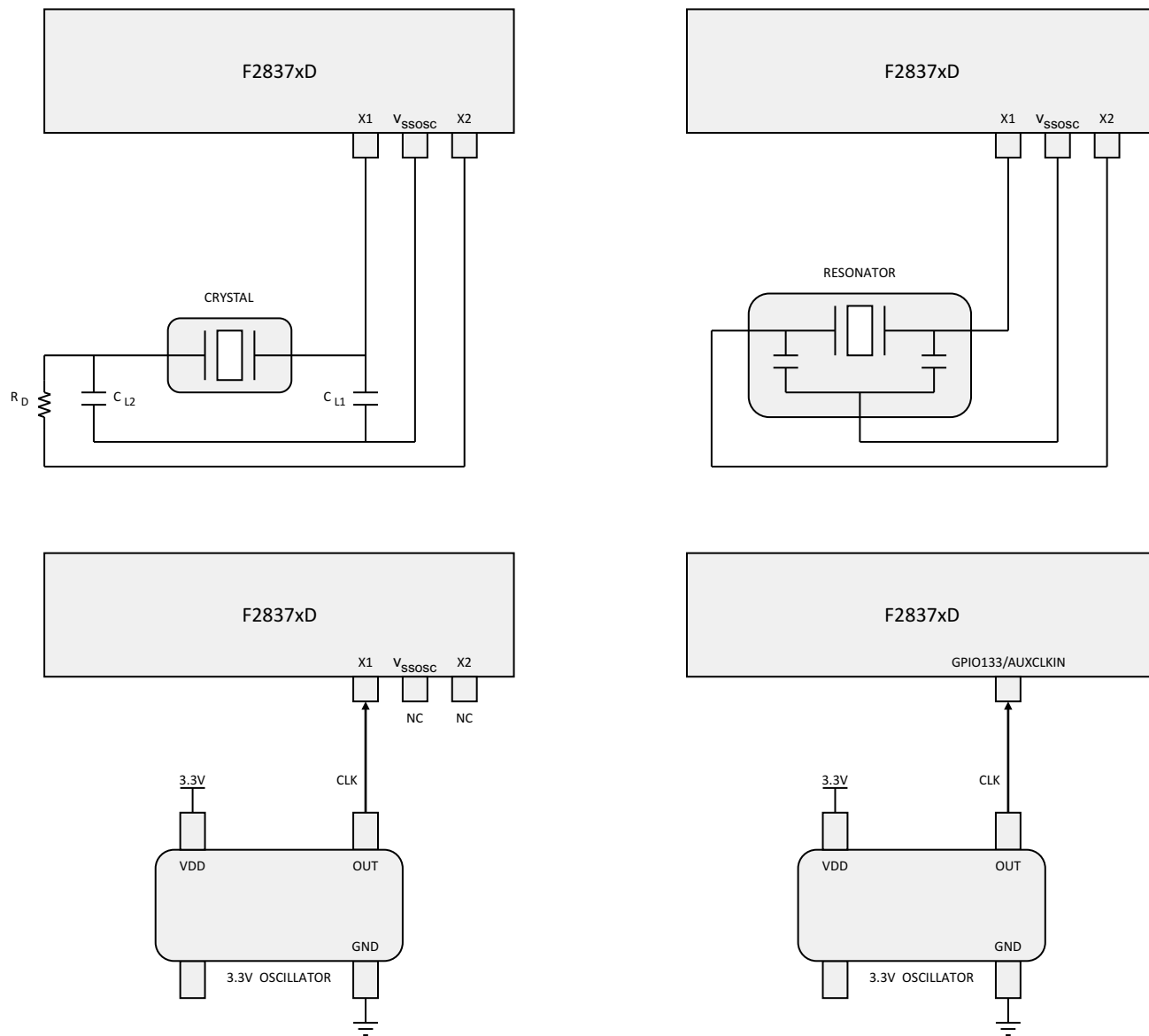


Figure 5-8. Connecting Input Clocks to a F2837xD Device

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### 5.8.4 Oscillators

**Table 5-18. Internal Oscillator Electrical Characteristics**

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Nominal frequency			10		MHz
Frequency accuracy	T <sub>J</sub> = 30°C		0.1		%
Drift of frequency across temperature and voltage			±3		%
Startup and settling time			22		µs

## 5.9 Timers

CPU-Timers 0, 1, and 2 are identical 32-bit timers with presetable periods and with 16-bit clock prescaling. The timers have a 32-bit count-down register, which generates an interrupt when the counter reaches zero. The counter is decremented at the CPU clock speed divided by the prescale value setting. When the counter reaches zero, it is automatically reloaded with a 32-bit period value.

CPU-Timer 0 is for general use and is connected to the PIE block. CPU-Timer 1 is also for general use and is connected to INT13 of the CPU. CPU-Timer 2 is reserved for SYSBIOS. It is connected to INT14 of the CPU. If SYSBIOS is not being used, CPU-Timer 2 is available for general use.

CPU-Timer 2 can be clocked by any one of the following:

- SYSCLKOUT (default)
- Internal zero-pin oscillator 1 (INTOSC1)
- Internal zero-pin oscillator 2 (INTOSC2)
- External clock source

### 5.10 Interrupts

Figure 5-9 provides a high-level view of the interrupt architecture.

As shown in Figure 5-9, the devices support five external interrupts (XINT1 to XINT5) that can be mapped onto any of the GPIO pins.

In this device, sixteen ePIE block interrupts are grouped into one CPU interrupt. In total, there are 12 CPU interrupt groups, with 16 interrupts per group.

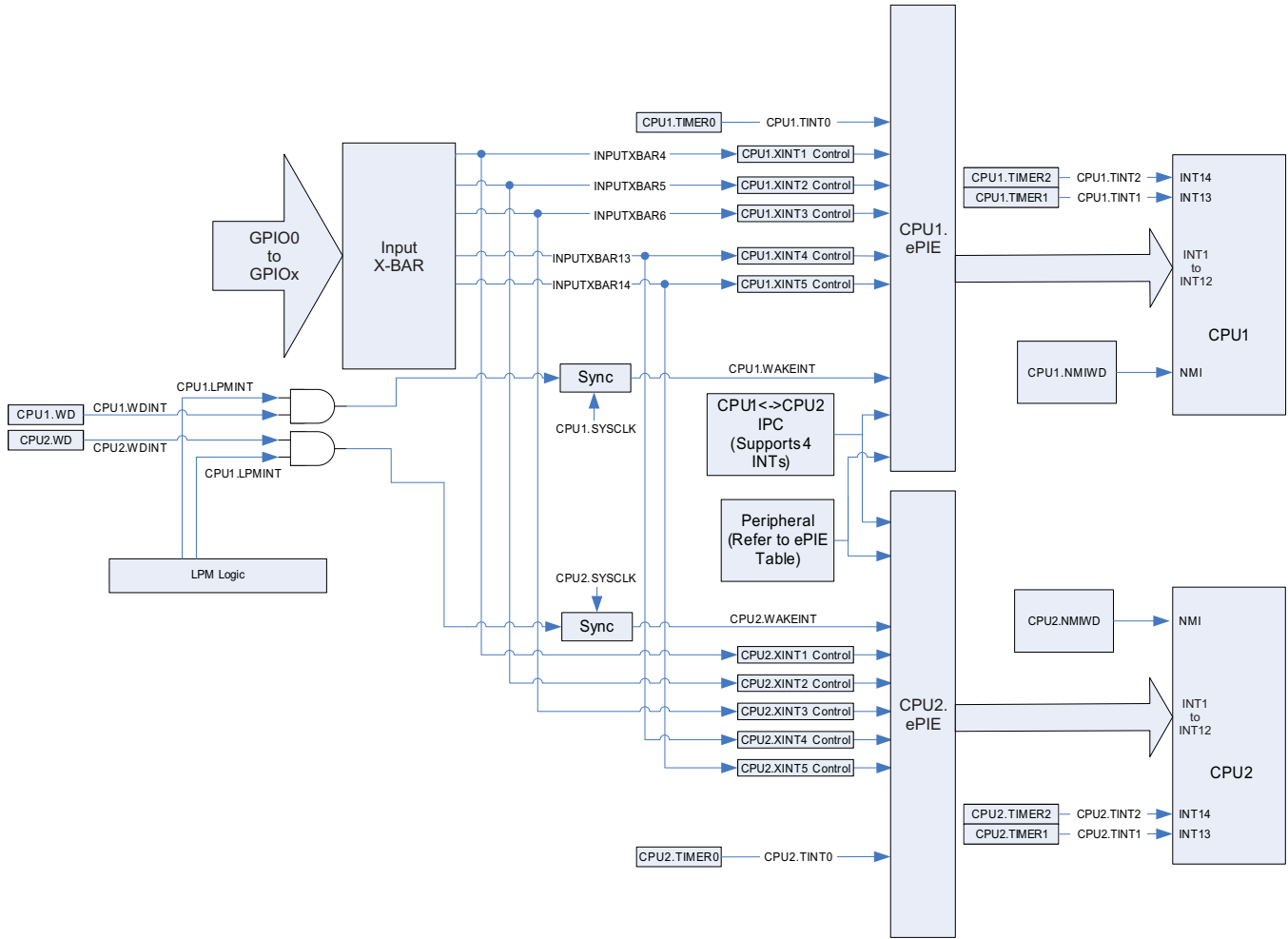


Figure 5-9. External and ePIE Interrupt Sources

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### 5.11 Nonmaskable Interrupt Watchdog (NMIWD)

The NMI interrupt is used to monitor erroneous conditions in the system. There is a NMIWD module for each CPU. The conditions monitored are:

- A missing clock condition
- Uncorrectable memory errors on C28x access to Flash
- Uncorrectable memory errors on C28x, CLA, or DMA access to RAM
- Vector fetch ERROR on the other CPU

If the software does not respond to the enabled latched FAIL condition, then the NMI watchdog would trigger a reset after a preprogrammed time interval.

### 5.12 Watchdog

The watchdog module is the same as the one on previous C2000™ devices, but with an optional lower limit on the time between software resets of the counter. This windowed countdown is disabled by default, so the watchdog is fully backwards-compatible.

The watchdog is capable of generating either a reset or an interrupt. It is clocked from the internal oscillator with a selectable frequency divider.

Figure 5-10 shows the various functional blocks within the watchdog module.

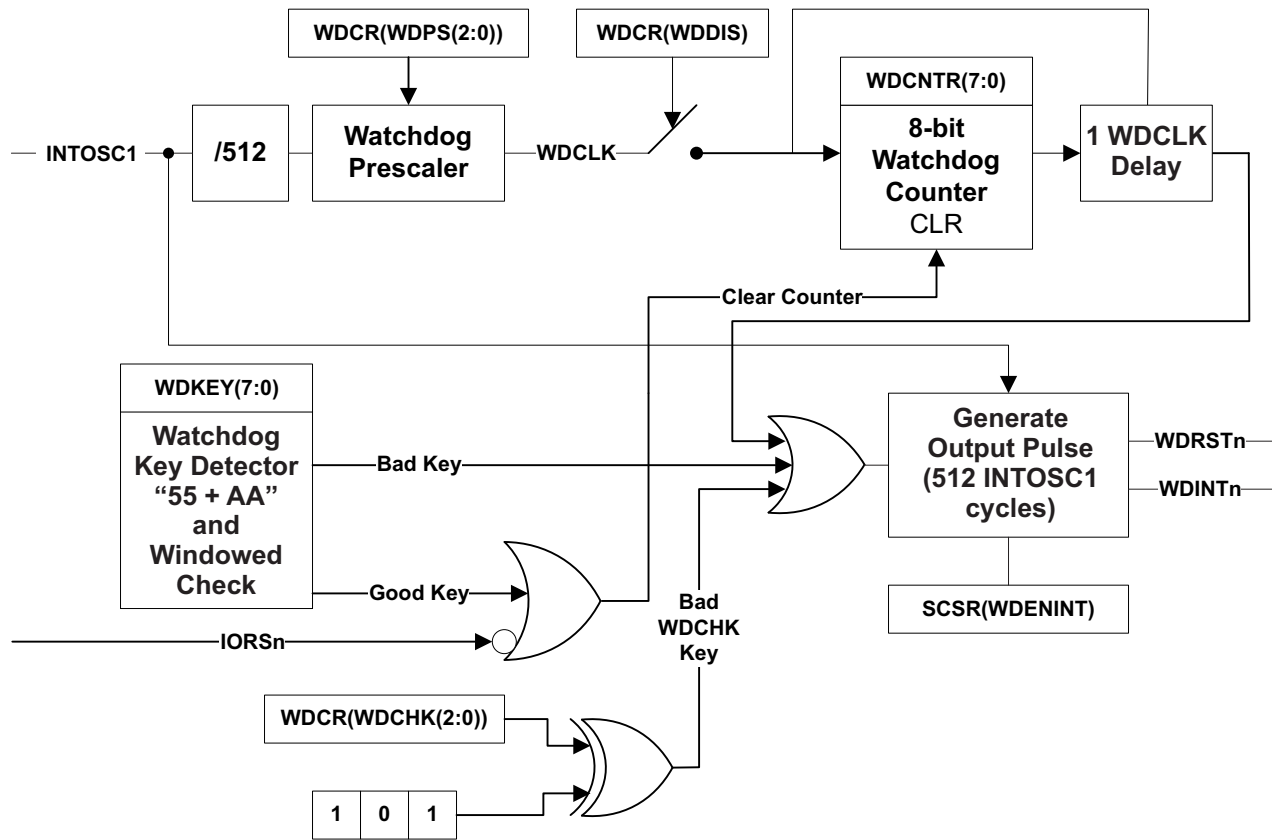


Figure 5-10. Windowed Watchdog

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## 5.13 Low-Power Modes

This device has three clock-gating low-power modes and a special power-gating mode.

Further details, as well as the entry and exit procedure, for all of the low-power modes can be found in the "Low Power Modes" section of the *TMS320F2837xD Delfino Technical Reference Manual* (literature number [SPRUHM8](#)).

### 5.13.1 Clock-Gating Low-Power Modes

IDLE, STANDBY, and HALT modes on this device are similar to those on other C28x devices. [Table 5-19](#) describes the effect on the system when any of the clock-gating low-power modes are entered.

**Table 5-19. Effect of Clock-Gating Low-Power Modes on the Device**

MODULES/ CLOCK DOMAIN	CPU1 IDLE	CPU1 STANDBY	CPU2 IDLE	CPU2 STANDBY	HALT
CPU1.CLKIN	Active	Gated	N/A	N/A	Gated
CPU1.SYSCLK	Active	Gated	N/A	N/A	Gated
CPU1.CPUCLK	Gated	Gated	N/A	N/A	Gated
CPU2.CLKIN	N/A	N/A	Active	Gated	Gated
CPU2.SYSCLK	N/A	N/A	Active	Gated	Gated
CPU2.CPUCLK	N/A	N/A	Gated	Gated	Gated
Clock to modules Connected to PERx.SYSCLK	Active	Gated if CPUSEL.PERx = CPU1	Active	Gated if CPUSEL.PERx = CPU2	Gated
WD1CLK	Active	Active	Active	Active	Gated if CLKSRCCTL1.WDHALTI = 0
WD2CLK	Active	Active	Active	Active	Gated
AUXPLLCLK	Active	Active	Active	Active	Gated
PLL	Powered	Powered	Powered	Powered	Powered-Down
INTOSC1	Powered	Powered	Powered	Powered	Powered down if CLKSRCCTL1.WDHALTI = 0
INTOSC2	Powered	Powered	Powered	Powered	Powered down if CLKSRCCTL1.WDHALTI = 0
Flash	Powered	Powered	Powered	Powered	Software-Controlled
X1,X2 OSC	Powered	Powered	Powered	Powered	Powered-Down

### 5.13.2 Power-Gating Low-Power Modes

HIBERNATE mode is the lowest power mode on this device. It is a global low-power mode that gates the supply voltages to most of the system. HIBERNATE is essentially a controlled power-down with remote wakeup capability, and can be used to save power during long periods of inactivity. [Table 5-20](#) describes the effects on the system when the HIBERNATE mode is entered.

**Table 5-20. Effect of Power-Gating Low-Power Mode on the Device**

MODULES/POWER DOMAINS	HIBERNATE
CPUx's M0 and M1 memories	<ul style="list-style-type: none"> <li>Remain on with memory retention if CPUx.LPMCR.M0M1MODE = 0x00</li> <li>Are off when CPUx.LPMCR.M0M1MODE = 0x01</li> </ul>
CPU1, CPU2, digital peripherals	Powered down
Dx, LSx, GSx memories	Power down, memory contents are lost
IOs	On with output state preserved
Oscillators, PLL, analog peripherals, Flash	Enters Low-Power Mode

## 6 Peripheral Information and Timings

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### NOTE

For the actual number of each peripheral on this device, see [Table 2-1](#).

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### 6.1 Analog Peripherals

The analog subsystem consists of:

- Four ADCs with selectable resolution of 16 bits or 12 bits
- Eight comparator subsystems (CMPSS), each containing a 12-bit reference DAC, two comparators, and a digital deglitching filter
- Three 12-bit buffered output DACs

[Figure 6-1](#) shows the Analog Subsystem Block Diagram for the 337-ball ZWT package. [Figure 6-2](#) shows the Analog Subsystem Block Diagram for the 176-pin PTP package.

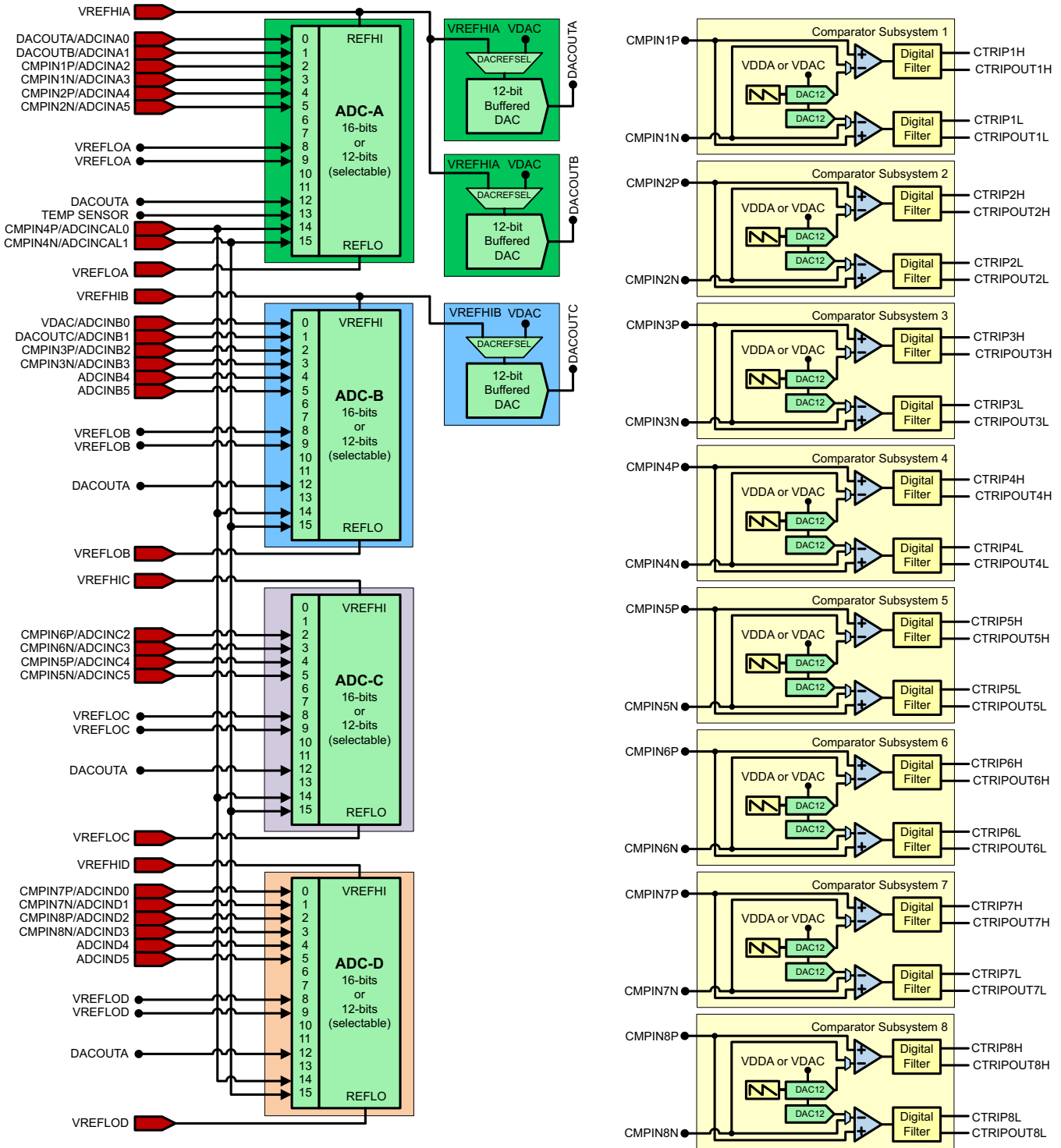


Figure 6-1. Analog Subsystem Block Diagram (337-Ball ZWT)

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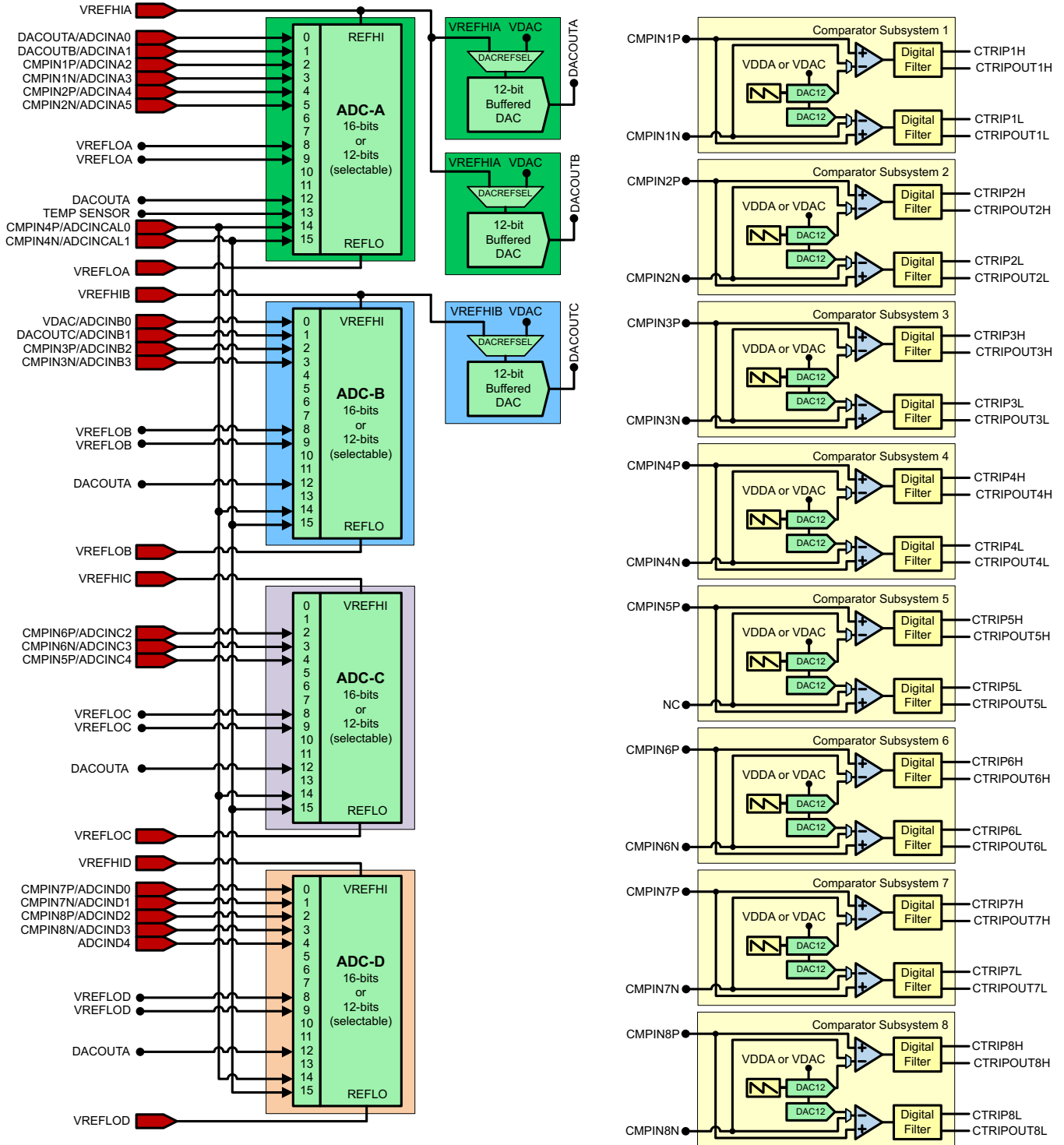


Figure 6-2. Analog Subsystem Block Diagram (176-Pin PTP)

### 6.1.1 Analog-to-Digital Converter (ADC)

The ADCs on this device are successive approximation (SAR) style ADCs with selectable resolution of either 16 bits or 12 bits. There are multiple ADC modules, allowing simultaneous sampling or independent operation. The ADC wrapper is start-of-conversion (SOC) based [see the "SOC Principle of Operation" section of the *TMS320F2837xD Delfino Technical Reference Manual* (literature number [SPRUHM8](#))].

Each ADC has the following features:

- Selectable resolution of 16 bits or 12 bits
- Ratiometric external reference set by  $V_{REFHI}$  and  $V_{REFLO}$
- Differential signal conversions
- Single-ended signal conversions (12-bit mode only)
- Input multiplexer with up to 16 channels (single-ended) or 8 channels (differential)
- 16 configurable SOCs
- 16 individually addressable result registers
- Multiple trigger sources
  - Software immediate start
  - All ePWMs - ADCSOC A, B, C, or D
  - GPIO XINT2
  - CPU timers
  - ADCINT1 or 2
- Four flexible PIE interrupts
- Burst mode
- Four post-processing blocks, each with:
  - Saturating offset calibration
  - Error from setpoint calculation
  - High, low, and zero-crossing compare, with interrupt and ePWM trip capability
  - Trigger-to-sample delay capture

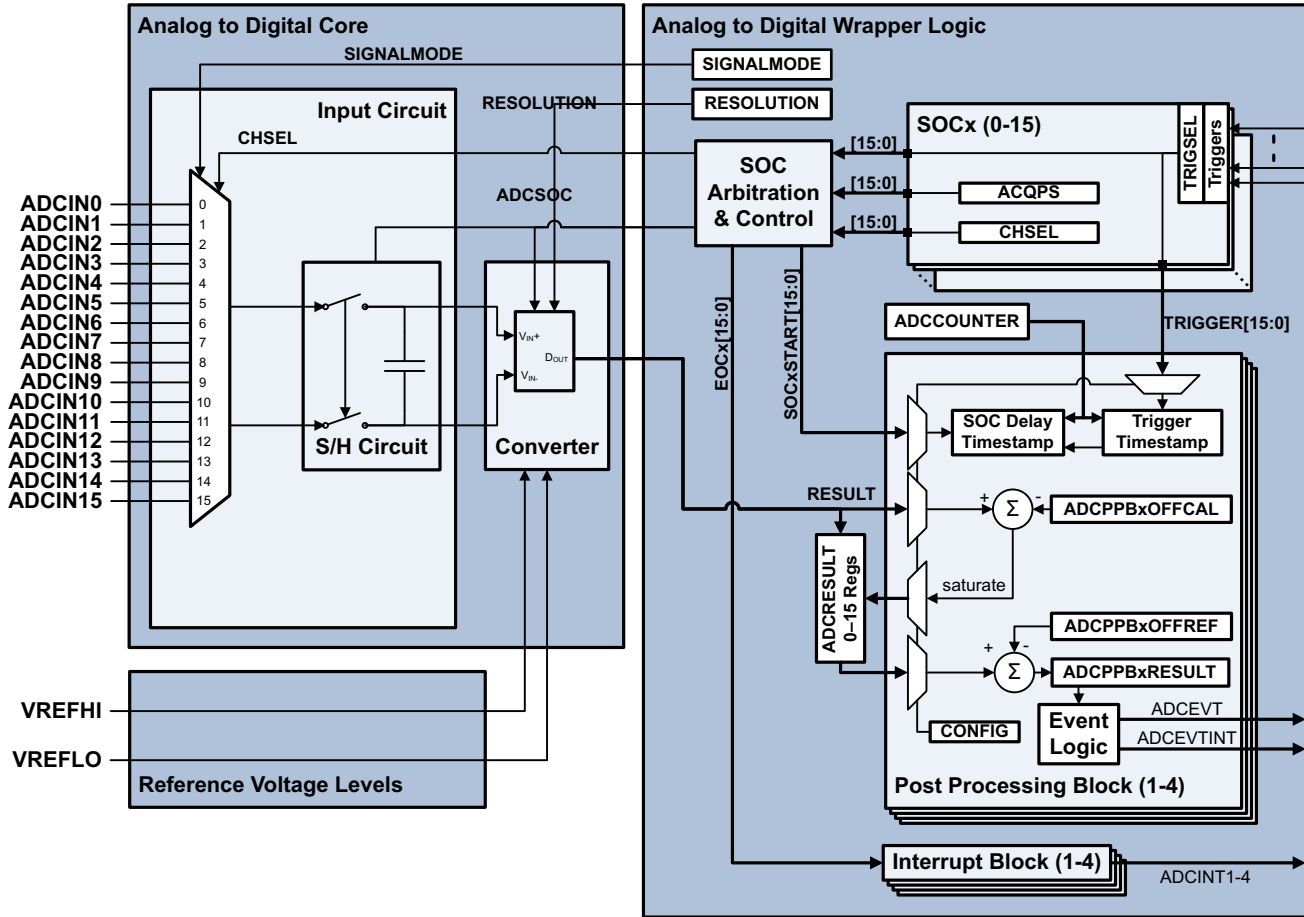


Figure 6-3. ADC Module Block Diagram

### 6.1.1.1 ADC Electrical Data and Timing

**Table 6-1. ADC Characteristics (16-Bit Mode)**

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input clock		1		50	MHz
Sample window duration		320			ns
ADC conversion cycles			29.5		ADCCLKs
Conversion range		$V_{REFLO}$		$V_{REFHI}$	V
$V_{REFHI}$		1.98	2.5	$V_{DDA}$	V
$V_{REFLO}$			0		V
Gain error			$\pm 64$		LSB
Offset error	$T_J = 30^\circ\text{C}$		$\pm 1$		mV
Offset error drift			$\pm 0.01$		mV/ $^\circ\text{C}$
DNL			$\pm 0.5$		LSB
INL			$\pm 1.5$		LSB
Channel-to-channel offset error			$\pm 2$		LSB
Common mode voltage <sup>(1)</sup>		$V_{REFCM} - 50$		$V_{REFCM} + 50$	mV

(1)  $V_{REFCM} = (V_{REFHI} + V_{REFLO})/2$ 
**Table 6-2. ADC Characteristics (12-Bit Mode)**

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input clock		1		50	MHz
Sample window duration		75			ns
ADC conversion cycles			10.5		ADCCLKs
Conversion range		$V_{REFLO}$		$V_{REFHI}$	V
$V_{REFHI}$		1.98	3.3	$V_{DDA}$	V
$V_{REFLO}$			0		V
Gain error			$\pm 4$		LSB
Offset error			$\pm 4$		LSB
DNL			$\pm 0.5$		LSB
INL			$\pm 1.5$		LSB
Channel-to-channel offset error			$\pm 2$		LSB
Common mode voltage <sup>(1)</sup>		$V_{REFCM} - 50$		$V_{REFCM} + 50$	mV

(1)  $V_{REFCM} = (V_{REFHI} + V_{REFLO})/2$ 

### 6.1.1.2 Temperature Sensor Electrical Data and Timing

**Table 6-3. Temperature Sensor Electrical Characteristics**

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Temperature accuracy			$\pm 15$		$^\circ\text{C}$
Startup time			500		$\mu\text{s}$

### 6.1.2 Buffered Digital-to-Analog Converter (DAC)

The Buffered DAC module consists of an internal reference DAC and an analog output buffer that is capable of driving an external load. An integrated pull-down resistor on the DAC output helps to provide a known pin voltage when the output buffer is disabled. This pull-down resistor cannot be disabled and remains as a passive component on the pin, even for other shared pinmux functions. Software writes to the DAC value register can take effect immediately or can be synchronized with PWMSYNC events.

Each Buffered DAC has the following features:

- 12-bit programmable internal DAC
- Selectable reference voltage
- Analog output buffer
- Pull-down resistor on output
- Ability to synchronize with PWMSYNC

The block diagram for the buffered DAC is shown in Figure 6-4.

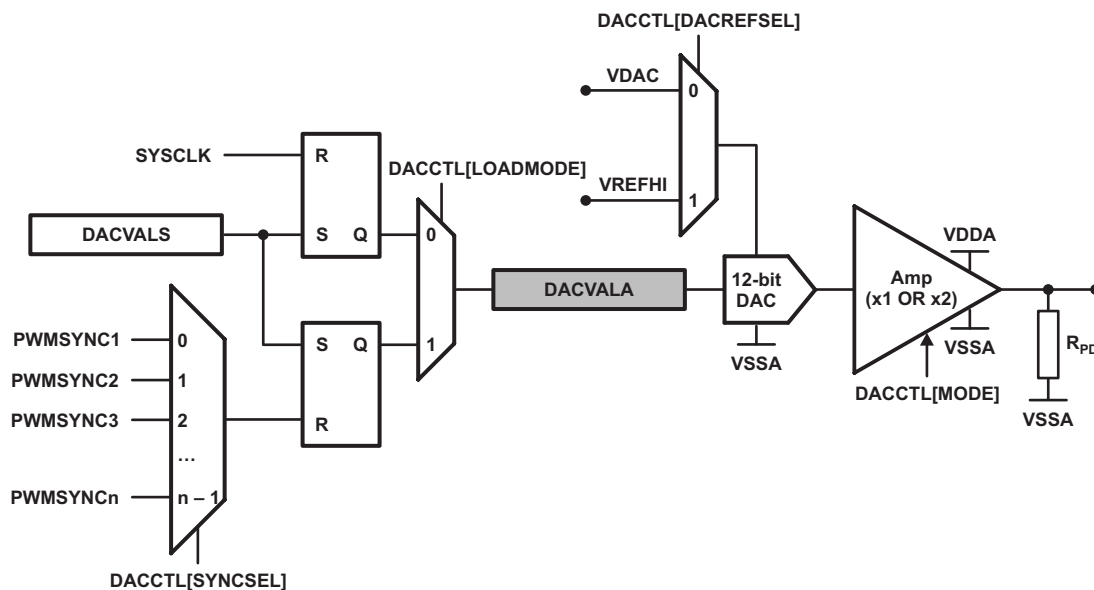


Figure 6-4. DAC Module Block Diagram

**6.1.2.1 Buffered DAC Electrical Data and Timing**
**Table 6-4. Buffered DAC Electrical Characteristics**

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power supply rejection	1 Hz		70		dB
Noise			500		μV
Untrimmed offset	End point corrected		±40		mV
Gain error			±2.5		% of FSR
DNL			±0.4		LSB
INL	End point corrected		±2		LSB
Voltage output settling time			2		μs
Resolution			12		Bit
Output range			0.6 to ( $V_{REF} - 0.6$ )		V
Maximum capacitive load			100		pF
Minimum resistive load			5		kΩ

### 6.1.3 Comparator Subsystem (CMPSS)

Each CMPSS module includes two sets of comparators, internal voltage reference DACs, digital glitch filters, and ramp generator logic. There are two inputs, CMPINxP and CMPINxN. Each of these will be internally connected to an ADCIN pin. The CMPINxP pin is always connected to the positive input of the CMPSS comparators. CMPINxN can be used instead of the DAC output to drive the negative comparator inputs. There are two comparators, and therefore two outputs from the CMPSS module, which are connected to the input of a digital filter module before being passed on to the Comparator TRIP crossbar and either PWM modules or directly to a GPIO pin. Figure 6-5 shows the CMPSS connectivity.

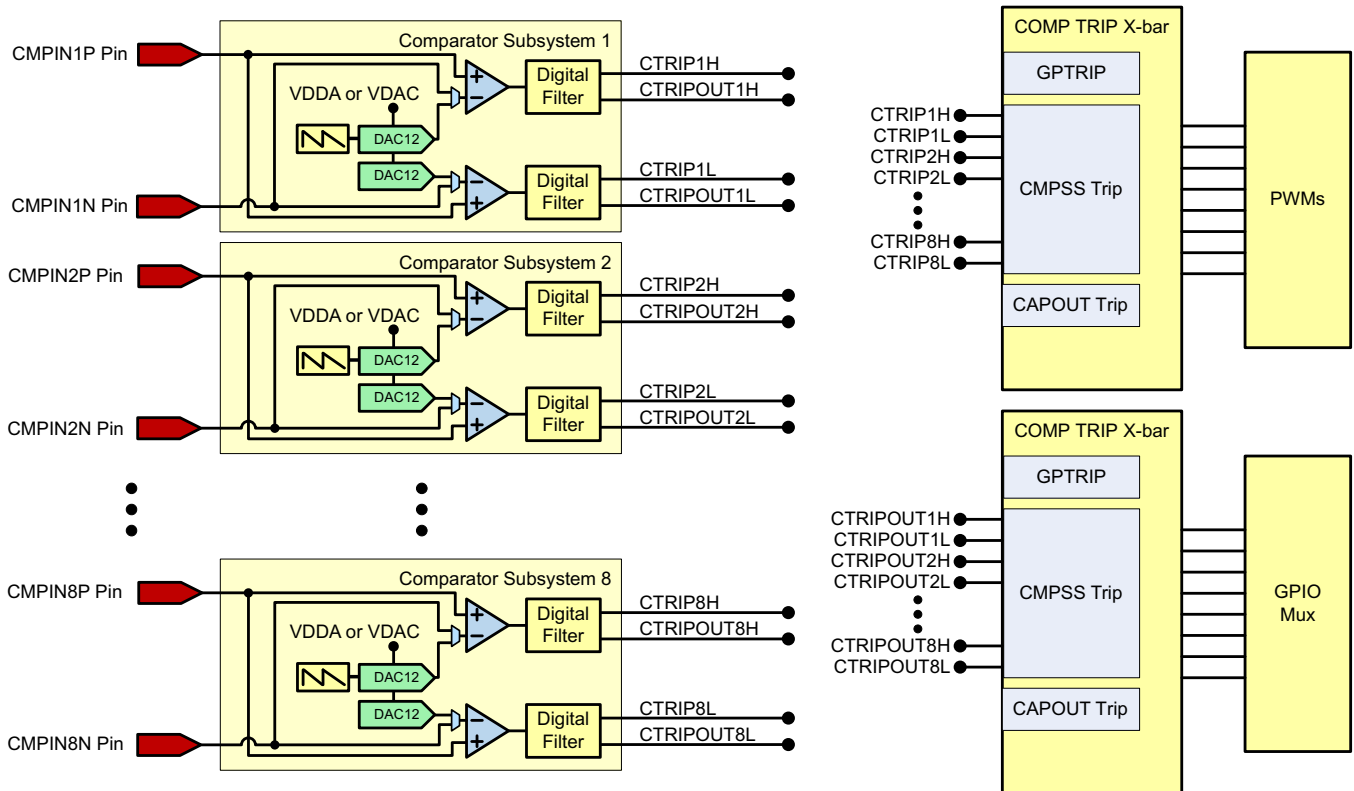


Figure 6-5. CMPSS Connectivity

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**6.1.3.1 CMPSS Electrical Data and Timing**
**Table 6-5. Comparator Electrical Characteristics**

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Comparator input referred offset			±20		mV
Comparator hysteresis values			7		mV

**Table 6-6. Comparator/DAC Electrical Characteristics**

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC offset			1		mV
DAC gain error			-1		%
DAC static INL			±16		LSB
DAC resolution			12		Bit

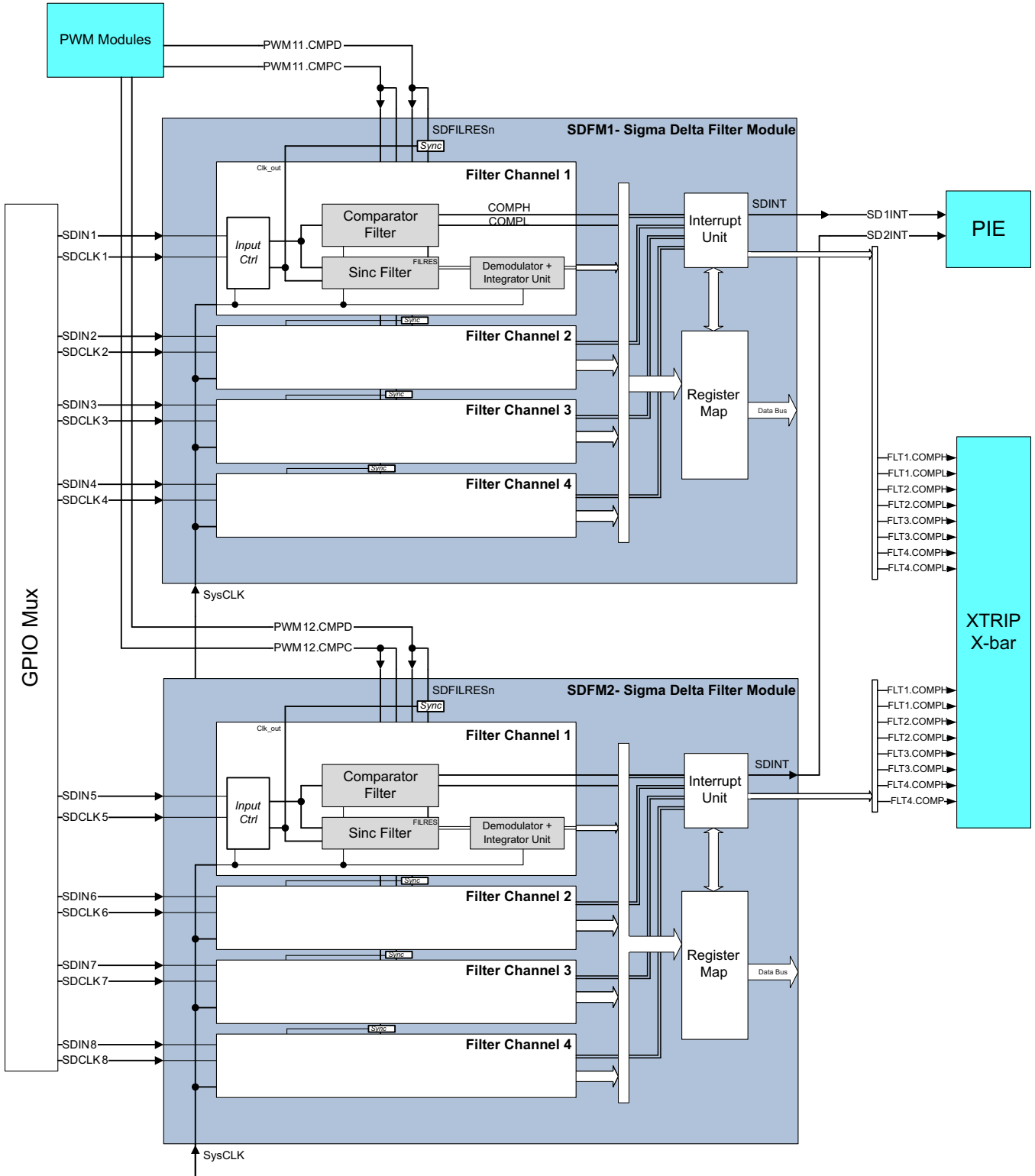
## 6.2 Control Peripherals

### 6.2.1 Sigma Delta Filter Module (SDFM)

SDFM is a four-channel digital filter designed specifically for current measurement and resolver position decoding in motor control applications. Each channel can receive an independent sigma-delta ( $\Sigma\Delta$ ) modulated bit stream. The bit streams are processed by four individually programmable digital decimation filters. The filter set includes a fast comparator for immediate digital threshold comparisons for over-current and under-current monitoring. The flexible SDFM also offers a filter-bypass mode to enable data logging, analysis, and customized filtering. [Figure 6-6](#) shows a block diagram of the SDFMs.

SDFM features include:

- Four external pins per SDFM module:
  - Four sigma delta data input pins per SDFM module (SD-Dx, where x = 1 to 4)
  - Four sigma delta clock input pins per SDFM module (SD-Cx, where x = 1 to 4)
- Four different configurable modulator clock modes:
  - Modulator clock rate equals modulator data rate
  - Modulator clock rate running at half the modulator data rate
  - Modulator data is Manchester encoded. Modulator clock not required.
  - Modulator clock rate is double that of modulator data rate
- Four independent configurable comparator units:
  - Four different filter type selection (Sinc1/Sinc2/Sincfast/Sinc3) options available
  - Ability to detect over-value and under-value conditions
  - OSR value for comparator programmable from 1 to 32
- Four independent configurable sinc filter units:
  - Four different filter type selection (Sinc1/Sinc2/Sincfast/Sinc3) options available
  - Ability to bypass filter module
  - OSR value for filter unit programmable from 1 to 256
  - Ability to enable or disable individual filter module
  - Ability to synchronize all four independent filters of a SDFM module using the Master Filter Enable (MFE) bit or the PWM signals.
- Filter data can be 16-bit or 32-bit representation
- PWMs can be used to generate carrier frequency for resolver applications



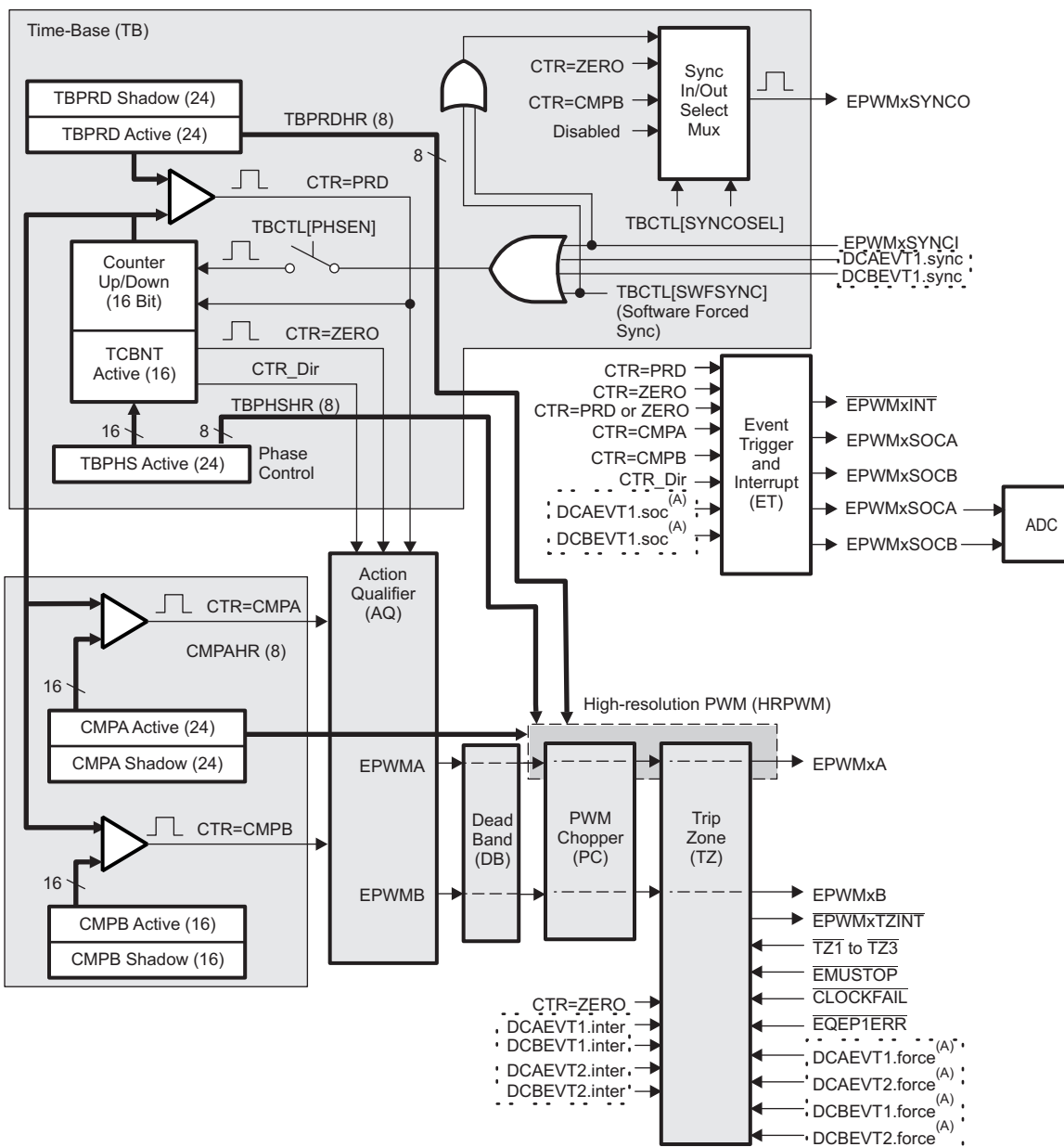
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Figure 6-6. SDFM

### 6.2.2 Enhanced Pulse Width Modulator (ePWM)

The enhanced pulse width modulator (ePWM) peripheral is a key element in controlling many of the power electronic systems found in both commercial and industrial equipment. The ePWM type-3 module is able to generate complex pulse width waveforms with minimal CPU overhead by building the peripheral up from smaller modules with separate resources that can operate together to form a system. Some of the highlights of the ePWM type-3 module include complex waveform generation, dead-band generation, a flexible synchronization scheme, advanced trip-zone functionality, and global register reload capabilities.

Figure 6-7 shows the signal interconnections with the ePWM.



A. These events are generated by the Type 1 ePWM digital compare (DC) submodule based on the levels of the COMPxOUT and TZ signals.

**Figure 6-7. ePWM Sub-Modules Showing Critical Internal Signal Interconnections**

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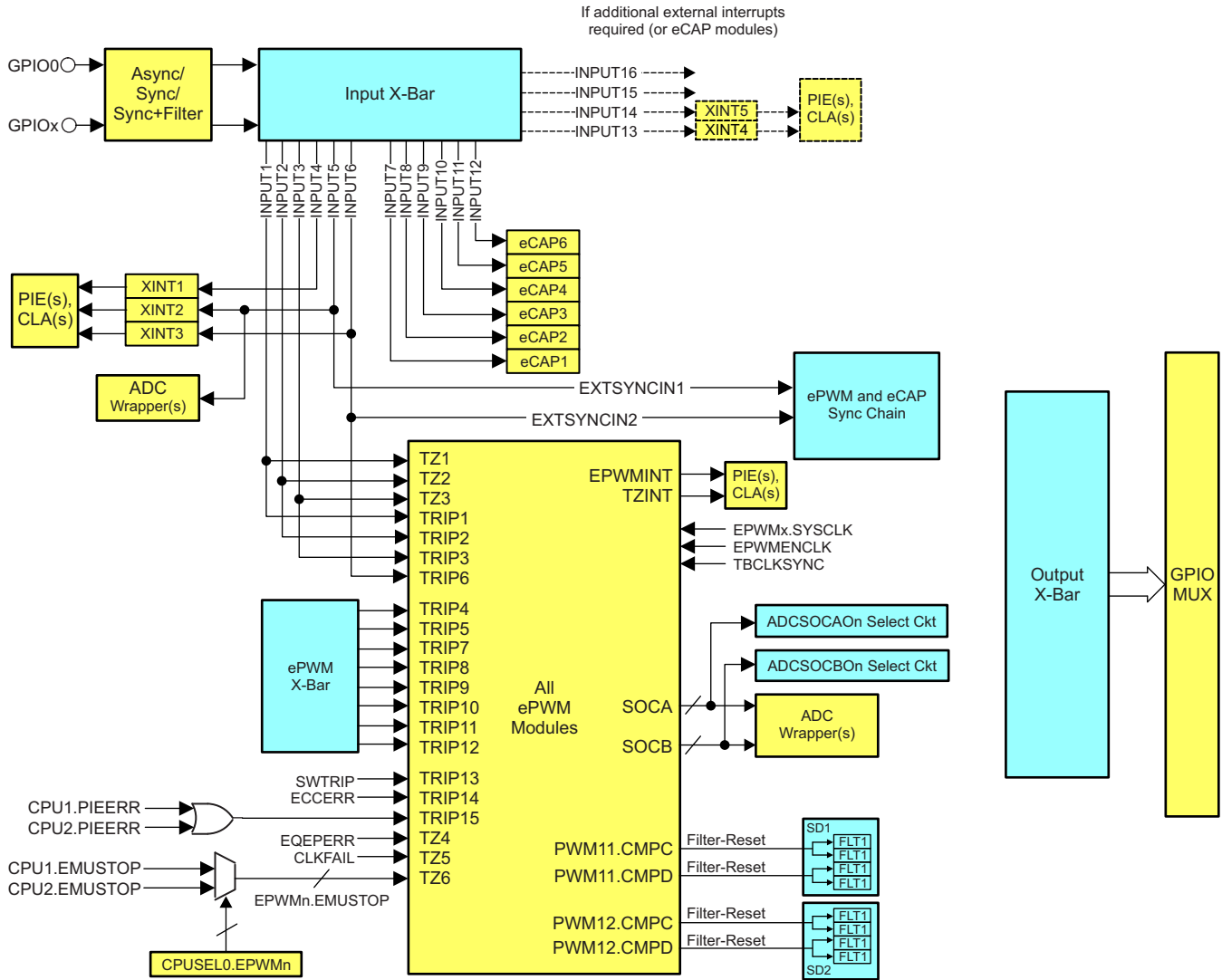


Figure 6-8. ePWM

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### 6.2.2.1 Control Peripherals Synchronization

The ePWM and eCAP Synchronization Chain on the device provides flexibility in partitioning the ePWM and eCAP modules between CPU1 and CPU2 and allows localized synchronization within the modules belonging to the same CPU. Like all F2837xD peripherals, the partitioning of the ePWM and eCAP modules needs to be done using the CPUSELx registers. Figure 6-9 shows the Synchronization Chain Architecture.

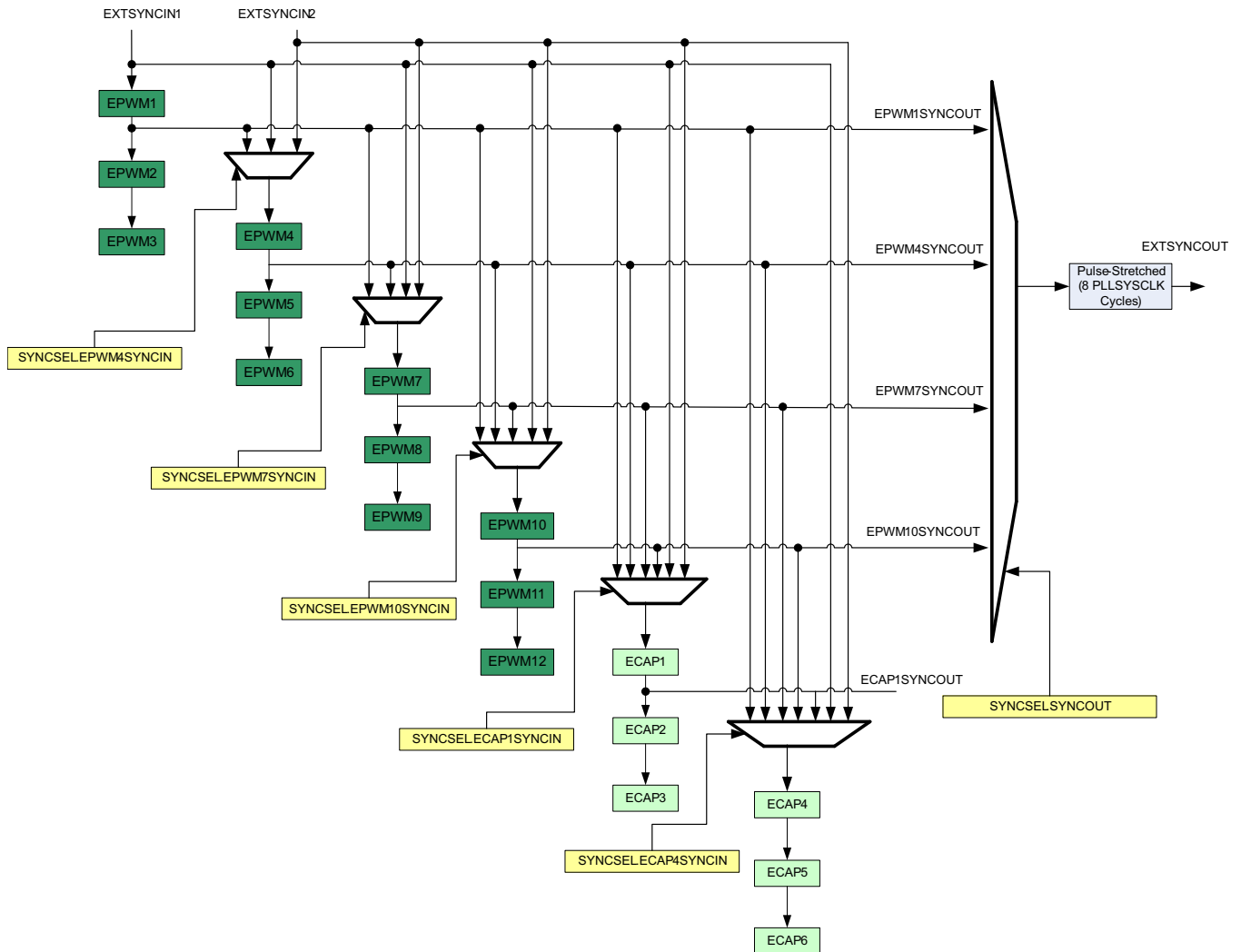


Figure 6-9. Synchronization Chain Architecture

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### 6.2.3 High-Resolution PWM (HRPWM)

This module combines multiple delay lines in a single module and a simplified calibration system by using a dedicated calibration delay line. For each ePWM module there is one HR delay line.

The HRPWM module offers PWM resolution (time granularity) that is significantly better than what can be achieved using conventionally derived digital PWM methods. The key points for the HRPWM module are:

- Significantly extends the time resolution capabilities of conventionally derived digital PWM
- This capability can be utilized in both single edge (duty cycle and phase-shift control) as well as dual edge control for frequency/period modulation.
- Finer time granularity control or edge positioning is controlled via extensions to the Compare A and Phase registers of the ePWM module.
- HRPWM capabilities, when available on a particular device, are offered only on the A signal path of an ePWM module (that is, on the EPWMxA output). EPWMxB output has conventional PWM capabilities.

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**NOTE**

The minimum SYSCLKOUT frequency allowed for HRPWM is 60 MHz.

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**NOTE**

When dual-edge high-resolution is enabled (high-resolution period mode), the PWMxB output is not available for use.

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### 6.2.4 Enhanced Capture (eCAP)

Figure 6-10 shows the block diagram of a module.

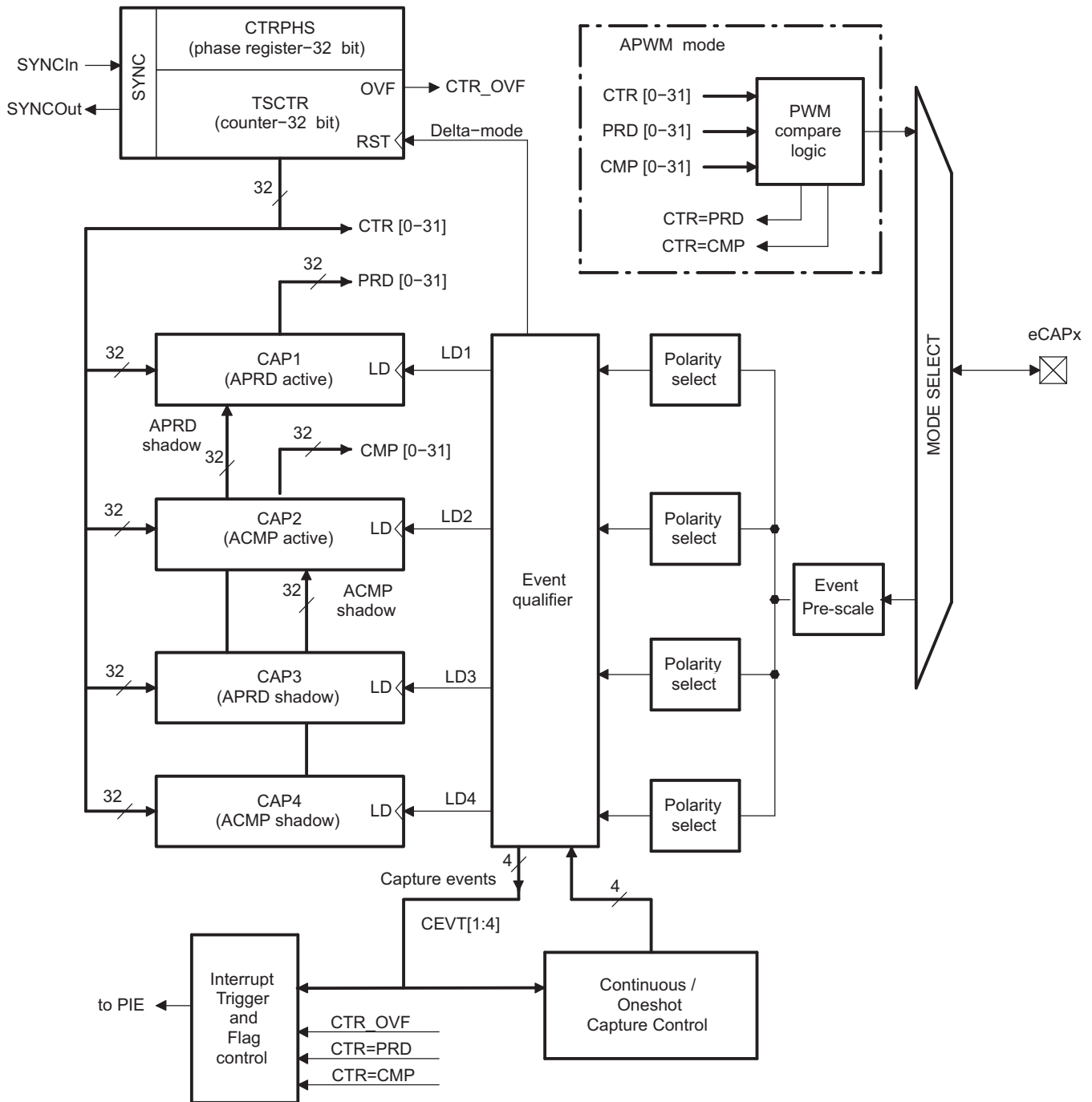


Figure 6-10. eCAP Block Diagram

The eCAP module is clocked at the SYSCLKOUT rate.

The clock enable bits (ECAP1 ENCLK) in the PCLKCR1 register turn off the eCAP module individually (for low power operation). Upon reset, ECAP1ENCLK is set to low, indicating that the peripheral clock is off.

### 6.2.5 Enhanced Quadrature Encoder Pulse (eQEP)

Figure 6-11 shows the eQEP block diagram.

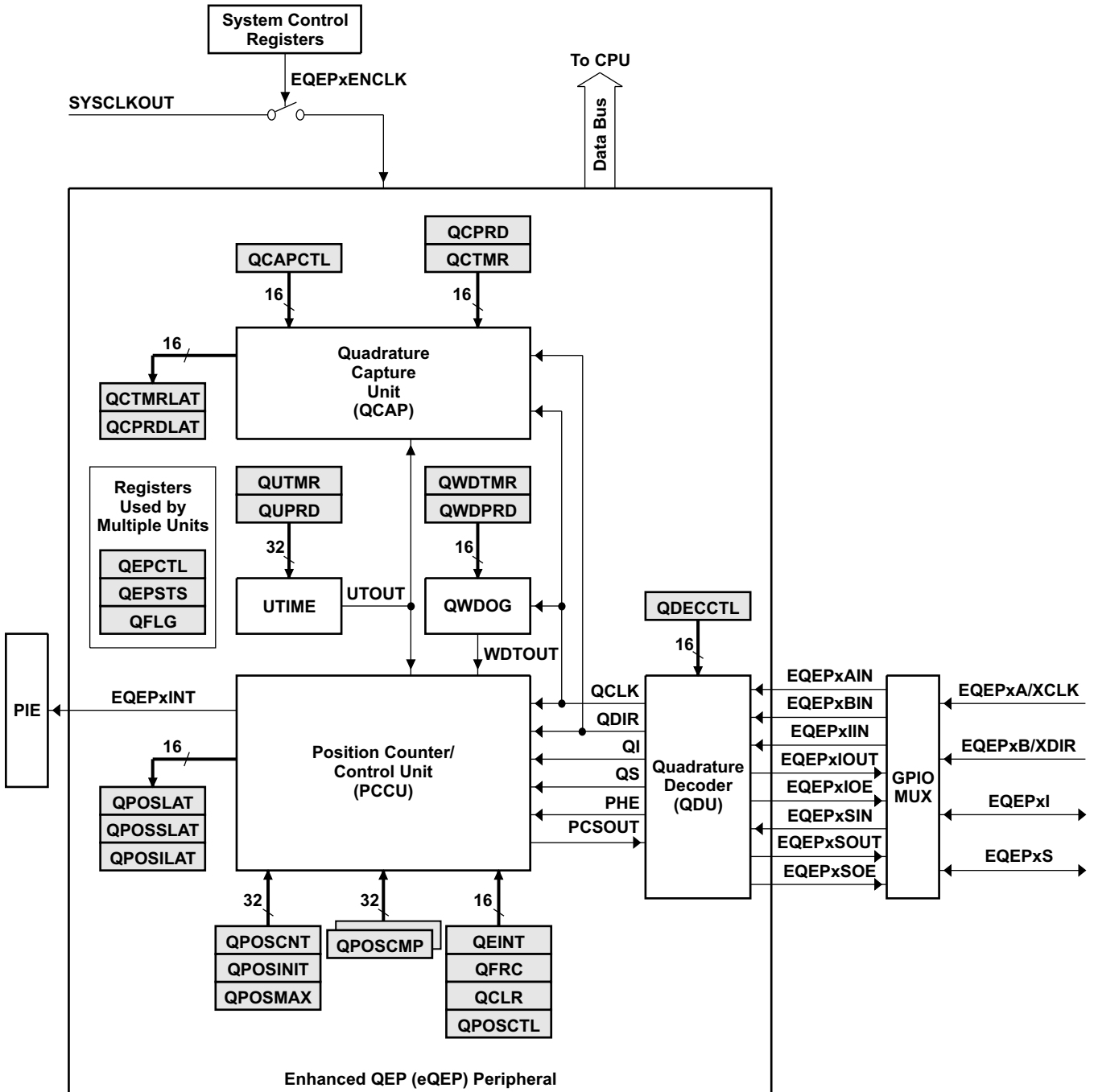


Figure 6-11. eQEP Block Diagram

ADVANCE INFORMATION

## 6.3 Communications Peripherals

### 6.3.1 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) is a high-speed synchronous serial input/output (I/O) port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communications between the microcontroller and external peripherals or another controller. Typical applications include external I/O or peripheral expansion via devices such as shift registers, display drivers, and analog-to-digital converters (ADCs). Multi-device communications are supported by the master/slave operation of the SPI. The port supports a 16-level, receive-and-transmit FIFO for reducing CPU servicing overhead.

The SPI module features include:

- SPISOMI: SPI slave-output/master-input pin
- SPISIMO: SPI slave-input/master-output pin
- SPISTE: SPI slave transmit-enable pin
- SPICLK: SPI serial-clock pin
- Two operational modes: master and slave
- Baud rate: 125 different programmable rates. The maximum baud rate that can be employed is limited by the maximum speed of the I/O buffers used on the SPI pins.
- Data word length: 1 to 16 data bits
- Four clocking schemes (controlled by clock polarity and clock phase bits) include:
  - Falling edge without phase delay: SPICLK active-high. SPI transmits data on the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
  - Falling edge with phase delay: SPICLK active-high. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge without phase delay: SPICLK inactive-low. SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge with phase delay: SPICLK inactive-low. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
- Simultaneous receive-and-transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithms.
- 16-level transmit and receive FIFO
- Delayed transmit control

The SPI operates in master or slave mode. The master initiates data transfer by sending the SPICLK signal. For both the slave and the master, data is shifted out of the shift registers on one edge of the SPICLK and latched into the shift register on the opposite SPICLK clock edge. If the CLOCK PHASE bit (SPICTL.3) is high, data is transmitted and received a half-cycle before the SPICLK transition. As a result, both controllers send and receive data simultaneously. The application software determines whether the data is meaningful or dummy data. There are three possible methods for data transmission:

- Master sends data; slave sends dummy data
- Master sends data; slave sends data
- Master sends dummy data; slave sends data

The master can initiate a data transfer at any time because it controls the SPICLK signal. The software, however, determines how the master detects when the slave is ready to broadcast data.

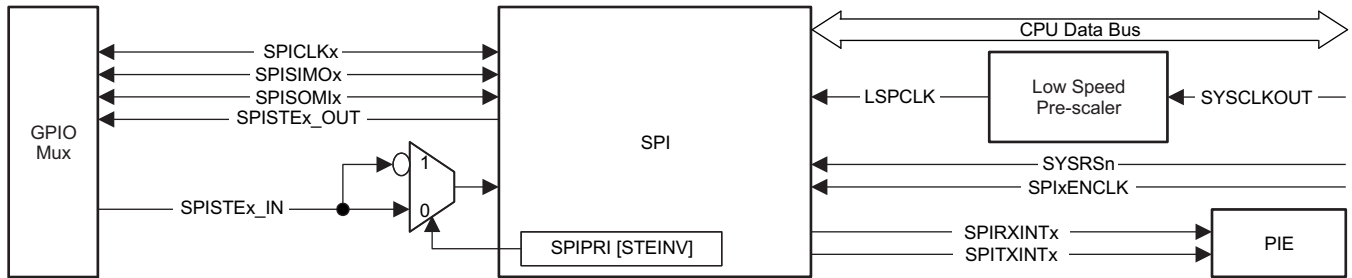


Figure 6-12. SPI

### 6.3.2 Serial Communications Interface (SCI)

SCI is a two-wire asynchronous serial port, commonly known as a UART. The SCI module supports digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format

The SCI receiver and transmitter each have a 16-level-deep FIFO for reducing servicing overhead, and each has its own separate enable and interrupt bits. Both can be operated independently for half-duplex communication, or simultaneously for full-duplex communication. To specify data integrity, the SCI checks received data for break detection, parity, overrun, and framing errors. The bit rate is programmable to different speeds through a 16-bit baud-select register.

Features of the SCI module include:

- Two external pins:
  - SCITXD: SCI transmit-output pin
  - SCIRXD: SCI receive-input pin
  - NOTE:** Both pins can be used as GPIO if not used for SCI.
  - Baud rate programmable to 64K different rates
- Data-word format
  - One start bit
  - Data-word length programmable from one to eight bits
  - Optional even/odd/no parity bit
  - One or two stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: idle-line and address bit
- Half- or full-duplex operation
- Double-buffered receive and transmit functions
- Transmitter and receiver operations can be accomplished through interrupt-driven or polled algorithms with status flags.
  - Transmitter: TXRDY flag (transmitter-buffer register is ready to receive another character) and TX EMPTY flag (transmitter-shift register is empty)
  - Receiver: RXRDY flag (receiver-buffer register is ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR flag (monitoring four interrupt conditions)
- Separate enable bits for transmitter and receiver interrupts (except BRKDT)
- NRZ (non-return-to-zero) format

---

#### NOTE

All registers in this module are 8-bit registers. When a register is accessed, the register data is in the lower byte (bits 7–0), and the upper byte (bits 15–8) is read as zeros. Writing to the upper byte has no effect.

---

- Auto baud-detect hardware logic
- 16-level transmit and receive FIFO

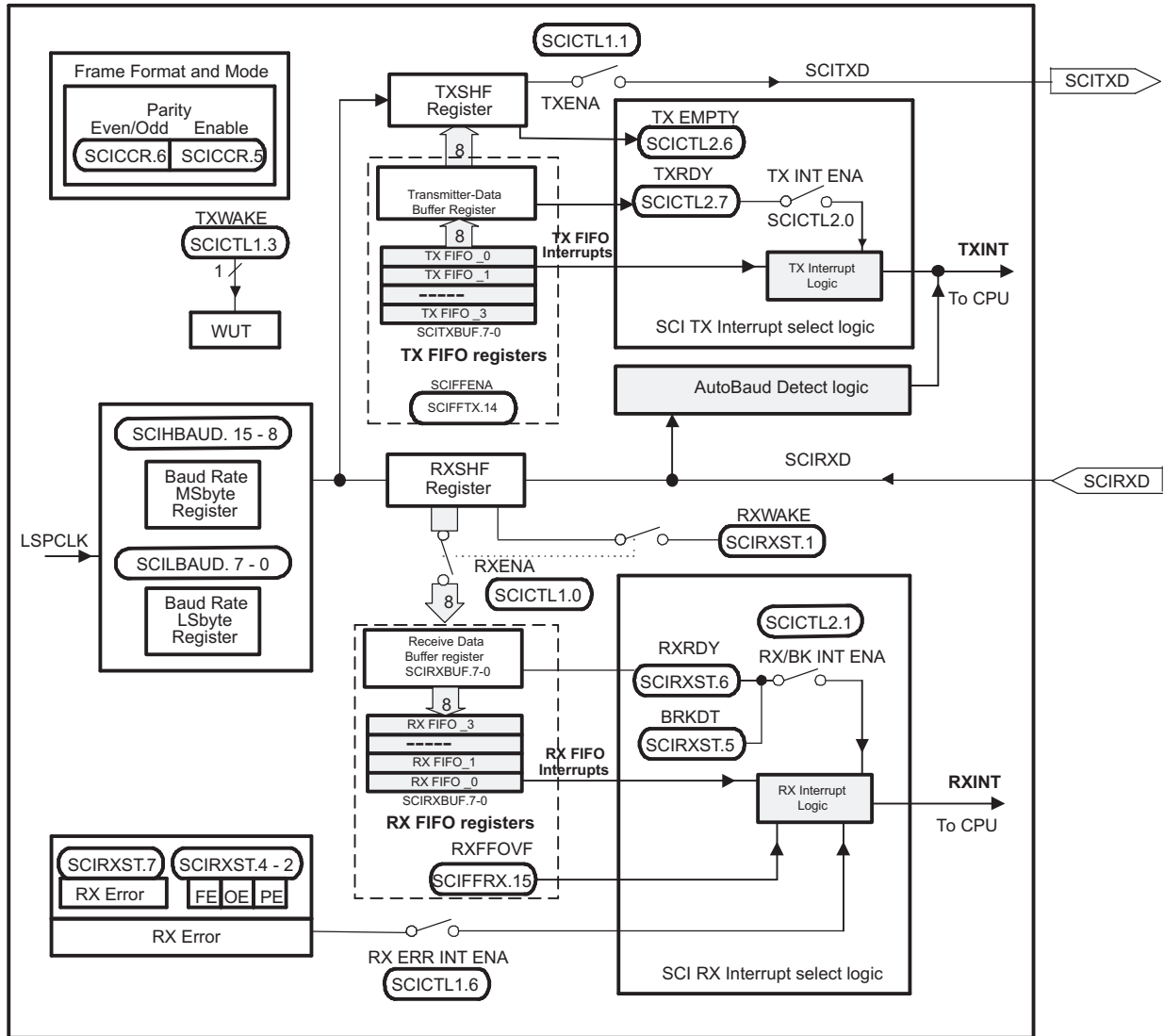


Figure 6-13. SCI Block Diagram

The major elements used in full-duplex operation include:

- A transmitter (TX) and its major registers:
  - SCITXBUF register – Transmitter Data Buffer register. Contains data (loaded by the CPU) to be transmitted
  - TXSHF register – Transmitter Shift register. Accepts data from the SCITXBUF register and shifts data onto the SCITXD pin, one bit at a time
- A receiver (RX) and its major registers:
  - RXSHF register – Receiver Shift register. Shifts data in from the SCIRXD pin, one bit at a time
  - SCIRXBUF register – Receiver Data Buffer register. Contains data to be read by the CPU. Data from a remote processor is loaded into the RXSHF register and then into the SCIRXBUF and SCIRXEMU registers
- A programmable baud generator
- Data-memory-mapped control and status registers enable the CPU to access the I<sup>2</sup>C module registers and FIFOs.

The SCI receiver and transmitter can operate either independently or simultaneously.

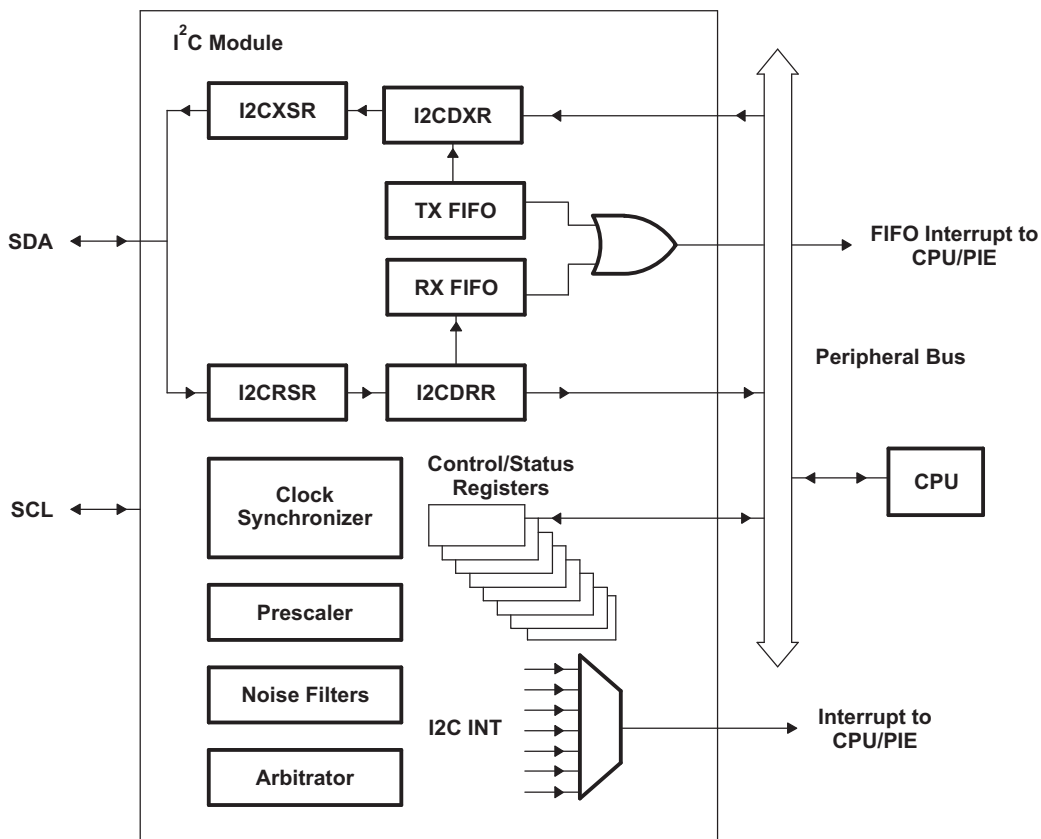
ADVANCE INFORMATION

### 6.3.3 Inter-Integrated Circuit (I<sup>2</sup>C)

The I<sup>2</sup>C module has the following features:

- Compliance with the Philips Semiconductors I<sup>2</sup>C-bus specification (version 2.1):
  - Support for 1-bit to 8-bit format transfers
  - 7-bit and 10-bit addressing modes
  - General call
  - START byte mode
  - Support for multiple master-transmitters and slave-receivers
  - Support for multiple slave-transmitters and master-receivers
  - Combined master transmit/receive and receive/transmit mode
  - Data transfer rate of from 10 kbps up to 400 kbps (I<sup>2</sup>C Fast-mode rate)
- One 4-word receive FIFO and one 4-word transmit FIFO
- One interrupt that can be used by the CPU. This interrupt can be generated as a result of one of the following conditions:
  - Transmit-data ready
  - Receive-data ready
  - Register-access ready
  - No-acknowledgment received
  - Arbitration lost
  - Stop condition detected
  - Addressed as slave
- An additional interrupt that can be used by the CPU when in FIFO mode
- Module enable/disable capability
- Free data format mode

Figure 6-14 shows how the I<sup>2</sup>C peripheral module interfaces within the device.



- A. The I<sup>2</sup>C registers are accessed at the SYSCLKOUT rate. The internal timing and signal waveforms of the I<sup>2</sup>C port are also at the SYSCLKOUT rate.
- B. The clock enable bit (I2CAENCLK) in the PCLKCRO register turns off the clock to the I<sup>2</sup>C port for low power operation. Upon reset, I2CAENCLK is clear, which indicates the peripheral internal clocks are off.

**Figure 6-14. I<sup>2</sup>C Peripheral Module Interfaces**

### 6.3.4 Multichannel Buffered Serial Port (McBSP)

The McBSP module has the following features:

- Compatible to McBSP in TMS320C54x™/ TMS320C55x™ DSP devices
- Full-duplex communication
- Double-buffered data registers that allow a continuous data stream
- Independent framing and clocking for receive and transmit
- External shift clock generation or an internal programmable frequency shift clock
- A wide selection of data sizes including 8-, 12-, 16-, 20-, 24-, or 32-bits
- 8-bit data transfers with LSB or MSB first
- Programmable polarity for both frame synchronization and data clocks
- Highly programmable internal clock and frame generation
- Direct interface to industry-standard CODECs, Analog Interface Chips (AICs), and other serially connected A/D and D/A devices
- Works with SPI-compatible devices
- The following application interfaces can be supported on the McBSP:
  - T1/E1 framers
  - IOM-2 compliant devices
  - AC97-compliant devices (the necessary multiphase frame synchronization capability is provided.)
  - IIS-compliant devices
  - SPI
- McBSP clock rate,

$$\text{CLKG} = \frac{\text{CLKSRG}}{(1 + \text{CLKGDV})}$$

where CLKSRG source could be LSPCLK, CLKX, or CLKR. Serial port performance is limited by I/O buffer switching speed. Internal prescalers must be adjusted such that the peripheral speed is less than the I/O buffer speed limit.

Figure 6-15 shows the block diagram of the McBSP module.

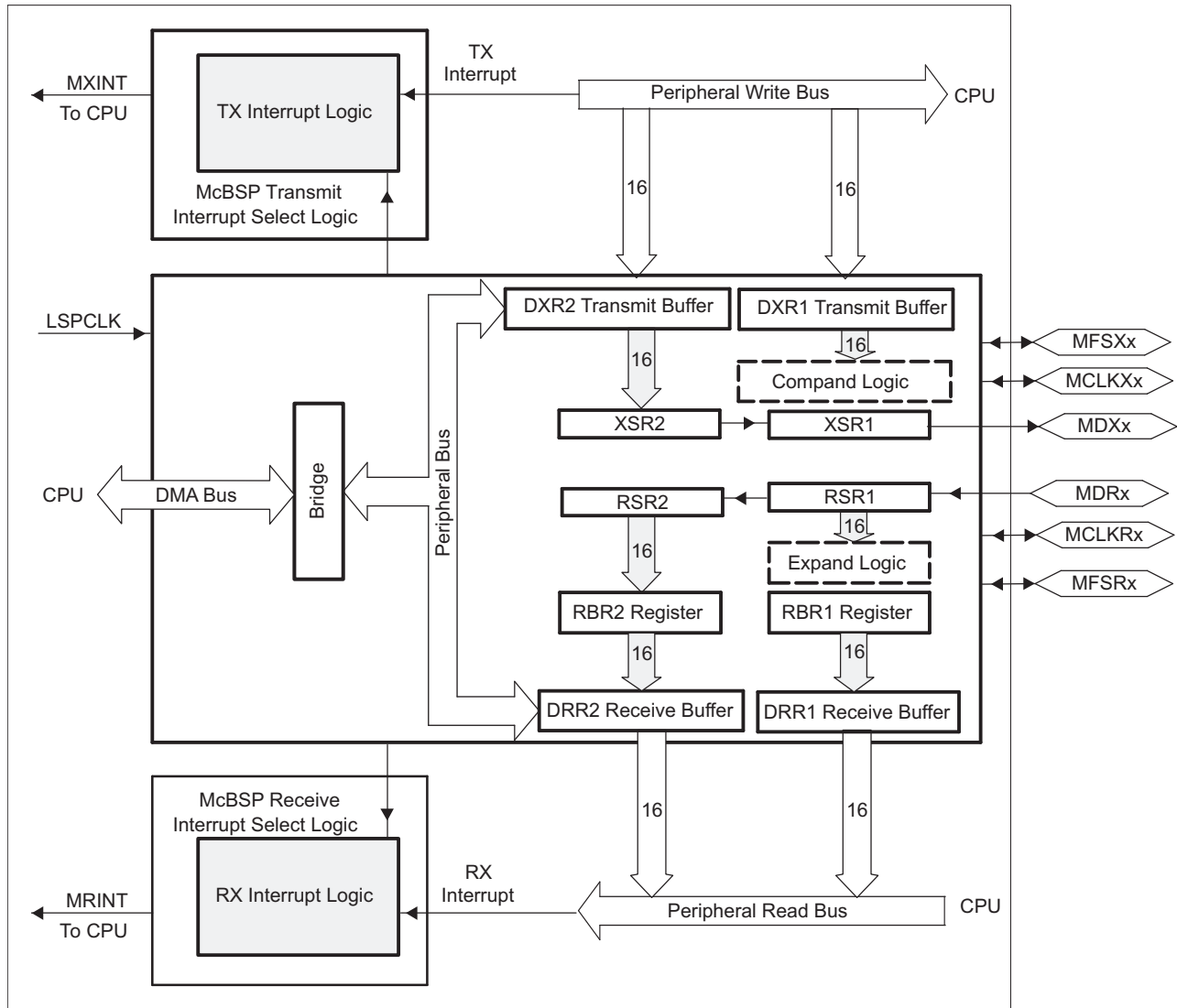


Figure 6-15. McBSP Block Diagram

ADVANCE INFORMATION

### 6.3.5 Universal Serial Bus (USB) Controller

The USB controller operates as a full-speed or low-speed function controller during point-to-point communications with USB host, device, or OTG functions.

The USB module has the following features:

- Complies with USB-IF certification standards
- USB 2.0 full-speed (12 Mbps) and low-speed (1.5 Mbps) operation
- Integrated PHY
- Four transfer types: control, interrupt, bulk, and isochronous
- 32 endpoints
  - One dedicated control IN endpoint and one dedicated control OUT endpoint
  - 15 configurable IN endpoints and 15 configurable OUT endpoints
- Four KB dedicated endpoint memory: one endpoint may be defined for double-buffered 1023-byte isochronous packet size
- VBUS droop and valid ID detection and interrupt
- Efficient transfers using direct memory access controller (DMA)
  - Separate channels for transmit and receive for up to three IN endpoints and three OUT endpoints
  - Channel requests asserted when FIFO contains required amount of data

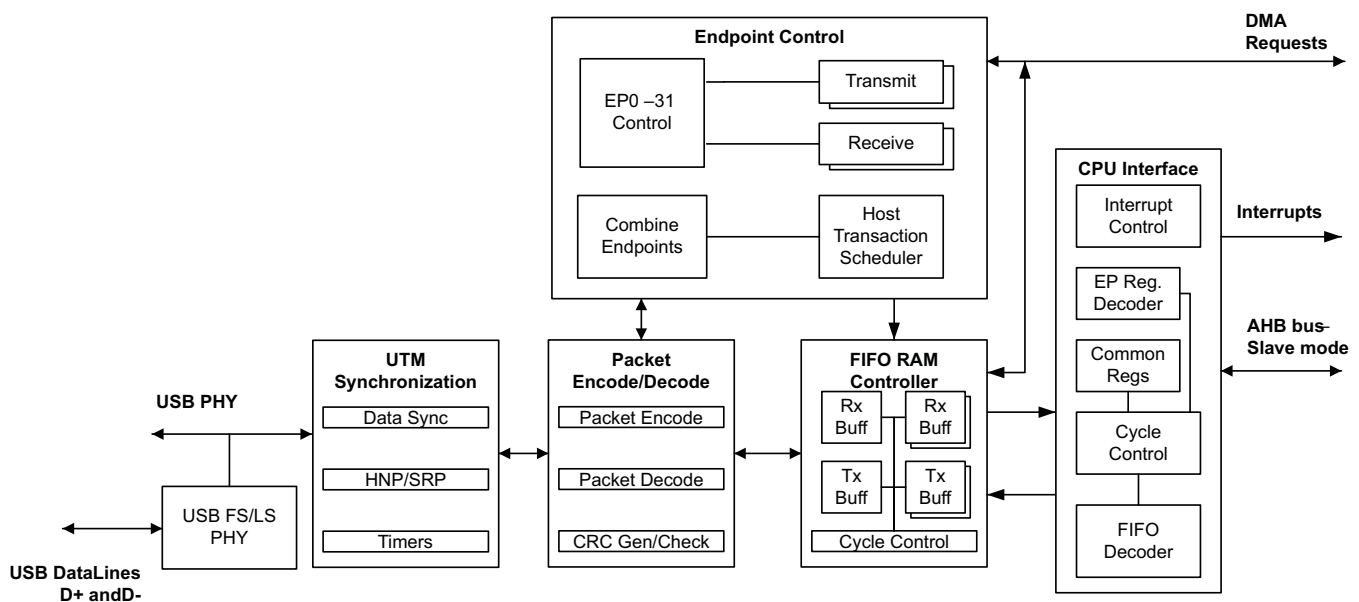


Figure 6-16. USB Block Diagram

### 6.3.6 Controller Area Network (CAN)

The CAN module (CAN) has the following features:

- Fully compliant with CAN protocol, version 2.0B
- Supports data rates up to 1 Mbps
- Thirty-two mailboxes, each with the following properties:
  - Configurable as receive or transmit
  - Configurable with standard or extended identifier
  - Has a programmable receive mask
  - Individual identifier mask for each message object
  - Supports data and remote frame
  - Composed of 0 to 8 bytes of data
  - Uses a 32-bit time stamp on receive and transmit message
  - Protects against reception of new message
  - Holds the dynamically programmable priority of transmit message
  - Employs a programmable interrupt scheme with two interrupt levels
  - Employs a programmable alarm on transmission or reception time-out
  - Programmable FIFO mode for message objects
  - Message RAM parity check mechanism
- Low-power mode
- Programmable wake-up on bus activity
- Automatic reply to a remote request message
- Automatic retransmission of a frame in case of loss of arbitration or error
- 32-bit local network time counter synchronized by a specific message (communication in conjunction with mailbox 16)
- Self-test mode
  - Operates in a loopback mode receiving its own message. A "dummy" acknowledge is provided, thereby eliminating the need for another node to provide the acknowledge bit.

**NOTE**

For a SYSCLKOUT of 200 MHz, the smallest bit rate possible is 7.8125 kbps.

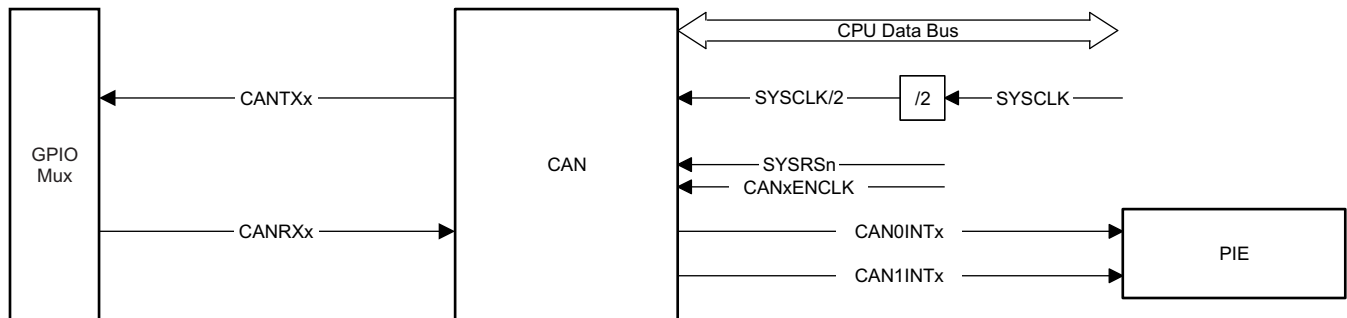


Figure 6-17. CAN

### 6.3.7 External Memory Interface (EMIF)

This EMIF memory controller is compliant with the JESD21-C SDR SDRAMs utilizing a 32-bit/16-bit data bus. The purpose of this EMIF is to provide a means for the CPU to connect to a variety of external devices.

#### 6.3.7.1 Asynchronous Memory Support

The EMIF supports asynchronous memories:

- SRAMs
- NOR Flash memories

There is an external wait input that allows slower asynchronous memories to extend the memory access. The EMIF module supports up to three chip selects (EMIF\_CS[4:2]). Each chip select has the following individually programmable attributes:

- Data bus width
- Read cycle timings: setup, hold, strobe
- Write cycle timings: setup, hold, strobe
- Bus turnaround time
- Extended wait option with programmable timeout
- Select strobe option

#### 6.3.7.2 Synchronous DRAM (SDRAM) Support

The EMIF module supports 16-bit/32-bit SDRAM, it has a single SDRAM chip select ( $\overline{\text{EMIF\_CS[0]}}$ ). SDRAM configurations supported are:

- One-bank, two-bank, and four-bank SDRAM devices
- Devices with eight, nine, ten, and eleven column addresses
- CAS latency of two or three clock cycles
- 16-bit/32-bit data bus width
- 3.3-V LVCMOS interface

Additionally, the EMIF supports placing the SDRAM in self-refresh and power-down modes. Self-refresh mode allows the SDRAM to be put in a low-power state while still retaining memory contents; since the SDRAM will continue to refresh itself even without clocks from the microcontroller. Power-down mode achieves even lower power, except the microcontroller must periodically wake up and issue refreshes if data retention is required. Note that the EMIF module does not support mobile SDRAM devices.

## 7 Device and Documentation Support

### 7.1 Device Support

#### 7.1.1 Development Support

Texas Instruments (TI) offers an extensive line of development tools for the C28x™ family of MCUs, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development:

##### Software Development Tools

- Code Composer Studio™ Integrated Development Environment (IDE)
  - C/C++ Compiler
  - Code generation tools
  - Assembler/Linker
  - Cycle Accurate Simulator
- Application algorithms
- Sample applications code

##### Hardware Development Tools

- Development and evaluation boards
- JTAG-based emulators - XDS510™ class, XDS560™ emulator, XDS100
- Flash programming tools

For a complete listing of development-support tools for the processor platform, visit the Texas Instruments website at [www.ti.com](http://www.ti.com). For technical questions, visit <http://e2e.ti.com>. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

#### 7.1.2 Device and Development Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320™ MCU devices and support tools. Each TMS320™ MCU commercial family member has one of three prefixes: TMX, TMP, or TMS (for example, **TMS320F28377D**). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (with TMX for devices and TMDX for tools) through fully qualified production devices and tools (with TMS for devices and TMDS for tools).

Device development evolutionary flow:

- |            |  |
|------------|--|
| <b>TMX</b> | Experimental device that is not necessarily representative of the final device's electrical specifications                           |
| <b>TMP</b> | Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification |
| <b>TMS</b> | Fully qualified production device  |

Support tool development evolutionary flow:

- |             |   |
|-------------|---|
| <b>TMDX</b> | Development-support product that has not yet completed Texas Instruments internal qualification testing |
| <b>TMDS</b> | Fully qualified development-support product   |

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

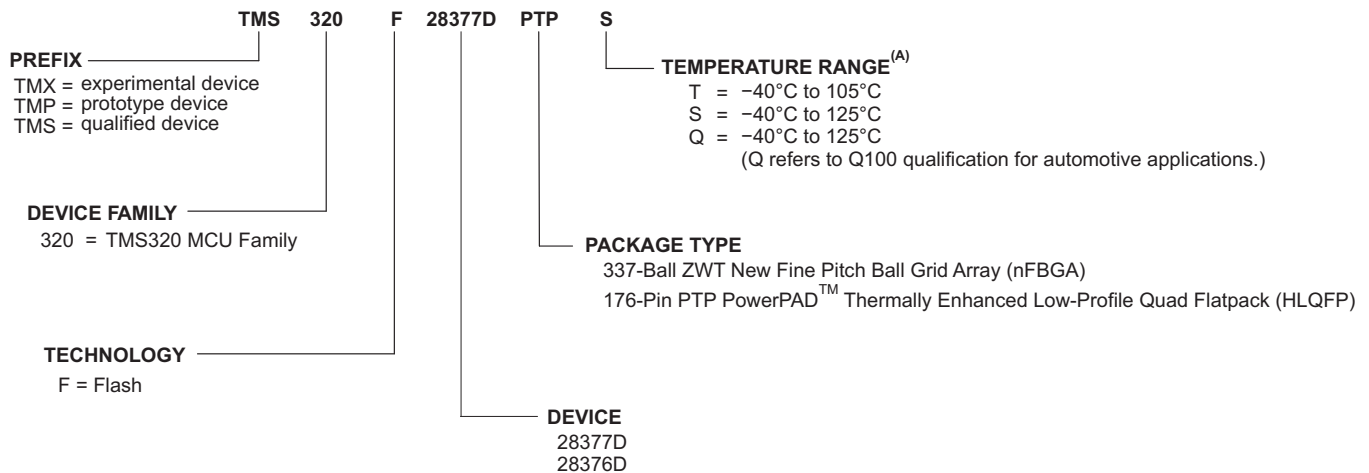
Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PTP) and temperature range (for example, S). [Figure 7-1](#) provides a legend for reading the complete device name for any family member.

For device part numbers and further ordering information, see the TI website ([www.ti.com](http://www.ti.com)) or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the *TMS320F28377D, TMS320F28376D Delfino Microcontrollers Silicon Errata* (literature number [SPRZ412](#)).

ADVANCE INFORMATION



A. The "Q" temperature option is not available on the 28376D device.

**Figure 7-1. Device Nomenclature**

## 7.2 Documentation Support

Extensive documentation supports all of the TMS320™ MCU family generations of devices from product announcement through applications development. The types of documentation available include: data sheets and data manuals, with design specifications; and hardware and software applications.

The following documents can be downloaded from the TI website ([www.ti.com](http://www.ti.com)):

### Data Manual and Errata

[SPRS880](#) **TMS320F28377D, TMS320F28376D Dual-Core Delfino™ Microcontrollers Data Manual** contains the pinout, signal descriptions, as well as electrical and timing specifications for the 2837xD devices.

[SPRZ412](#) **TMS320F28377D, TMS320F28376D Delfino Microcontrollers Silicon Errata** describes known advisories on silicon and provides workarounds.

### Technical Reference Manual

[SPRUHM8](#) **TMS320F2837xD Technical Reference Manual** details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the 2837xD microcontrollers.

### CPU User's Guides

[SPRU430](#) **TMS320C28x CPU and Instruction Set Reference Guide** describes the central processing unit (CPU) and the assembly language instructions of the TMS320C28x fixed-point digital signal processors (DSPs). This Reference Guide also describes emulation features available on these DSPs.

### Peripheral Guides

[SPRU566](#) **TMS320x28xx, 28xxx DSP Peripheral Reference Guide** describes the peripheral reference guides of the 28x digital signal processors (DSPs).

### Tools Guides

[SPRU513](#) **TMS320C28x Assembly Language Tools v5.0.0 User's Guide** describes the assembly language tools (assembler and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the TMS320C28x device.

[SPRU514](#) **TMS320C28x Optimizing C/C++ Compiler v5.0.0 User's Guide** describes the TMS320C28x™ C/C++ compiler. This compiler accepts ANSI standard C/C++ source code and produces TMS320 DSP assembly language source code for the TMS320C28x device.

[SPRU608](#) **TMS320C28x Instruction Set Simulator Technical Overview** describes the simulator, available within the Code Composer Studio for TMS320C2000 IDE, that simulates the instruction set of the C28x™ core.

## 7.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

[TI E2E Community](#) **TI's Engineer-to-Engineer (E2E) Community**. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

[TI Embedded Processors Wiki](#) **Texas Instruments Embedded Processors Wiki**. Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

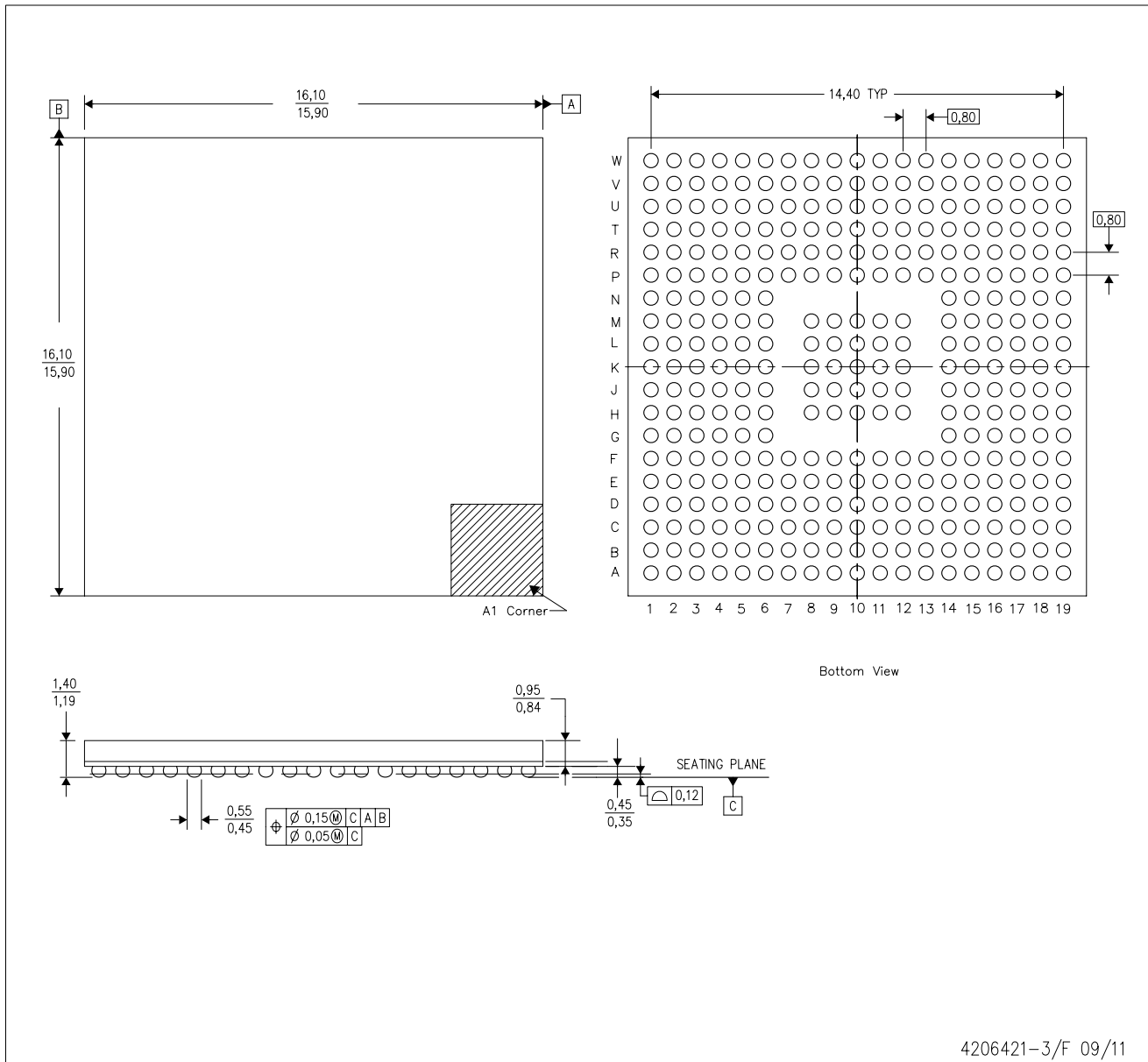
## 8 Mechanical Packaging and Orderable Information

### 8.1 Packaging Information

The following packaging information and addendum reflect the most current data available for the designated devices. This data is subject to change without notice and without revision of this document.

ZWT (S-PBGA-N337)

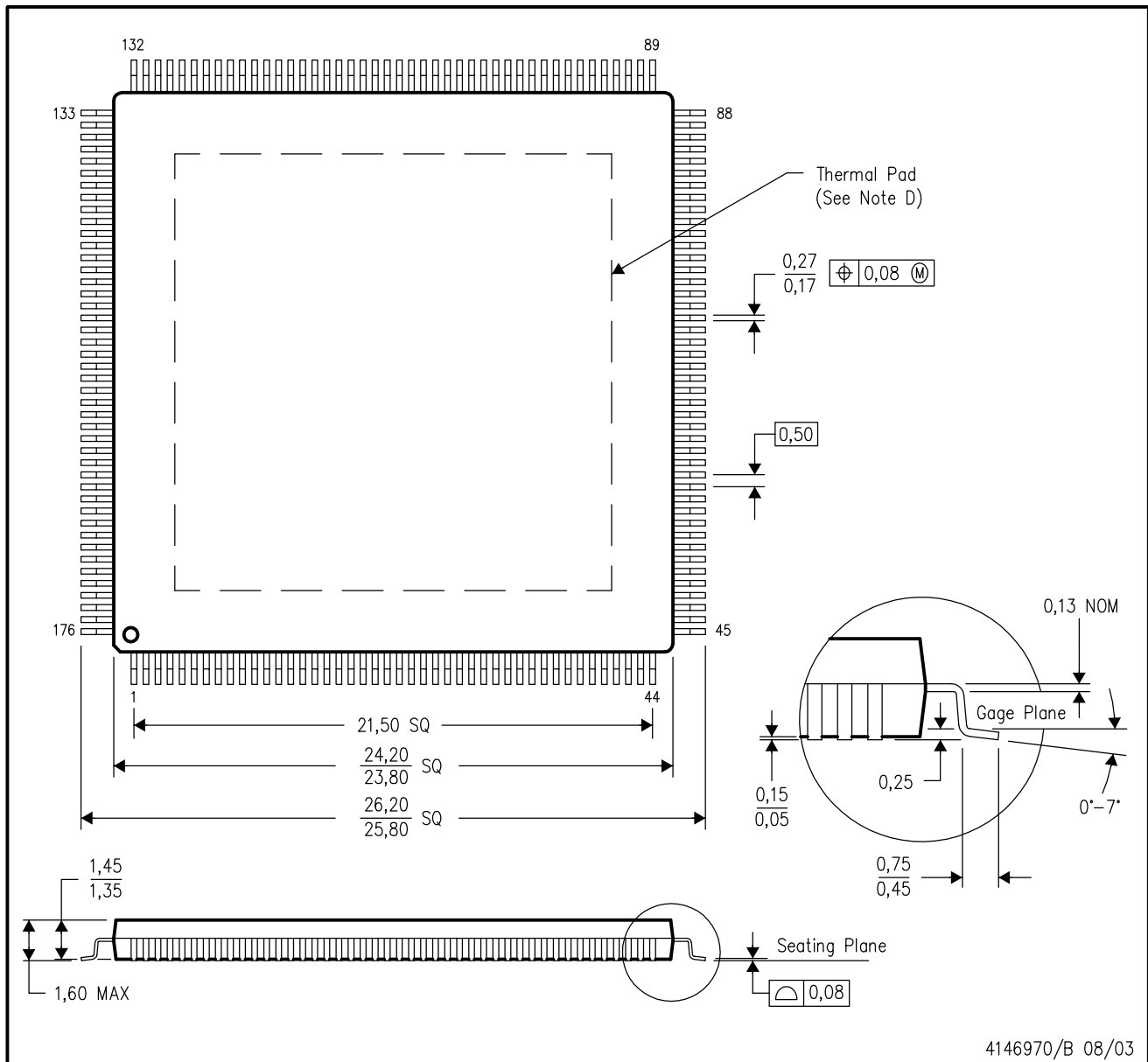
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. This is a Pb-free solder ball design.
  - D. Falls within JEDEC MO-275.

PTP (S-PQFP-G176)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Falls within JEDEC MO-026

PowerPAD is a trademark of Texas Instruments.

PTP (S-PQFP-G176)

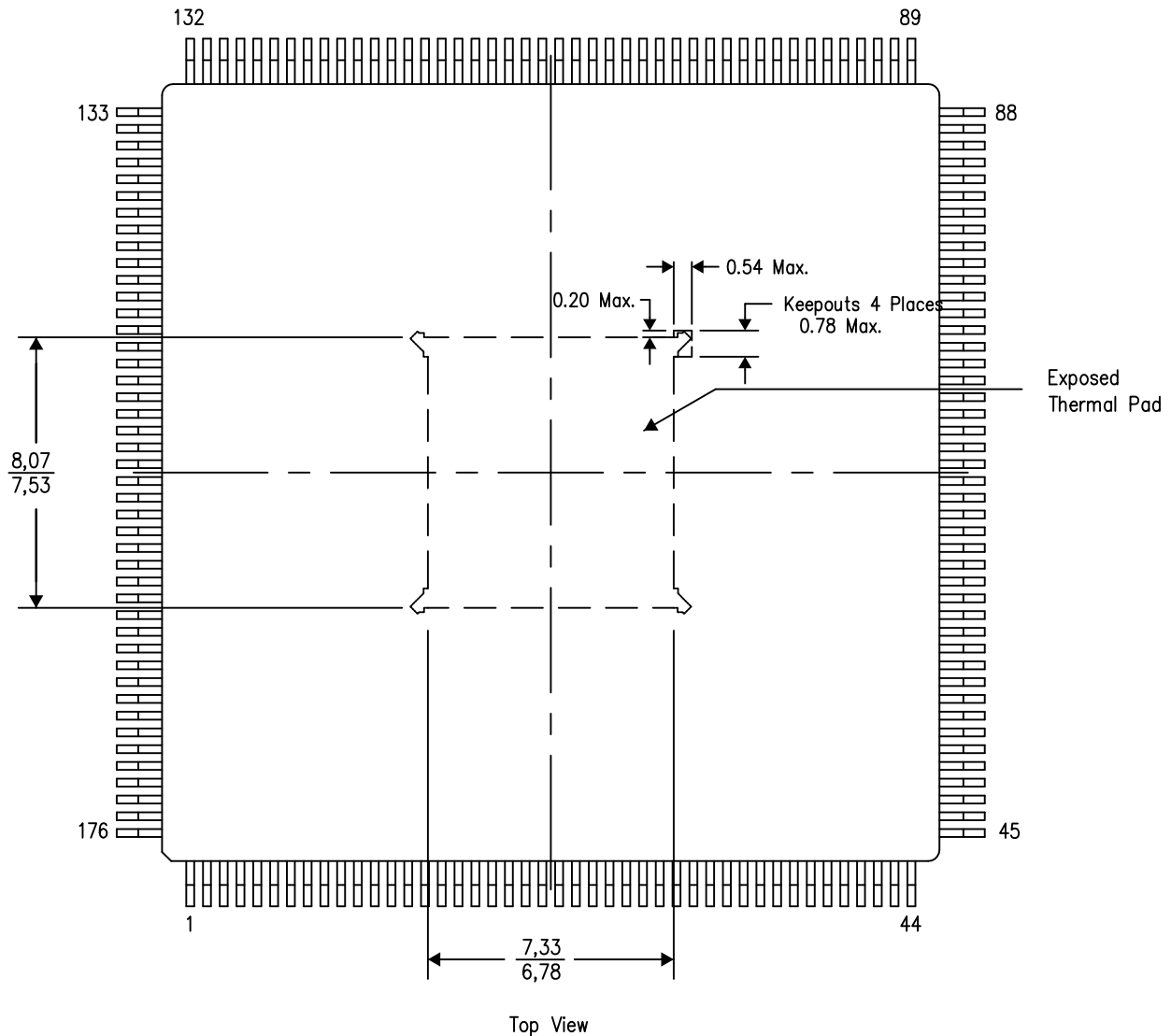
PowerPAD™ PLASTIC QUAD FLATPACK

**THERMAL INFORMATION**

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4209350-8/F 04/13

NOTE: All linear dimensions are in millimeters

NOTE: Keep-out features are identified to prevent board routing interference. These exposed metal features may vary within the identified area or be completely absent on some devices.

PowerPAD is a trademark of Texas Instruments

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMS320F28376DPTPS	PREVIEW	HLQFP	PTP	176	40	TBD	Call TI	Call TI	-40 to 125		
TMS320F28376DPTPT	PREVIEW	HLQFP	PTP	176	40	TBD	Call TI	Call TI	-40 to 105		
TMS320F28376DZWTS	PREVIEW	NFBGA	ZWT	337	90	TBD	Call TI	Call TI	-40 to 125		
TMS320F28376DZWTT	PREVIEW	NFBGA	ZWT	337	90	TBD	Call TI	Call TI	-40 to 105		
TMS320F28377DPTPQ	PREVIEW	HLQFP	PTP	176	40	TBD	Call TI	Call TI	-40 to 125		
TMS320F28377DPTPS	PREVIEW	HLQFP	PTP	176	40	TBD	Call TI	Call TI	-40 to 125		
TMS320F28377DPTPT	PREVIEW	HLQFP	PTP	176	40	TBD	Call TI	Call TI	-40 to 105		
TMS320F28377DZWTQ	PREVIEW	NFBGA	ZWT	337	90	TBD	Call TI	Call TI	-40 to 125		
TMS320F28377DZWTS	PREVIEW	NFBGA	ZWT	337	90	TBD	Call TI	Call TI	-40 to 105		
TMS320F28377DZWTT	PREVIEW	NFBGA	ZWT	337	90	TBD	Call TI	Call TI	-40 to 105		
TMX320F28377DPTPT	ACTIVE	HLQFP	PTP	176	1	TBD	Call TI	Call TI	-40 to 105		Samples
TMX320F28377DZWTT	ACTIVE	NFBGA	ZWT	337	1	TBD	Call TI	Call TI	-40 to 105		Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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