- **Highest-Performance Floating-Point Digital Signal Processors (DSPs): C6713/C6713B**
  - **Eight 32-Bit Instructions/Cycle**
  - **32/64-Bit Data Word**
  - **300-, 225-, 200-MHz (GDP), and 225-, 200-, 167-MHz (PYP) Clock Rates**
  - **3.3-, 4.4-, 5-, 6-Instruction Cycle Times**
  - **2400/1800, 1800/1350, 1600 /1200, and 1336/1000 MIPS /MFLOPS**
  - **Rich Peripheral Set, Optimized for Audio**
  - **Highly Optimized C/C++ Compiler**
  - **Extended Temperature Devices Available**
- **Advanced Very Long Instruction Word (VLIW) TMS320C67x™ DSP Core**
  - **Eight Independent Functional Units:**
    - **Two ALUs (Fixed-Point)**
    - **Four ALUs (Floating- and Fixed-Point)**
    - **Two Multipliers (Floating- and Fixed-Point)**
  - **Load-Store Architecture With 32 32-Bit General-Purpose Registers**
  - **Instruction Packing Reduces Code Size**
  - **All Instructions Conditional**
- **Instruction Set Features**
  - **Native Instructions for IEEE 754**
    - **Single- and Double-Precision**
  - **Byte-Addressable (8-, 16-, 32-Bit Data)**
  - **8-Bit Overflow Protection**
  - **Saturation; Bit-Field Extract, Set, Clear; Bit-Counting; Normalization**
- **L1/L2 Memory Architecture**
  - **4K-Byte L1P Program Cache (Direct-Mapped)**
  - **4K-Byte L1D Data Cache (2-Way)**
  - **256K-Byte L2 Memory Total: 64K-Byte L2 Unified Cache/Mapped RAM, and 192K-Byte Additional L2 Mapped RAM**
- **Device Configuration**
  - **Boot Mode: HPI, 8-, 16-, 32-Bit ROM Boot**
  - **Endianness: Little Endian, Big Endian**
- **32-Bit External Memory Interface (EMIF)**
  - **Glueless Interface to SRAM, EPROM, Flash, SBSRAM, and SDRAM**
  - **512M-Byte Total Addressable External Memory Space**
- **Enhanced Direct-Memory-Access (EDMA) Controller (16 Independent Channels)**
- **16-Bit Host-Port Interface (HPI)**
- **Two McASPs**
  - **Two Independent Clock Zones Each (1 TX and 1 RX)**
  - **Eight Serial Data Pins Per Port: Individually Assignable to any of the Clock Zones**
  - **Each Clock Zone Includes:**
    - **Programmable Clock Generator**
    - **Programmable Frame Sync Generator**
    - **TDM Streams From 2-32 Time Slots**
    - **Support for Slot Size: 8, 12, 16, 20, 24, 28, 32 Bits**
    - **Data Formatter for Bit Manipulation**
  - **Wide Variety of I2S and Similar Bit Stream Formats**
  - **Integrated Digital Audio Interface Transmitter (DIT) Supports:**
    - **S/PDIF, IEC60958-1, AES-3, CP-430 Formats**
    - **Up to 16 transmit pins**
    - **Enhanced Channel Status/User Data**
  - **Extensive Error Checking and Recovery**
- **Two Inter-Integrated Circuit Bus (I^2C Bus™) Multi-Master and Slave Interfaces**
- **Two Multichannel Buffered Serial Ports:**
  - **Serial-Peripheral-Interface (SPI)**
  - **High-Speed TDM Interface**
  - **AC97 Interface**
- **Two 32-Bit General-Purpose Timers**
- **Dedicated GPIO Module With 16 pins (External Interrupt Capable)**
- **Flexible Phase-Locked-Loop (PLL) Based Clock Generator Module**
- **IEEE-1149.1 (JTAG†) Boundary-Scan-Compatible**
- **208-Pin PowerPAD™ Plastic (Low-Profile) Quad Flatpack (PYP)**
- **272-BGA Packages (GDP and ZDP)**
- **0.13-μm/6-Level Copper Metal Process**
  - **CMOS Technology**
- **3.3-V I/Os, 1.2†-V Internal (GDP & PYP)**
- **3.3-V I/Os, 1.4-V Internal (GDP) [300 MHz]**

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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I^2C Bus is a trademark of Philips Electronics N.V. Corporation
All trademarks are the property of their respective owners.
† IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.
‡ These values are compatible with existing 1.26V designs.

Table of Contents

REVISION HISTORY

This data sheet revision history highlights the technical changes made to the SPRS186I device-specific data sheet to make it an SPRS186J revision.

Scope: Applicable updates to the C67x device family, specifically relating to the C6713 and C6713B devices, have been incorporated. All devices are now at the Production Data (PD) stage of development.

Added/incorporated the device-specific information for the *new* C6713**B** commercial and extended temperature devices (13**B**PYP-225 and 13**B**PYP**A**−200 MHz).

PAGE(S) NO.	ADDITIONS/CHANGES/DELETIONS
	Global: Added “ZDP” mechanical packaging information Added PYP −225 device to all Electrical Characteristics and Timings tables for the C6713B device *only* Added PYPA −200 device to all Electrical Characteristics and Timings tables for the C6713B device *only*
1	Features section: Added **225** for PYP to “300-, 200-MHz (GDP), and 200-, 167-MHz (PYP) Clock Rates” bullet Added “Extended Temperature Devices Available” sub-bullet to “Highest-Performance Floating-Point Digital Signal Processors“ bullet Added “and ZDP” in the “272-Pin BGA ...” bullet
12	Table 2, Characteristics of the C6713 and C6713B Processors: Updated Frequency for PYP to include 225 Updated Cycle Time for PYP to include C6713BPYP−225 *and* C6713BPYPA−200
33	Device Configurations section: Device Configurations at Device Reset: Added paragraphs
34	Device Configurations Pins at Device Reset (HD[4:3], HD8, HD12 [13B only], and CLKMODE0): Updated the Functional Description for the HD12 Configuration Pin.
48	Debugging Considerations section: Added “For a list of routed out, 3−stated, or not-driven pins recommended for *external* pullup/pulldown resistors, and *internal* pullup/pulldown resistors for all device pins, etc., see the Terminal Functions table” sentence to the “Internal pullup/pulldown resistors also exist on the ...” paragraph.
49, 51−52	Terminal Functions table: Added footnote for clarity Updated/changed the HD12 Functional Description Deleted “These IPD/IPU signal pins feature a 30-kΩ IPD or IPU resistor” from “For C6713, IPD = Internal Pulldown ...” and “For C6713/13B IPD = Internal Pulldown ...” footnote Added *new* “For **C6713B**, to ensure a proper logic during reset level when these pins are ***both*** routed out ***and*** 3-stated or not driven, it is recommended that an external 10-kΩ pullup/pulldown resistor be included to sustain the IPU/IPD, respectively” **footnote**
60, 61	Moved footnote for the CV_{DD} into pin description
66	Device Support, Device and Development-Support Tool Nomenclature section: Deleted the “TMS320C6713 and C6713B Device Part Numbers (P/Ns) and Ordering Information” table and associated paragraph Updated the “To designate the stages in the product development cycle...” paragraph Updated the “TMX and TMP devices...” paragraph Updated the “TI device nomenclature also includes ...” paragraph Added “The ZDP package, like the GDP package, is ...” paragraph

PAGE(S) NO.	ADDITIONS/CHANGES/DELETIONS
67	Figure 12. TMS320C6000 DSP Device Nomenclature (Including the TMS320C6713 and TMS320C6713B Devices): Added “ZDP” package and associated footnote Added the “For actual device part numbers (P/Ns) and ordering information, ...” footnote
96	IEEE 1149.1 JTAG Compatibility Statement section: Updated/added paragraphs for clarity
99	Reset section: Added *new* section
100	Absolute Maximum Ratings Over Operating Case Temperature Range section: Updated Operating Case Temperature Ranges, T_C: A version (extended temperature) device names ***from*** [**13**GDPA−200 and **13**PYPA−167 ***to*** [GDPA−200 and PYPA−167] Added **13BPYPA−200** device to Operating case temperature ranges, T_C: A version (extended temperature)
101	Recommended Operating Conditions section: T_C Operating Case Temperature: Updated A version device names and added **13BPYPA−200** device
102	Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Case Temperature: I_{DD2V} Core Supply Current: Added **13BPYPA** to PYP Test Conditions
106	Input and Output Clocks: Time Requirements for CLKIN for C6713BGDP-300: Added column for **“**13BPYP−225**”** and updated title for table
106	Input and Output Clocks section: Timing Requirements for CLKIN for C6713/13BPYP-200 and C6713/13BGDP-225 section: Updated the No. 1 $t_{c(CLKIN)}$ Bypass Mode for the PYP−200 MIN value *from* **5** ns to **6.7** ns Updated the No. 1 $t_{c(CLKIN)}$ Bypass Mode for the GDP−225 MIN value *from* **4.4** ns to **6.7** ns Timing Requirements for CLKIN for C6713BPYP-225 and C6713BGDP-300 section: Added columns for **13BPYP−225** device Updated the No. 1 $t_{c(CLKIN)}$ PLL Mode for the GDP −300 MIN value *from* **3.3** ns to **4** ns Updated the No. 1 $t_{c(CLKIN}$ Bypass Mode for the GDP −300 MIN value *from* **3.3** ns to **6.7** ns Timing Requirements for CLKIN for C6713PYPA-167 and C6713GDPA-200 section: Updated the No. 1 $t_{c(CLKIN}$ Bypass Mode for the PYPA−167 MIN value *from* **6** ns to **6.7** ns Updated the No. 1 $t_{c(CLKIN}$ Bypass Mode for the GDPA−200 MIN value *from* **5** ns to **6.7** ns Changed column title ***from*** “timing requirements for CLKIN for **6713PYPA**-167, **6713GDPA**-200“ ***to*** “timing requirements for CLKIN for **PYPA**-167, **GDPA**-200“ Updated table title GDPA−200 to include the **13BPYPA−200** device Updated column title GDPA−200 to include **13BPYPA−200** device
107	Input and Output Clocks section: Switching Characteristics Over Recommended Operating Conditions for CLKOUT3 [C6713B only] table: Changed the “C3 = CLKOUT3 period ...” footnote ***from*** “... RATIO field in the PLLDIV3 register” ***to*** “... OSCDIV1 register. For more details, see PLL and PLL controller.”
150−152	Mechanical Data for C6713/13B section: Deleted the “GFN (S-PBGA-N256) [C6713 only]” and “GDP (S−PBGA−N272) [C6713B only]” mechanical data package diagrams; now an automated merge process. Added “Thermal Resistance Characteristics (S-PBGA package) for ZDP [C671B] only” table Added new “Packaging Information” title and lead-in sentence

DEVICE CONFIGURATIONS (CONTINUED)

Table 23. C6713/13B Device Multiplexed/Shared Pins

MULTIPLEXED PINS			DEFAULT FUNCTION	DEFAULT SETTING	DESCRIPTION
NAME	PYP	GDP			
CLKOUT2/GP[2]	82	Y12	CLKOUT2	GP2EN = 0 (GPEN register bit) GP[2] function disabled, CLKOUT2 enabled	When the CLKOUT2 pin is enabled, the CLK2EN bit in the EMIF global control register (GBLCTL) controls the CLKOUT2 pin. CLK2EN = 0: CLKOUT2 held high CLK2EN = 1: CLKOUT2 enabled to clock [default] To use these software-configurable GPIO pins, the GPxEN bits in the GP Enable Register and the GPxDIR bits in the GP Direction Register must be properly configured. GPxEN = 1: GP[x] pin enabled GPxDIR = 0: GP[x] pin is an input GPxDIR = 1: GP[x] pin is an output To use AMUTEIN0/1 pin function, the GP[5]/GP[4] pins must be configured as an input, the INEN bit set to 1, and the polarity through the INPOL bit selected in the associated McASP AMUTE register.
GP[5](EXT_INT5)/AMUTEIN0 GP[4](EXT_INT4)/AMUTEIN1	6 1	C1 C2	GP[5](EXT_INT5) GP[4](EXT_INT4)	No Function GPxDIR = 0 (input) GP5EN = 0 (disabled) GP4EN = 0 (disabled) [(GPEN register bits) GP[x] function disabled]	
CLKS0/AHCLKR0	28	K3	McBSP0 pin function	MCBSP0DIS = 0 (DEVCFG register bit) McASP0 pins disabled, McBSP0 pins enabled	By default, McBSP0 peripheral pins are enabled upon reset (McASP0 pins are disabled). To enable the McASP0 peripheral pins, the MCBSP0DIS bit in the DEVCFG register must be set to 1 (disabling the McBSP0 peripheral pins).
DR0/AXR0[0]	27	J1			
DX0/AXR0[1]	20	H2			
FSR0/AFSR0	24	J3			
FSX0/AFSX0	21	H1			
CLKR0/ACLKR0	19	H3			
CLKX0/ACLKX0	16	G3			
CLKS1/SCL1	8	E1	McBSP1 pin function	MCBSP1DIS = 0 (DEVCFG register bit) I2C1 and McASP0 pins disabled, McBSP1 pins enabled	By default, McBSP1 peripheral pins are enabled upon reset (I2C1 and McASP0 pins are disabled). To enable the I2C1 and McASP0 peripheral pins, the MCBSP1DIS bit in the DEVCFG register must be set to 1 (disabling the McBSP1 peripheral pins).
DR1/SDA1	37	M2			
DX1/AXR0[5]	32	L2			
FSR1/AXR0[7]	38	M3			
CLKR1/AXR0[6]	36	M1			
CLKX1/AMUTE0	33	L3			

DEVICE CONFIGURATIONS (CONTINUED)

Table 23. C6713/13B Device Multiplexed/Shared Pins (Continued)

MULTIPLEXED PINS			DEFAULT FUNCTION	DEFAULT SETTING	DESCRIPTION
NAME	PYP	GDP			
$\overline{\text{HINT}}$/GP[1]	135	J20	HPI pin function	HPI_EN (HD14 pin) = 1 (HPI enabled) McASP1 pins and eleven GPIO pins are disabled.	By default, the HPI peripheral pins are enabled at reset. McASP1 peripheral pins and eleven GPIO pins are disabled. To enable the McASP1 peripheral pins and the eleven GPIO pins, an external pulldown resistor must be provided on the HD14 pin setting HPI_EN = 0 at reset. To use these software-configurable GPIO pins, the GPxEN bits in the GP Enable Register and the GPxDIR bits in the GP Direction Register must be properly configured. GPxEN = 1: GP[x] pin enabled GPxDIR = 0: GP[x] pin is an input GPxDIR = 1: GP[x] pin is an output McASP1 pin direction is controlled by the PDIR[x] bits in the McASP1PDIR register.
HD15/GP[15]	174	B14			
HD14/GP[14]	173	C14			
HD13/GP[13]	172	A15			
HD12/GP[12]	168	C15			
HD11/GP[11]	167	A16			
HD10/GP[10]	166	B16			
HD9/GP[9]	165	C16			
HD8/GP[8]	160	B17			
HD7/GP[3]	164	A18			
HD4/GP[0]	156	C19			
HD1/AXR1[7]	152	D20			
HD0/AXR1[4]	147	E20			
HCNTL1/AXR1[1]	144	G19			
HCNTL0/AXR1[3]	146	G18			
HR/$\overline{\text{W}}$/AXR1[0]	143	G20			
$\overline{\text{HDS1}}$/AXR1[6]	151	E19			
$\overline{\text{HDS2}}$/AXR1[5]	150	F18			
$\overline{\text{HCS}}$/AXR1[2]	145	F20			
HD6/AHCLKR1	161	C17			
HD5/AHCLKX1	159	B18			
HD3/AMUTE1	154	C20			
HD2/AFSX1	155	D18			
HHWIL/AFSR1	139	H20			
$\overline{\text{HRDY}}$/ACLKR1	140	H19			
$\overline{\text{HAS}}$/ACLKX1	153	E18			
TINP0/AXR0[3]	17	G2	Timer 0 input function	McASP0PDIR = 0 (input) [specifically AXR0[3] bit]	By default, the Timer 0 input pin is enabled (and a shared input until the McASP0 peripheral forces an output). McASP0PDIR = 0 input, = 1 output
TOUT0/AXR0[2]	18	G1	Timer 0 output function	TOUT0SEL = 0 (DEVCFG register bit) [TOUT0 pin enabled and McASP0 AXR0[2] pin disabled]	By default, the Timer 0 output pin is enabled. To enable the McASP0 AXR0[2] pin, the TOUT0SEL bit in the DEVCFG register must be set to 1 (disabling the Timer 0 peripheral output pin function). The AXR2 bit in the McASP0PDIR register controls the direction (input/output) of the AXR0[2] pin McASP0PDIR = 0 input, = 1 output

development support

TI offers an extensive line of development tools for the TMS320C6000™ DSP platform, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development of C6000™ DSP-based applications:

Software Development Tools:
Code Composer Studio™ Integrated Development Environment (IDE): including Editor
C/C++/Assembly Code Generation, and Debug plus additional development tools
Scalable, Real-Time Foundation Software (DSP/BIOS™), which provides the basic run-time target software needed to support any DSP application.

Hardware Development Tools:
Extended Development System (XDS™) Emulator (supports C6000™ DSP multiprocessor system debug)
EVM (Evaluation Module)

For a complete listing of development-support tools for the TMS320C6000™ DSP platform, visit the Texas Instruments web site on the Worldwide Web at http://www.ti.com uniform resource locator (URL). For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

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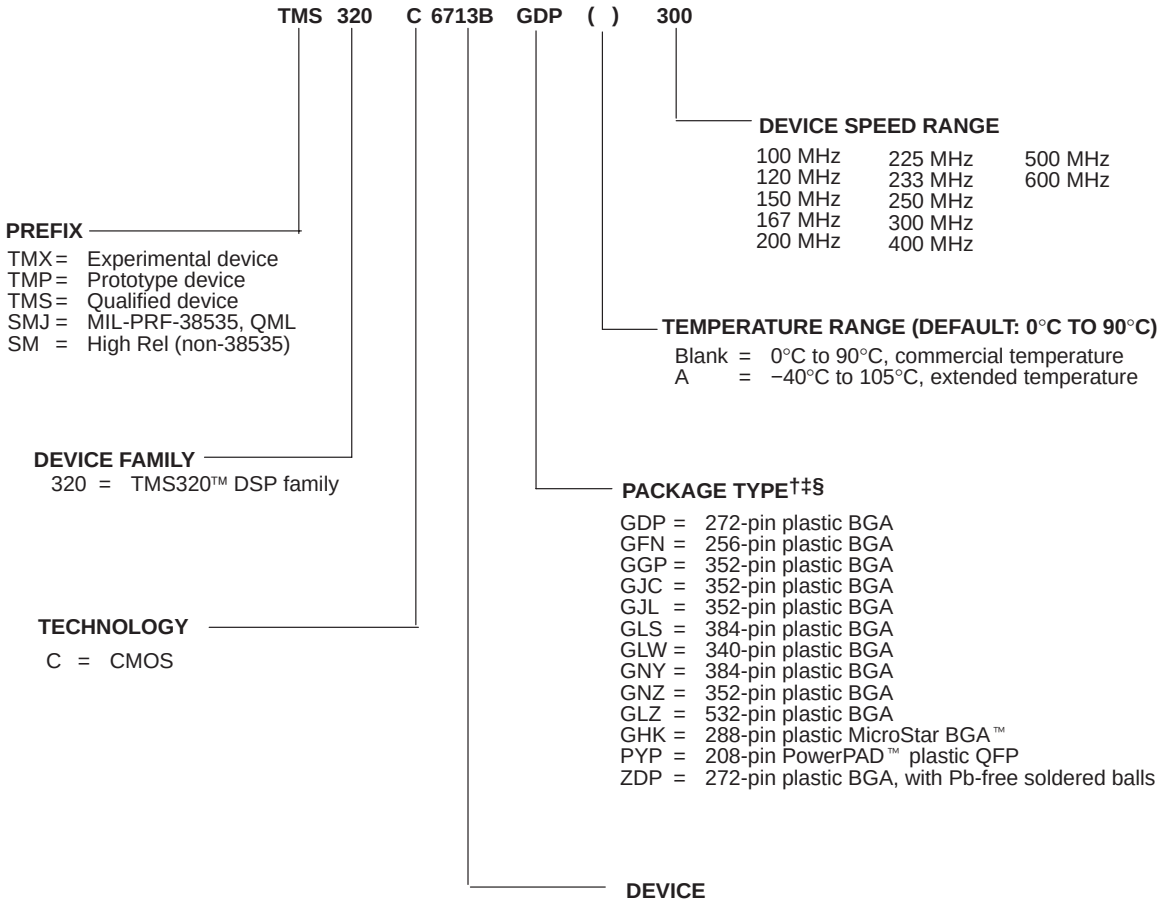
device and development-support tool nomenclature (continued)



† BGA = Ball Grid Array
QFP = Quad Flatpack

‡ The ZDP mechanical package designator represents the version of the GDP with Pb−Free soldered balls.

§ For actual device part numbers (P/Ns) and ordering information, see the Mechanical Data section of this document or the TI website (www.ti.com).

Figure 12. TMS320C6000™ DSP Device Nomenclature (Including the TMS320C6713 and C6713B Devices)

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documentation support

Extensive documentation supports all TMS320™ DSP family generations of devices from product announcement through applications development. The types of documentation available include: data sheets, such as this document, with design specifications; complete user's reference guides for all devices and tools; technical briefs; development-support tools; on-line help; and hardware and software applications. The following is a brief, descriptive list of support documentation specific to the C6000™ DSP devices:

The *TMS320C6000 CPU and Instruction Set Reference Guide* (literature number SPRU189) describes the C6000™ CPU (DSP core) architecture, instruction set, pipeline, and associated interrupts.

The *TMS320C6000 DSP Peripherals Overview Reference Guide* [hereafter referred to as the C6000 PRG Overview] (literature number SPRU190) provides an overview and briefly describes the functionality of the peripherals available on the C6000™ DSP platform of devices. This document also includes a table listing the peripherals available on the C6000 devices along with literature numbers and hyperlinks to the associated peripheral documents. These C6713/13B peripherals are similar to the peripherals on the TMS320C6711 and TMS320C64x devices; therefore, see the TMS320C6711 (C6711 or C67x) peripheral information, and in some cases, where indicated, see the TMS320C6711 (C6711 or C671x) peripheral information and in some cases, where indicated, see the C64x information in the C6000 PRG Overview (literature number SPRU190).

The *TMS320DA6000 DSP Multichannel Audio Serial Port (McASP) Reference Guide* (literature number SPRU041) describes the functionality of the McASP peripherals available on the C6713/13B device.

TMS320C6000 DSP Software-Programmable Phase-Locked Loop (PLL) Controller Reference Guide (literature number SPRU233) describes the functionality of the PLL peripheral available on the C6713/13B device.

TMS320C6000 DSP Inter-Integrated Circuit (I2C) Module Reference Guide (literature number SPRU175) describes the functionality of the I2C peripherals available on the C6713/13B device.

The *PowerPAD Thermally Enhanced Package Technical Brief* (literature number SLMA002) focuses on the specifics of integrating a PowerPAD package into the printed circuit board design to make optimum use of the thermal efficiencies designed into the PowerPAD package.

The *TMS320C6000 Technical Brief* (literature number SPRU197) gives an introduction to the C62x™/C67x™ devices, associated development tools, and third-party support.

The *Migrating from TMS320C6211(B)/C6711(B) to TMS320C6713* application report (literature number SPRA851) indicates the differences and describes the issues of interest related to the migration from the Texas Instruments TMS320C6211(B)/C6711(B), GFN package, to the TMS320C6713, GDP package.

The *TMS320C6713, TMS320C6713B Digital Signal Processors Silicon Errata* (literature number SPRZ191) describes the known exceptions to the functional specifications for particular silicon revisions of the TMS320C6713 and TMS320C6713B devices.

The *TMS320C6713/12C/11C Power Consumption Summary* application report (literature number SPRA889) discusses the power consumption for user applications with the TMS320C6713/13B, TMS320C6712C/12D, and TMS320C6711C/11D DSP devices.

The *Using IBIS Models for Timing Analysis* application report (literature number SPRA839) describes how to properly use IBIS models to attain accurate timing analysis for a given system.

The tools support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE). For a complete listing of C6000™ DSP latest documentation, visit the Texas Instruments web site on the Worldwide Web at http://www.ti.com uniform resource locator (URL).

See the Worldwide Web URL for the application report *How To Begin Development Today With the TMS320C6713 Floating-Point DSP* (literature number SPRA809), which describes in more detail the similarities/differences between the C6713 and C6711 C6000™ DSP devices.

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recommended operating conditions†

			MIN	NOM	MAX	UNIT
CV_{DD}	Supply voltage, Core referenced to V_{SS}	PYP packages only	1.14	1.20	1.32	V
		GDP packages for C6713/C6713B only	1.14‡	1.20‡	1.32	V
		GDP packages for C6713B−300 only	1.33	1.4	1.47	V
DV_{DD}	Supply voltage, I/O referenced to V_{SS}		3.13	3.3	3.47	V
V_{IH}	High-level input voltage	All signals except CLKS1/SCL1, DR1/SDA1, SCL0, SDA0, and $\overline{\text{RESET}}$	2			V
		CLKS1/SCL1, DR1/SDA1, SCL0, SDA0, and $\overline{\text{RESET}}$	2			V
V_{IL}	Low-level input voltage	All signals except CLKS1/SCL1, DR1/SDA1, SCL0, SDA0, and $\overline{\text{RESET}}$			0.8	V
		CLKS1/SCL1, DR1/SDA1, SCL0, SDA0, and $\overline{\text{RESET}}$			0.3*DV_{DD}	V
I_{OH}	High-level output current **(C6713)**§	All signals except ECLKOUT, CLKOUT2, **CLKOUT3**, CLKS1/SCL1, DR1/SDA1, SCL0, and SDA0			−8	mA
		ECLKOUT, CLKOUT2, and **CLKOUT3**			−16	mA
	High-level output current (C6713**B**)§	All signals except ECLKOUT, CLKOUT2, CLKS1/SCL1, DR1/SDA1, SCL0, and SDA0			−8	mA
		ECLKOUT and CLKOUT2			−16	mA
I_{OL}	Low-level output current **(C6713)**§	All signals except ECLKOUT, CLKOUT2, **CLKOUT3**, CLKS1/SCL1, DR1/SDA1, SCL0, and SDA0			8	mA
		ECLKOUT, CLKOUT2, and **CLKOUT3**			16	mA
		CLKS1/SCL1, DR1/SDA1, SCL0, and SDA0			3	mA
	Low-level output current (C6713**B**)§	All signals except ECLKOUT, CLKOUT2, CLKS1/SCL1, DR1/SDA1, SCL0, and SDA0			8	mA
		ECLKOUT and CLKOUT2			16	mA
		CLKS1/SCL1, DR1/SDA1, SCL0, and SDA0			3	mA
T_C	Operating case temperature	Default	0		90	°C
		A version (GDPA-200, PYPA-167 and 13BPYPA−200)	–40		105	°C

† The core supply should be powered up prior to (and powered down after), the I/O supply. Systems should be designed to ensure that neither supply is powered up for an extended period of time if the other supply is below the proper operating voltage.
‡ These values are compatible with existing 1.26V designs.
§ Refers to DC (or steady state) currents only, actual switching currents are higher. For more details, see the device-specific IBIS models.

electrical characteristics over recommended ranges of supply voltage and operating case temperature† (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	All signals except SCL1, SDA1, SCL0, and SDA0	I_{OH} =MAX	2.4			V
V_{OL}	Low-level output voltage	All signals except SCL1, SDA1, SCL0, and SDA0	I_{OL} = MAX			0.4	V
		SCL1, SDA1, SCL0, and SDA0	I_{OL} = MAX			0.4	V
I_I	Input current	All signals except SCL1, SDA1, SCL0, and SDA0	$V_I = V_{SS}$ to DV_{DD}			±170	uA
		SCL1, SDA1, SCL0, and SDA0				±10	uA
I_{OZ}	Off-state output current	All signals except SCL1, SDA1, SCL0, and SDA0	$V_O = DV_{DD}$ or 0 V			±170	uA
		SCL1, SDA1, SCL0, and SDA0				±10	uA
I_{DD2V}	Core supply current‡		GDP, CV_{DD} = 1.4 V, CPU clock = 300 MHz		945		mA
			GDP, CV_{DD} = 1.26 V, CPU clock = 225 MHz		625		mA
			13GDPA, CV_{DD} = 1.26 V, CPU clock = 200 MHz		560		mA
			PYP, 13BPYPA CV_{DD} = 1.2 V CPU clock = 200 MHz		565		mA
			13PYPA, CV_{DD} = 1.2 V, CPU clock = 167 MHz		480		mA
I_{DD3V}	I/O supply current‡		C6713/13B, DV_{DD} = 3.3 V, EMIF speed = 100 MHz		75		mA
C_i	Input capacitance					7	pF
C_o	Output capacitance					7	pF

† For test conditions shown as MIN, MAX, or NOM, use the appropriate value specified in the recommended operating conditions table.

‡ Measured with average activity (50% high/50% low power) at 25°C case temperature and 100-MHz EMIF. This model represents a device performing high-DSP-activity operations 50% of the time, and the remainder performing low-DSP-activity operations. The high/low-DSP-activity models are defined as follows:

High-DSP-Activity Model:

CPU: 8 instructions/cycle with 2 LDDW instructions [L1 Data Memory: 128 bits/cycle via LDDW instructions; L1 Program Memory: 256 bits/cycle; L2/EMIF EDMA: 50% writes, 50% reads to/from SDRAM (50% bit-switching)]

McBSP: 2 channels at E1 rate

Timers: 2 timers at maximum rate

Low-DSP-Activity Model:

CPU: 2 instructions/cycle with 1 LDH instruction [L1 Data Memory: 16 bits/cycle; L1 Program Memory: 256 bits per 4 cycles; L2/EMIF EDMA: None]

McBSP: 2 channels at E1 rate

Timers: 2 timers at maximum rate

The actual current draw is highly application-dependent. For more details on core and I/O activity, refer to the *TMS320C6713/12C/11C Power Consumption Summary* application report (literature number SPRA889).

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

timing requirements for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 0†‡ (see Figure 60)

NO.			PYPA−167 13BPYPA−200 PYP−200, −225 GDPA−200 GDP−225 GDP−300				UNIT
			MASTER		SLAVE		
			MIN	MAX	MIN	MAX	
4	$t_{su(DRV-CKXH)}$	Setup time, DR valid before CLKX high	12		2 − 6P		ns
5	$t_{h(CKXH-DRV)}$	Hold time, DR valid after CLKX high	4		5 + 12P		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 300 MHz, use P = 3.3 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

switching characteristics over recommended operating conditions for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 0†‡ (see Figure 60)

NO.	PARAMETER		13PYPA−167 13PYP−200 13GDPA−200 13GDP−225				13BPYPA−167 13BPYPA−200 13BPYP−200 13BPYP−225 13BGDPA−200 13BGDP−225 13BGDP−300				UNIT
			MASTER§		SLAVE		MASTER§		SLAVE		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{h(CKXL-FXL)}$	Hold time, FSX low after CLKX low¶	L − 2	L + 3			L − 2	L + 3			ns
2	$t_{d(FXL-CKXH)}$	Delay time, FSX low to CLKX high#	T − 2	T + 3			T − 2	T + 3			ns
3	$t_{d(CKXL-DXV)}$	Delay time, CLKX low to DX valid	−3	4	6P + 2	10P + 17	−3	4	6P + 2	10P + 17	ns
6	$t_{dis(CKXL-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX low	−4	4	6P + 1.5	10P + 17	−2	4	6P + 3	10P + 17	ns
7	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	H − 2	H + 4	4P + 2	8P + 17	H − 2	H + 6.5	4P + 2	8P + 17	ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 300 MHz, use P = 3.3 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
§ S = Sample rate generator input clock = 2P if CLKSM = 1 (P = 1/CPU clock frequency)
= Sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
T = CLKX period = (1 + CLKGDV) * S
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
¶ FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

MULTICHANNEL BUFFERED SERIAL PORT TIMING (CONTINUED)

timing requirements for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 1†‡ (see Figure 62)

NO.			PYPA−167 13BPYPA−200 PYP−200, −225 GDPA−200 GDP−225 GDP−300				UNIT
			MASTER		SLAVE		
			MIN	MAX	MIN	MAX	
4	$t_{su(DRV-CKXH)}$	Setup time, DR valid before CLKX high	12		2 − 6P		ns
5	$t_{h(CKXH-DRV)}$	Hold time, DR valid after CLKX high	4		5 + 12P		ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 300 MHz, use P = 3.3 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

switching characteristics over recommended operating conditions for McBSP as SPI master or slave: CLKSTP = 11b, CLKXP = 1†‡ (see Figure 62)

NO.	PARAMETER		13PYPA−167 13PYP−200 13GDPA−200 13GDP−225				13BPYPA−167 13BPYPA−200 13BPYP−200 13BPYP−225 13BGDPA−200 13BGDP−225 13BGDP−300				UNIT
			MASTER§		SLAVE		MASTER§		SLAVE		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{h(CKXH-FXL)}$	Hold time, FSX low after CLKX high¶	H − 2	H + 3			H − 2	H + 3			ns
2	$t_{d(FXL-CKXL)}$	Delay time, FSX low to CLKX low#	T − 2	T + 3			T − 2	T + 3			ns
3	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid	−3	4	6P + 2	10P + 17	−3	4	6P + 2	10P + 17	ns
6	$t_{dis(CKXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high	−3.6	4	6P + 1.5	10P + 17	−2	4	6P + 3	10P + 17	ns
7	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	L − 2	L + 4	4P + 2	8P + 17	L − 2	L + 6.5	4P + 2	8P + 17	ns

† P = 1/CPU clock frequency in ns. For example, when running parts at 300 MHz, use P = 3.3 ns.
‡ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.
§ S = Sample rate generator input clock = 2P if CLKSM = 1 (P = 1/CPU clock frequency)
= Sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
T = CLKX period = (1 + CLKGDV) * S
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
¶ FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP
# FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

MECHANICAL DATA FOR C6713/13B

The following tables show the thermal resistance characteristics for the GDP and ZDP mechanical packages.

thermal resistance characteristics (S-PBGA package) for GDP

NO			°C/W	Air Flow (m/s)†
Two Signals, Two Planes (4-Layer Board)				
1	$R\Theta_{JC}$	Junction-to-case	9.7	N/A
2	Psi_{JT}	Junction-to-package top	1.5	0.0
3	$R\Theta_{JB}$	Junction-to-board	19	N/A
4	$R\Theta_{JA}$	Junction-to-free air	22	0.0
5	$R\Theta_{JA}$	Junction-to-free air	21	0.5
6	$R\Theta_{JA}$	Junction-to-free air	20	1.0
7	$R\Theta_{JA}$	Junction-to-free air	19	2.0
8	$R\Theta_{JA}$	Junction-to-free air	18	4.0
9	Psi_{JB}	Junction-to-board	16	0.0

† m/s = meters per second

thermal resistance characteristics (S-PBGA package) for ZDP

NO			°C/W	Air Flow (m/s)†
Two Signals, Two Planes (4-Layer Board)				
1	$R\Theta_{JC}$	Junction-to-case	9.7	N/A
2	Psi_{JT}	Junction-to-package top	1.5	0.0
3	$R\Theta_{JB}$	Junction-to-board	19	N/A
4	$R\Theta_{JA}$	Junction-to-free air	22	0.0
5	$R\Theta_{JA}$	Junction-to-free air	21	0.5
6	$R\Theta_{JA}$	Junction-to-free air	20	1.0
7	$R\Theta_{JA}$	Junction-to-free air	19	2.0
8	$R\Theta_{JA}$	Junction-to-free air	18	4.0
9	Psi_{JB}	Junction-to-board	16	0.0

† m/s = meters per second

The following table shows the thermal resistance characteristics for the PYP mechanical package.

thermal resistance characteristics (S-PQFP-G208 package) for PYP

NO			°C/W
Junction-to-Pad			
Two Signals, Two Planes (4-Layer Board) − 208-pin PYP			
1	$R\Theta_{JP}$	Junction-to-pad, 26 x 26 copper pad on top and bottom of PCB with solder connection and vias going to GND plane, isolated from power plane.	0.2
Junction-to-Package Top			
Two Signals, Two Planes (4-Layer Board) − 208-pin PYP			
2	Psi_{JT}	Junction-to-package top, 26 x 26 copper pad on top and bottom of PCB with solder connection and vias going to GND plane, isolated from power plane.	0.18
3	Psi_{JT}	Junction-to-package top, 7.5 x 7.5 copper pad on top and bottom of PCB with solder connection and vias going to GND plane, isolated from power plane.	0.23
Two Signals (2-Layer Board)			
4	Psi_{JT}	Junction-to-package top, 26 x 26 copper pad on top of PCB with solder connection and vias going to copper plane on bottom of board.	0.18
5	Psi_{JT}	Junction-to-package top, 7.5 x 7.5 copper pad on top of PCB with solder connection and vias going to copper plane on bottom of board.	0.23
Junction-to-Still Air			
Two Signals, Two Planes (4-Layer Board) − 208-pin PYP			
6	$R\Theta_{JA}$	Junction-to-still air, 26 x 26 copper pad on top and bottom of PCB with solder connection and vias going to GND plane, isolated from power plane.	13
7	$R\Theta_{JA}$	Junction-to-still air, 7.5 x 7.5 copper pad on top and bottom of PCB with solder connection and vias going to GND plane, isolated from power plane.	20
Two Signals (2-Layer Board)			
8	$R\Theta_{JA}$	Junction-to-still air, 26 x 26 copper pad on top of PCB with solder connection and vias going to copper plane on bottom of board.	14
9	$R\Theta_{JA}$	Junction-to-still air, 7.5 x 7.5 copper pad on top of PCB with solder connection and vias going to copper plane on bottom of board.	20

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TMS320C6713BGDP225	ACTIVE	BGA	GDP	272	40	TBD	SNPB	Level-3-220C-168HR
TMS320C6713BGDP300	ACTIVE	BGA	GDP	272	40	TBD	SNPB	Level-3-220C-168HR
TMS320C6713BPYP200	ACTIVE	HLQFP	PYP	208	36	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72HR
TMS320C6713BZDP225	ACTIVE	BGA	ZDP	272	40	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168HR
TMS32C6713BGDPA200	ACTIVE	BGA	GDP	272	40	TBD	SNPB	Level-3-220C-168HR
TMS32C6713BPYPA167	ACTIVE	HLQFP	PYP	208	36	TBD	CU NIPDAU	Level-4-220C-72HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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