

TMS320DM369

Digital Media System-on-Chip (DMSoC)

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1.1 Features

- **Highlights**
 - High-Performance Digital Media System-on-Chip (DMSoC)
 - 432-MHz ARM926EJ-S Clock Rate
 - Three Video Image Co-processors (Noise Filtering, CHDVICP, MJCP) Engines
 - Supports a Range of Encode, Decode, and Video Quality Operations
 - Video Processing Subsystem
 - HW Face Detect Engine
 - Resize Engine from 1/16x to 8x
 - 16-Bit Parallel AFE (Analog Front-End) Interface Up to 120 MHz
 - 4:2:2 (8-/16-bit) Interface
 - 8-/16-bit YCC and Up to 24-Bit RGB888 Digital Output
 - 3 DACs for HD Analog Video Output
 - Hardware On-Screen Display (OSD)
 - Capable of 1080p 30fps H.264 video processing
 - Peripherals include EMAC, USB 2.0 OTG, DDR2/NAND, 5 SPIs, 2 UARTs, 2 MMC/SD/SDIO, Key Scan
 - 8 Different Boot Modes and Configurable Power-Saving Modes
 - Pin-to-pin and software compatible with DM365
 - Extended temperature (-40°C to 85°C) available
 - 3.3-V and 1.8-V I/O, 1.35-V Core
 - 338-Pin Ball Grid Array at 65nm Process Technology
- High-Performance Digital Media System-on-Chip (DMSoC)
 - 432-MHz ARM926EJ-S Clock Rate
 - 4:2:2 (8-/16-Bit) Interface
 - Capable of 1080p 30fps H.264 video processing
 - Pin compatible with DM365 processors
 - Fully Software-Compatible With ARM9™
 - Extended temperature available for 432-MHz device
- ARM926EJ-S™ Core
 - Support for 32-Bit and 16-Bit (Thumb® Mode) Instruction Sets
 - DSP Instruction Extensions and Single Cycle MAC
 - ARM® Jazelle® Technology
 - Embedded ICE-RT Logic for Real-Time Debug
- ARM9 Memory Architecture
 - 16K-Byte Instruction Cache
 - 8K-Byte Data Cache
 - 32K-Byte RAM
 - 16K-Byte ROM
 - Little Endian
- Three Video Image Co-processors (Noise Filtering, HDVICP, MJCP) Engines
 - Support a Range of Encode and Decode Operations
 - H.264, MPEG4, MPEG2, MJPEG, JPEG, WMV9/VC1
 - Noise Filtering Engine
- Video Processing Subsystem
 - Front End Provides:
 - HW Face Detect Engine
 - Hardware IPIPE for Real-Time Image Processing
 - Resize Engine
 - Resize Images From 1/16x to 8x
 - Separate Horizontal/Vertical Control
 - Two Simultaneous Output Paths
 - IPIPE Interface (IPIPEIF)
 - Image Sensor Interface (ISIF) and CMOS Imager Interface
 - 16-Bit Parallel AFE (Analog Front End) Interface Up to 120 MHz
 - Glueless Interface to Common Video Decoders
 - BT.601/BT.656/BT.1120 Digital YCbCr 4:2:2 (8-/16-Bit) Interface
 - Histogram Module
 - Lens distortion correction module (LDC)
- Back End Provides:



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

- Hardware On-Screen Display (OSD)
- Composite NTSC/PAL video encoder output
- 8-/16-bit YCC and Up to 24-Bit RGB888 Digital Output
- 3 DACs for HD Analog Video Output
- LCD Controller
- BT.601/BT.656 Digital YCbCr 4:2:2 (8-/16-Bit) Interface
- Analog-to-Digital Converter (ADC)
- Power Management and Real Time Clock Subsystem (PRTCSS)
 - Real Time Clock
- 16-Bit Host-Port Interface (HPI)
- 10/100 Mb/s Ethernet Media Access Controller (EMAC) - Digital Media
 - IEEE 802.3 Compliant
 - Supports Media Independent Interface (MII)
 - Management Data I/O (MDIO) Module
- Key Scan
- Voice Codec
- External Memory Interfaces (EMIFs)
 - DDR2 and mDDR SDRAM 16-bit wide EMIF With 256 MByte Address Space (1.8-V I/O)
 - Asynchronous 16-/8-bit Wide EMIF (AEMIF)
 - Flash Memory Interfaces
 - NAND (8-/16-bit Wide Data)
 - 16 MB NOR Flash, SRAM
 - OneNAND (16-bit Wide Data)
- Flash Card Interfaces
 - Two Multimedia Card (MMC) / Secure Digital (SD/SDIO)
 - SmartMedia/xD
- Enhanced Direct-Memory-Access (EDMA) Controller (64 Independent Channels)
- USB Port with Integrated 2.0 High-Speed PHY that Supports
 - USB 2.0 High-Speed Device
 - USB 2.0 High-Speed Host (mini-host, supporting one external device)
 - USB On The Go (HS-USB OTG)
- Four 64-Bit General-Purpose Timers (each configurable as two 32-bit timers)
- One 64-Bit Watch Dog Timer
- Two UARTs (One fast UART with RTS and CTS Flow Control)
- Five Serial Port Interfaces (SPI) each with two Chip-Selects
- One Master/Slave Inter-Integrated Circuit (I²C) Bus™
- One Multi-Channel Buffered Serial Port (McBSP)
 - I2S
 - AC97 Audio Codec Interface
 - S/PDIF via Software
 - Standard Voice Codec Interface (AIC12)
 - SPI Protocol (Master Mode Only)
 - Direct Interface to T1/E1 Framers
 - Time Division Multiplexed Mode (TDM)
 - 128 Channel Mode
- Four Pulse Width Modulator (PWM) Outputs
- Four RTO (Real Time Out) Outputs
- Up to 104 General-Purpose I/O (GPIO) Pins (Multiplexed with Other Device Functions)
- Boot Modes
 - On-Chip ARM ROM Bootloader (RBL) to Boot From NAND Flash, MMC/SD, UART, USB, SPI, EMAC, or HPI
 - AEMIF (NOR and OneNAND)
- Configurable Power-Saving Modes
- Crystal or External Clock Input (typically 19.2 MHz, 24 MHz, 27 MHz or 36 MHz)
- Flexible PLL Clock Generators
- Debug Interface Support
 - IEEE-1149.1 (JTAG™) Boundary-Scan-Compatible
 - ETB (Embedded Trace Buffer) with 4K-Bytes Trace Buffer memory
 - Device Revision ID Readable by ARM
- 338-Pin Ball Grid Array (BGA) Package (ZCE Suffix), 0.65-mm Ball Pitch
- 65nm Process Technology
- 3.3-V and 1.8-V I/O, 1.35-V Internal
- Community Resources
 - [TI E2E Community](#)
 - [TI Embedded Processors Wiki](#)

1.2 Description

Developers can now deliver crystal clear multi-format video at up to 1080p H.264 at 30fps (encode and closed-looped decode) in their digital video designs without concerns of video format support, constrained network bandwidth, limited system storage capacity or cost with the new TMS320DM369 DaVinci™ video processors from Texas Instruments Incorporated (TI).

The DM369 is uniquely capable of running TI's 3rd Generation Noise Filtering technology while achieving low light HD H.264 720p30 video compression and is pin-to-pin compatible with the DM365 processors, using the same ARM926EJ-S core running at 432 MHz. This ARM9-based DM369 device supports production-qualified H.264BP/MP/HP, MPEG-4, MPEG-2, MJPEG and VC1/WMV9 codecs providing customers with the flexibility to select the right video codec for their application. These codecs run on independent coprocessors (HDVICP and MJCP) offloading all compression needs from the main ARM core. This allows developers to obtain optimal performance from the ARM for their applications, including their multi-channel, multi-stream and multi-format needs.

Video surveillance designers achieve greater compression efficiency to provide more storage without straining the network bandwidth. Developers of media playback and camera-driven applications, such as video doorbells, digital signage, digital video recorders, portable media players and more can take advantage of the low power consumption and can ensure interoperability, as well as product scalability by taking advantage of the full suite of codecs supported on the DM369.

Along with multi-format HD video, the DM369 also features a suite of peripherals saving developers on system cost and complexity to enable a seamless interface to most additional external devices required for video applications. The image sensor interface is flexible enough to support CCD, CMOS, and various other interfaces such as BT.656, BT1120. The DM369 also offers a high level of integration with HD display support, including three built-in 10-bit HD analog video digital-to-analog converters (DACs), DDR2/mDDR, Ethernet MAC, USB 2.0, integrated audio, host port interface (HPI), analog-to-digital converter and many more features saving developers on overall system costs, as well as real estate on their circuit boards allowing for a slimmer, sleeker design.

1.3 Functional Block Diagram

Figure 1-1 shows the functional block diagram of the TMS320DM369 device.

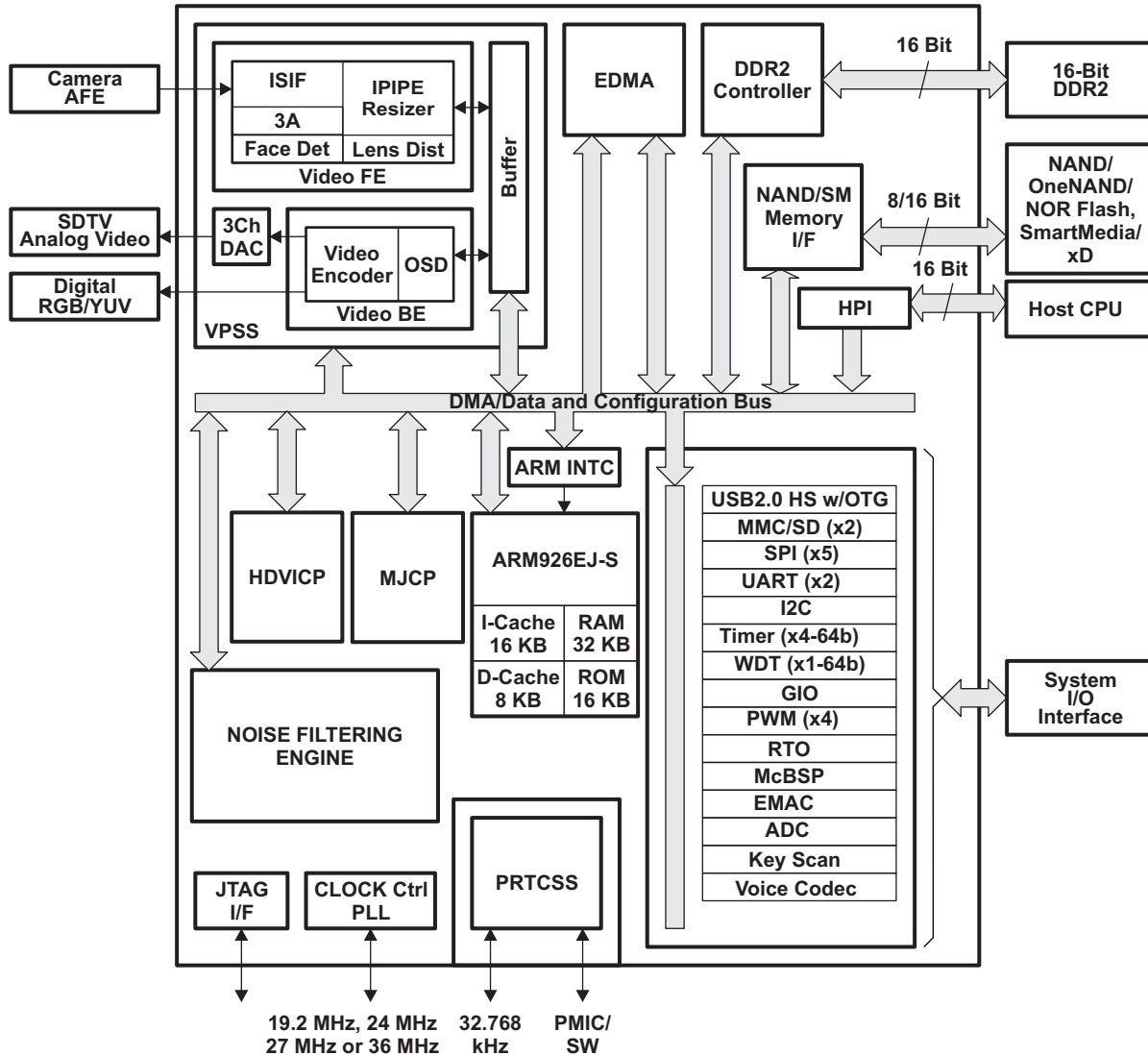


Figure 1-1. Functional Block Diagram

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TMS320DM369ZCE	ACTIVE	NFBGA	ZCE	338	160	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	0 to 85	DM369ZCE 570	Samples
TMS320DM369ZCED	ACTIVE	NFBGA	ZCE	338	160	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	DM369ZCED 570	Samples
TMS320DM369ZCEDF	ACTIVE	NFBGA	ZCE	338	160	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	DM369ZCEDF 570	Samples
TMS320DM369ZCEF	ACTIVE	NFBGA	ZCE	338	160	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 85	DM369ZCEF 570	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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