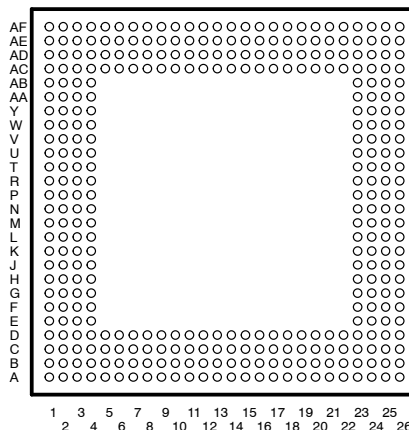


TMS320C6201 FIXED-POINT DIGITAL SIGNAL PROCESSOR

SPRS051H – JANUARY 1997 – REVISED MARCH 2004

- **High-Performance Fixed-Point Digital Signal Processor (DSP) TMS320C6201**
 - 5-ns Instruction Cycle Time
 - 200-MHz Clock Rate
 - Eight 32-Bit Instructions/Cycle
 - 1600 MIPS
- **VelociTI™ Advanced Very Long Instruction Word (VLIW) TMS320C62x™ DSP CPU Core**
 - Eight Independent Functional Units:
 - Six ALUs (32-/40-Bit)
 - Two 16-Bit Multipliers (32-Bit Results)
 - Load-Store Architecture With 32 32-Bit General-Purpose Registers
 - Instruction Packing Reduces Code Size
 - All Instructions Conditional
- **Instruction Set Features**
 - Byte-Addressable (8-, 16-, 32-Bit Data)
 - 32-Bit Address Range
 - 8-Bit Overflow Protection
 - Saturation
 - Bit-Field Extract, Set, Clear
 - Bit-Counting
 - Normalization
- **1M-Bit On-Chip SRAM**
 - 512K-Bit Internal Program/Cache (16K 32-Bit Instructions)
 - 512K-Bit Dual-Access Internal Data (64K Bytes) Organized as Two Blocks for Improved Concurrency
- **32-Bit External Memory Interface (EMIF)**
 - Glueless Interface to Asynchronous Memories: SRAM and EPROM
 - Glueless Interface to Synchronous Memories: SDRAM and SBSRAM
- **Four-Channel Bootloading Direct-Memory-Access (DMA) Controller with an Auxiliary Channel**
- **16-Bit Host-Port Interface (HPI)**
 - Access to Entire Memory Map

GJC/GJL
352-PIN BALL GRID ARRAY (BGA) PACKAGES
(BOTTOM VIEW)



- **Two Multichannel Buffered Serial Ports (McBSPs)**
 - Direct Interface to T1/E1, MVIP, SCSPA Framers
 - ST-Bus-Switching Compatible
 - Up to 256 Channels Each
 - AC97-Compatible
 - Serial Peripheral Interface (SPI) Compatible (Motorola™)
- **Two 32-Bit General-Purpose Timers**
- **Flexible Phase-Locked Loop (PLL) Clock Generator**
- **IEEE-1149.1 (JTAG†) Boundary-Scan Compatible**
- **352-Pin BGA Package (GJC Suffix)**
- **352-Pin BGA Package (GJL Suffix)**
- **CMOS Technology**
 - 0.18-μm/5-Level Metal Process
- **3.3-V I/Os, 1.8-V Internal**



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† IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.

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TMS320C6201 FIXED-POINT DIGITAL SIGNAL PROCESSOR

SPRS051H – JANUARY 1997 – REVISED MARCH 2004

Table of Contents

GJC/GJL BGA packages (bottom view)	1	parameter measurement information	30
description	2	input and output clocks	31
device characteristics	3	asynchronous memory timing	33
functional and CPU (DSP core) block diagram	4	synchronous-burst memory timing	35
CPU (DSP core) description	5	synchronous DRAM timing	39
signal groups description	7	HOLD/HOLDA timing	43
signal descriptions	9	reset timing	44
development support	20	external interrupt timing	46
documentation support	23	host-port interface timing	47
clock PLL	24	multichannel buffered serial port timing	50
power-down mode logic	25	DMAC, timer, power-down timing	61
power-supply sequencing	27	JTAG test-port timing	62
absolute maximum ratings over operating case temperature ranges	28	mechanical data	63
recommended operating conditions	28	revision history	65
electrical characteristics over recommended ranges of supply voltage and operating case temperature	29		

description

The TMS320C62x™ DSPs (including the TMS320C6201†) are the fixed-point DSP family in the TMS320C6000™ DSP platform. The C6201 device is based on the high-performance, advanced VelociTI™ very-long-instruction-word (VLIW) architecture developed by Texas Instruments (TI), making these DSPs an excellent choice for multichannel and multifunction applications. With performance of up to 1600 MIPS at a clock rate of 200 MHz, the C6201 offers cost-effective solutions to high-performance DSP programming challenges. The C6201 DSP possesses the operational flexibility of high-speed controllers and the numerical capability of array processors. The processor has 32 general-purpose registers of 32-bit word length and eight highly independent functional units. The eight functional units provide six arithmetic logic units (ALUs) for a high degree of parallelism and two 16-bit multipliers for a 32-bit result. The C6201 can produce two multiply-accumulates (MACs) per cycle—for a total of 466 million MACs per second (MMACS). The C62x™ DSP also has application-specific hardware logic, on-chip memory, and additional on-chip peripherals.

The C6201 includes a large bank of on-chip memory and has a powerful and diverse set of peripherals. Program memory consists of a 64K-byte block that is user-configurable as cache or memory-mapped program space. Data memory of the C6201 consists of two 32K-byte blocks of RAM for improved concurrency. The peripheral set includes two multichannel buffered serial ports (McBSPs), two general-purpose timers, a host-port interface (HPI), and a glueless external memory interface (EMIF) capable of interfacing to SDRAM or SBSRAM and asynchronous peripherals.

The C62x™ DSP has a complete set of development tools which includes: a new C compiler, an assembly optimizer to simplify programming and scheduling, and a Windows™ debugger interface for visibility into source code execution.

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Windows is a registered trademark of the Microsoft Corporation.

† The TMS320C6201 device shall be referred to as C6201 throughout the remainder of this document.



device characteristics

Table 1 provides an overview of the C6201 DSP. The table shows significant features of each device, including the capacity of on-chip RAM, the peripherals, the execution time, and the package type with pin count.

Table 1. Characteristics of the C6201 Processor

HARDWARE FEATURES		C6201 (FIXED-POINT DSP)
Peripherals	EMIF	1
	DMA	1
	HPI	1
	McBSPs	2
	32-Bit Timers	2
On-Chip Memory	Size (Bytes)	72K
	Organization	512-Kbit Program Memory 512-Kbit Data Memory (organized as two blocks)
CPU ID+Rev ID	Control Status Register (CSR.[31:16])	0x0002
Frequency	MHz	200
Cycle Time	ns	5 ns (C6201-200)
Voltage	Core (V)	1.8
	I/O (V)	3.3
PLL Options	CLKIN frequency multiplier	Bypass (x1), x4
BGA Packages	27 x 27 mm	352-Pin BGA (GJL)
	35 x 35 mm	352-Pin BGA (GJC)
Process Technology	μm	0.18 μm
Product Status	Product Preview (PP) Advance Information (AI) Production Data (PD)	PD
Device Part Numbers	(For more details on the C6000™ DSP part numbering, see Figure 4)	TMS320C6201GJC200 TMS320C6201GJCA200 TMS320C6201GJL200 TMS320C6201GJLA200

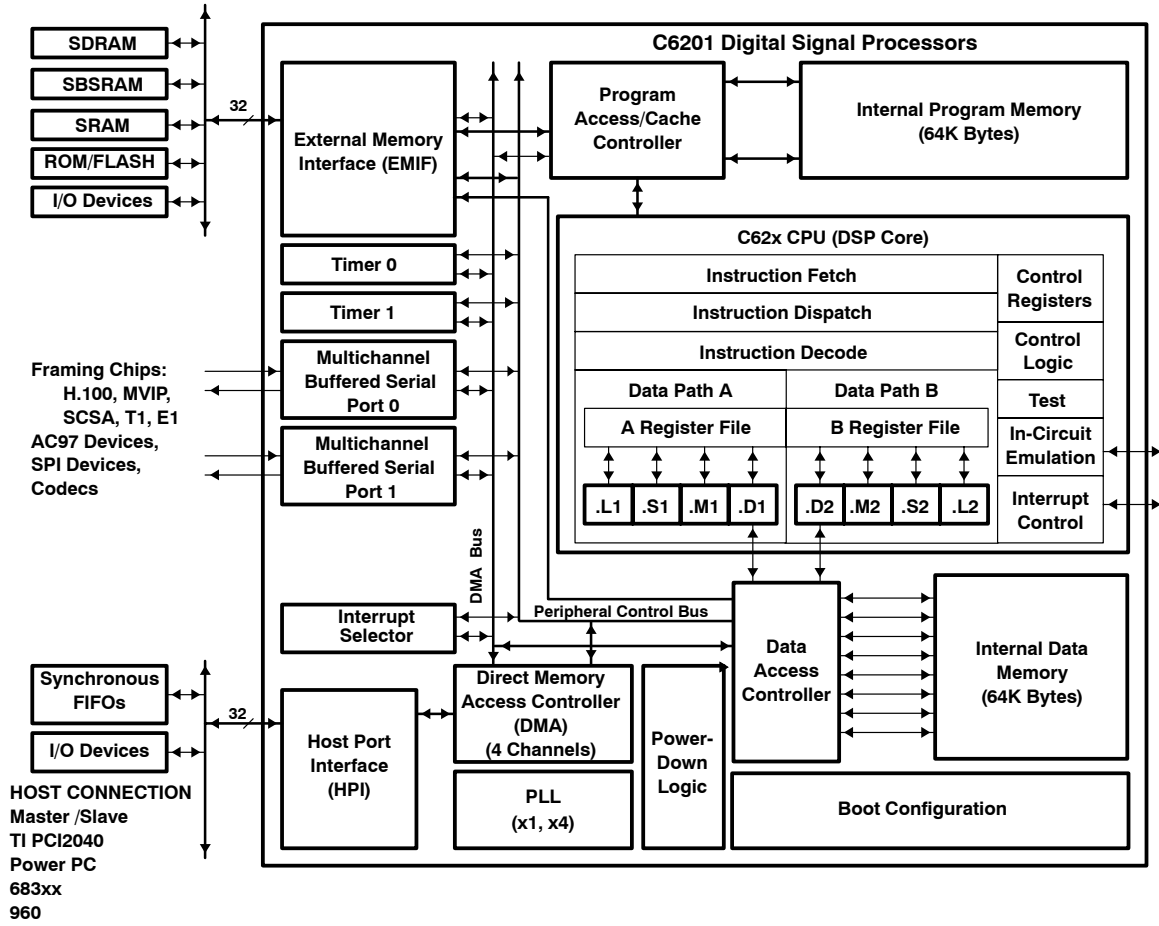
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TMS320C6201 FIXED-POINT DIGITAL SIGNAL PROCESSOR

SPRS051H – JANUARY 1997 – REVISED MARCH 2004

functional and CPU (DSP core) block diagram



CPU (DSP core) description

The CPU fetches VelociTI™ advanced very-long instruction words (VLIW) (256 bits wide) to supply up to eight 32-bit instructions to the eight functional units during every clock cycle. The VelociTI™ VLIW architecture features controls by which all eight units do not have to be supplied with instructions if they are not ready to execute. The first bit of every 32-bit instruction determines if the next instruction belongs to the same execute packet as the previous instruction, or whether it should be executed in the following clock as a part of the next execute packet. Fetch packets are always 256 bits wide; however, the execute packets can vary in size. The variable-length execute packets are a key memory-saving feature, distinguishing the C62x CPU from other VLIW architectures.

The CPU features two sets of functional units. Each set contains four units and a register file. One set contains functional units .L1, .S1, .M1, and .D1; the other set contains units .D2, .M2, .S2, and .L2. The two register files each contain 16 32-bit registers for a total of 32 general-purpose registers. The two sets of functional units, along with two register files, compose sides A and B of the CPU [see functional and CPU (DSP core) block diagram and Figure 1]. The four functional units on each side of the CPU can freely share the 16 registers belonging to that side. Additionally, each side features a single data bus connected to all the registers on the other side, by which the two sets of functional units can access data from the register files on the opposite side. While register access by functional units on the same side of the CPU as the register file can service all the units in a single clock cycle, register access using the register file across the CPU supports one read and one write per cycle.

Another key feature of the C62x CPU is the load/store architecture, where all instructions operate on registers (as opposed to data in memory). Two sets of data-addressing units (.D1 and .D2) are responsible for all data transfers between the register files and the memory. The data address driven by the .D units allows data addresses generated from one register file to be used to load or store data to or from the other register file. The C62x CPU supports a variety of indirect addressing modes using either linear- or circular-addressing modes with 5- or 15-bit offsets. All instructions are conditional, and most can access any one of the 32 registers. Some registers, however, are singled out to support specific addressing or to hold the condition for conditional instructions (if the condition is not automatically “true”). The two .M functional units are dedicated for multiplies. The two .S and .L functional units perform a general set of arithmetic, logical, and branch functions with results available every clock cycle.

The processing flow begins when a 256-bit-wide instruction fetch packet is fetched from a program memory. The 32-bit instructions destined for the individual functional units are “linked” together by “1” bits in the least significant bit (LSB) position of the instructions. The instructions that are “chained” together for simultaneous execution (up to eight in total) compose an execute packet. A “0” in the LSB of an instruction breaks the chain, effectively placing the instructions that follow it in the next execute packet. If an execute packet crosses the fetch packet boundary (256 bits wide), the assembler places it in the next fetch packet, while the remainder of the current fetch packet is padded with NOP instructions. The number of execute packets within a fetch packet can vary from one to eight. Execute packets are dispatched to their respective functional units at the rate of one per clock cycle and the next 256-bit fetch packet is not fetched until all the execute packets from the current fetch packet have been dispatched. After decoding, the instructions simultaneously drive all active functional units for a maximum execution rate of eight instructions every clock cycle. While most results are stored in 32-bit registers, they can be subsequently moved to memory as bytes or half-words as well. All load and store instructions are byte-, half-word, or word-addressable.

TMS320C6201 FIXED-POINT DIGITAL SIGNAL PROCESSOR

SPRS051H - JANUARY 1997 - REVISED MARCH 2004

CPU (DSP core) description (continued)

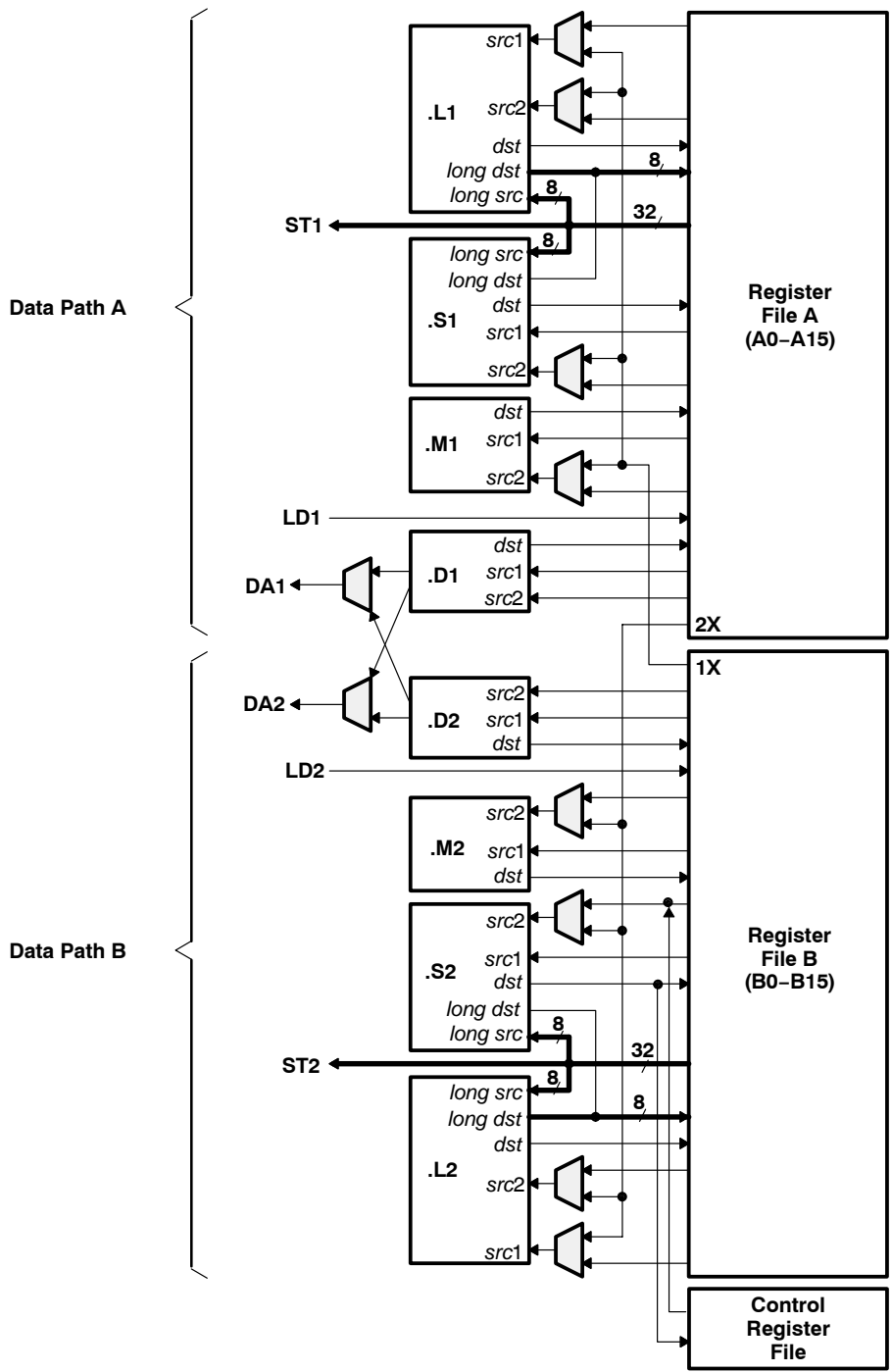


Figure 1. TMS320C62x CPU (DSP Core) Data Paths

signal groups description

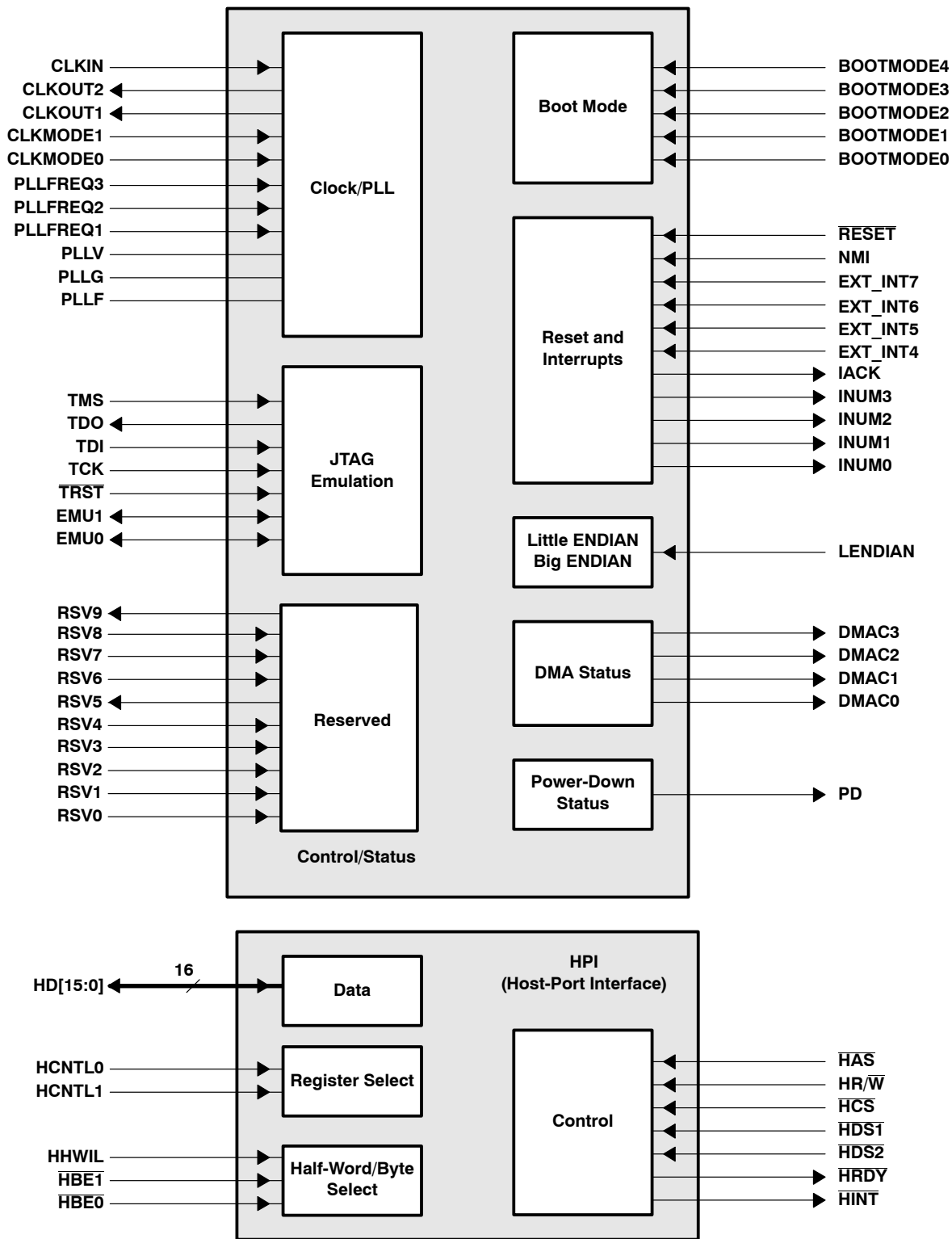


Figure 2. CPU (DSP Core) and Peripheral Signals

TMS320C6201 FIXED-POINT DIGITAL SIGNAL PROCESSOR

SPRS051H - JANUARY 1997 - REVISED MARCH 2004

signal groups description (continued)

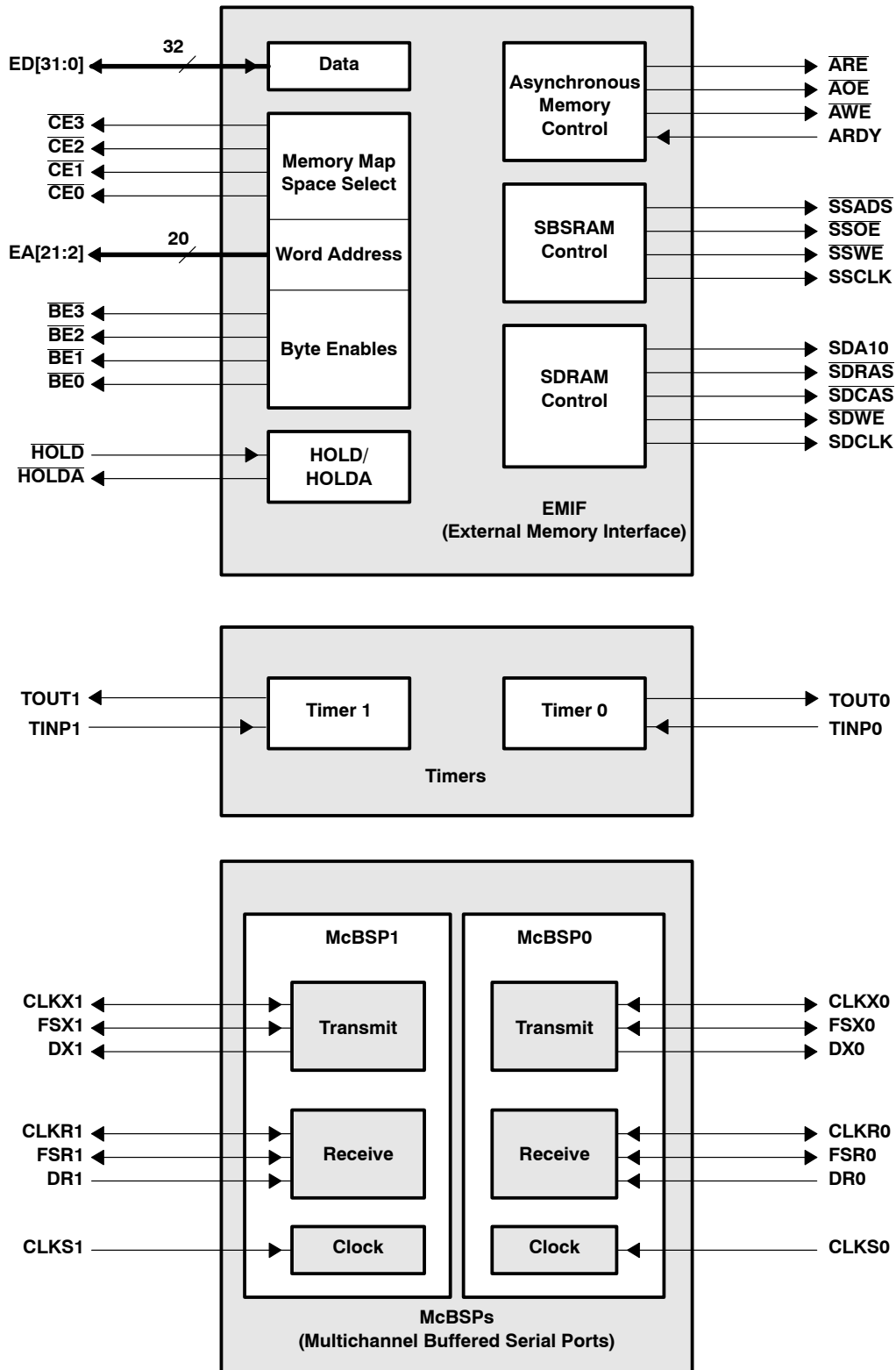


Figure 3. Peripheral Signals

Signal Descriptions

SIGNAL NAME	PIN NO.		TYPE†	DESCRIPTION
	GJC	GJL		
CLOCK/PLL				
CLKIN	C10	B9	I	Clock Input
CLKOUT1	AF22	AC18	O	Clock output at full device speed
CLKOUT2	AF20	AC16	O	Clock output at half of device speed
CLKMODE1	C6	D8	I	Clock mode selects <input type="checkbox"/> Selects whether the CPU clock frequency = input clock frequency x4 or x1 For more details on the GJC and GJL CLKMODE pins and the PLL multiply factors, see the <i>Clock PLL</i> section of this data sheet.
CLKMODE0	C5	C7		
PLLREQ3	A9	A9	I	PLL frequency range (3, 2, and 1) <input type="checkbox"/> The target range for CLKOUT1 frequency is determined by the 3-bit value of the PLLREQ pins.
PLLREQ2	D11	D11		
PLLREQ1	B10	B10		
PLLV‡	D12	B11	A§	PLL analog V _{CC} connection for the low-pass filter
PLLG‡	C12	C12	A§	PLL analog GND connection for the low-pass filter
PLLF	A11	D12	A§	PLL low-pass filter connection to external components and a bypass capacitor
JTAG EMULATION				
TMS	L3	L3	I	JTAG test port mode select (features an internal pullup)
TDO	W2	U4	O/Z	JTAG test port data out
TDI	R4	T2	I	JTAG test port data in (features an internal pullup)
TCK	R3	R3	I	JTAG test port clock
TRST	T1	R4	I	JTAG test port reset (features an internal pulldown)
EMU1	Y1	V3	I/O/Z	Emulation pin 1, pullup with a dedicated 20-kΩ resistor¶
EMU0	W3	W2	I/O/Z	Emulation pin 0, pullup with a dedicated 20-kΩ resistor¶
RESET AND INTERRUPTS				
RESET	K2	K2	I	Device reset
NMI	L2	L2	I	Nonmaskable interrupt <input type="checkbox"/> Edge-driven (rising edge)
EXT_INT7	U3	U2	I	External interrupts <input type="checkbox"/> Edge-driven <input type="checkbox"/> Polarity independently selected via the external interrupt polarity register bits (EXTPOL.[3:0])
EXT_INT6	V2	T4		
EXT_INT5	W1	V1		
EXT_INT4	U4	V2		
IACK	Y2	Y1	O	Interrupt acknowledge for all active interrupts serviced by the CPU
INUM3	AA1	V4	O	Active interrupt identification number <input type="checkbox"/> Valid during IACK for all active interrupts (not just external) <input type="checkbox"/> Encoding order follows the interrupt-service fetch-packet ordering
INUM2	W4	Y2		
INUM1	AA2	AA1		
INUM0	AB1	W4		
LITTLE ENDIAN/BIG ENDIAN				
LENDIAN	H3	G2	I	If high, LENDIAN selects little-endian byte/half-word addressing order within a word If low, LENDIAN selects big-endian addressing
POWER-DOWN STATUS				
PD	D3	E2	O	Power-down mode 2 or 3 (active if high)

† I = Input, O = Output, Z = High Impedance, S = Supply Voltage, GND = Ground

‡ PLLV and PLLG are not part of external voltage supply or ground. See the *clock PLL* section for information on how to connect these pins.

§ A = Analog Signal (PLL Filter)

¶ For emulation and normal operation, pull up EMU1 and EMU0 with a dedicated 20-kΩ resistor. For boundary scan, pull down EMU1 and EMU0 with a dedicated 20-kΩ resistor.

TMS320C6201 FIXED-POINT DIGITAL SIGNAL PROCESSOR

SPRS051H – JANUARY 1997 – REVISED MARCH 2004

Signal Descriptions (Continued)

SIGNAL NAME	PIN NO.		TYPE†	DESCRIPTION
	GJC	GJL		
HOST-PORT INTERFACE (HPI)				
HINT	H26	J26	O	Host interrupt (from DSP to host)
HCNTL1	F23	G24	I	Host control – selects between control, address, or data registers
HCNTL0	D25	F25	I	Host control – selects between control, address, or data registers
HHWIL	C26	E26	I	Host half-word select – first or second half-word (not necessarily high or low order)
HBE1	E23	F24	I	Host byte select within word or half-word
HBE0	D24	E25	I	Host byte select within word or half-word
HR/W	C23	B22	I	Host read or write select
HD15	B13	A12	I/O/Z	Host-port data (used for transfer of data, address, and control)
HD14	B14	D13		
HD13	C14	C13		
HD12	B15	D14		
HD11	D15	B15		
HD10	B16	C15		
HD9	A17	D15		
HD8	B17	B16		
HD7	D16	C16		
HD6	B18	B17		
HD5	A19	D16		
HD4	C18	A18		
HD3	B19	B18		
HD2	C19	D17		
HD1	B20	C18		
HD0	B21	A20		
HAS	C22	C20	I	Host address strobe
HCS	B23	B21	I	Host chip select
HDS1	D22	C21	I	Host data strobe 1
HDS2	A24	D20	I	Host data strobe 2
HRDY	J24	J25	O	Host ready (from DSP to host)
BOOT MODE				
BOOTMODE4	D8	C8	I	Boot mode
BOOTMODE3	B4	B6		
BOOTMODE2	A3	D7		
BOOTMODE1	D5	C6		
BOOTMODE0	C4	B5		

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Signal Descriptions (Continued)

SIGNAL NAME	PIN NO.		TYPE†	DESCRIPTION
	GJC	GJL		
EMIF – CONTROL SIGNALS COMMON TO ALL TYPES OF MEMORY				
$\overline{CE3}$	AE22	AD20	O/Z	Memory space enables <input type="checkbox"/> Enabled by bits 24 and 25 of the word address <input type="checkbox"/> Only one asserted during any external data access
$\overline{CE2}$	AD26	AA24		
$\overline{CE1}$	AB24	AB26		
$\overline{CE0}$	AC26	AA25		
$\overline{BE3}$	AB25	Y24	O/Z	Byte-enable control <input type="checkbox"/> Decoded from the two lowest bits of the internal address <input type="checkbox"/> Byte-write enables for most types of memory <input type="checkbox"/> Can be directly connected to SDRAM read and write mask signal (SDQM)
$\overline{BE2}$	AA24	W23		
$\overline{BE1}$	Y23	AA26		
$\overline{BE0}$	AA26	W25		
EMIF – ADDRESS				
EA21	J26	K25	O/Z	External address (word address)
EA20	K25	L24		
EA19	L24	L25		
EA18	K26	M23		
EA17	M26	M25		
EA16	M25	M24		
EA15	P25	N23		
EA14	P24	P24		
EA13	R25	P23		
EA12	T26	R25		
EA11	R23	R24		
EA10	U26	R23		
EA9	U25	T25		
EA8	T23	T24		
EA7	V26	U25		
EA6	V25	T23		
EA5	W26	V26		
EA4	V24	V25		
EA3	W25	U23		
EA2	Y26	V24		

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TMS320C6201 FIXED-POINT DIGITAL SIGNAL PROCESSOR

SPRS051H – JANUARY 1997 – REVISED MARCH 2004

Signal Descriptions (Continued)

SIGNAL NAME	PIN NO.		TYPE†	DESCRIPTION
	GJC	GJL		
EMIF – DATA				
ED31	AB2	Y3	I/O/Z	External data
ED30	AC1	AA2		
ED29	AA4	AB1		
ED28	AD1	AA3		
ED27	AC3	AB2		
ED26	AD4	AE5		
ED25	AF3	AD6		
ED24	AE4	AC7		
ED23	AD5	AE6		
ED22	AF4	AD7		
ED21	AE5	AC8		
ED20	AD6	AD8		
ED19	AE6	AC9		
ED18	AD7	AF7		
ED17	AC8	AD9		
ED16	AF7	AC10		
ED15	AD9	AE9		
ED14	AD10	AF9		
ED13	AF9	AC11		
ED12	AC11	AE10		
ED11	AE10	AD11		
ED10	AE11	AE11		
ED9	AF11	AC12		
ED8	AE14	AD12		
ED7	AF15	AE12		
ED6	AE15	AC13		
ED5	AF16	AD14		
ED4	AC15	AC14		
ED3	AE17	AE15		
ED2	AF18	AD15		
ED1	AF19	AE16		
ED0	AC17	AD16		
EMIF – ASYNCHRONOUS MEMORY CONTROL				
ARE	Y24	V23	O/Z	Asynchronous memory read enable
\overline{AOE}	AC24	AB25	O/Z	Asynchronous memory output enable
\overline{AWE}	AD23	AE22	O/Z	Asynchronous memory write enable
ARDY	W23	Y26	I	Asynchronous memory ready input

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Signal Descriptions (Continued)

SIGNAL NAME	PIN NO.		TYPE†	DESCRIPTION
	GJC	GJL		
EMIF – SYNCHRONOUS BURST SRAM (SBSRAM) CONTROL				
\overline{SSADS}	AC20	AD19	O/Z	SBSRAM address strobe
\overline{SSOE}	AF21	AD18	O/Z	SBSRAM output enable
\overline{SSWE}	AD19	AF18	O/Z	SBSRAM write enable
SSCLK	AD17	AC15	O	SBSRAM clock
EMIF – SYNCHRONOUS DRAM (SDRAM) CONTROL				
SDA10	AD21	AC19	O/Z	SDRAM address 10 (separate for deactivate command)
\overline{SDRAS}	AF24	AD21	O/Z	SDRAM row-address strobe
\overline{SDCAS}	AD22	AC20	O/Z	SDRAM column-address strobe
\overline{SDWE}	AF23	AE21	O/Z	SDRAM write enable
SDCLK	AE20	AC17	O	SDRAM clock
EMIF – BUS ARBITRATION				
HOLD	AA25	Y25	I	Hold request from the host
HOLDA	A7	C9	O	Hold-request acknowledge to the host
TIMER1				
TOUT1	H24	K23	O	Timer 1 or general-purpose output
TINP1	K24	L23	I	Timer 1 or general-purpose input
TIMERO				
TOUT0	M4	M4	O	Timer 0 or general-purpose output
TINP0	K4	H2	I	Timer 0 or general-purpose input
DMA ACTION COMPLETE STATUS				
DMAC3	D2	E1	O	DMA action complete
DMAC2	F4	F2		
DMAC1	D1	G3		
DMAC0	E2	H4		
MULTICHANNEL BUFFERED SERIAL PORT 1 (McBSP1)				
CLKS1	E25	F26	I	External clock source (as opposed to internal)
CLKR1	H23	H25	I/O/Z	Receive clock
CLKX1	F26	J24	I/O/Z	Transmit clock
DR1	D26	H23	I	Receive data
DX1	G23	G25	O/Z	Transmit data
FSR1	E26	J23	I/O/Z	Receive frame sync
FSX1	F25	G26	I/O/Z	Transmit frame sync

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TMS320C6201 FIXED-POINT DIGITAL SIGNAL PROCESSOR

SPRS051H – JANUARY 1997 – REVISED MARCH 2004

Signal Descriptions (Continued)

SIGNAL NAME	PIN NO.		TYPE†	DESCRIPTION
	GJC	GJL		
MULTICHANNEL BUFFERED SERIAL PORT 0 (McBSP0)				
CLKS0	L4	L4	I	External clock source (as opposed to internal)
CLKR0	M2	M2	I/O/Z	Receive clock
CLKX0	L1	M3	I/O/Z	Transmit clock
DR0	J1	J1	I	Receive data
DX0	R1	P4	O/Z	Transmit data
FSR0	P4	N3	I/O/Z	Receive frame sync
FSX0	P3	N4	I/O/Z	Transmit frame sync
RESERVED FOR TEST				
RSV0	T2	T3	I	Reserved for testing, pullup with a dedicated 20-kΩ resistor
RSV1	G2	F1	I	Reserved for testing, pullup with a dedicated 20-kΩ resistor
RSV2	C11	C11	I	Reserved for testing, pullup with a dedicated 20-kΩ resistor
RSV3	B9	D10	I	Reserved for testing, pullup with a dedicated 20-kΩ resistor
RSV4	A6	D9	I	Reserved for testing, pulldown with a dedicated 20-kΩ resistor
RSV5	C8	A7	O	Reserved (leave unconnected, do not connect to power or ground)
RSV6	C21	D18	I	Reserved for testing, pullup with a dedicated 20-kΩ resistor
RSV7	B22	C19	I	Reserved for testing, pullup with a dedicated 20-kΩ resistor
RSV8	A23	D19	I	Reserved for testing, pullup with a dedicated 20-kΩ resistor
RSV9	E4	F3	O	Reserved (leave unconnected, do not connect to power or ground)
UNCONNECTED PINS				
NC	A8	AF20		Unconnected pins
	B8	AE18		
	C9	AE17		
	D10	–		
	D21	–		
	G1	J4		
	H1	J3		
	H2	G1		
	J2	K4		
	K3	J2		
	R2	R2		

† I = Input, O = Output, Z = High Impedance, S = Supply Voltage, GND = Ground



Signal Descriptions (Continued)

SIGNAL NAME	PIN NO.		TYPE†	DESCRIPTION
	GJC	GJL		
3.3-V SUPPLY VOLTAGE PINS				
DV _{DD}	A10	A5	S	3.3-V supply voltage
	A15	A11		
	A18	A16		
	A21	A22		
	A22	B7		
	B7	B8		
	C1	B19		
	D17	B20		
	F3	C10		
	G24	C14		
	G25	C17		
	H25	G4		
	J25	G23		
	L25	H3		
	M3	H24		
	N3	K3		
	N23	K24		
	R26	L1		
	T24	L26		
	U24	N24		
	W24	P3		
	Y4	T1		
	AB3	T26		
	AB4	U3		
	AB26	U24		
	AC6	W3		
	AC10	W24		
	AC19	Y4		
	AC21	Y23		
	AC22	AD10		
	AC25	AD13		
	AD11	AD17		
	AD13	AE7		
AD15	AE8			
AD18	AE19			
AE18	AE20			
AE21	AF5			
AF5	AF11			
AF6	AF16			
AF17	AF22			

† I = Input, O = Output, Z = High Impedance, S = Supply Voltage, GND = Ground

TMS320C6201 FIXED-POINT DIGITAL SIGNAL PROCESSOR

SPRS051H – JANUARY 1997 – REVISED MARCH 2004

Signal Descriptions (Continued)

SIGNAL NAME	PIN NO.		TYPE†	DESCRIPTION
	GJC	GJL		
1.8-V SUPPLY VOLTAGE PINS				
CV _{DD}	A5	A1	S	1.8-V supply voltage
	A12	A2		
	A16	A3		
	A20	A24		
	B2	A25		
	B6	A26		
	B11	B1		
	B12	B2		
	B25	B3		
	C3	B24		
	C15	B25		
	C20	B26		
	C24	C1		
	D4	C2		
	D6	C3		
	D7	C4		
	D9	C23		
	D14	C24		
	D18	C25		
	D20	C26		
	D23	D3		
	E1	D4		
	F1	D5		
	H4	D22		
	J4	D23		
	J23	D24		
	K1	E4		
	K23	E23		
	M1	AB4		
	M24	AB23		
N4	AC3			
N25	AC4			
P2	AC5			
P23	AC22			
T3	AC23			
T4	AC24			
U1	AD1			
V4	AD2			

† I = Input, O = Output, Z = High Impedance, S = Supply Voltage, GND = Ground



Signal Descriptions (Continued)

SIGNAL NAME	PIN NO.		TYPE†	DESCRIPTION
	GJC	GJL		
1.8-V SUPPLY VOLTAGE PINS (CONTINUED)				
CV _{DD}	V23	AD3	S	1.8-V supply voltage
	AC4	AD4		
	AC9	AD23		
	AC12	AD24		
	AC13	AD25		
	AC18	AD26		
	AC23	AE1		
	AD3	AE2		
	AD8	AE3		
	AD14	AE24		
	AD24	AE25		
	AE2	AE26		
	AE8	AF1		
	AE12	AF2		
	AE25	AF3		
	AF12	AF24		
-	AF25			
-	AF26			
GROUND PINS				
V _{SS}	A1	A4	GND	Ground pins
	A2	A6		
	A4	A8		
	A13	A10		
	A14	A13		
	A25	A14		
	A26	A15		
	B1	A17		
	B3	A19		
	B5	A21		
	B24	A23		
	B26	B4		
	C2	B12		
	C7	B13		
	C13	B14		
	C16	B23		
	C17	C5		
	C25	C22		
D13	D1			

† I = Input, O = Output, Z = High Impedance, S = Supply Voltage, GND = Ground

TMS320C6201 FIXED-POINT DIGITAL SIGNAL PROCESSOR

SPRS051H - JANUARY 1997 - REVISED MARCH 2004

Signal Descriptions (Continued)

SIGNAL NAME	PIN NO.		TYPE†	DESCRIPTION
	GJC	GJL		
GROUND PINS (CONTINUED)				
V _{SS}	D19	D2	GND	Ground pins
	E3	D6		
	E24	D21		
	F2	D25		
	F24	D26		
	G3	E3		
	G4	E24		
	G26	F4		
	J3	F23		
	L23	H1		
	L26	H26		
	M23	K1		
	N1	K26		
	N2	M1		
	N24	M26		
	N26	N1		
	P1	N2		
	P26	N25		
	R24	N26		
	T25	P1		
	U2	P2		
	U23	P25		
	V1	P26		
	V3	R1		
	Y3	R26		
	Y25	U1		
	AA3	U26		
	AA23	W1		
	AB23	W26		
	AC2	AA4		
	AC5	AA23		
	AC7	AB3		
AC14	AB24			
AC16	AC1			
AD2	AC2			
AD12	AC6			
AD16	AC21			
AD20	AC25			

† I = Input, O = Output, Z = High Impedance, S = Supply Voltage, GND = Ground



TMS320C6201 FIXED-POINT DIGITAL SIGNAL PROCESSOR

SPRS051H – JANUARY 1997 – REVISED MARCH 2004

Signal Descriptions (Continued)

SIGNAL NAME	PIN NO.		TYPE†	DESCRIPTION
	GJC	GJL		
GROUND PINS (CONTINUED)				
V _{SS}	AD25	AC26	GND	Ground pins
	AE1	AD5		
	AE3	AD22		
	AE7	AE4		
	AE9	AE13		
	AE13	AE14		
	AE16	AE23		
	AE19	AF4		
	AE23	AF6		
	AE24	AF8		
	AE26	AF10		
	AF1	AF12		
	AF2	AF13		
	AF8	AF14		
	AF10	AF15		
	AF13	AF17		
	AF14	AF19		
AF25	AF21			
AF26	AF23			

† I = Input, O = Output, Z = High Impedance, S = Supply Voltage, GND = Ground



TMS320C6201

FIXED-POINT DIGITAL SIGNAL PROCESSOR

SPRS051H – JANUARY 1997 – REVISED MARCH 2004

development support

TI offers an extensive line of development tools for the TMS320C6000™ DSP platform, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development of C6000™ DSP-based applications:

Software Development Tools:

Code Composer Studio™ Integrated Development Environment (IDE) including Editor

C/C++/Assembly Code Generation, and Debug plus additional development tools

Scalable, Real-Time Foundation Software (DSP BIOS), which provides the basic run-time target software needed to support any DSP application.

Hardware Development Tools:

Extended Development System (XDS™) Emulator (supports C6000™ DSP multiprocessor system debug)
EVM (Evaluation Module)

The *TMS320 DSP Development Support Reference Guide* (SPRU011) contains information about development-support products for all TMS320™ DSP family member devices, including documentation. See this document for further information on TMS320™ DSP documentation or any TMS320™ DSP support products from Texas Instruments. An additional document, the *TMS320 Third-Party Support Reference Guide* (SPRU052), contains information about TMS320™ DSP-related products from other companies in the industry. To receive TMS320™ DSP literature, contact the Literature Response Center at 800/477-8924.

For a complete listing of development-support tools for the TMS320C6000™ DSP platform, visit the Texas Instruments web site on the Worldwide Web at <http://www.ti.com> uniform resource locator (URL) and under “Development Tools”, select “Digital Signal Processors”. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

Code Composer Studio, XDS, and TMS320 are trademarks of Texas Instruments.



device and development-support tool nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320 DSP devices and support tools. Each TMS320 DSP commercial family member has one of three prefixes: TMX, TMP, or TMS. Texas Instruments recommends two of three possible prefix designators for support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

- TMX** Experimental device that is not necessarily representative of the final device's electrical specifications
- TMP** Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification
- TMS** Fully qualified production device

Support tool development evolutionary flow:

- TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing.
- TMDS** Fully qualified development-support product

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

“Developmental product is intended for internal evaluation purposes.”

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

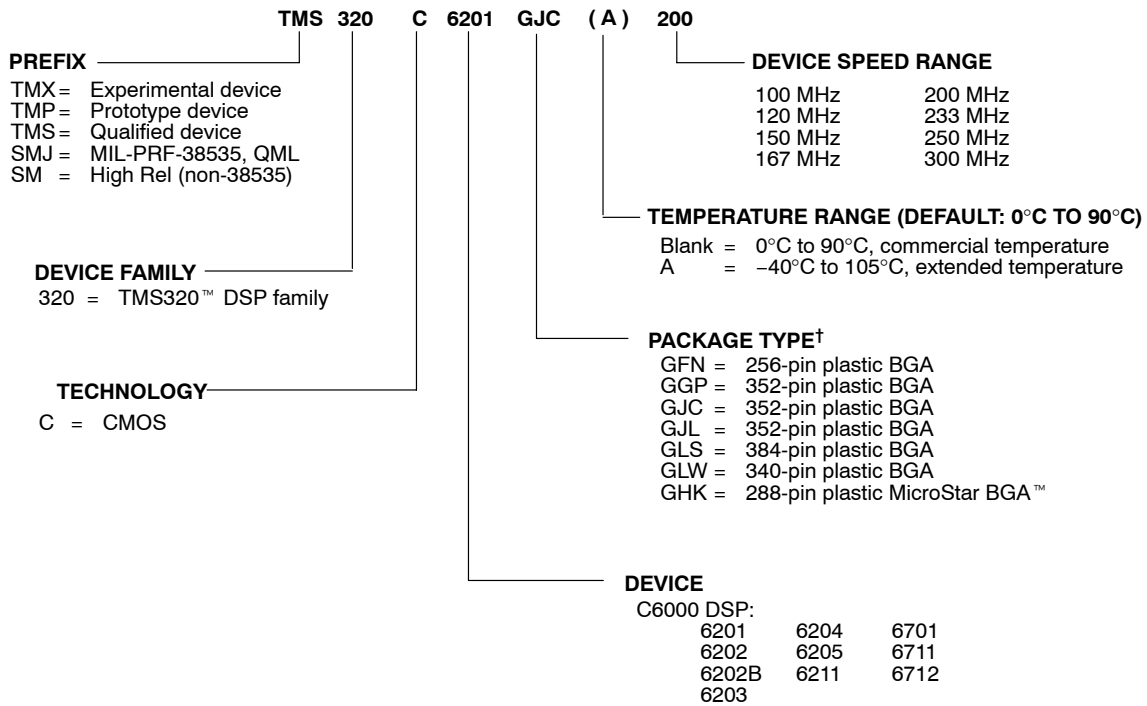
Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, GJC or GJL), the temperature range (for example, blank is the default commercial temperature range), and the device speed range in megahertz (for example, -200 is 200 MHz). Figure 4 provides a legend for reading the complete device name for any TMS320C6000 DSP family member.

TMS320C6201 FIXED-POINT DIGITAL SIGNAL PROCESSOR

SPRS051H – JANUARY 1997 – REVISED MARCH 2004

device and development-support tool nomenclature (continued)



† BGA = Ball Grid Array

Figure 4. TMS320C6000 Device Nomenclature (Including TMS320C6201)

MicroStar BGA is a trademark of Texas Instruments.



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documentation support

Extensive documentation supports all TMS320 DSP family devices from product announcement through applications development. The types of documentation available include: data sheets, such as this document, with design specifications; complete user's reference guides for all devices and tools; technical briefs; development-support tools; on-line help; and hardware and software applications. The following is a brief, descriptive list of support documentation specific to the C6000 DSP devices:

The *TMS320C6000 CPU and Instruction Set Reference Guide* (literature number SPRU189) describes the C6000 CPU (DSP core) architecture, instruction set, pipeline, and associated interrupts.

The *TMS320C6000 DSP Peripherals Overview Reference Guide* (literature number SPRU190) briefly describes the functionality of the peripherals available on the C6000™ DSP platform of devices, such as the 64-/32-/16-bit external memory interfaces (EMIFs), 32-/16-bit host-port interfaces (HPIs), multichannel buffered serial ports (McBSPs), direct memory access (DMA), enhanced direct-memory-access (EDMA) controller, expansion bus (XB), peripheral component interconnect (PCI), clocking and phase-locked loop (PLL); and power-down modes.

The *TMS320C6000 Technical Brief* (literature number SPRU197) gives an introduction to the C62x/C67x™ devices, associated development tools, and third-party support.

The tools support documentation is electronically available within the Code Composer Studio™ IDE. For a complete listing of the latest C6000™ DSP documentation, visit the Texas Instruments web site on the Worldwide Web at <http://www.ti.com> uniform resource locator (URL).

C67x is a trademark of Texas Instruments.



Table 3. Characteristics of the Power-Down Modes

PRWD FIELD (BITS 15–10)	POWER-DOWN MODE	WAKE-UP METHOD	EFFECT ON CHIP'S OPERATION
000000	No power-down	—	—
001001	PD1	Wake by an enabled interrupt	CPU halted (except for the interrupt logic) Power-down mode blocks the internal clock inputs at the boundary of the CPU, preventing most of the CPU's logic from switching. During PD1, DMA transactions can proceed between peripherals and internal memory.
010001	PD1	Wake by an enabled or non-enabled interrupt	
011010	PD2 [†]	Wake by a device reset	Output clock from PLL is halted, stopping the internal clock structure from switching and resulting in the entire chip being halted. All register and internal RAM contents are preserved. All functional I/O "freeze" in the last state when the PLL clock is turned off.
011100	PD3 [†]	Wake by a device reset	Input clock to the PLL stops generating clocks. All register and internal RAM contents are preserved. All functional I/O "freeze" in the last state when the PLL clock is turned off. Following reset, the PLL needs time to re-lock, just as it does following power-up. Wake-up from PD3 takes longer than wake-up from PD2 because the PLL needs to be re-locked.
All others	Reserved	—	—

[†] When entering PD2 and PD3, all functional I/O remains in the previous state. However, for peripherals which are asynchronous in nature or peripherals with an external clock source, output signals may transition in response to stimulus on the inputs. Under these conditions, peripherals will not operate according to specifications.

power-supply sequencing

TI DSPs do not require specific power sequencing between the core supply and the I/O supply. However, systems should be designed to ensure that neither supply is powered up for extended periods of time if the other supply is below the proper operating voltage.

system-level design considerations

System-level design considerations, such as bus contention, may require supply sequencing to be implemented. In this case, the core supply should be powered up at the same time as, or prior to (and powered down after), the I/O buffers. This is to ensure that the I/O buffers receive valid inputs from the core before the output buffers are powered up, thus, preventing bus contention with other chips on the board.

power-supply design considerations

For systems using the C6000 DSP platform of devices, the core supply may be required to provide in excess of 2 A per DSP until the I/O supply is powered up. This extra current condition is a result of uninitialized logic within the DSP(s) and is corrected once the CPU sees an internal clock pulse. With the PLL enabled, as the I/O supply is powered on, a clock pulse is produced stopping the extra current draw from the supply. With the PLL disabled, an external clock pulse may be required to stop this extra current draw. A normal current state returns once the I/O power supply is turned on and the CPU sees a clock pulse. Decreasing the amount of time between the core supply power up and the I/O supply power up can minimize the effects of this current draw.

A dual-power supply with simultaneous sequencing, such as available with TPS563xx controllers or PT69xx plug-in power modules, can be used to eliminate the delay between core and I/O power up [see the *Using the TPS56300 to Power DSPs Application Report* (literature number SLVA088)]. A Schottky diode can also be used to tie the core rail to the I/O rail, effectively pulling up the I/O power supply to a level that can help initialize the logic within the DSP.

TMS320C6201 FIXED-POINT DIGITAL SIGNAL PROCESSOR

SPRS051H – JANUARY 1997 – REVISED MARCH 2004

Core and I/O supply voltage regulators should be located close to the DSP (or DSP array) to minimize inductance and resistance in the power delivery path. Additionally, when designing for high-performance applications utilizing the C6000 platform of DSPs, the PC board should include separate power planes for core, I/O, and ground, all bypassed with high-quality low-ESL/ESR capacitors.

absolute maximum ratings over operating case temperature ranges (unless otherwise noted)[†]

Supply voltage range, CV_{DD} (see Note 1)	-0.3 V to 2.3 V
Supply voltage range, DV_{DD} (see Note 1)	-0.3 V to 4 V
Input voltage range	-0.3 V to 4 V
Output voltage range	-0.3 V to 4 V
Operating case temperature ranges T_C : (default)	0°C to 90°C
(A version)	-40°C to 105°C
Storage temperature range, T_{stg}	-65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS} .

recommended operating conditions

		MIN	NOM	MAX	UNIT
CV_{DD}	Supply voltage	1.71	1.8	1.89	V
DV_{DD}	Supply voltage	3.14	3.30	3.46	V
V_{SS}	Supply ground	0	0	0	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			-12	mA
I_{OL}	Low-level output current			12	mA
T_C	Operating case temperature	Default	0	90	°C
		A version	-40	105	



TMS320C6201 FIXED-POINT DIGITAL SIGNAL PROCESSOR

SPRS051H – JANUARY 1997 – REVISED MARCH 2004

electrical characteristics over recommended ranges of supply voltage and operating case temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OH}	High-level output voltage	DV _{DD} = MIN, I _{OH} = MAX	2.4			V
V _{OL}	Low-level output voltage	DV _{DD} = MIN, I _{OL} = MAX			0.6	V
I _I	Input current [‡]	V _I = V _{SS} to DV _{DD}			±10	µA
I _{OZ}	Off-state output current	V _O = DV _{DD} or 0 V			±10	µA
I _{DD2V}	Supply current, CPU + CPU memory access [§]	CV _{DD} = NOM, CPU clock = 167 MHz		380		mA
I _{DD2V}	Supply current, peripherals [§]	CV _{DD} = NOM, CPU clock = 167 MHz		240		mA
I _{DD3V}	Supply current, I/O pins [§]	DV _{DD} = NOM, CPU clock = 167 MHz		90		mA
C _i	Input capacitance				10	pF
C _o	Output capacitance				10	pF

[‡] TMS and TDI are not included due to internal pullups. TRST is not included due to internal pulldown.

[§] Measured with average activity (50% high / 50% low power). For more details on CPU, peripheral, and I/O activity, see the *TMS320C6000 Power Consumption Summary* application report (literature number SPRA486).

ASYNCHRONOUS MEMORY TIMING

timing requirements for asynchronous memory cycles[†] (see Figure 15 and Figure 16)

NO.			-200		UNIT
			MIN	MAX	
6	$t_{su}(EDV-CKO1H)$	Setup time, read EDx valid before CLKOUT1 high	4		ns
7	$t_h(CKO1H-EDV)$	Hold time, read EDx valid after CLKOUT1 high	0.8		ns
10	$t_{su}(ARDY-CKO1H)$	Setup time, ARDY valid before CLKOUT1 high	3		ns
11	$t_h(CKO1H-ARDY)$	Hold time, ARDY valid after CLKOUT1 high	1.8		ns

[†] To ensure data setup time, simply program the strobe width wide enough. ARDY is internally synchronized. If ARDY does not meet setup or hold time, it may be recognized in the current cycle or the next cycle. Thus, ARDY can be an asynchronous input.

switching characteristics over recommended operating conditions for asynchronous memory cycles[‡] (see Figure 15 and Figure 16)

NO.	PARAMETER		-200		UNIT
			MIN	MAX	
1	$t_d(CKO1H-CEV)$	Delay time, CLKOUT1 high to \overline{CEx} valid	-0.2	4	ns
2	$t_d(CKO1H-BEV)$	Delay time, CLKOUT1 high to \overline{BEx} valid		4	ns
3	$t_d(CKO1H-BEIV)$	Delay time, CLKOUT1 high to \overline{BEx} invalid	-0.2		ns
4	$t_d(CKO1H-EAV)$	Delay time, CLKOUT1 high to EAx valid		4	ns
5	$t_d(CKO1H-EAIV)$	Delay time, CLKOUT1 high to EAx invalid	-0.2		ns
8	$t_d(CKO1H-AOEV)$	Delay time, CLKOUT1 high to \overline{AOE} valid	-0.2	4	ns
9	$t_d(CKO1H-AREV)$	Delay time, CLKOUT1 high to \overline{ARE} valid	-0.2	4	ns
12	$t_d(CKO1H-EDV)$	Delay time, CLKOUT1 high to EDx valid		4	ns
13	$t_d(CKO1H-EDIV)$	Delay time, CLKOUT1 high to EDx invalid	-0.2		ns
14	$t_d(CKO1H-AWEV)$	Delay time, CLKOUT1 high to \overline{AWE} valid	-0.2	4	ns

[‡] The minimum delay is also the minimum output hold after CLKOUT1 high.

SYNCHRONOUS-BURST MEMORY TIMING

timing requirements for synchronous-burst SRAM cycles (full-rate SSCLK) (see Figure 17)

NO.		-200		UNIT
		MIN	MAX	
7	$t_{su}(EDV-SSCLKH)$ Setup time, read EDx valid before SSCLK high	1.5		ns
8	$t_h(SSCLKH-EDV)$ Hold time, read EDx valid after SSCLK high	1.5		ns

switching characteristics over recommended operating conditions for synchronous-burst SRAM cycles[†] (full-rate SSCLK) (see Figure 17 and Figure 18)

NO.	PARAMETER	-200		UNIT
		MIN	MAX	
1	$t_{osu}(CEV-SSCLKH)$ Output setup time, \overline{CEx} valid before SSCLK high	0.5P	1.3	ns
2	$t_{oh}(SSCLKH-CEV)$ Output hold time, \overline{CEx} valid after SSCLK high	0.5P	2.3	ns
3	$t_{osu}(BEV-SSCLKH)$ Output setup time, \overline{BEx} valid before SSCLK high	0.5P	1.3	ns
4	$t_{oh}(SSCLKH-BEV)$ Output hold time, \overline{BEx} invalid after SSCLK high	0.5P	2.3	ns
5	$t_{osu}(EAV-SSCLKH)$ Output setup time, EAx valid before SSCLK high	0.5P	1.3	ns
6	$t_{oh}(SSCLKH-EAV)$ Output hold time, EAx invalid after SSCLK high	0.5P	2.3	ns
9	$t_{osu}(ADSV-SSCLKH)$ Output setup time, \overline{SSADS} valid before SSCLK high	0.5P	1.3	ns
10	$t_{oh}(SSCLKH-ADSV)$ Output hold time, \overline{SSADS} valid after SSCLK high	0.5P	2.3	ns
11	$t_{osu}(OEV-SSCLKH)$ Output setup time, \overline{SSOE} valid before SSCLK high	0.5P	1.3	ns
12	$t_{oh}(SSCLKH-OEV)$ Output hold time, \overline{SSOE} valid after SSCLK high	0.5P	2.3	ns
13	$t_{osu}(EDV-SSCLKH)$ Output setup time, EDx valid before SSCLK high	0.5P	1.3	ns
14	$t_{oh}(SSCLKH-EDV)$ Output hold time, EDx invalid after SSCLK high	0.5P	2.3	ns
15	$t_{osu}(WEV-SSCLKH)$ Output setup time, \overline{SSWE} valid before SSCLK high	0.5P	1.3	ns
16	$t_{oh}(SSCLKH-WEV)$ Output hold time, \overline{SSWE} valid after SSCLK high	0.5P	2.3	ns

[†] When the PLL is used (CLKMODE x4), P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns. For CLKMODE x1, 0.5P is defined as PH (pulse duration of CLKIN high) for all output setup times; 0.5P is defined as PL (pulse duration of CLKIN low) for all output hold times.

SYNCHRONOUS-BURST MEMORY TIMING (CONTINUED)

timing requirements for synchronous-burst SRAM cycles (half-rate SSCLK) (see Figure 19)

NO.		-200		UNIT
		MIN	MAX	
7	$t_{su}(EDV-SSCLKH)$ Setup time, read EDx valid before SSCLK high	2.5		ns
8	$t_h(SSCLKH-EDV)$ Hold time, read EDx valid after SSCLK high	1.5		ns

switching characteristics over recommended operating conditions for synchronous-burst SRAM cycles[†] (half-rate SSCLK) (see Figure 19 and Figure 20)

NO.	PARAMETER	-200		UNIT
		MIN	MAX	
1	$t_{osu}(CEV-SSCLKH)$ Output setup time, \overline{CEx} valid before SSCLK high	1.5P – 3		ns
2	$t_{oh}(SSCLKH-CEV)$ Output hold time, \overline{CEx} valid after SSCLK high	0.5P – 1.5		ns
3	$t_{osu}(BEV-SSCLKH)$ Output setup time, \overline{BEx} valid before SSCLK high	1.5P – 3		ns
4	$t_{oh}(SSCLKH-BEIV)$ Output hold time, \overline{BEx} invalid after SSCLK high	0.5P – 1.5		ns
5	$t_{osu}(EAV-SSCLKH)$ Output setup time, EAx valid before SSCLK high	1.5P – 3		ns
6	$t_{oh}(SSCLKH-EAIV)$ Output hold time, EAx invalid after SSCLK high	0.5P – 1.5		ns
9	$t_{osu}(ADSV-SSCLKH)$ Output setup time, \overline{SSADS} valid before SSCLK high	1.5P – 3		ns
10	$t_{oh}(SSCLKH-ADSV)$ Output hold time, \overline{SSADS} valid after SSCLK high	0.5P – 1.5		ns
11	$t_{osu}(OEV-SSCLKH)$ Output setup time, \overline{SSOE} valid before SSCLK high	1.5P – 3		ns
12	$t_{oh}(SSCLKH-OEV)$ Output hold time, \overline{SSOE} valid after SSCLK high	0.5P – 1.5		ns
13	$t_{osu}(EDV-SSCLKH)$ Output setup time, EDx valid before SSCLK high	1.5P – 3		ns
14	$t_{oh}(SSCLKH-EDIV)$ Output hold time, EDx invalid after SSCLK high	0.5P – 1.5		ns
15	$t_{osu}(WEV-SSCLKH)$ Output setup time, \overline{SSWE} valid before SSCLK high	1.5P – 3		ns
16	$t_{oh}(SSCLKH-WEV)$ Output hold time, \overline{SSWE} valid after SSCLK high	0.5P – 1.5		ns

[†] When the PLL is used (CLKMODE x4), P = 1/CPU clock frequency in ns. For example, when running parts at 200 MHz, use P = 5 ns.

For CLKMODE x1:

1.5P = P + PH, where P = 1/CPU clock frequency, and PH = pulse duration of CLKIN high.

0.5P = PL, where PL = pulse duration of CLKIN low.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TMS320C6201GGP167	OBSOLETE	BGA	GGP	352		TBD	Call TI	Call TI
TMS320C6201GGP200	OBSOLETE	BGA	GGP	352		TBD	Call TI	Call TI
TMS320C6201GJC200	ACTIVE	FC/CSP	GJC	352	24	TBD	SN/PB	Level-4-220C-72HR
TMS320C6201GJCA200	ACTIVE	FC/CSP	GJC	352	24	TBD	SN/PB	Level-4-220C-72HR
TMS320C6201GJL200	ACTIVE	FC/CSP	GJL	352	40	TBD	SNPB	Level-4-220C-72HR
TMS320C6201GJLA200	ACTIVE	FC/CSP	GJL	352	40	TBD	SNPB	Level-4-220C-72HR
TMX320C6201BGJL	OBSOLETE	FC/CSP	GJL	352		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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