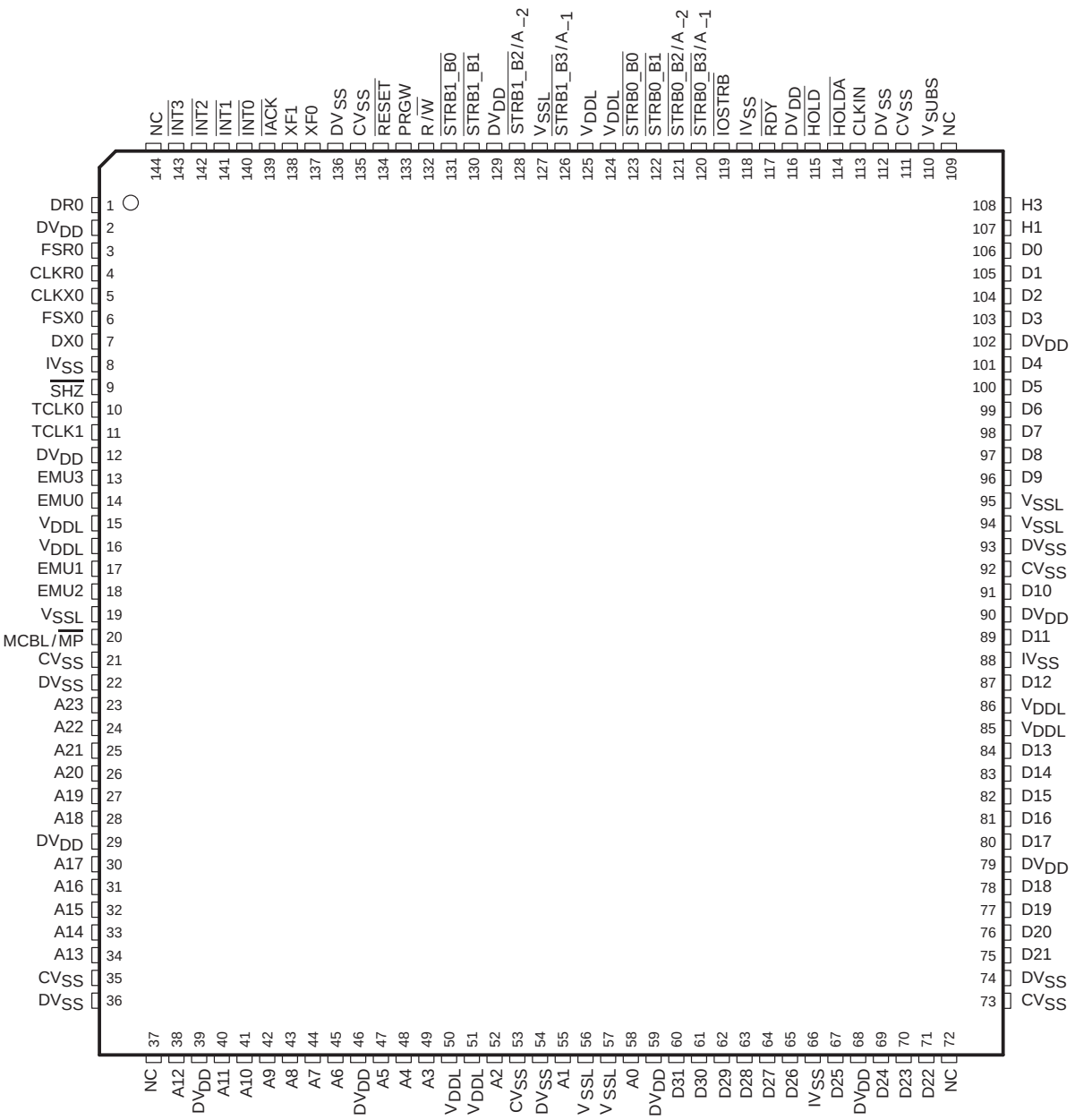
- **High-Performance Floating-Point DSP**
  - **TMS320C32-60 (5 V)**
    33-ns Instruction Cycle Time
    330 Million Operations Per Second (MOPS), 60 Million Floating-Point Operations Per Second (MFLOPS), 30 Million Instructions Per Second (MIPS)
  - **TMS320C32-50 (5 V)**
    40-ns Instruction Cycle Time
    275 MOPS, 50 MFLOPS, 25 MIPS
  - **TMS320C32-40 (5 V)**
    50-ns Instruction Cycle Time
    220 MOPS, 40 MFLOPS, 20 MIPS
- **32-Bit High-Performance CPU**
- **16-/32-Bit Integer and 32-/40-Bit Floating-Point Operations**
- **32-Bit Instruction Word, 24-Bit Addresses**
- **Two 256 × 32-Bit Single-Cycle, Dual-Access On-Chip RAM Blocks**
- **Flexible Boot-Program Loader**
- **On-Chip Memory-Mapped Peripherals:**
  - **One Serial Port**
  - **Two 32-Bit Timers**
  - **Two-Channel Direct Memory Access (DMA) Coprocessor With Configurable Priorities**
- **Enhanced External Memory Interface That Supports 8-/16-/32-Bit-Wide External RAM for Data Access and Program Execution From 16-/32-Bit-Wide External RAM**
- **TMS320C30 and TMS320C31 Object Code Compatible**
- **Fabricated using 0.7 μm Enhanced Performance Implanted CMOS (EPIC™) Technology by Texas Instruments (TI™)**
- **144-Pin Plastic Quad Flat Package (PCM Suffix) 5 V**
- **Eight Extended-Precision Registers**
- **Two Address Generators With Eight Auxiliary Registers and Two Auxiliary Register Arithmetic Units (ARAUs)**
- **Two Low-Power Modes**
- **Two- and Three-Operand Instructions**
- **Parallel Arithmetic Logic Unit (ALU) and Multiplier Execution in a Single Cycle**
- **Block-Repeat Capability**
- **Zero-Overhead Loops With Single-Cycle Branches**
- **Conditional Calls and Returns**
- **Interlocked Instructions for Multiprocessing Support**
- **One External Pin, PRGW, That Configures the External-Program-Memory Width to 16 or 32 Bits**
- **Two Sets of Memory Strobes ($\overline{\text{STRB0}}$ and $\overline{\text{STRB1}}$) and One I/O Strobe ($\overline{\text{IOSTRB}}$) Allow Zero-Glue Logic Interface to Two Banks of Memory and One Bank of External Peripherals**
- **Separate Bus-Control Registers for Each Strobe-Control Wait-State Generation, External Memory Width, and Data Type Size**
- **$\overline{\text{STRB0}}$ and $\overline{\text{STRB1}}$ Memory Strobes Handle 8-, 16-, or 32-Bit External Data Accesses (Reads and Writes)**
- **Multiprocessor Support Through the $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ Signals Is Valid for All Strobes**

description

The TMS320C32 is the newest member of the TMS320C3x generation of digital signal processors (DSPs) from Texas Instruments. The TMS320C32 is an enhanced 32-bit floating-point processor manufactured in 0.7-μm triple-level-metal CMOS technology. The enhancements to the TMS320C3x architecture include a variable-width external-memory interface, faster instruction cycle time, power-down modes, two-channel DMA coprocessor with configurable priorities, flexible boot loader, relocatable interrupt-vector table, and edge- or level-triggered interrupts.

pin assignments

PCM PACKAGE †
(TOP VIEW)



† NC=No internal connection

Pin Assignments

PIN NUMBER	PIN NAME	PIN NUMBER	PIN NAME	PIN NUMBER	PIN NAME	PIN NUMBER	PIN NAME	PIN NUMBER	PIN NAME
1	DR0	30	A17	59	DV_{DD}	88	IV_{SS}	117	$\overline{RDY}$
2	DV_{DD}	31	A16	60	D31	89	D11	118	IV_{SS}
3	FSR0	32	A15	61	D30	90	DV_{DD}	119	$\overline{IOSTRB}$
4	CLKR0	33	A14	62	D29	91	D10	120	$\overline{STRB0\_B3}/A_{-1}$
5	CLKX0	34	A13	63	D28	92	CV_{SS}	121	$\overline{STRB0\_B2}/A_{-2}$
6	FSX0	35	CV_{SS}	64	D27	93	DV_{SS}	122	$\overline{STRB0\_B1}$
7	DX0	36	DV_{SS}	65	D26	94	V_{SSL}	123	$\overline{STRB0\_B0}$
8	IV_{SS}	37	NC	66	IV_{SS}	95	V_{SSL}	124	V_{DDL}
9	$\overline{SHZ}$	38	A12	67	D25	96	D9	125	V_{DDL}
10	TCLK0	39	DV_{DD}	68	DV_{DD}	97	D8	126	$\overline{STRB1\_B3}/A_{-1}$
11	TCLK1	40	A11	69	D24	98	D7	127	V_{SSL}
12	DV_{DD}	41	A10	70	D23	99	D6	128	$\overline{STRB1\_B2}/A_{-2}$
13	EMU3	42	A9	71	D22	100	D5	129	DV_{DD}
14	EMU0	43	A8	72	NC	101	D4	130	$\overline{STRB1\_B1}$
15	V_{DDL}	44	A7	73	CV_{SS}	102	DV_{DD}	131	$\overline{STRB1\_B0}$
16	V_{DDL}	45	A6	74	DV_{SS}	103	D3	132	$R/\overline{W}$
17	EMU1	46	DV_{DD}	75	D21	104	D2	133	PRGW
18	EMU2	47	A5	76	D20	105	D1	134	$\overline{RESET}$
19	V_{SSL}	48	A4	77	D19	106	D0	135	CV_{SS}
20	$MCBL/\overline{MP}$	49	A3	78	D18	107	H1	136	DV_{SS}
21	CV_{SS}	50	V_{DDL}	79	DV_{DD}	108	H3	137	XF0
22	DV_{SS}	51	V_{DDL}	80	D17	109	NC	138	XF1
23	A23	52	A2	81	D16	110	V_{SUBS}	139	$\overline{IACK}$
24	A22	53	CV_{SS}	82	D15	111	CV_{SS}	140	$\overline{INT0}$
25	A21	54	DV_{SS}	83	D14	112	DV_{SS}	141	$\overline{INT1}$
26	A20	55	A1	84	D13	113	CLKIN	142	$\overline{INT2}$
27	A19	56	V_{SSL}	85	V_{DDL}	114	$\overline{HOLDA}$	143	$\overline{INT3}$
28	A18	57	V_{SSL}	86	V_{DDL}	115	$\overline{HOLD}$	144	NC
29	DV_{DD}	58	A0	87	D12	116	DV_{DD}		

pin functions

This section provides signal descriptions for the TMS320C32 device. The following table lists each signal, the number of pins, operating modes, and a brief signal description. The following table groups the signals according to their function.

TMS320C32 Pin Functions

PIN NAME	PIN NO.	TYPE†	DESCRIPTION	CONDITIONS WHEN SIGNAL IS IN HIGH Z‡
EXTERNAL-BUS INTERFACE (70 PINS)				
A23–A0	24	O/Z	24-bit address port of the external-bus interface	S H R
D31–D0	32	I/O/Z	32-bit data port of the external-bus interface	S H R
R/$\overline{W}$	1	O/Z	Read/write for external-memory interface. R/$\overline{W}$ is high when a read is performed and low when a write is performed over the parallel interface.	S H
$\overline{IOSTRB}$	1	O/Z	External-peripheral I/O strobe for the external-memory interface	S H
$\overline{STRB0\_B3}$/A–1	1	O/Z	External-memory access strobe 0, byte enable 3 for 32-bit external-memory interface, and address pin for 8-bit and 16-bit external-memory interface	S H
$\overline{STRB0\_B2}$/A–2	1	O/Z	External-memory access strobe 0, byte enable 2 for 32-bit external-memory interface, and address pin for 8-bit external-memory interface	S H
$\overline{STRB0\_B1}$	1	O/Z	External-memory access strobe 0, byte enable 1 for the external-memory interface	S H
$\overline{STRB0\_B0}$	1	O/Z	External-memory access strobe 0, byte enable 0 for the external-memory interface	S H
$\overline{STRB1\_B3}$/A–1	1	O/Z	External-memory access strobe 1, byte enable 3 for 32-bit external-memory interface, and address pin for 8-bit and 16-bit external-memory interface	S H
$\overline{STRB1\_B2}$/A–2	1	O/Z	External-memory access strobe 1, byte enable 2 for 32-bit external-memory interface, and address pin for 8-bit external-memory interface	S H
$\overline{STRB1\_B1}$	1	O/Z	External-memory access strobe 1, byte enable 1 for the external-memory interface	S H
$\overline{STRB1\_B0}$	1	O/Z	External-memory access strobe 1, byte enable 0 for the external-memory interface	S H
$\overline{RDY}$	1	I	Ready. $\overline{RDY}$ indicates that the external device is prepared for an external-memory interface transaction to complete.	
$\overline{HOLD}$	1	I	Hold signal for external-memory interface. When $\overline{HOLD}$ is a logic low, any ongoing transaction is completed. A23–A0, D31–D0, $\overline{IOSTRB}$, $\overline{STRB0\_Bx}$, $\overline{STRB1\_Bx}$, and R/$\overline{W}$ are placed in the high-impedance state, and all transactions over the external-memory interface are held until $\overline{HOLD}$ becomes a logic high or the NOHOLD bit of the STRB0 bus-control register is set.	
$\overline{HOLDA}$	1	O/Z	Hold acknowledge for external-memory interface. $\overline{HOLDA}$ is generated in response to a logic low on $\overline{HOLD}$. $\overline{HOLDA}$ indicates that A23–A0, D31–D0, $\overline{IOSTRB}$, $\overline{STRB0\_Bx}$, $\overline{STRB1\_Bx}$, and R/$\overline{W}$ are in the high-impedance state and that all transactions over the memory are held. $\overline{HOLDA}$ is high in response to a logic high of $\overline{HOLD}$ or when the NOHOLD bit of the external bus-control register is set.	S
PRGW	1	I	Program memory width select. When PRGW is a logic low, program is fetched as a single 32-bit word. When PRGW is a logic high, two 16-bit program fetches are performed to fetch a single 32-bit instruction word. The status of PRGW at device reset affects the reset value of the STRB0 and STRB1 bus-control register.	
A23–A0	24	O/Z	24-bit address port of the external-bus interface	S H R

† I = input, O = output, Z = high-impedance state
‡ S = $\overline{SHZ}$ active, H = $\overline{HOLD}$ active, R = $\overline{RESET}$ active

TMS320C32 Pin Functions (Continued)

PIN NAME	PIN NO.	TYPE†	DESCRIPTION	CONDITIONS WHEN SIGNAL IS IN HIGH Z‡
CONTROL SIGNALS (9 PINS)				
$\overline{\text{RESET}}$	1	I	Reset. When $\overline{\text{RESET}}$ is a logic low, the device is in the reset condition. When $\overline{\text{RESET}}$ becomes a logic high, execution begins from the location specified by the reset vector.	
$\overline{\text{INT3}}$–$\overline{\text{INT0}}$	4	I	External interrupts	
$\overline{\text{IACK}}$	1	O/Z	Interrupt acknowledge. $\overline{\text{IACK}}$ is generated by the IACK instruction. This signal can be used to indicate the beginning or end of an interrupt-service routine.	S
MCBL/$\overline{\text{MP}}$	1	I	Microcomputer boot loader/microprocessor mode	
XF1–XF0	2	I/O/Z	External flags. XF1 and XF0 are used as general-purpose I/Os or used to support interlocked-processor instructions.	S R
SERIAL PORT SIGNALS (6 PINS)				
CLKX0	1	I/O/Z	Serial-port 0 transmit clock. CLKX0 is the serial shift clock for the serial port 0 transmitter.	S R
DX0	1	I/O/Z	Data-transmit output. Serial port 0 transmits serial data on DX0.	S R
FSX0	1	I/O/Z	Frame-synchronization pulse for transmit. The FSX0 pulse initiates the transmit-data process over DX0.	S R
CLKR0	1	I/O/Z	Serial-port 0 receive clock. CLKR0 is the serial-shift clock for the serial-port 0 receiver.	S R
DR0	1	I/O/Z	Data receive. Serial port 0 receives serial data on DR0.	S R
FSR0	1	I/O/Z	Frame-synchronization pulse for receive. The FSR0 pulse initiates the receive-data process over DR0.	S R
TIMER SIGNALS (2 PINS)				
TCLK0	1	I/O/Z	Timer clock 0. As an input, TCLK0 is used by timer 0 to count external pulses. As an output, TCLK0 outputs pulses generated by timer 0.	S R
TCLK1	1	I/O/Z	Timer clock 1. As an input, TCLK1 is used by timer 1 to count external pulses. As an output, TCLK1 outputs pulses generated by timer 1.	S R
CLOCK SIGNALS (3 PINS)				
CLKIN	1	I	Input to the internal oscillator from an external clock source	
H1	1	O/Z	External H1 clock. H1 has a period equal to twice CLKIN.	S
H3	1	O/Z	External H3 clock. H3 has a period equal to twice CLKIN.	S
RESERVED (5 PINS)				
EMU0–EMU2	3	I	Reserved for emulation. Use 18 kΩ–22 kΩ pullup resistors to 5 V.	
EMU3	1	O/Z	Reserved for emulation	S
$\overline{\text{SHZ}}$	1	I	Shutdown high impedance. When active, $\overline{\text{SHZ}}$ shuts down the ’C32 and places all 3-state I/O pins in the high-impedance state. $\overline{\text{SHZ}}$ is used for board-level testing to ensure that no dual-drive conditions occur. **CAUTION:** A low on $\overline{\text{SHZ}}$ corrupts ’C32 memory and register contents. Reset the device with $\overline{\text{SHZ}}$ high to restore it to a known operating condition.	

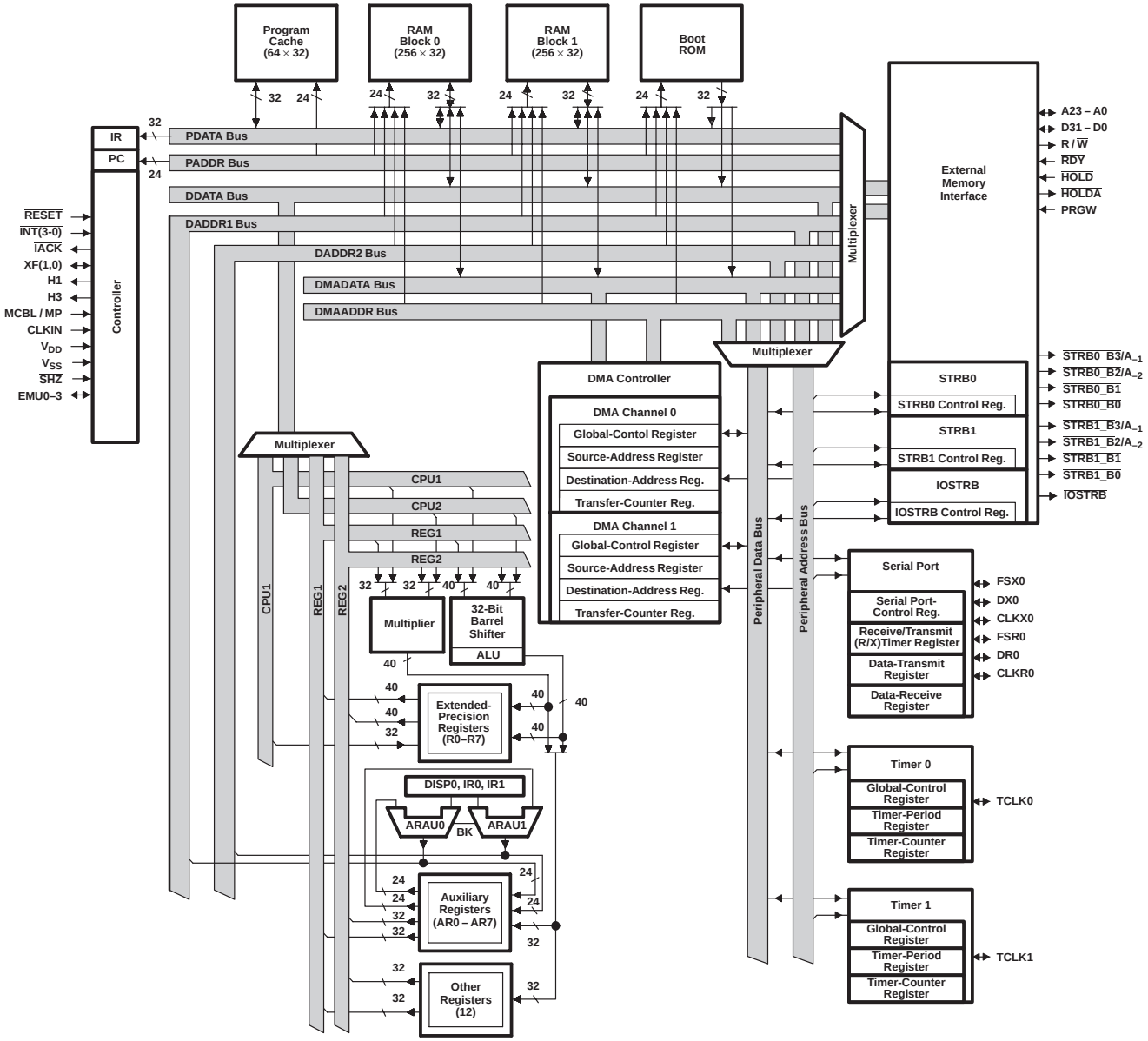
† I = input, O = output, Z = high-impedance state
‡ S = $\overline{\text{SHZ}}$ active, H = $\overline{\text{HOLD}}$ active, R = $\overline{\text{RESET}}$ active

TMS320C32 Pin Functions (Continued)

PIN NAME	PIN NO.	TYPE†	DESCRIPTION	CONDITIONS WHEN SIGNAL IS IN HIGH Z‡
POWER / GROUND				
CV_{SS}	7	I	Ground	
DV_{SS}	7	I	Ground	
IV_{SS}	4	I	Ground	
DV_{DD}	12	I	+ 5-V dc supply§	
V_{DDL}	8	I	+ 5-V dc supply§	
V_{SSL}	6	I	Ground	
V_{SUBS}	1	I	Substrate, tie to ground	

† I = input, O = output, Z = high-impedance state
‡ S = SHZ active, H = HOLD active, R = RESET active
§ Recommended decoupling capacitor is 0.1 μF.

functional block diagram



operation

Operation of the TMS320C32 is identical to the TMS320C30 and TMS320C31 digital signal processors, with the exception of an enhanced external memory interface and the addition of two CPU power-management modes.

external-memory interface

The TMS320C32 has a configurable external-memory interface with a 24-bit address bus, a 32-bit data bus, and three independent multifunction strobes. The flexibility of this unique interface enables product designers to minimize external-memory chip count.

external memory interface (continued)

Up to three mutually exclusive memory areas (one program area and two data areas) can be implemented. Each memory area configuration is independent of the physical memory width and independent of the configuration of other memory areas. See Figure 1.

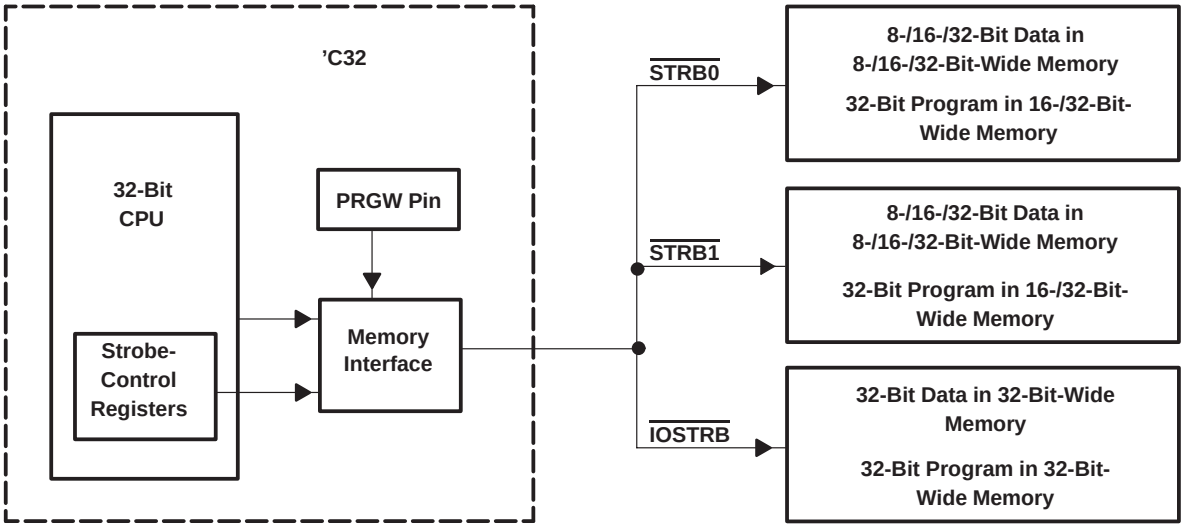


Figure 1. 'C32 External Memory Interface

The TMS320C32's external-memory configuration is controlled by a combination of hardware configuration and memory-mapped control registers and can be reconfigured dynamically. The signals that control external-memory configuration are the PRGW, $\overline{\text{STRB0}}$, $\overline{\text{STRB1}}$, and $\overline{\text{IOSTRB}}$. The signals work as follows:

- The TMS320C32 is a 32-bit microprocessor, that is, the CPU operates on 32-bit program words. The external-memory interface provides the capability of fetching instructions as either 32-bit words or two 16-bit half words from consecutive addresses. Program memory width is 16 bits if the PRGW signal is high, 32 bits if the PRGW signal is low.
- $\overline{\text{STRB0}}$ and $\overline{\text{STRB1}}$ are sets of control signals, four signals each, that are mapped to specific ranges of external-memory addresses. When an address within one of these ranges is accessed by a read or write instruction (CPU or DMA), the corresponding set of control signals is activated. Figure 8 illustrates the TMS320C32 memory map, showing the address ranges for which the strobe signals become active.

The behavior of the $\overline{\text{STRB0}}$ and $\overline{\text{STRB1}}$ control signals is determined by the contents of the $\overline{\text{STRB0}}$ and $\overline{\text{STRB1}}$ control registers.

The $\overline{\text{STRB0}}$ and $\overline{\text{STRB1}}$ control registers each have a field that specifies the physical memory width (8, 16, or 32 bits) of the external-memory address ranges they control. Another field specifies the data width (8, 16, or 32 bits) of the data contained in those addresses. The values in these fields are not required to match. For example, a 32-bit-wide physical memory space can be configured to segment each 32-bit word into four consecutive 8-bit locations, each having its own address.

Each control-signal set has two pins ($\overline{\text{STRBx\_B2}}$/A_2 and $\overline{\text{STRBx\_B3}}$/A_1) that can act as either byte-enable (chip-select) pins or address pins, and two dedicated byte-enable (chip-select) pins ($\overline{\text{STRBx\_B0}}$ and $\overline{\text{STRBx\_B1}}$). The pin functions are determined by the physical memory width specified in the corresponding control register.

external memory interface (continued)

- For 8-bit-wide physical memory, the $\overline{\text{STRBx\_B2}}$/A_2 and $\overline{\text{STRBx\_B3}}$/A_1 pins function as address pins (least significant address bits) and the $\overline{\text{STRBx\_B0}}$ pin functions as a byte-enable (chip-select) pin. $\overline{\text{STRBx\_B1}}$ is unused. See Figure 2.

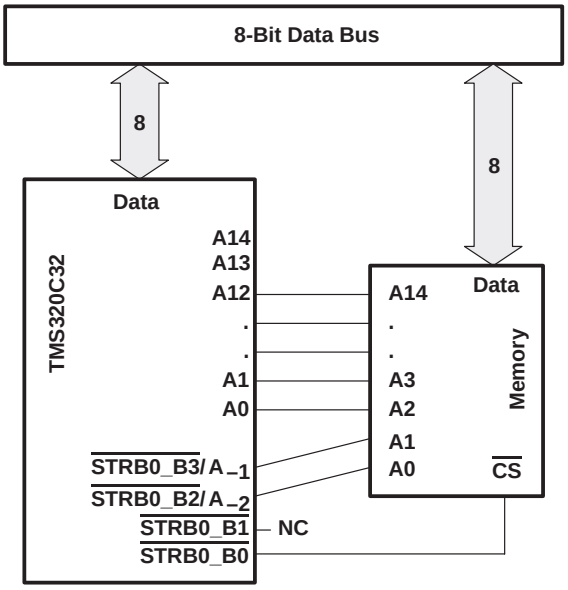


Figure 2. ’C32 With 8-Bit-Wide External Memory

- For 16-bit-wide physical memory, the $\overline{\text{STRBx\_B3}}$/A_1 pin functions as an address pin (least significant address bits). The $\overline{\text{STRBx\_B0}}$ and $\overline{\text{STRBx\_B1}}$ pins function as byte-enable (chip-select) pins. $\overline{\text{STRBx\_B2}}$/A_2 is unused. See Figure 3.

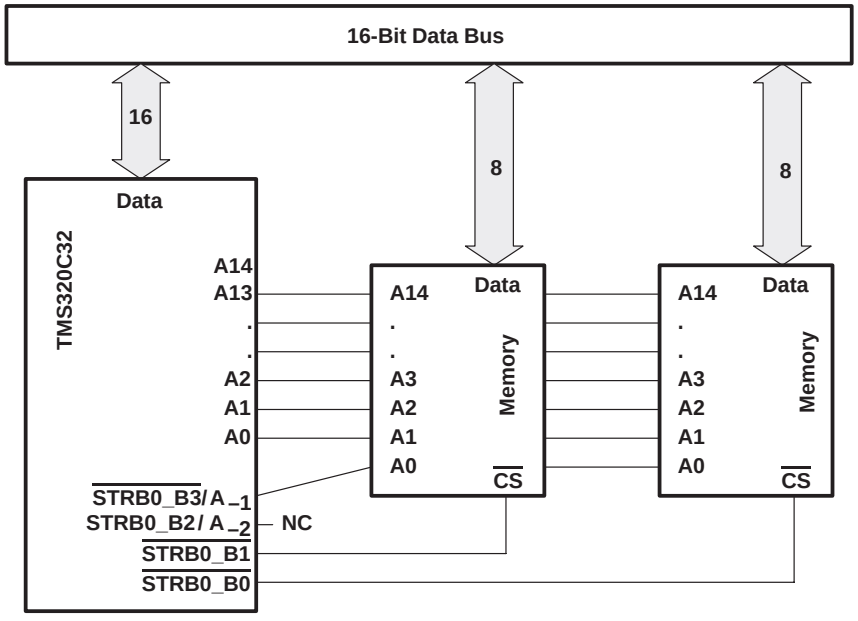


Figure 3. ’C32 With 16-Bit-Wide External Memory

external memory interface (continued)

- For 32-bit-wide physical memory, all $\overline{\text{STRB0}}$ and $\overline{\text{STRB1}}$ pins function as byte-enable (chip-select) pins. See Figure 4.

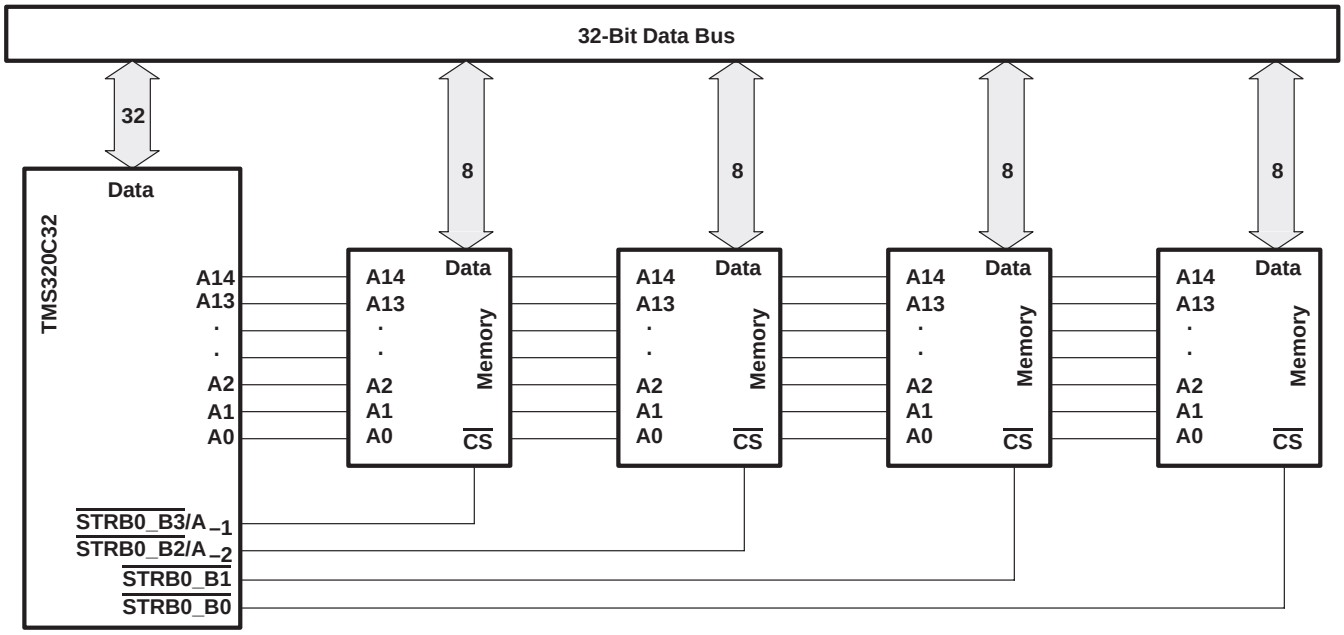


Figure 4. ’C32 With 32-Bit-Wide External Memory

For more detailed information and examples see *TMS320C32 Addendum to the TMS320C3x User’s Guide* (literature number SPRU132) and *Interfacing Memory to the TMS320C32 DSP Application Report* (literature number SPRA040).

- The $\overline{\text{IOSTRB}}$ control signal, like $\overline{\text{STRB0}}$ and $\overline{\text{STRB1}}$, also is mapped to a specific range of addresses but it is a single signal that can access only 32-bit data from 32-bit-wide memory. Its range of addresses appears in the TMS320C32 memory map, shown in Figure 8. The $\overline{\text{IOSTRB}}$ bus timing is different from the $\overline{\text{STRB0}}$ and $\overline{\text{STRB1}}$ bus timings to accommodate slower I/O peripherals.

external memory interface (continued)

examples

Figure 5 and Figure 6 show examples of external memory configurations that can be implemented using the TMS320C32 external memory interface. The first example has a 32-bit-wide external memory with 8- and 16-bit data areas and a 32-bit program area.

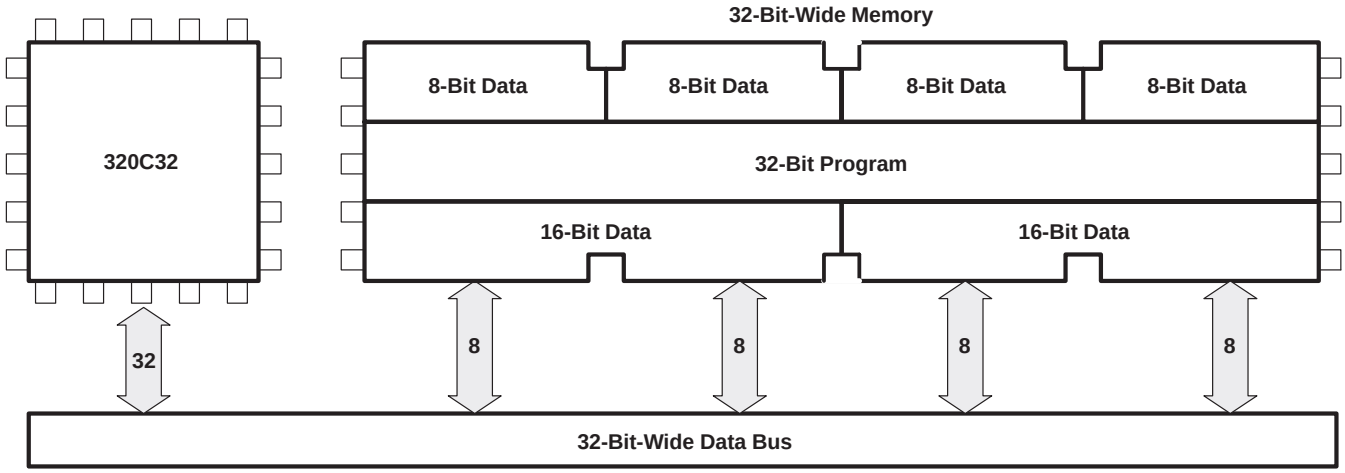


Figure 5. 32-Bit-Wide External Memory Configured With 8- and 16-Bit Data Areas and 32-Bit Program Memory

Figure 6 shows a configuration that can be implemented with 16-bit external memory. The 32-bit data and program words can be stored and retrieved as half-words.

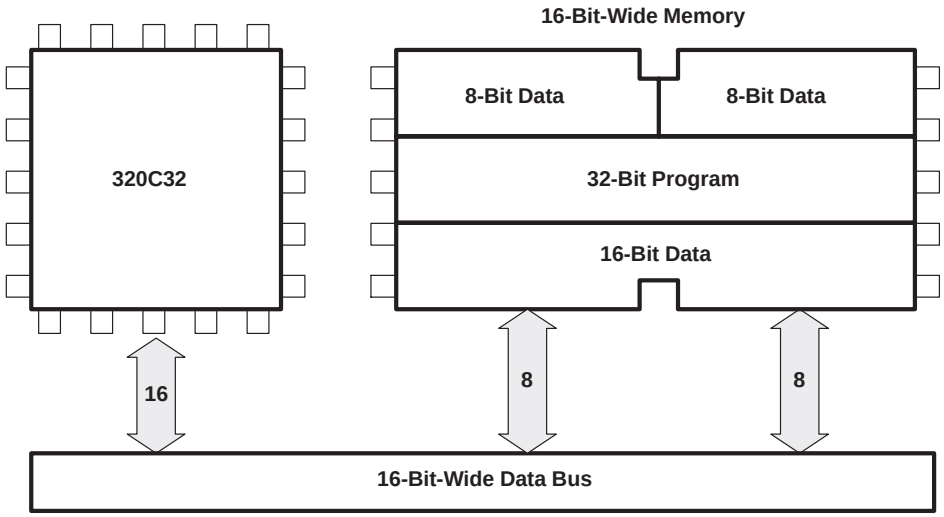


Figure 6. 16-Bit-Wide External Memory Configured With 8- and 16-Bit Data Areas and a 32-Bit Program Area

external memory interface (continued)

Figure 7 shows one possible configuration that can be implemented with 8-bit external memory. Program words, which are 32-bit, cannot be executed from 8-bit-wide memory.

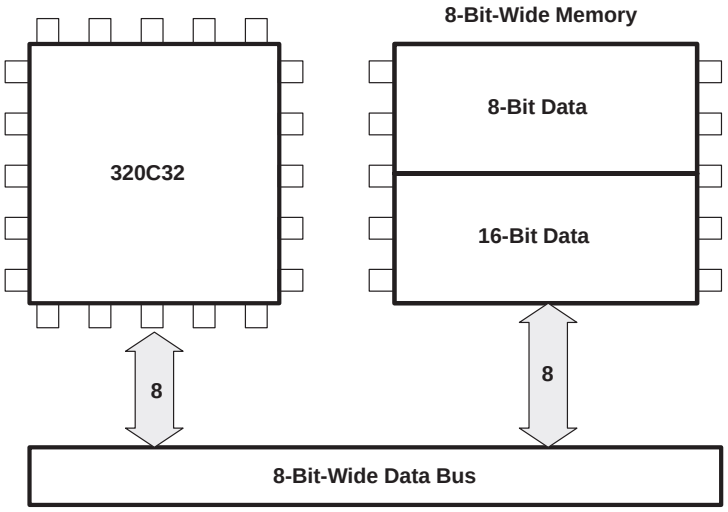


Figure 7. 8-Bit-Wide External Memory Configured With 8- and 16-Bit Data Areas

memory map

Figure 8 depicts the memory map for the TMS320C32. Refer to theTMS320C32 Addendum to the *TMS320C3x User's Guide* (literature number SPRU132) for a detailed description of this memory mapping, with shading to indicate external memory.

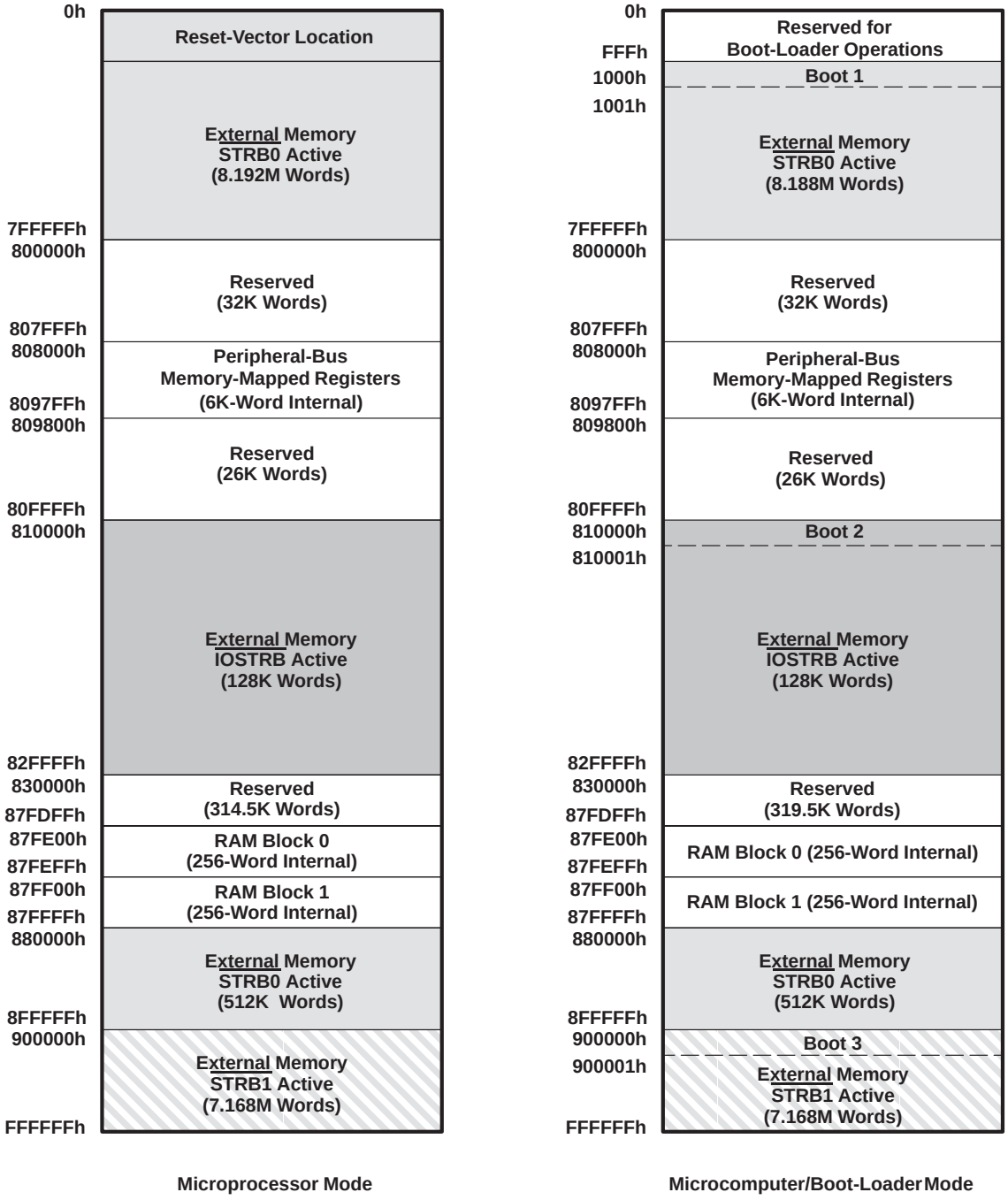


Figure 8. TMS320C32 Memory Map

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TMS320C32PCM40	ACTIVE	QFP	PCM	144	24	TBD	CU SNPB	Level-4-220C-72HR
TMS320C32PCM50	ACTIVE	QFP	PCM	144	24	TBD	CU SNPB	Level-4-220C-72HR
TMS320C32PCM60	ACTIVE	QFP	PCM	144	24	TBD	CU SNPB	Level-4-220C-72HR
TMS320C32PCMA40	ACTIVE	QFP	PCM	144	24	TBD	CU SNPB	Level-4-220C-72HR
TMS320C32PCMA50	ACTIVE	QFP	PCM	144	24	TBD	CU SNPB	Level-4-220C-72HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.