TLV707xx, TLV707xxP 200-mA, Low-I_Q, Low-Noise, Low-Dropout Regulator for Portable Devices

1 Features

- 0.5% Typical Accuracy
- Supports 200-mA Output
- Low I_Q: 25 µA
- Fixed-Output Voltage Combinations Possible from 0.85 V to 5.0 V(1)
- High PSRR:
  - 70 dB at 100 Hz
  - 50 dB at 1 MHz
- Stable With Effective Capacitance of 0.1 µF(2)
- Thermal Shutdown and Overcurrent Protection
- Package: 1-mm × 1-mm DFN (X2SON)

(1) For all available voltage options, see the orderable addendum at the end of the data sheet.

(2) See *Mechanical, Packaging, and Orderable Information* for more details.

2 Applications

- Wireless Handsets, Smart Phones, and PDAs
- MP3 Players and Other Handheld Devices
- WLAN and Other PC Add-On Cards

3 Description

The TLV707 series (TLV707xx and TLV707xxP) of low-dropout linear regulators (LDOs) are low quiescent current devices with excellent line and load transient performance for power-sensitive applications. These devices provide a typical accuracy of 0.5%. All versions have thermal shutdown and overcurrent protection for safety.

Furthermore, these devices are stable with an effective output capacitance of only 0.1 µF. This feature enables the use of cost-effective capacitors that have higher bias voltages and temperature derating. These devices also regulate to the specified accuracy with no output load.

The TLV707xxP also provides an active pulldown circuit to quickly discharge the outputs.

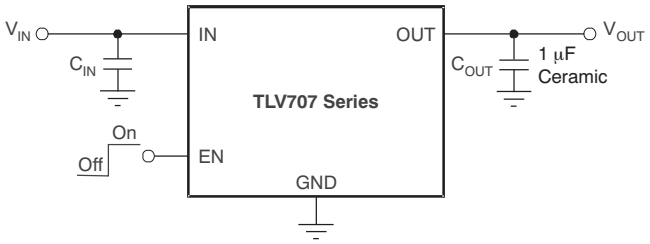
These LDOs also provide an active pulldown circuit to quickly discharge the outputs. The TLV707 series of LDOs are available in a 1-mm x 1-mm DQN (X2SON) package that makes them ideal for handheld applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV707xx	X2SON (4)	1.00 mm × 1.00 mm
TLV707xxP		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Typical Application Circuit (Fixed-Voltage Versions)



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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (November 2012) to Revision D — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed references to *DFN (SON)* package to *DQN (X2SON)* throughout document ... 1
- Changed Features list bullets ... 1
- Changed fourth paragraph of Description section ... 1
- Changed Pin Descriptions table contents ... 4
- Changed *Overview* section ... 17
- Changed *Internal Current Limit* section ... 18
- Changed *Input and Output Capacitor Requirements* section ... 20

Changes from Revision B (October 2011) to Revision C — **Page**

- Changed voltage range in fourth *Features* bullet ... 1
- Changed front page pinout drawing ... 1
- Changed *Output voltage range* parameter minimum specification in Electrical Characteristics table ... 6
- Changed *DC output accuracy* parameter test conditions in Electrical Characteristics table ... 6
- Changed voltage range in footnote 2 of Ordering Information table ... 25

Changes from Revision A (August 2011) to Revision B — **Page**

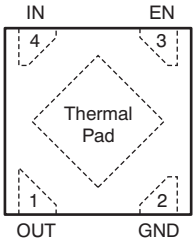
- Deleted reference to DCK package from Features ... 1
- Deleted DCK package pinout drawing ... 1
- Deleted column for DCK package from Pin Descriptions table ... 4
- Deleted DCK package from Thermal Information table ... 5

Changes from Original (February 2011) to Revision A **Page**

- Added footnote to Features to show available voltage options 1
- Added preview banner over DCK pinout drawing 1

6 Pin Configuration and Functions

DQN PACKAGE
X2SON-4
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	3	I	Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode. For TLV707xxP, output voltage is discharged through an internal 120-Ω resistor when device is shut down.
GND	2	—	Ground pin
IN	4	I	Input pin. For good transient performance, place a small 1-µF ceramic capacitor from this pin to ground. See *Input and Output Capacitor Requirements* for more details.
OUT	1	O	Regulated output voltage pin. A small 1-µF ceramic capacitor is required from this pin to ground to assure stability. See *Input and Output Capacitor Requirements* for more details.

7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	IN	–0.3	6.0	V
	EN	–0.3	6.0	V
	OUT	–0.3	6.0	V
Current (source)	OUT	Internally limited		
Output short-circuit duration		Indefinite		
Temperature	Operating junction, T_J	–55	150	°C
	Storage, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM) QSS 009-105 (JESD22-A114A)(1)	±2000	V
		Charged device model (CDM) QSS 009-147 (JESD22-C101B.01)(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_I	Input voltage	2.0		5.5	V
I_O	Output current	0		200	mA
T_J	Operating junction temperature range	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TLV707xx, TLV707xxP DFN (X2SON) 4 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	249.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.0	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

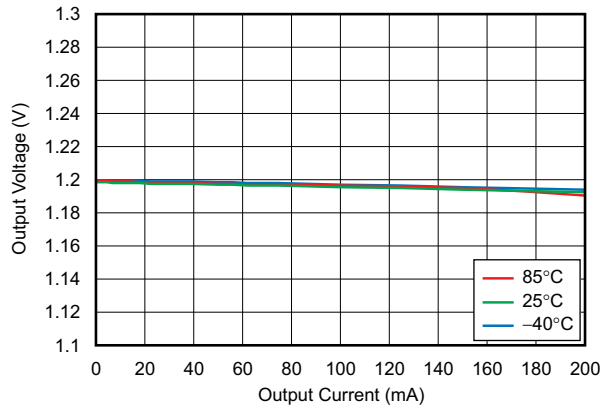
At V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater); I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 0.47 µF, and T_A = –40°C to 85°C, unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range				2		5.5	V
V_{OUT}	Output voltage range				0.85		5	V
	DC output accuracy	T_A = 25°C				0.5%		
		V_{OUT} ≥ 0.85 V, T_A = –40°C to 85°C			–1.5%		+1.5%	
$\Delta V_{O(\Delta VI)}$	Line regulation					1	5	mV
$\Delta V_{O(\Delta IO)}$	Load regulation	0 mA ≤ I_{OUT} ≤ 150 mA				10	20	mV
$V_{(DO)}$	Dropout voltage	V_{IN} = 0.98 x $V_{OUT(nom)}$	2.0 V < V_{OUT} ≤ 2.4 V	I_{OUT} = 30 mA		65		mV
				I_{OUT} = 150 mA		325	360	
			2.4 V < V_{OUT} ≤ 2.8 V	I_{OUT} = 30 mA		50		
				I_{OUT} = 150 mA		250	300	
			2.8 V < V_{OUT} ≤ 3.3 V	I_{OUT} = 30 mA		45		
				I_{OUT} = 150 mA		220	270	
			3.3 V < V_{OUT} ≤ 5.0 V	I_{OUT} = 30 mA		40		
				I_{OUT} = 150 mA		200	250	
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(nom)}$			240	300	450	mA
$I_{(GND)}$	Ground pin current	I_{OUT} = 0 mA				25	50	µA
$I_{(EN)}$	EN pin current	V_{EN} = 5.5 V				0.01		µA
$I_{SHUTDOWN}$	Shutdown current	V_{EN} ≤ 0.4 V, 2.0 V ≤ V_{IN} ≤ 4.5 V				1		µA
$V_{IL(EN)}$	EN pin low-level input voltage (disable device)				0		0.4	V
$V_{IH(EN)}$	EN pin high-level input voltage (enable device)				0.9		V_{IN}	V
PSRR	Power-supply rejection ratio	V_{IN} = 3.3 V, V_{OUT} = 2.8 V, I_{OUT} = 30 mA		f = 100 Hz		70		dB
				f = 10 kHz		55		
				f = 1 MHz		50		
V_n	Output noise voltage	BW = 100 Hz to 100 kHz, V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA				45		μV_{RMS}
t_{STR}	Startup time (1)	C_{OUT} = 1.0 µF, I_{OUT} = 150 mA				100		µs
UVLO	Undervoltage lockout	V_{IN} rising				1.9		V
$R_{PULLDOWN}$	Pulldown resistance (TLV707xxP only)					120		Ω
T_J	Operating junction temperature				–40		125	°C

(1) Startup time = time from EN assertion to 0.98 × Vout.

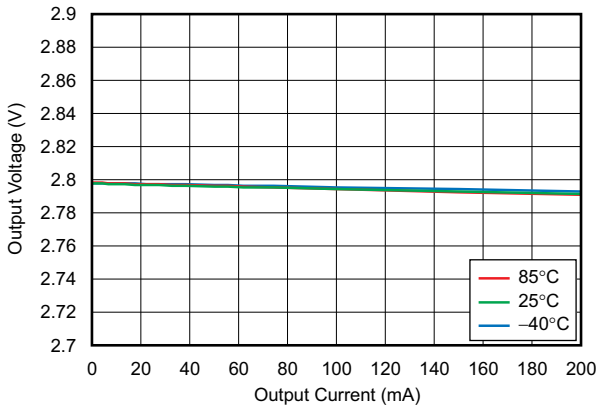
7.6 Typical Characteristics

At T_J = –40°C to 85°C, $V_I = V_{O(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_O = 10 mA, $V_{EN} = V_I$, and C_{OUT} = 1 µF, unless otherwise noted. Typical values are at T_J = 25°C.



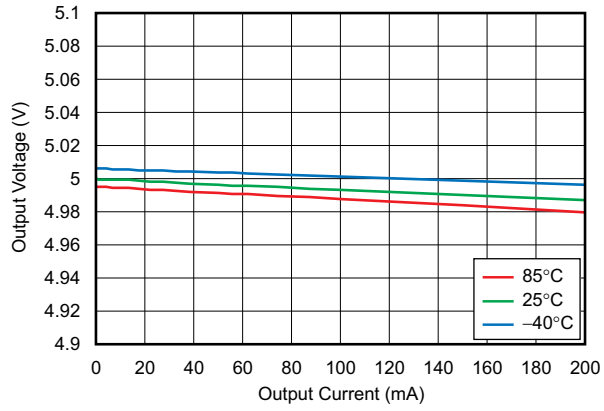
V_O = 1.2 V

Figure 1. Load Regulation



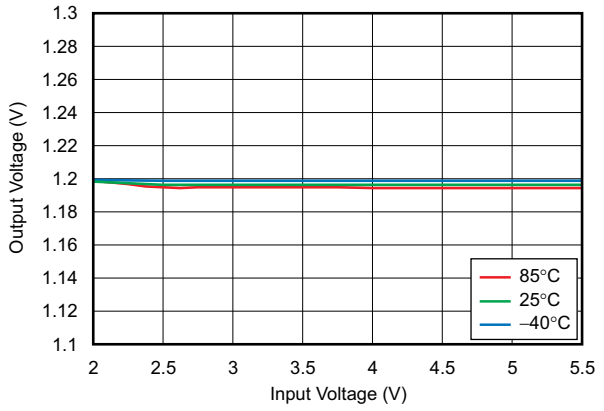
V_O = 2.8 V

Figure 2. Load Regulation



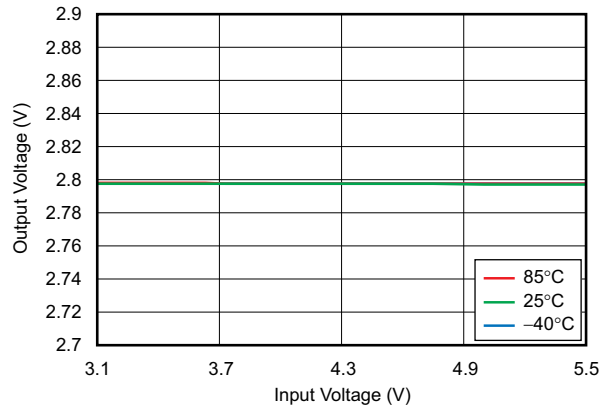
V_O = 5.0 V

Figure 3. Load Regulation



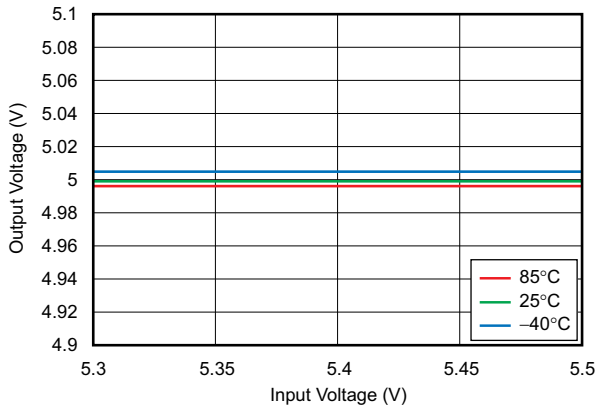
V_O = 1.2 V I_O = 10 mA

Figure 4. Line Regulation



V_O = 2.8 V I_O = 10 mA

Figure 5. Line Regulation

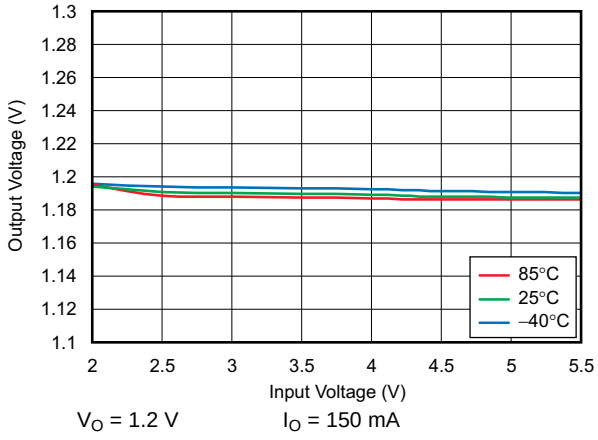


V_O = 5.0 V I_O = 10 mA

Figure 6. Line Regulation

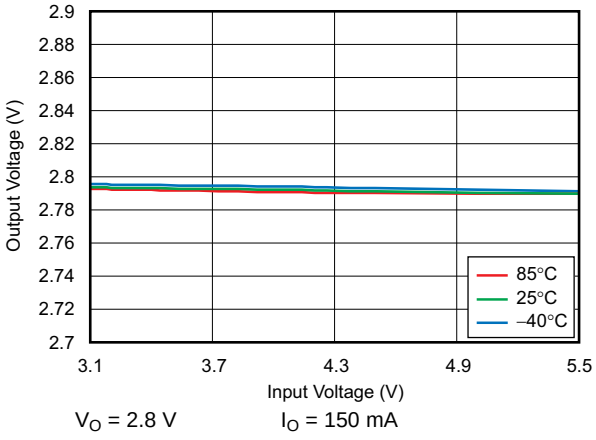
Typical Characteristics (continued)

At T_J = –40°C to 85°C, $V_I = V_{O(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_O = 10 mA, $V_{EN} = V_I$, and C_{OUT} = 1 µF, unless otherwise noted. Typical values are at T_J = 25°C.



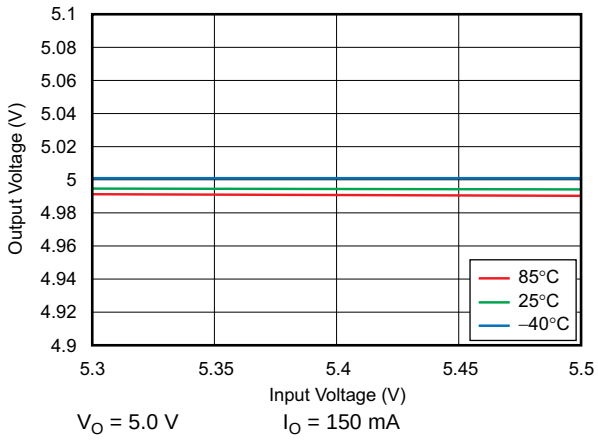
V_O = 1.2 V I_O = 150 mA

Figure 7. Line Regulation



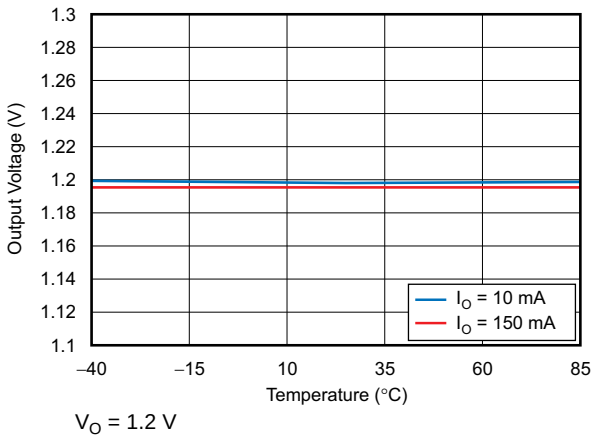
V_O = 2.8 V I_O = 150 mA

Figure 8. Line Regulation



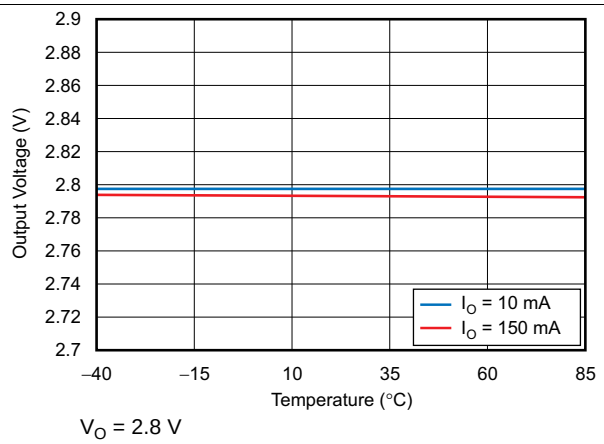
V_O = 5.0 V I_O = 150 mA

Figure 9. Line Regulation



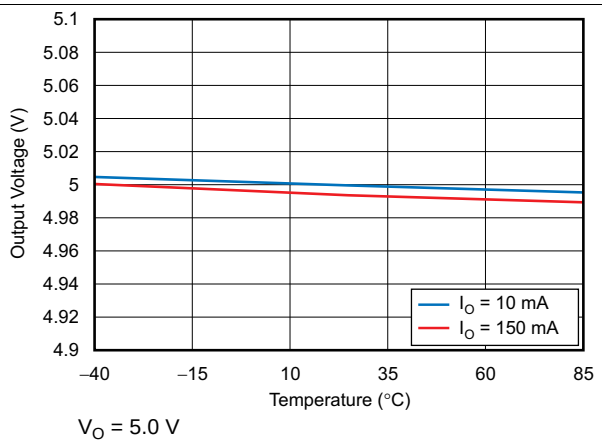
V_O = 1.2 V

Figure 10. Output Voltage vs Temperature



V_O = 2.8 V

Figure 11. Output Voltage vs Temperature

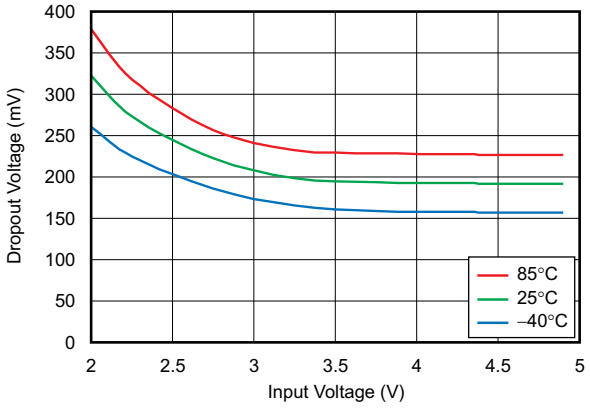


V_O = 5.0 V

Figure 12. Output Voltage vs Temperature

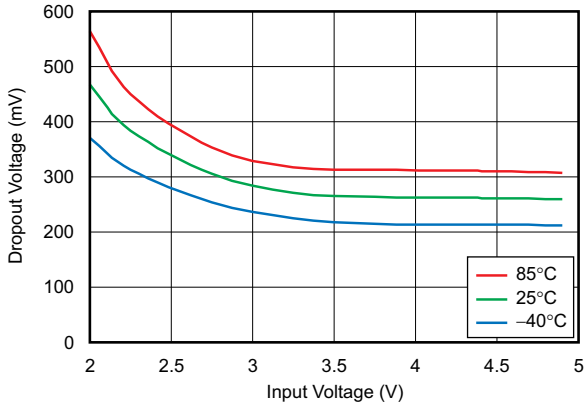
Typical Characteristics (continued)

At T_J = –40°C to 85°C, $V_I = V_{O(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_O = 10 mA, $V_{EN} = V_I$, and C_{OUT} = 1 µF, unless otherwise noted. Typical values are at T_J = 25°C.



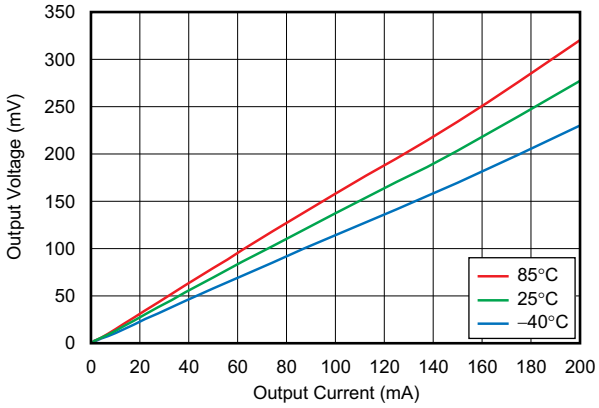
I_O = 150 mA

Figure 13. Dropout Voltage vs Input Voltage



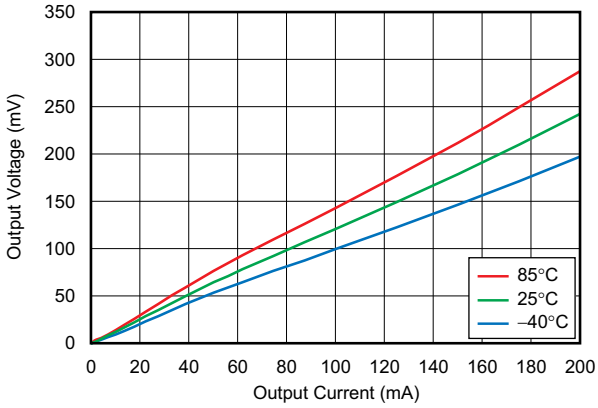
I_O = 200 mA

Figure 14. Dropout Voltage vs Input Voltage



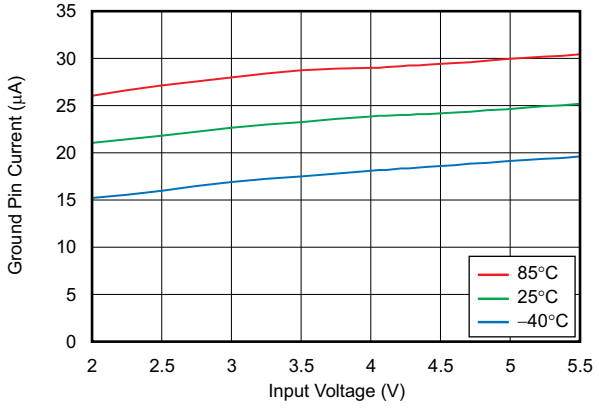
V_O = 2.8 V

Figure 15. Dropout Voltage vs Output Current



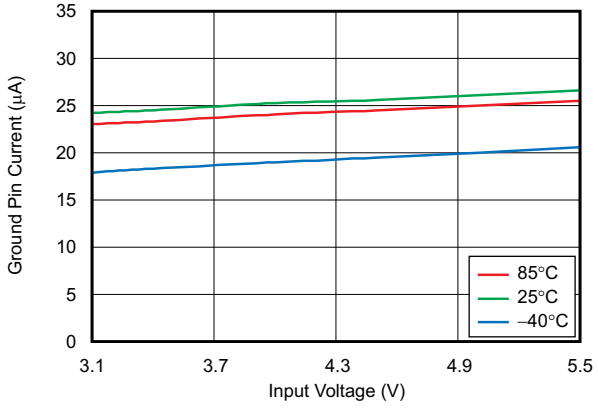
V_O = 5.0 V

Figure 16. Dropout Voltage vs Output Current



V_O = 1.2 V I_O = 0 mA

Figure 17. Ground Pin Current vs Input Voltage

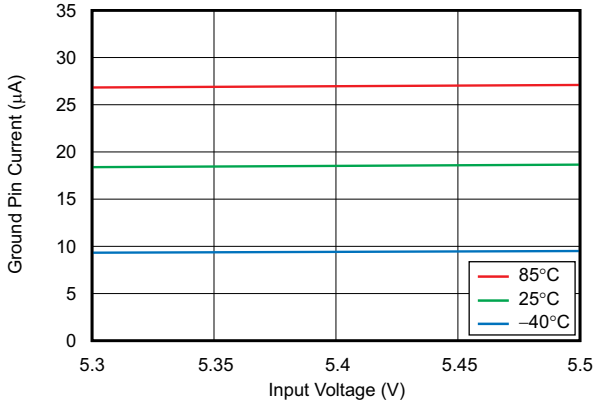


V_O = 2.8 V I_O = 0 mA

Figure 18. Ground Pin Current vs Input Voltage

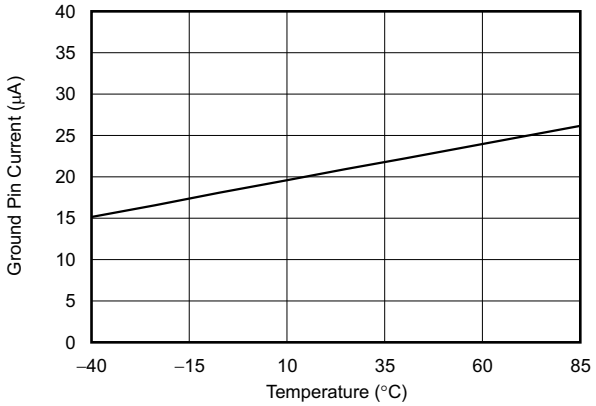
Typical Characteristics (continued)

At T_J = –40°C to 85°C, $V_I = V_{O(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_O = 10 mA, $V_{EN} = V_I$, and C_{OUT} = 1 µF, unless otherwise noted. Typical values are at T_J = 25°C.



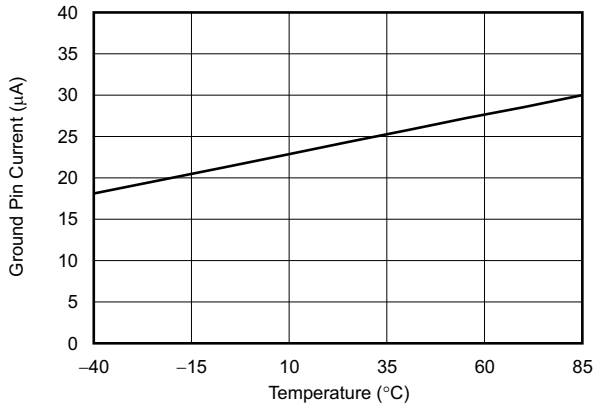
V_O = 5.0 V I_O = 0 mA

Figure 19. Ground Pin Current vs Input Voltage



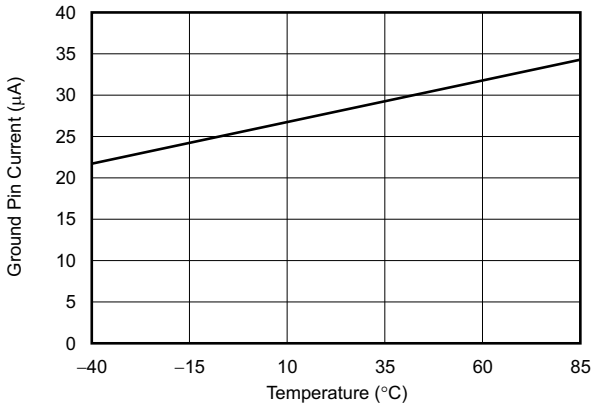
V_O = 1.2 V I_O = 0 mA

Figure 20. Ground Pin Current vs Temperature



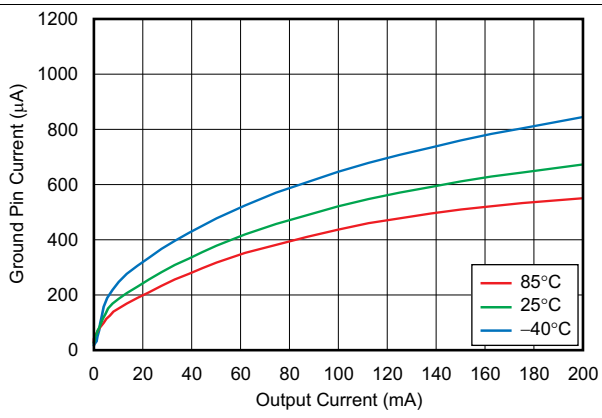
V_O = 2.8 V I_O = 0 mA

Figure 21. Ground Pin Current vs Temperature



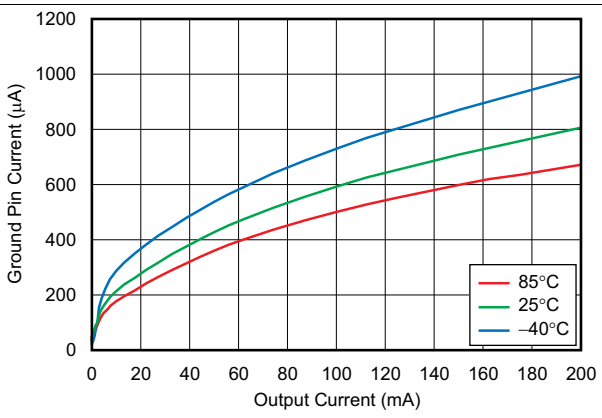
V_O = 5.0 V I_O = 0 mA

Figure 22. Ground Pin Current vs Temperature



V_O = 1.2 V

Figure 23. Ground Pin Current vs Output Current

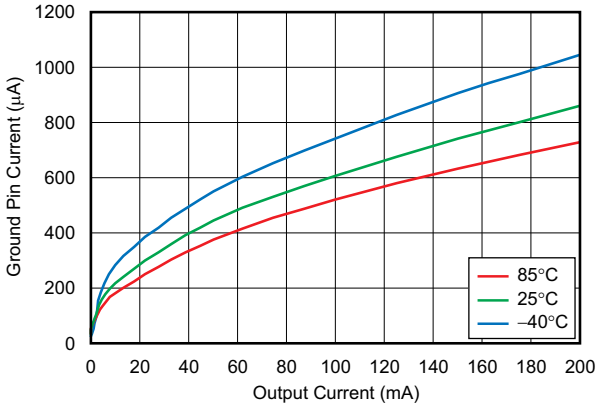


V_O = 2.8 V

Figure 24. Ground Pin Current vs Output Current

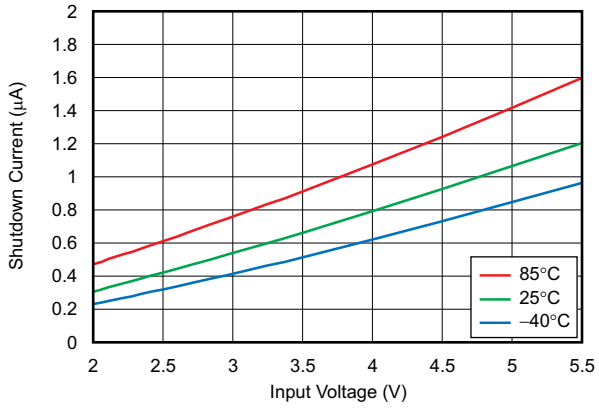
Typical Characteristics (continued)

At T_J = –40°C to 85°C, V_I = $V_{O(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_O = 10 mA, V_{EN} = V_I, and C_{OUT} = 1 µF, unless otherwise noted. Typical values are at T_J = 25°C.



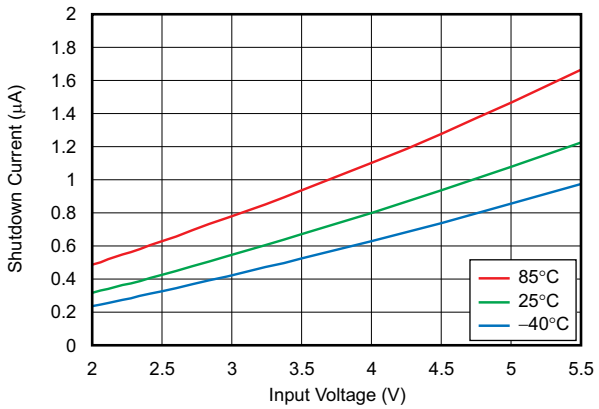
V_O = 5.0 V

Figure 25. Ground Pin Current vs Output Current



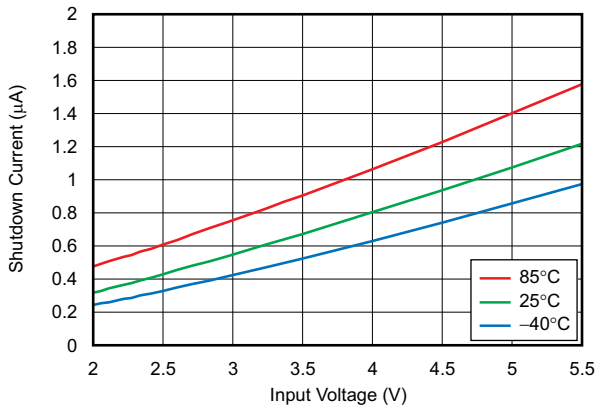
V_O = 1.2 V

Figure 26. Shutdown Current vs Input Voltage



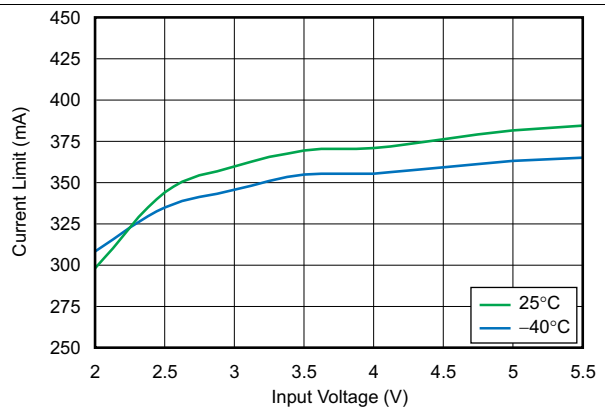
V_O = 2.8 V

Figure 27. Shutdown Current vs Input Voltage



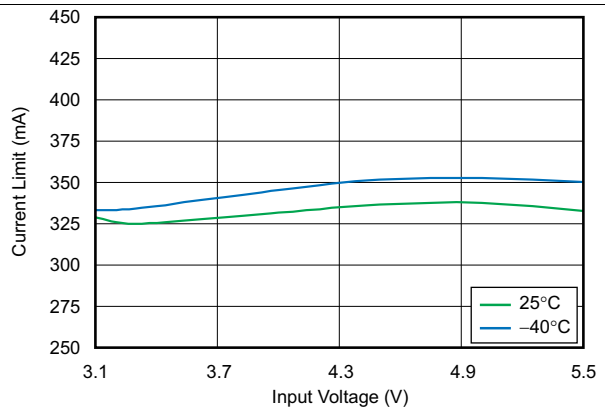
V_O = 5.0 V

Figure 28. Shutdown Current vs Input Voltage



V_O = 1.2 V

Figure 29. Current Limit vs Input Voltage

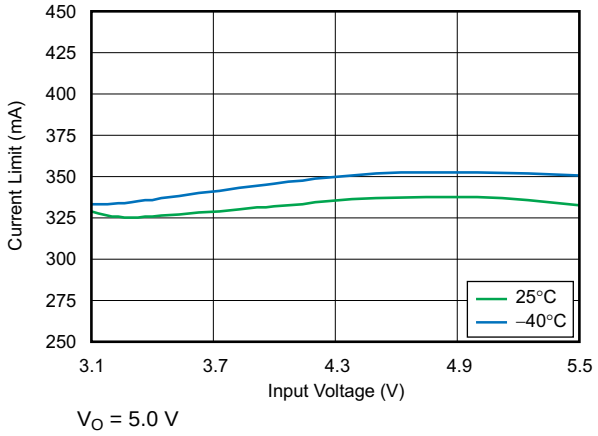


V_O = 2.8 V

Figure 30. Current Limit vs Input Voltage

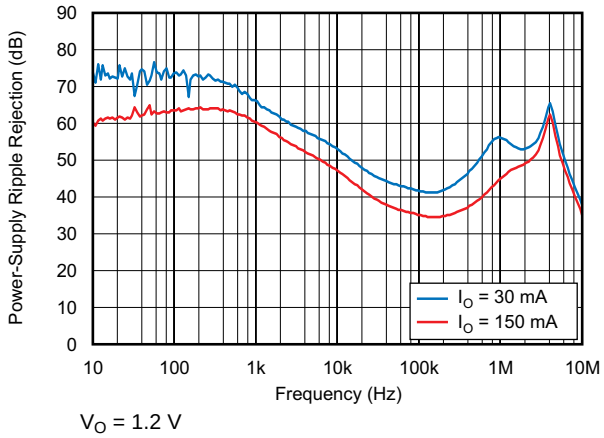
Typical Characteristics (continued)

At T_J = –40°C to 85°C, V_I = $V_{O(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_O = 10 mA, V_{EN} = V_I, and C_{OUT} = 1 µF, unless otherwise noted. Typical values are at T_J = 25°C.



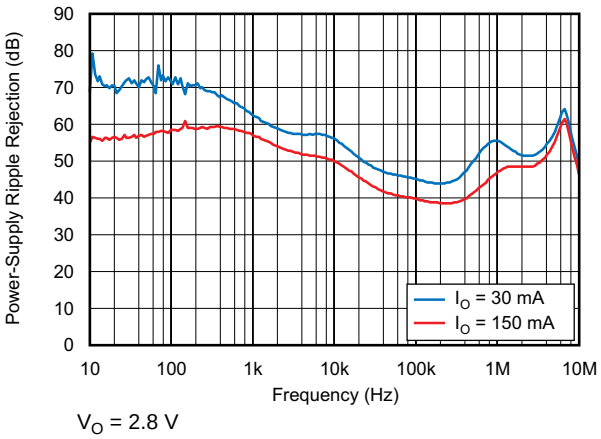
V_O = 5.0 V

Figure 31. Current Limit vs Input Voltage



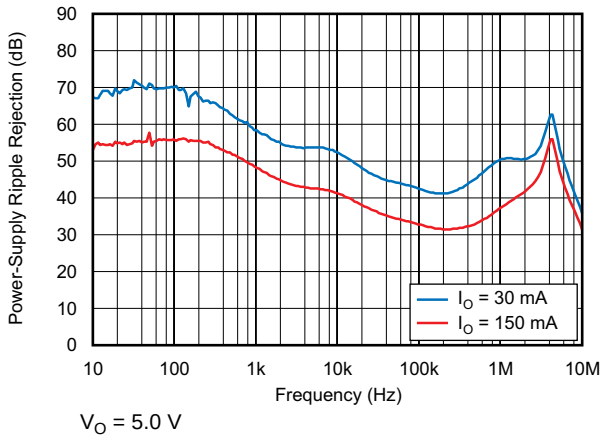
V_O = 1.2 V

Figure 32. Power-Supply Ripple Rejection vs Frequency



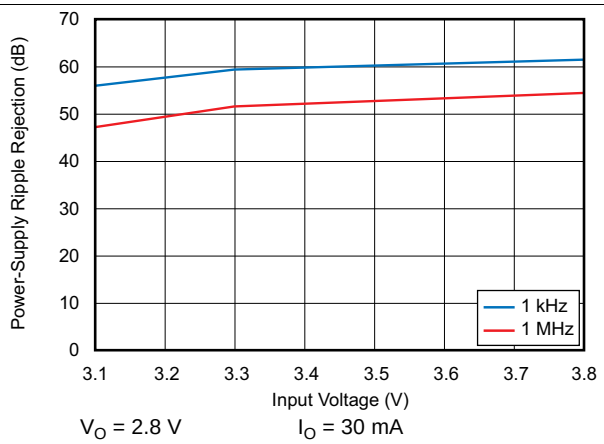
V_O = 2.8 V

Figure 33. Power-Supply Ripple Rejection vs Frequency



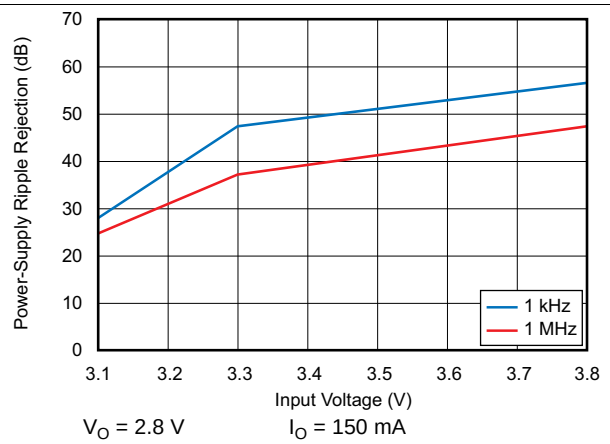
V_O = 5.0 V

Figure 34. Power-Supply Ripple Rejection vs Frequency



V_O = 2.8 V I_O = 30 mA

Figure 35. Power-Supply Ripple Rejection vs Input Voltage

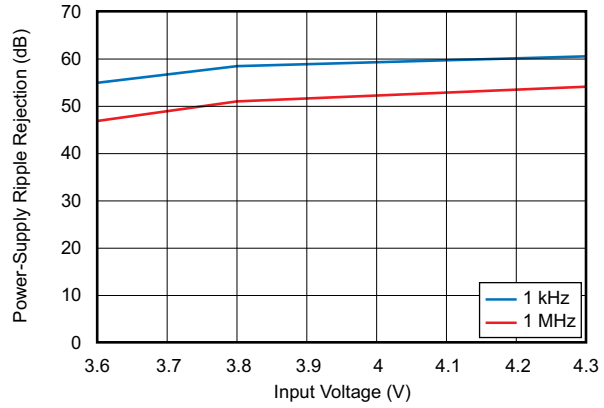


V_O = 2.8 V I_O = 150 mA

Figure 36. Power-Supply Ripple Rejection vs Input Voltage

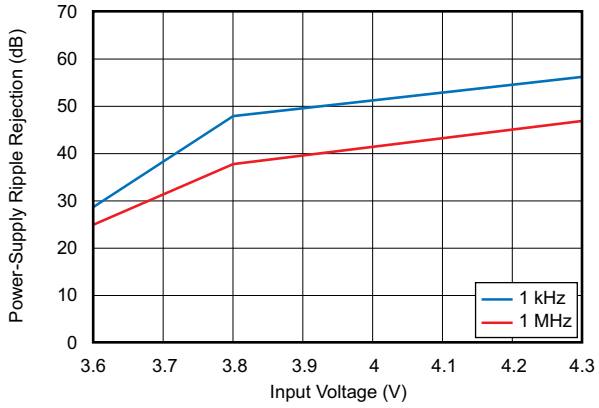
Typical Characteristics (continued)

At T_J = –40°C to 85°C, $V_I = V_{O(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_O = 10 mA, $V_{EN} = V_I$, and C_{OUT} = 1 µF, unless otherwise noted. Typical values are at T_J = 25°C.



V_O = 3.3 V I_O = 30 mA

Figure 37. Power-Supply Ripple Rejection vs Input Voltage



V_O = 3.3 V I_O = 150 mA

Figure 38. Power-Supply Ripple Rejection vs Input Voltage

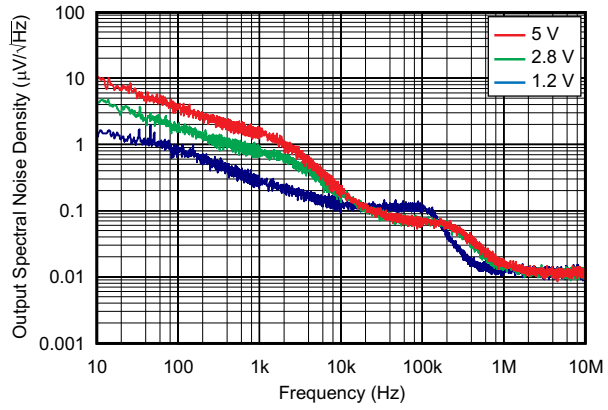
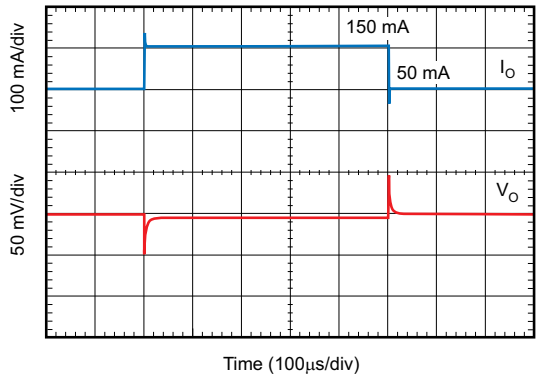
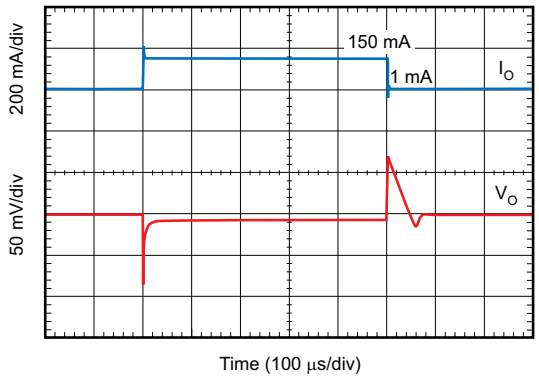


Figure 39. Output Spectral Noise Density vs Frequency



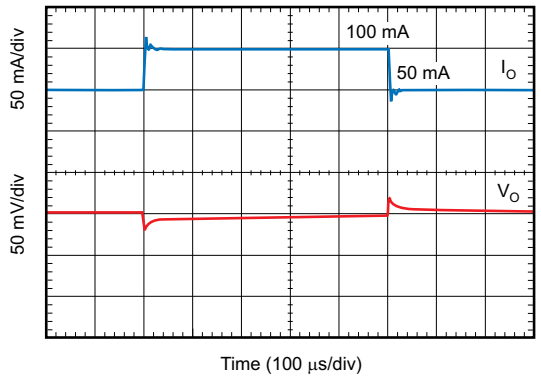
V_O = 1.2 V

Figure 40. Load Transient Response



V_O = 1.2 V

Figure 41. Load Transient Response

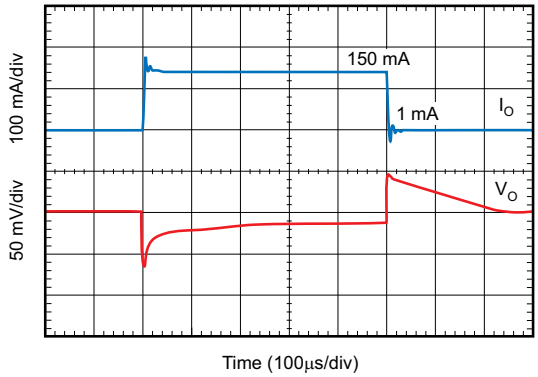


V_O = 2.8 V

Figure 42. Load Transient Response

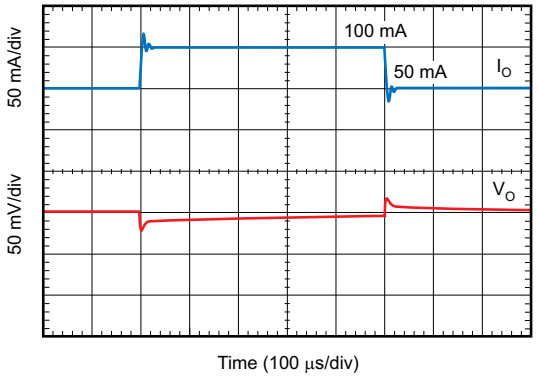
Typical Characteristics (continued)

At T_J = –40°C to 85°C, V_I = $V_{O(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_O = 10 mA, V_{EN} = V_I, and C_{OUT} = 1 µF, unless otherwise noted. Typical values are at T_J = 25°C.



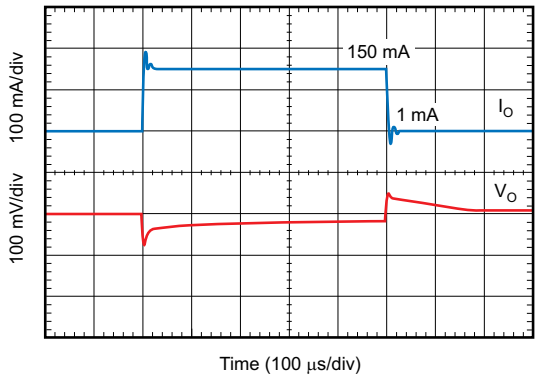
V_O = 2.8 V

Figure 43. Load Transient Response



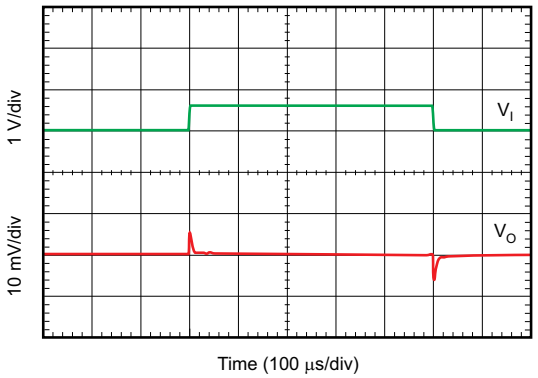
V_O = 5.0 V

Figure 44. Load Transient Response



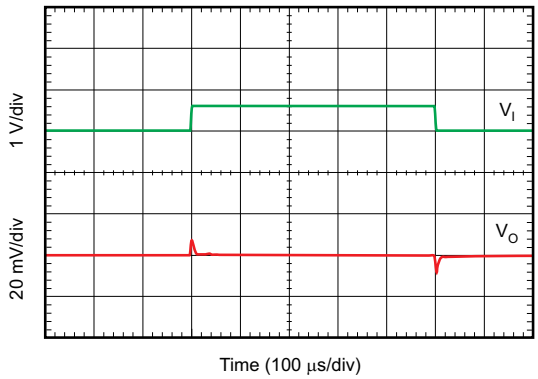
V_O = 5.0 V

Figure 45. Load Transient Response



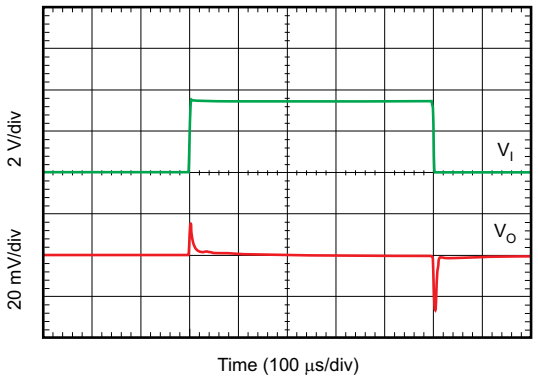
V_O = 1.2 V I_O = 150 mA

Figure 46. Line Transient Response



V_O = 1.2 V I_O = 200 mA

Figure 47. Line Transient Response

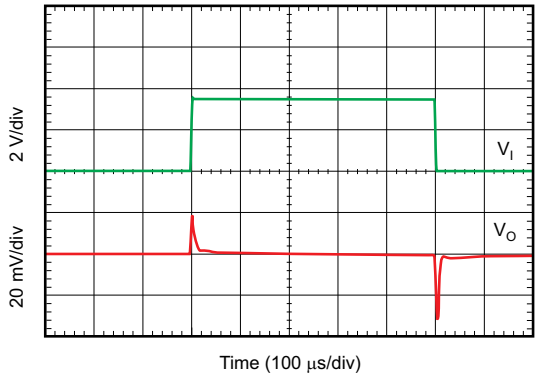


V_O = 1.2 V I_O = 150 mA

Figure 48. Line Transient Response

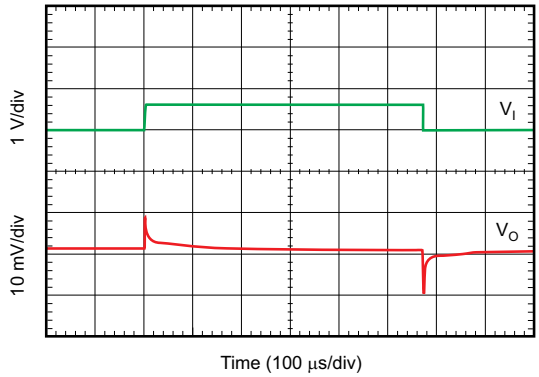
Typical Characteristics (continued)

At T_J = –40°C to 85°C, V_I = $V_{O(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_O = 10 mA, V_{EN} = V_I, and C_{OUT} = 1 µF, unless otherwise noted. Typical values are at T_J = 25°C.



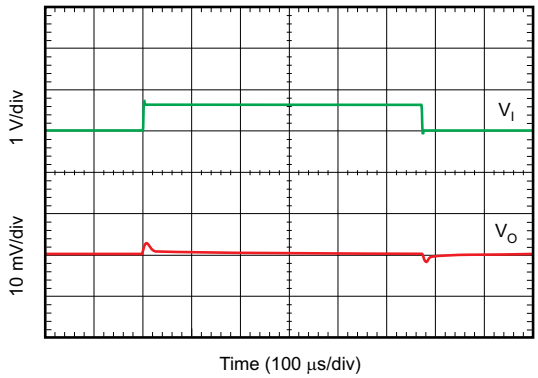
V_O = 1.2 V I_O = 200 mA

Figure 49. Line Transient Response



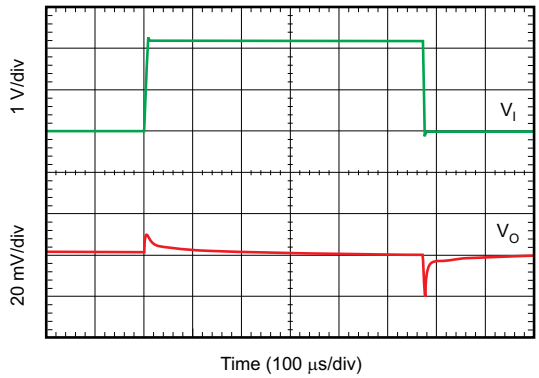
V_O = 2.8 V I_O = 150 mA

Figure 50. Line Transient Response



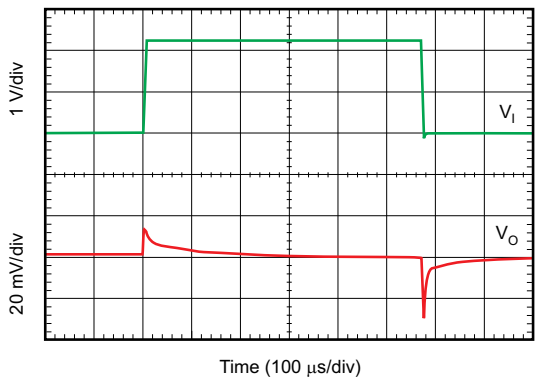
V_O = 2.8 V I_O = 200 mA

Figure 51. Line Transient Response



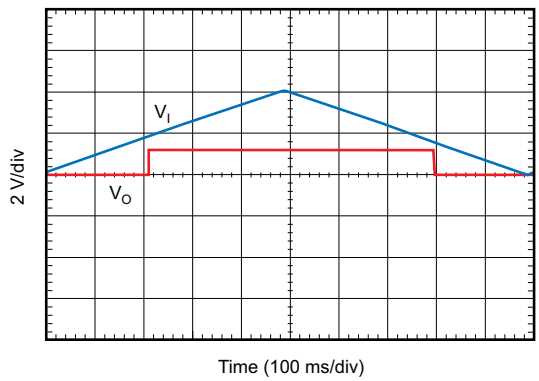
V_O = 2.8 V I_O = 200 mA

Figure 52. Line Transient Response



V_O = 2.8 V I_O = 200 mA

Figure 53. Line Transient Response

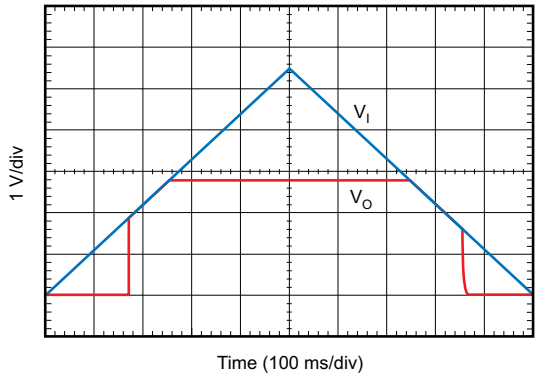


V_O = 1.2 V I_O = 30 mA

Figure 54. V_I Ramp Up, Ramp Down Response

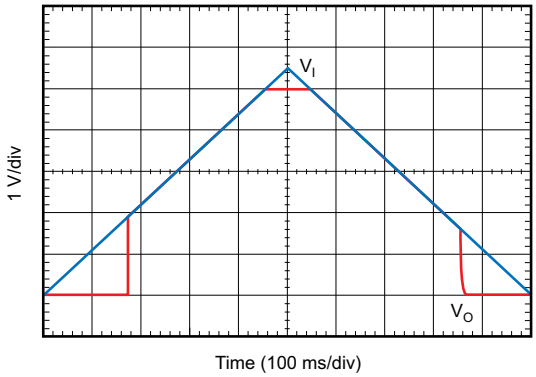
Typical Characteristics (continued)

At T_J = –40°C to 85°C, V_I = $V_{O(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_O = 10 mA, V_{EN} = V_I, and C_{OUT} = 1 µF, unless otherwise noted. Typical values are at T_J = 25°C.



V_O = 2.8 V I_O = 30 mA

Figure 55. V_I Ramp Up, Ramp Down Response



V_O = 5 V I_O = 30 mA

Figure 56. V_I Ramp Up, Ramp Down Response

8 Detailed Description

8.1 Overview

The TLV707 series (TLV707xx and TLV707xxP) belongs to a family of low-dropout regulators (LDOs). This device consumes low quiescent current and delivers excellent line and load transient performance. These characteristics, combined with low noise and very good PSRR with little (V_I – V_O) headroom, make this device ideal for portable RF applications.

8.2 Functional Block Diagrams

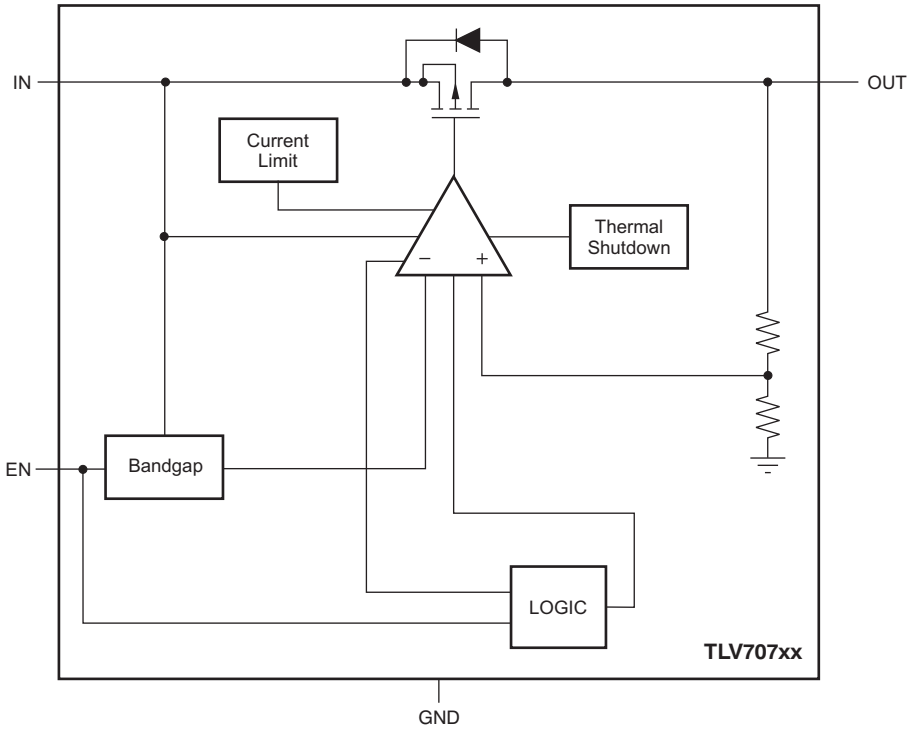


Figure 57. TLV707xx Block Diagram

Functional Block Diagrams (continued)

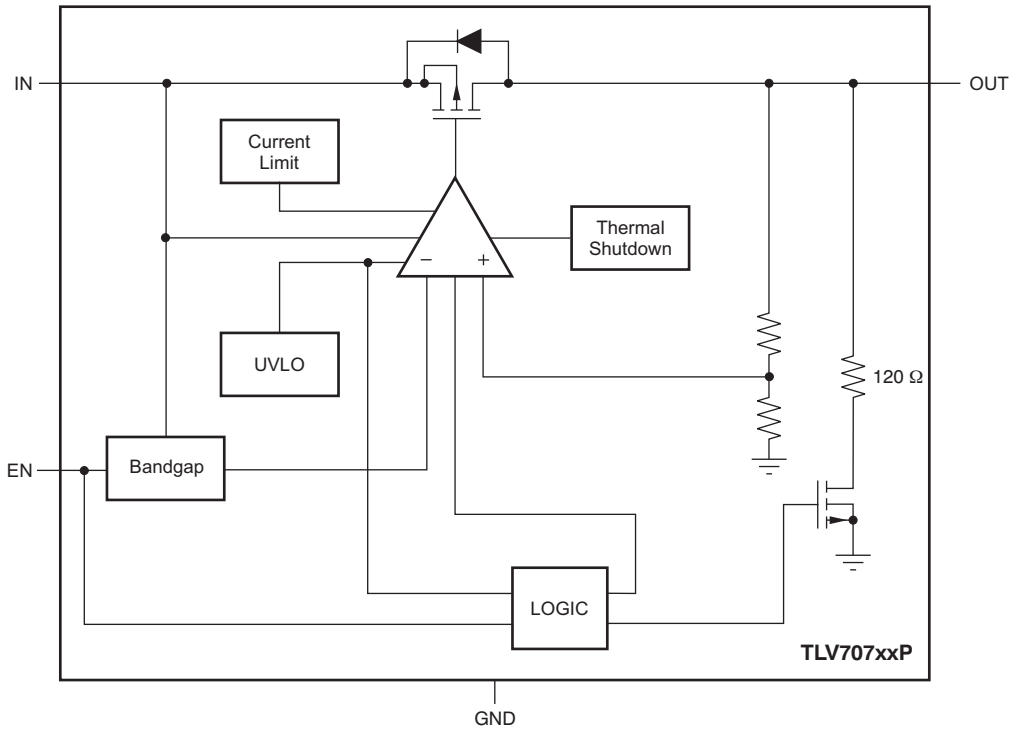


Figure 58. TLV707xxP Block Diagram

8.3 Feature Description

This LDO regulator offers current limit and thermal protection. The operating junction temperature of this device is –40°C to 125°C.

8.3.1 Internal Current Limit

The internal current limit helps to protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of the output voltage. In such a case, the output voltage is not regulated, and is $V_O = I_{LIMIT} \times R_{LOAD}$. The PMOS pass transistor dissipates $(V_I – V_O) \times I_{LIMIT}$ until thermal shutdown is triggered and the device turns off. When the device cools, the internal thermal shutdown circuit turns the device back on. If the fault condition continues, the device cycles between current limit and thermal shutdown. See *Thermal Information* for more details.

The PMOS pass element has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

Feature Description (continued)

8.3.2 Shutdown

The enable pin (EN) is active high. The device is enabled when voltage at the EN pin goes above 0.9 V. This relatively lower voltage value required to turn on the LDO can also be used to power the device when it is connected to a GPIO of a newer processor, where the GPIO Logic 1 voltage level is lower than that of traditional microcontrollers. The device is turned off when the EN pin is held at less than 0.4 V. When shutdown capability is not required, EN can be connected to the IN pin.

The TLV707xxP version has internal active pulldown circuitry that discharges the output with a time constant of:

$$\tau = \frac{(120 \bullet R_L)}{(120 + R_L)} \bullet C_{OUT} \quad (1)$$

where:

- R_L = Load resistance
- C_{OUT} = Output capacitor

8.3.3 Undervoltage Lockout (UVLO)

The TLV707 uses a UVLO circuit to keep the output shut off until internal circuitry is operating properly.

8.4 Device Functional Modes

In order to turn on the regulator, it is required to drive the EN pin over 0.9 V. Driving the EN pin below 0.4 V causes the regulator to enter shutdown mode.

In shutdown, the current consumption of the device is reduced to 1 μA, typically.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLV707 series is a low-dropout regulator (LDO) with low quiescent current that delivers excellent line and load transient performance. This LDO regulator offers current limit and thermal protection. The operating junction temperature of this device series is –40°C to 125°C.

9.2 Typical Application

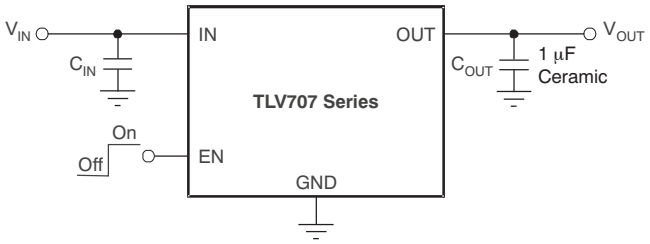


Figure 59. Typical Application Circuit, Fixed-Voltage Versions

9.2.1 Design Requirements

Provide an input supply with adequate headroom to meet minimum VIN requirements, compensate for the GND terminal current, and to power the load.

Table 1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	1.8 V - 3.6 V
Output voltage	1.2 V
Output current	100-mA

9.2.2 Detailed Design Procedure

9.2.2.1 Input and Output Capacitor Requirements

Generally, 1.0-µF X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

However, the TLV707 is designed to be stable with an effective capacitance of 0.1 µF or larger at the output. Thus, the device is stable with capacitors of other dielectric types as well, as long as the effective capacitance under operating bias voltage and temperature is greater than 0.1 µF. This effective capacitance refers to the capacitance that the LDO detects under operating bias voltage and temperature conditions; that is, the capacitance after taking both bias voltage and temperature derating into consideration. In addition to allowing the use of less expensive dielectrics, this capability of being stable with 0.1-µF effective capacitance also enables the use of smaller footprint capacitors that have higher derating in size- and space-constrained applications.

Using a 0.1-µF rated capacitor at the output of the LDO does not ensure stability because the effective capacitance under the specified operating conditions is less than 0.1 µF. Maximum ESR must be less than 200 mΩ.

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1-µF to 1.0-µF, low ESR capacitor across the IN pin and GND pin of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source. If source impedance is more than 2-Ω, a 0.1-µF input capacitor may be necessary to ensure stability.

9.2.2.2 Dropout Voltage

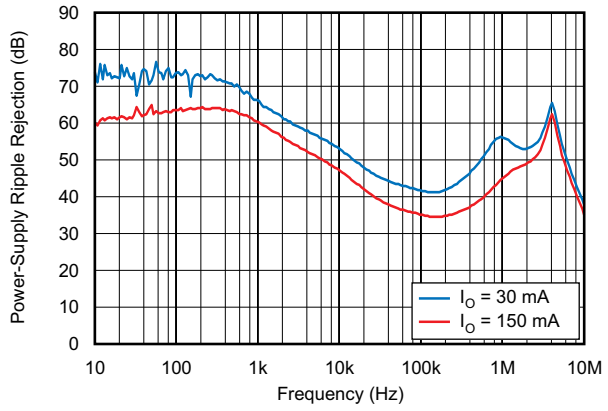
The TLV707 series of LDOs use a PMOS pass transistor to achieve low dropout. When (V_I – V_O) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device functions similar to a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded when (V_I – V_O) approaches dropout.

9.2.2.3 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over- and undershoot magnitude but increases the duration of the transient response.

9.2.3 Application Curves



V_O = 1.2 V

Figure 60. Power-Supply Ripple Rejection vs Frequency

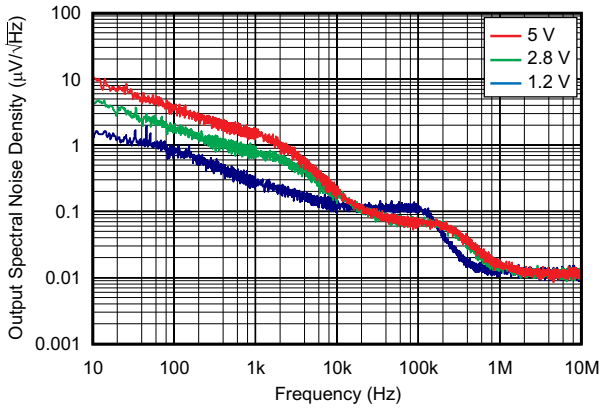
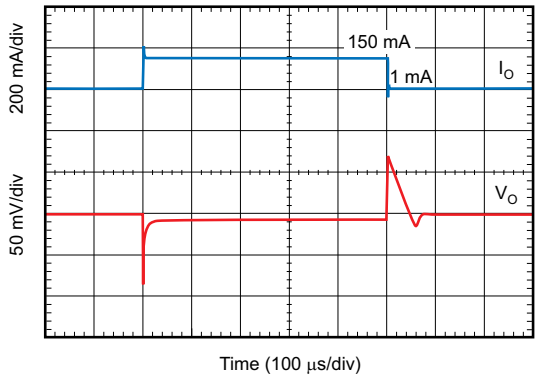
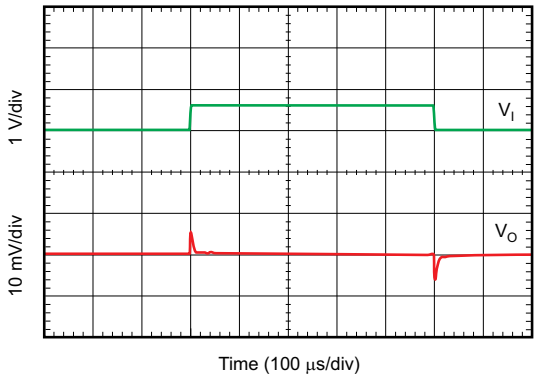


Figure 61. Output Spectral Noise Density vs Frequency



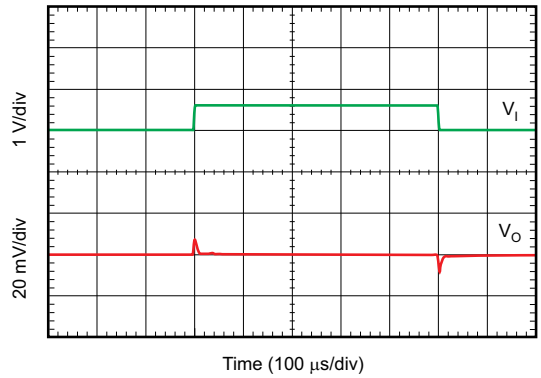
V_O = 1.2 V

Figure 62. Load Transient Response



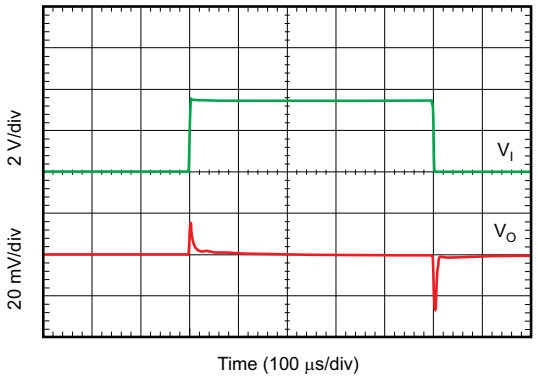
V_O = 1.2 V I_O = 150 mA

Figure 63. Line Transient Response



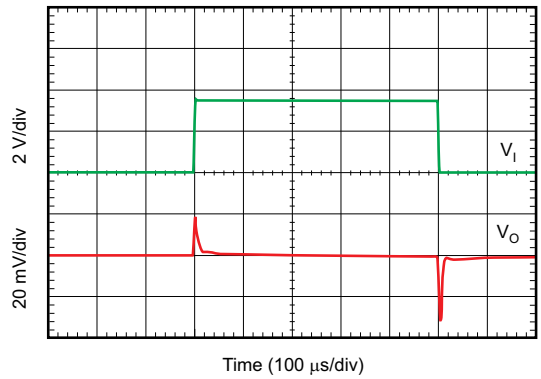
V_O = 1.2 V I_O = 200 mA

Figure 64. Line Transient Response



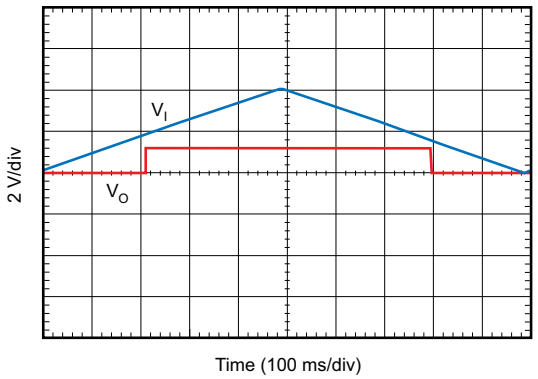
V_O = 1.2 V I_O = 150 mA

Figure 65. Line Transient Response



V_O = 1.2 V I_O = 200 mA

Figure 66. Line Transient Response



V_O = 1.2 V I_O = 30 mA

Figure 67. V_{IN} Ramp Up, Ramp Down Response

9.3 Do's and Don'ts

Place at least one 1.0-µF ceramic capacitor as close as possible to the OUT terminal of the regulator.

Do not place the output capacitor more than 10 mm away from the regulator.

Connect a 1.0-µF low equivalent series resistance (ESR) capacitor across the IN terminal and GND input of the regulator for improved transient performance.

Do not exceed the absolute maximum ratings.

10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.0 V and 5.5 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply must be well regulated (see Figure 46 through Figure 53). If the input supply is noisy, additional input capacitors with low ESR help improve the output noise performance.

11 Layout

11.1 Layout Guidelines

11.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

Place input and output capacitors as close to the device pins as possible. To improve ac performance (such as PSRR, output noise, and transient response), TI recommends that the board be designed with separate ground planes for V_I and V_O, with the ground plane connected only at the GND pin of the device. In addition, connect the ground connection for the output capacitor directly to the GND pin of the device. High ESR capacitors may degrade PSRR performance.

11.1.2 Package Mounting

Solder pad footprint recommendations are available from TI's website at www.ti.com. The recommended land pattern for the DQN (X2SON-4) package is shown in *Mechanical, Packaging, and Orderable Information*.

11.2 Layout Example

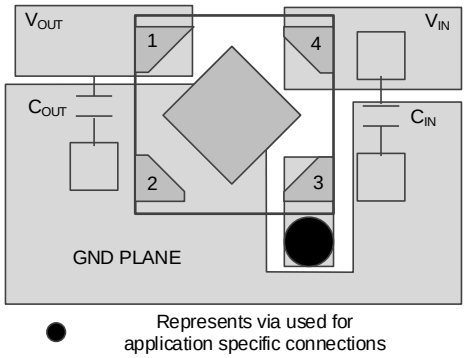


Figure 68. Recommended Layout Example

11.3 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, thus protecting the regulator from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to 125°C (maximum). To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

For good reliability, thermal protection triggers at least 35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the LDO is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the LDO into thermal shutdown degrades device reliability.

11.4 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed-circuit-board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air.

Performance data for JEDEC low- and high-K boards are given in *Thermal Information*. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element, as shown in *Mechanical, Packaging, and Orderable Information*.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TLV707xx and TLV707xxP. SLVU416 details the design kits and evaluation modules for TLV70728EVM-612.

The EVM can be requested at the Texas Instruments web site through the TLV707xx and TLV707xxP product folders, or purchased directly from the TI eStore.

12.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TLV707xx and TLV707xxP is available through the respective device product folders under *Simulation Models*.

12.1.2 Device Nomenclature

Table 2. Ordering Information(1)

PRODUCT	V_{OUT} (2)
TLV707**xx(x)***Pyyyz*	**XX(X)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 18 = 1.8 V, 285 = 2.85 V). **P** is optional; devices with P have an LDO regulator with an active output discharge. **YYY** is the package designator. **Z** is package quantity. Use ***R*** for reel (3000 pieces), and ***T*** for tape (250 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
(2) Output voltages from 0.85 V to 5.0 V in 50-mV increments are available. Contact factory for details and availability.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- *TLV70728EVM-612 Evaluation Module*, SLVU416

12.3 Trademarks

All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated family of devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV707085DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BY	Samples
TLV707085DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BY	Samples
TLV70710DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BB	Samples
TLV70710DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BB	Samples
TLV70710PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BC	Samples
TLV70710PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BC	Samples
TLV707115DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	B3	Samples
TLV707115DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	B3	Samples
TLV70711PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C3	Samples
TLV70711PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C3	Samples
TLV70712PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	WJ	Samples
TLV70712PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	WJ	Samples
TLV70715PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WI	Samples
TLV70715PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WI	Samples
TLV70717DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	GD	Samples
TLV70717DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	GD	Samples
TLV707185DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZN	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV707185DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZN	Samples
TLV707185PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	B1	Samples
TLV707185PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	B1	Samples
TLV70718DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZC	Samples
TLV70718DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZC	Samples
TLV70718PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	SB	Samples
TLV70718PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	SB	Samples
TLV70719PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ZM	Samples
TLV70719PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ZM	Samples
TLV70725DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BM	Samples
TLV70725DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BM	Samples
TLV70725PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AT	Samples
TLV70726DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RF	Samples
TLV70726DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RF	Samples
TLV70726PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SC	Samples
TLV707285DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RZ	Samples
TLV707285DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RZ	Samples
TLV707285PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	XE	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV707285PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	XE	Samples
TLV70728PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SD	Samples
TLV70728PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SD	Samples
TLV70729DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BF	Samples
TLV70729DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BF	Samples
TLV70729PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BG	Samples
TLV70729PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BG	Samples
TLV70730DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HJ	Samples
TLV70730DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HJ	Samples
TLV70730PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SE	Samples
TLV70730PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SE	Samples
TLV70731DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DI	Samples
TLV70731DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DI	Samples
TLV70732DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	C8	Samples
TLV70732DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	C8	Samples
TLV707335DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	F6	Samples
TLV707335DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	F6	Samples
TLV70733DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YH	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV70733DQNR1	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	BN	Samples
TLV70733DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YH	Samples
TLV70733PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TI	Samples
TLV70733PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TI	Samples
TLV70734DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AQ	Samples
TLV70734DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AQ	Samples
TLV70734PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AP	Samples
TLV70734PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AP	Samples
TLV70736DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CC	Samples
TLV70736DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CC	Samples
TLV70736PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ZO	Samples
TLV70736PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ZO	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

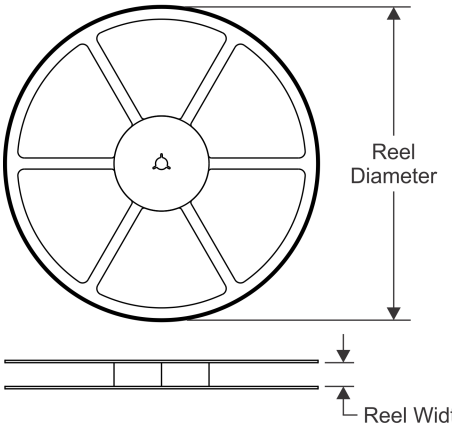
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

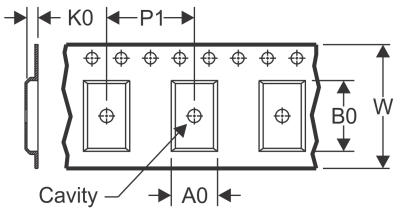
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

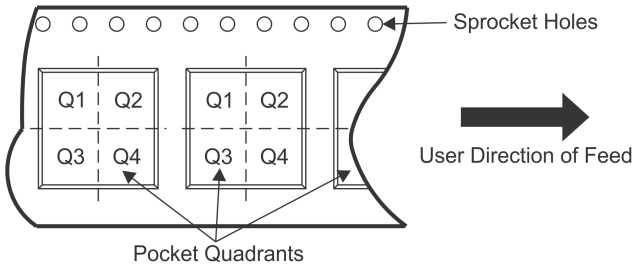


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



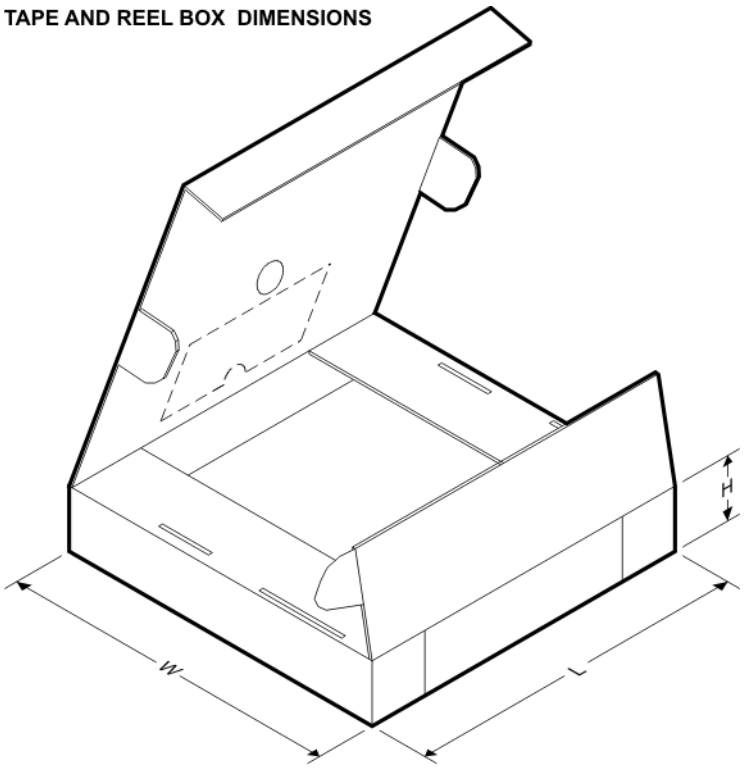
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV707085DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV707085DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70710DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70710DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70710DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70710DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70710PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70710PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70710PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70710PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV707115DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV707115DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV707115DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV707115DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70711PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70711PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70715PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70715PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV70715PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70715PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70717DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70717DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV707185DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV707185DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV707185DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV707185PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV707185PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV707185PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV707185PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70718DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70718DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70718PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70718PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70718PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70718PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70719PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70719PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70719PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70719PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70725DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70725DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70726DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70726DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70726DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70726DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70726PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70726PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV707285DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV707285DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV707285DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV707285DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70728PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70728PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70728PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70728PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70729DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70729DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70729DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70729DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70729PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70729PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV70729PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70729PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70730DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70730DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70730DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70730DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70730PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70730PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70730PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70730PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70731DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70731DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV707335DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV707335DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70733DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70733DQNR1	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	2.0	8.0	Q1
TLV70733DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70733PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70733PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70733PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70733PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70734DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70734DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70734DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70734DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70734PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70734PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70736DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70736DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70736DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV70736DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70736PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70736PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



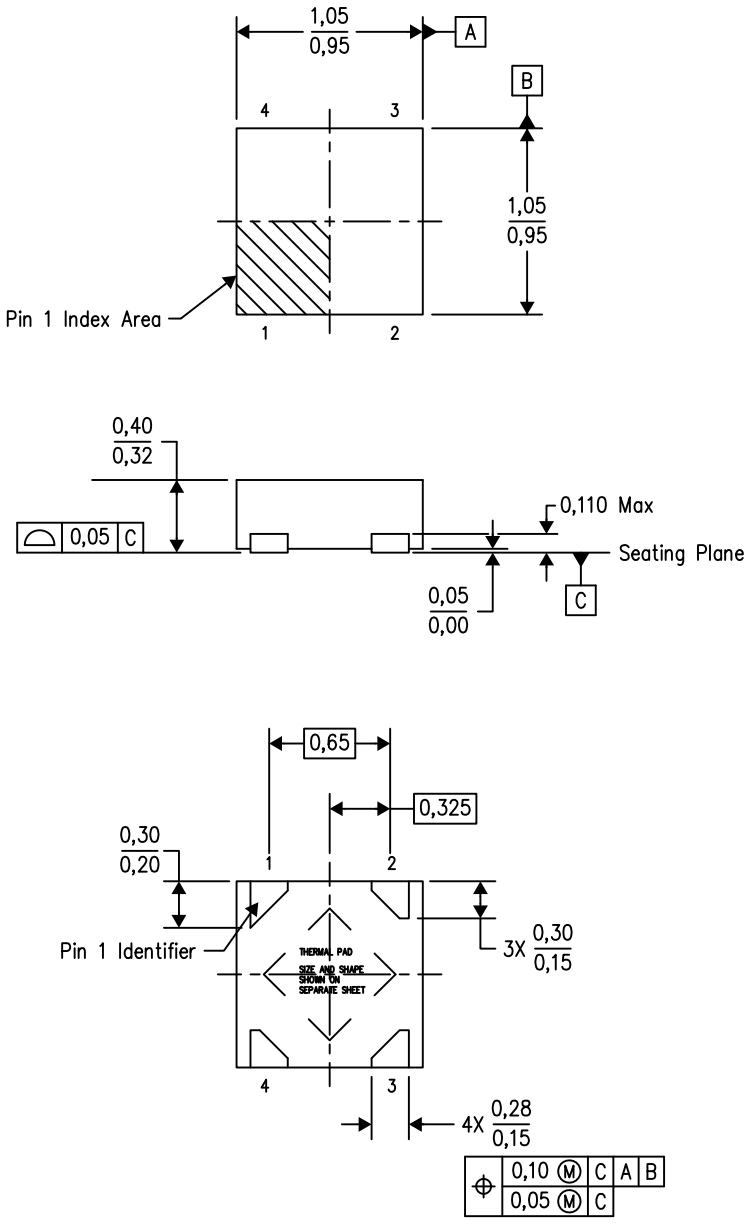
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV707085DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV707085DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70710DQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV70710DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70710DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70710DQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV70710PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70710PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV70710PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70710PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV707115DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV707115DQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV707115DQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV707115DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70711PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70711PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70715PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70715PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV70715PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70715PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV70717DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70717DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV707185DQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV707185DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV707185DQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV707185PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV707185PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV707185PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV707185PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70718DQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV70718DQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV70718PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV70718PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70718PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70718PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV70719PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV70719PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70719PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70719PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV70725DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70725DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70726DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70726DQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV70726DQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV70726DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70726PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV70726PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV707285DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV707285DQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV707285DQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV707285DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70728PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV70728PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70728PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV70728PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70729DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70729DQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV70729DQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV70729DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70729PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70729PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV70729PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV70729PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70730DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV70730DQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV70730DQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV70730DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70730PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70730PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV70730PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70730PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV70731DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70731DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV707335DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV707335DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70733DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70733DQNR1	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70733DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70733PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70733PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV70733PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV70733PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70734DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70734DQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV70734DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70734DQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV70734PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70734PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70736DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70736DQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV70736DQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV70736DQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV70736PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV70736PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0

DQN (S–PX2SON–N4) PLASTIC SMALL OUTLINE NO–LEAD



4210367/D 09/2012

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

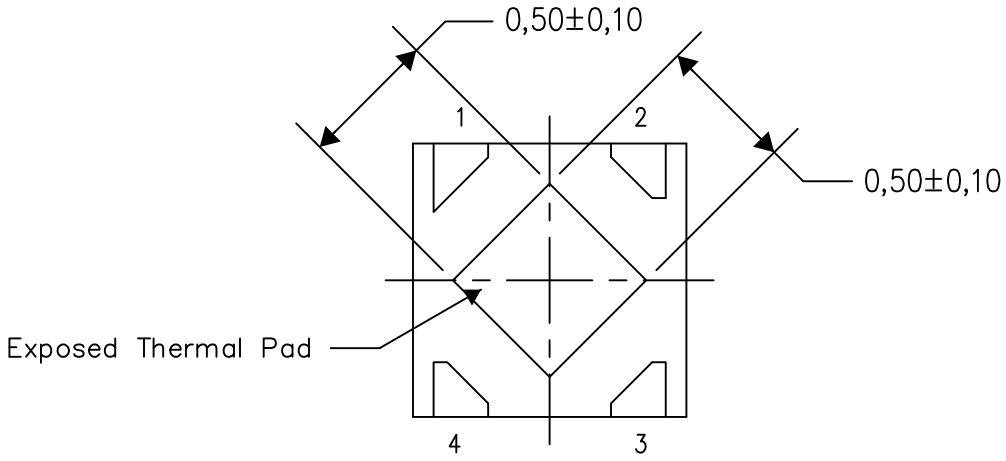
DQN (S–PX2SON–N4) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



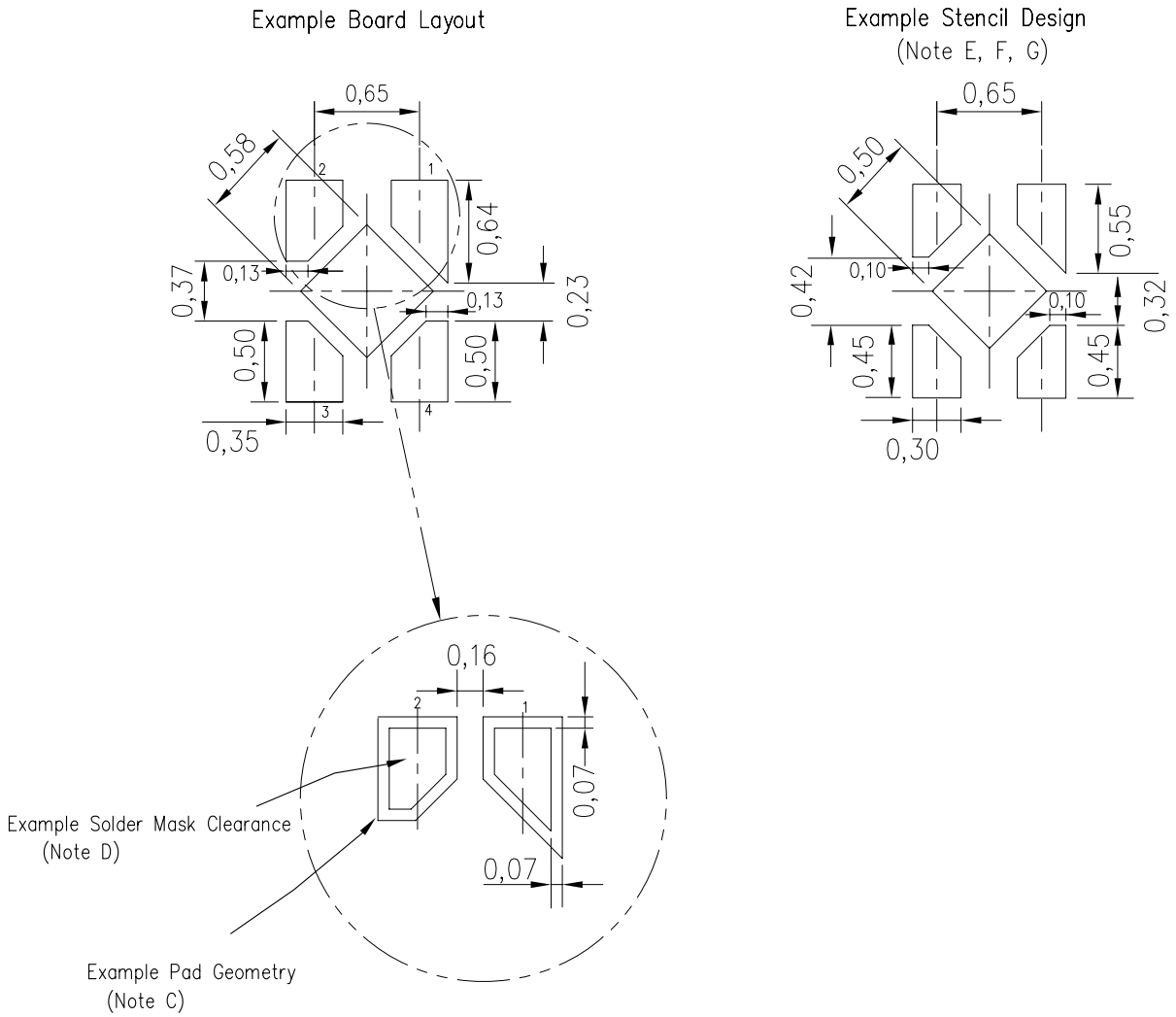
Bottom View

Exposed Thermal Pad Dimensions

4210393–2/E 04/12

NOTE: All linear dimensions are in millimeters

DQN (S–PX2SON–N4) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

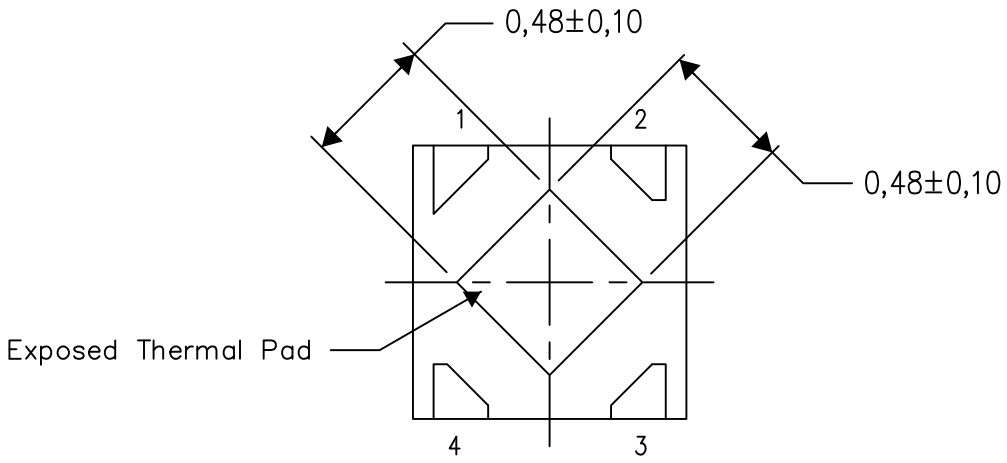
DQN (S–PX2SON–N4) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



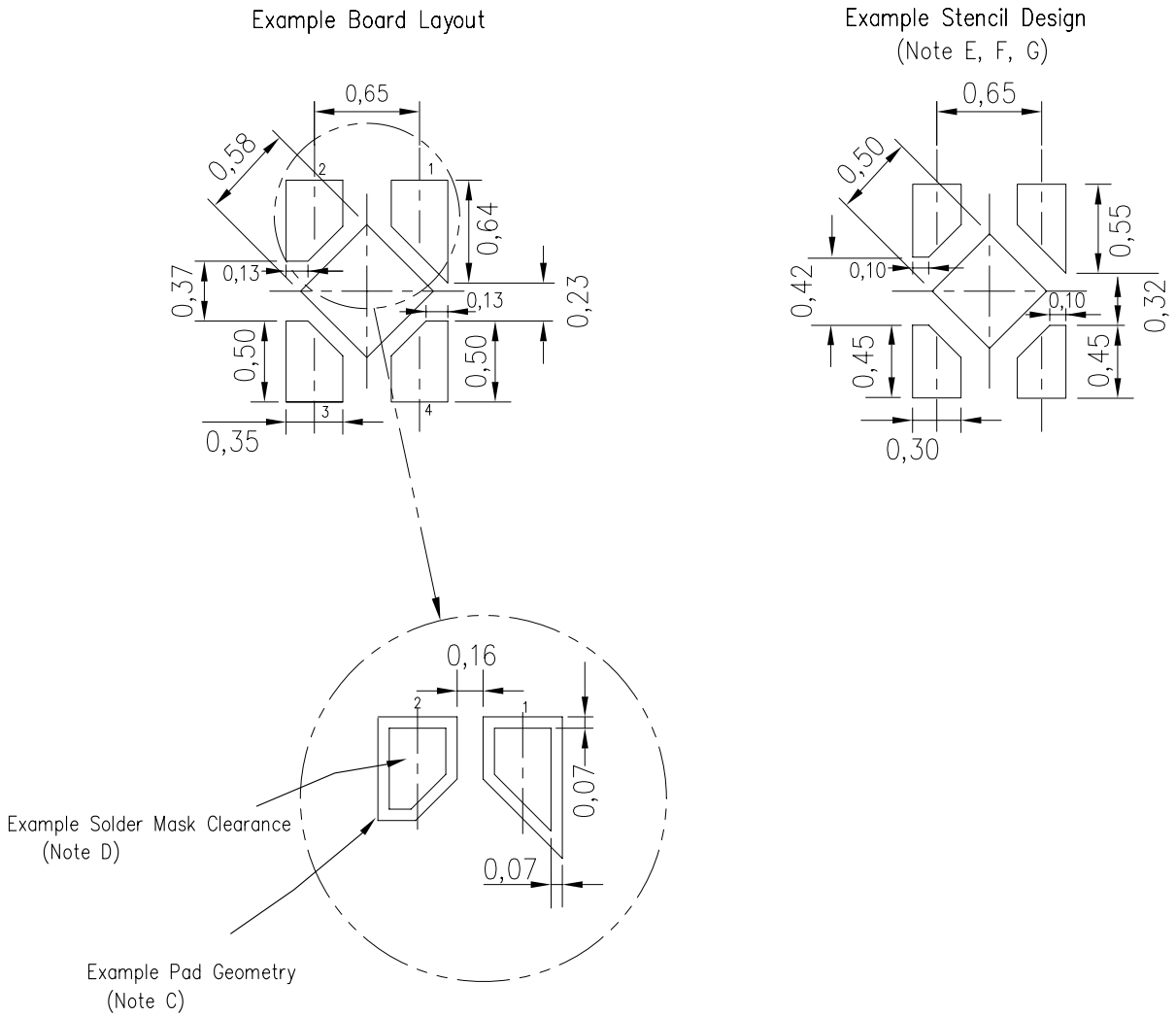
Bottom View

Exposed Thermal Pad Dimensions

4210393–3/E 04/12

NOTE: All linear dimensions are in millimeters

DQN (S–PX2SON–N4) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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