

TLV5618A

2.7-V TO 5.5-V LOW-POWER DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTER WITH POWER DOWN

SLAS230H – JULY 1999 – REVISED JULY 2002

features

- Dual 12-Bit Voltage Output DAC
- Programmable Settling Time
 - 3 μ s in Fast Mode
 - 10 μ s in Slow Mode
- Compatible With TMS320 and SPI Serial Ports
- Differential Nonlinearity <0.5 LSB Typ
- Monotonic Over Temperature
- Direct Replacement for TLC5618A (C and I Suffixes)
- Available in Q-Temp Automotive HighRel Automotive Applications Configuration Control/Print Support Qualification to Automotive Standards

applications

- Digital Servo Control Loops
- Digital Offset and Gain Adjustment
- Industrial Process Control
- Machine and Motion Control Devices
- Mass Storage Devices

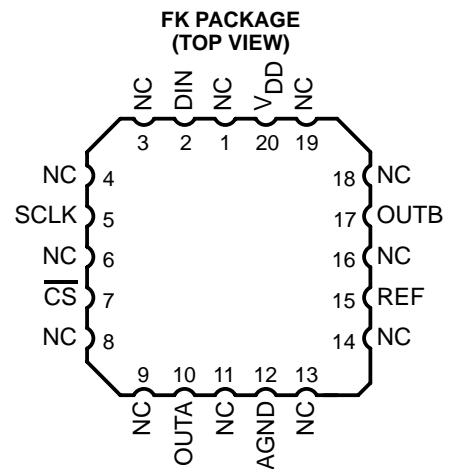
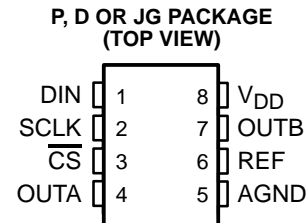
description

The TLV5618A is a dual 12-bit voltage output DAC with a flexible 3-wire serial interface. The serial interface is compatible with TMS320, SPI™, QSPI™, and Microwire™ serial ports. It is programmed with a 16-bit serial string containing 4 control and 12 data bits.

The resistor string output voltage is buffered by an x2 gain rail-to-rail output buffer. The buffer features a Class-AB output stage to improve stability and reduce settling time. The programmable settling time of the DAC allows the designer to optimize speed versus power dissipation.

Implemented with a CMOS process, the device is designed for single supply operation from 2.7 V to 5.5 V. It is available in an 8-pin SOIC package in standard commercial and industrial temperature ranges.

The TLV5618AC is characterized for operation from 0°C to 70°C. The TLV5618AI is characterized for operation from –40°C to 85°C. The TLV5618AQ is characterized for operation from –40°C to 125°C. The TLV5618AM is characterized for operation from –55°C to 125°C.



AVAILABLE OPTIONS

T _A	PACKAGE			
	PLASTIC DIP (P)	SOIC (D)	CERAMIC DIP (JG)	20 PAD LCCC (FK)
0°C to 70°C	TLV5618ACP	TLV5618ACD	—	—
–40°C to 85°C	TLV5618AIP	TLV5618AID	—	—
–40°C to 125°C	—	TLV5618AQD TLV5618AQDR	—	—
–55°C to 125°C	—	—	TLV5618AMJG	TLV5618AMFK



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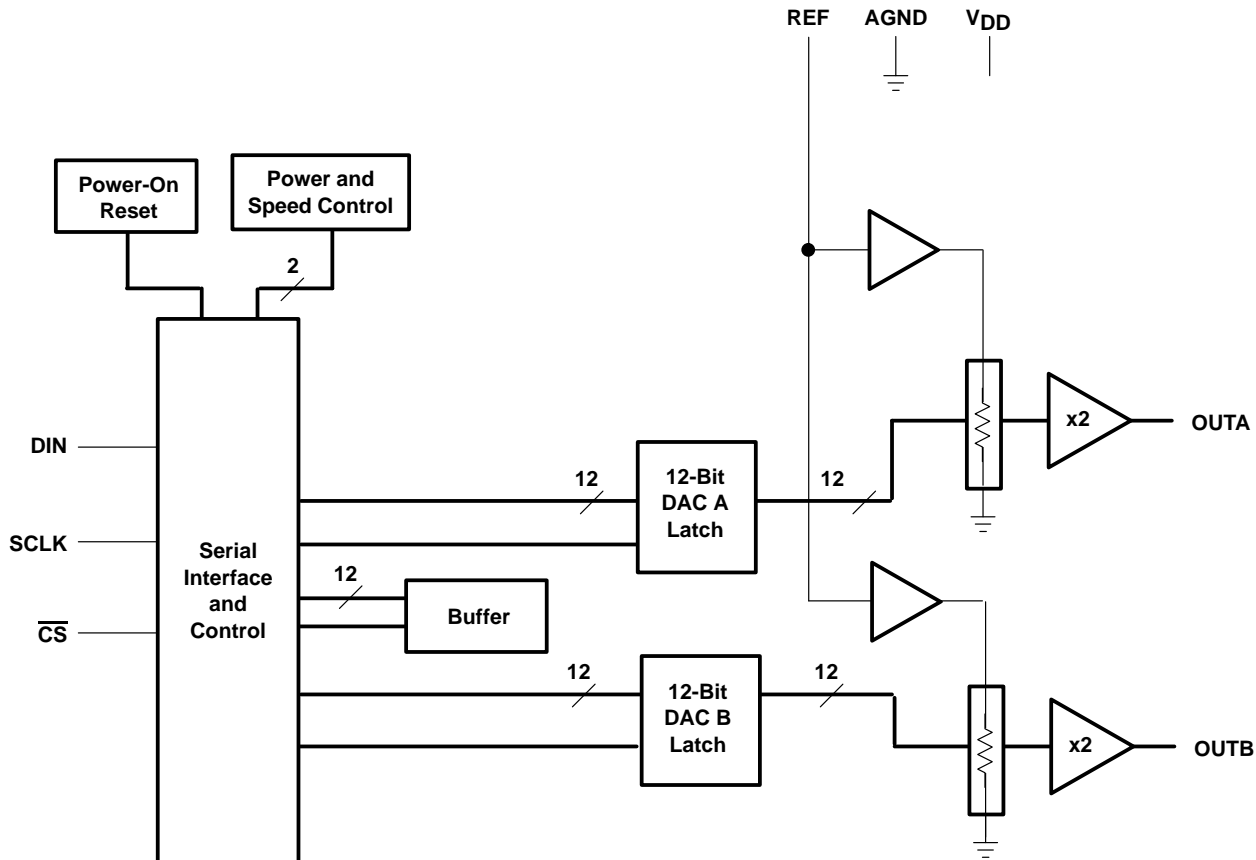
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functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O/P	DESCRIPTION
AGND	5	P	Ground
$\overline{\text{CS}}$	3	I	Chip select. Digital input active low, used to enable/disable inputs.
DIN	1	I	Digital serial data input
OUTA	4	O	DAC A analog voltage output
OUTB	7	O	DAC B analog voltage output
REF	6	I	Analog reference voltage input
SCLK	2	I	Digital serial clock input
VDD	8	P	Positive power supply

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electrical characteristics over recommended operating conditions (unless otherwise noted)

power supply

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I _{DD}	Power supply current	No load, All inputs = AGND or V _{DD} , DAC latch = All ones	V _{DD} = 4.5 V to 5.5 V	C & I suffixes	Fast	1.8	2.5	mA
					Slow	0.8	1	
			V _{DD} = 2.7 V to 3.3 V		Fast	1.6	2.2	mA
					Slow	0.6	0.9	
			V _{DD} = 2.7 V to 5.5 V	M & Q suffixes	Fast	1.8	2.3	mA
					Slow	0.8	1	
Power down supply current						1	μA	
PSRR	Power supply rejection ratio	Zero scale, See Note 2				-65		dB
		Full scale, See Note 3				-65		

- NOTES: 2. Power supply rejection ratio at zero scale is measured by varying V_{DD} and is given by:
 $PSRR = 20 \log [(E_{ZS}(V_{DDmax}) - E_{ZS}(V_{DDmin})/V_{DDmax}]$
3. Power supply rejection ratio at full scale is measured by varying V_{DD} and is given by:
 $PSRR = 20 \log [(E_G(V_{DDmax}) - E_G(V_{DDmin})/V_{DDmax}]$

static DAC specifications

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
Resolution					12			bits
INL	Integral nonlinearity	See Note 4				±2	±4	LSB
DNL	Differential nonlinearity	See Note 5				±0.5	±1	LSB
E _{ZS}	Zero-scale error (offset error at zero scale)	See Note 6					±12	mV
E _{ZS} (TC)	Zero-scale-error temperature coefficient	See Note 7				3		ppm/°C
E _G	Gain error	See Note 8	C & I suffixes	V _{DD} = 4.5 V – 5.5 V		±0.29		% full scale V
				V _{DD} = 2.7 V – 3.3 V		±0.6		
			M & Q suffixes	V _{DD} = 2.7 V – 5.5 V		±0.6		
E _G (TC)	Gain-error temperature coefficient	See Note 9				1		ppm/°C

- NOTES: 4. The relative accuracy of integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale, excluding the effects of zero-code and full-scale errors.
5. The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1-LSB amplitude change of any two adjacent codes.
6. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
7. Zero-scale-error temperature coefficient is given by: $E_{ZS} TC = [E_{ZS}(T_{max}) - E_{ZS}(T_{min})]/2V_{ref} \times 10^6/(T_{max} - T_{min})$.
8. Gain error is the deviation from the ideal output (2V_{ref} – 1 LSB) with an output load of 10 kΩ.
9. Gain temperature coefficient is given by: $E_G TC = [E_G(T_{max}) - E_G(T_{min})]/2V_{ref} \times 10^6/(T_{max} - T_{min})$.

output specifications

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V _O	Output voltage range	R _L = 10 kΩ			0		V _{DD} -0.4	V
Output load regulation accuracy		V _O = 4.096 V, 2.048 V, R _L = 2 kΩ to 10 kΩ					±0.29	% FS



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electrical characteristics over recommended operating conditions (unless otherwise noted)
(continued)

reference input

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _I Input voltage range		0	V _{DD} -1.5		V
R _I Input resistance			10		MΩ
C _I Input capacitance			5		pF
Reference input bandwidth	REF = 0.2 V _{pp} + 1.024 V dc	Fast	1.3		MHz
		Slow	525		kHz
Reference feedthrough	REF = 1 V _{pp} at 1 kHz + 1.024 V dc (see Note 10)		-80		dB

NOTE 10: Reference feedthrough is measured at the DAC output with an input code = 0x000.

digital inputs

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{IH} High-level digital input current	V _I = V _{DD}			1	μA
I _{IL} Low-level digital input current	V _I = 0 V	-1			μA
C _i Input capacitance			8		pF

analog output dynamic performance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _s (FS) Output settling time, full scale	R _L = 10 kΩ, C _L = 100 pF, See Note 11	Fast	1	3	μs
		Slow	3	10	
t _s (CC) Output settling time, code to code	R _L = 10 kΩ, C _L = 100 pF, See Note 12	Fast	1		μs
		Slow	2		
SR Slew rate	R _L = 10 kΩ, C _L = 100 pF, See Note 13	Fast	3		V/μs
		Slow	0.5		
Glitch energy	DIN = 0 to 1, FCLK = 100 kHz, CS = V _{DD}		5		nV-s
SNR Signal-to-noise ratio	f _s = 102 kSPS, f _{out} = 1 kHz, R _L = 10 kΩ, C _L = 100 pF		76		dB
SINAD Signal-to-noise + distortion			68		
THD Total harmonic distortion			-68		
SFDR Spurious free dynamic range			72		

- NOTES: 11. Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of 0x020 to 0xFDF and 0xFDF to 0x020 respectively. Not tested, assured by design.
12. Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of one count. Not tested, assured by design.
13. Slew rate determines the time it takes for a change of the DAC output from 10% to 90% of full-scale voltage.

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digital input timing requirements

		MIN	NOM	MAX	UNIT
$t_{su}(CS-CK)$	Setup time, \overline{CS} low before first negative SCLK edge	C and I suffixes	$V_{DD} = 5\text{ V}$	5	ns
			$V_{DD} = 3\text{ V}$	10	
			Q and M suffixes		10
$t_{su}(C16-CS)$	Setup time, 16 th negative SCLK edge before \overline{CS} rising edge			10	ns
$t_w(H)$	SCLK pulse width high			25	ns
$t_w(L)$	SCLK pulse width low			25	ns
$t_{su}(D)$	Setup time, data ready before SCLK falling edge	C and I suffixes	$V_{DD} = 5\text{ V}$	5	ns
			$V_{DD} = 3\text{ V}$	10	
			Q and M suffixes		8
$t_h(D)$	Hold time, data held valid after SCLK falling edge	C and I suffixes	$V_{DD} = 5\text{ V}$	5	ns
			$V_{DD} = 3\text{ V}$	10	
			Q and M suffixes		10
$t_h(CSH)$	Hold time, \overline{CS} high between cycles		$V_{DD} = 5\text{ V}$	25	ns
			$V_{DD} = 3\text{ V}$	50	

timing requirements

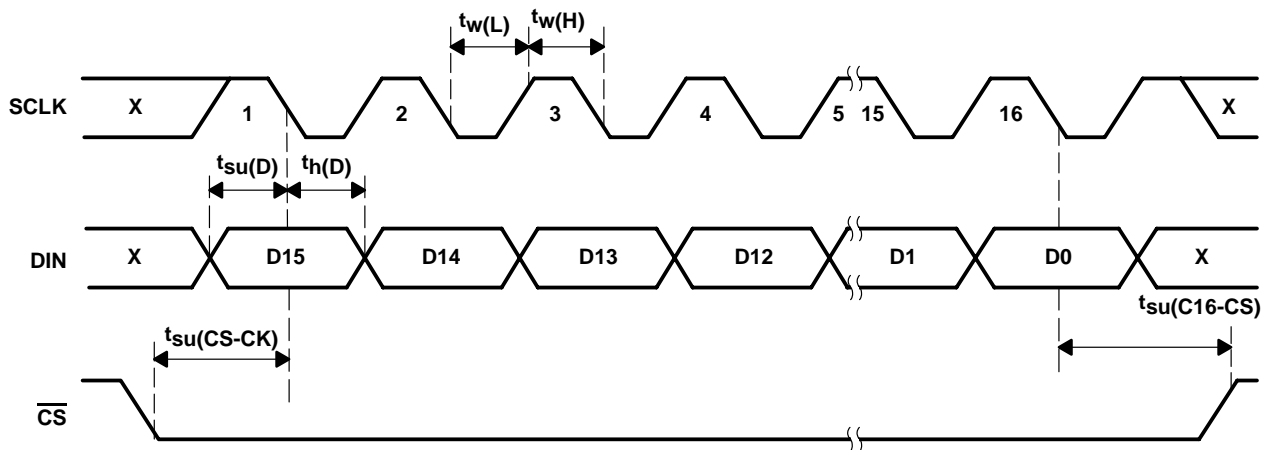


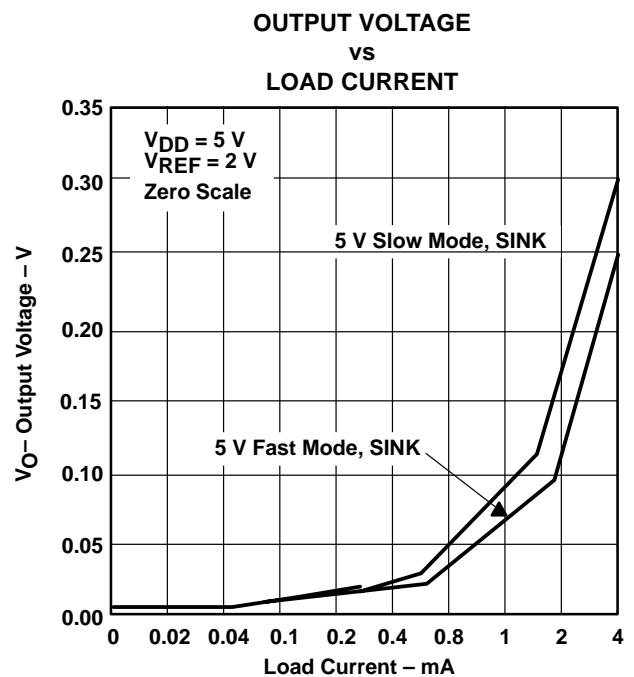
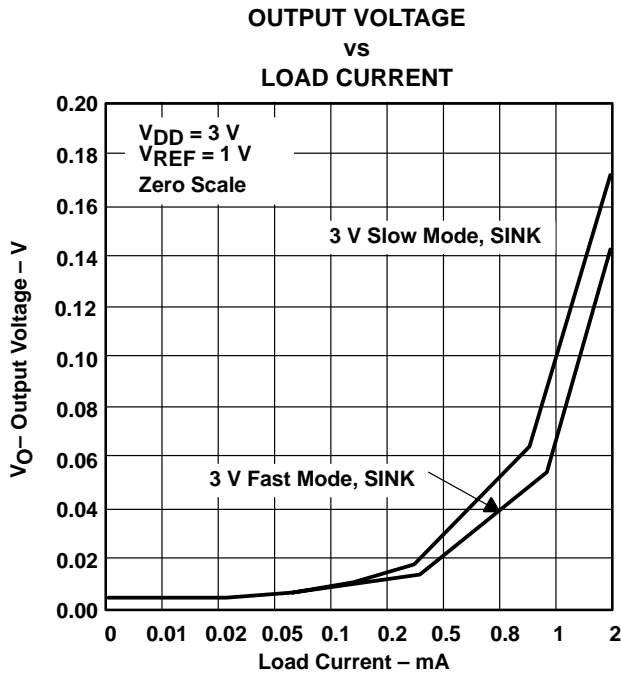
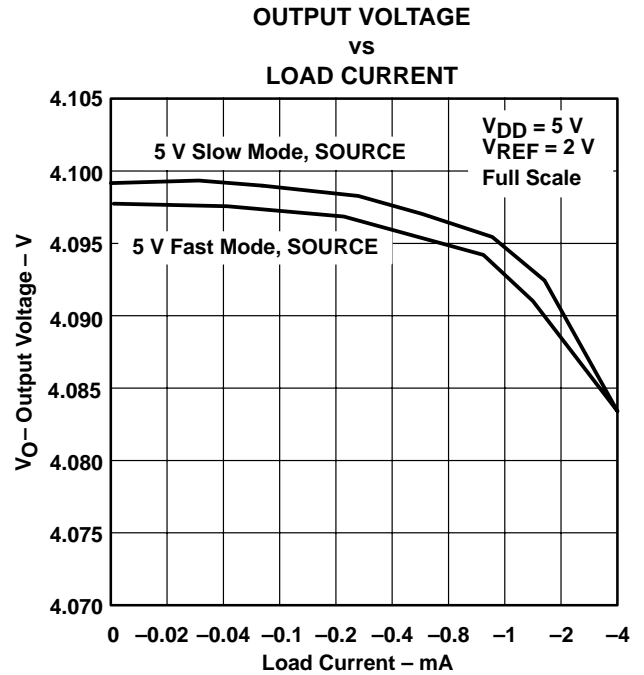
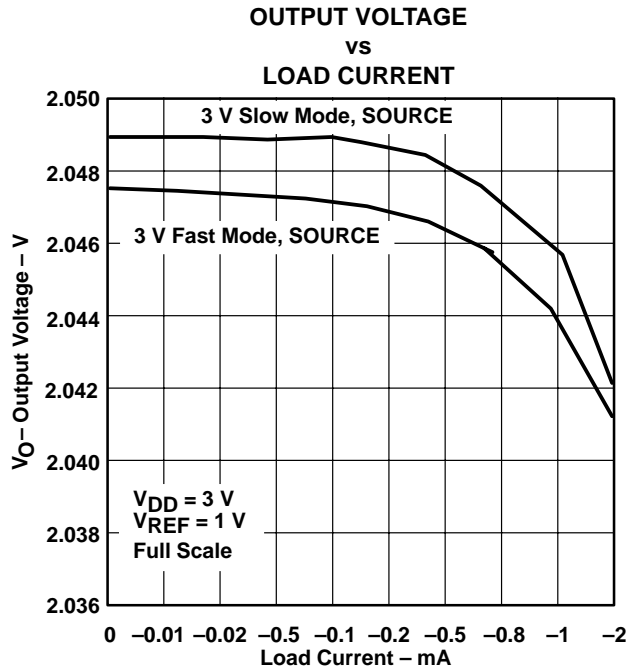
Figure 1. Timing Diagram



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TYPICAL CHARACTERISTICS



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TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

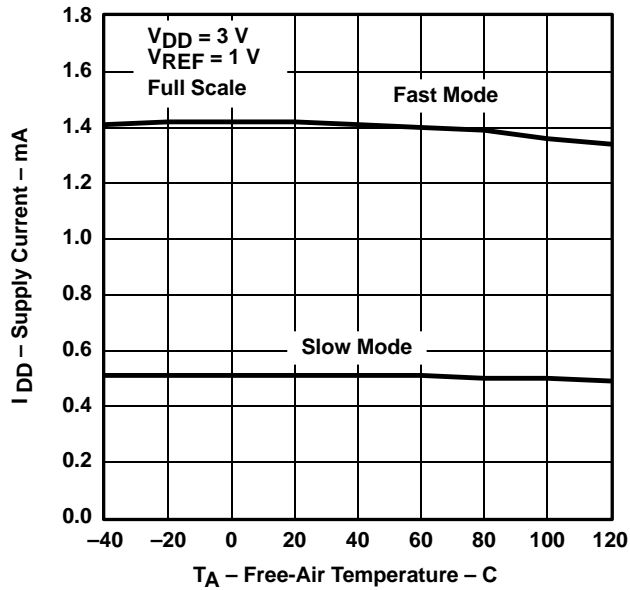


Figure 6

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

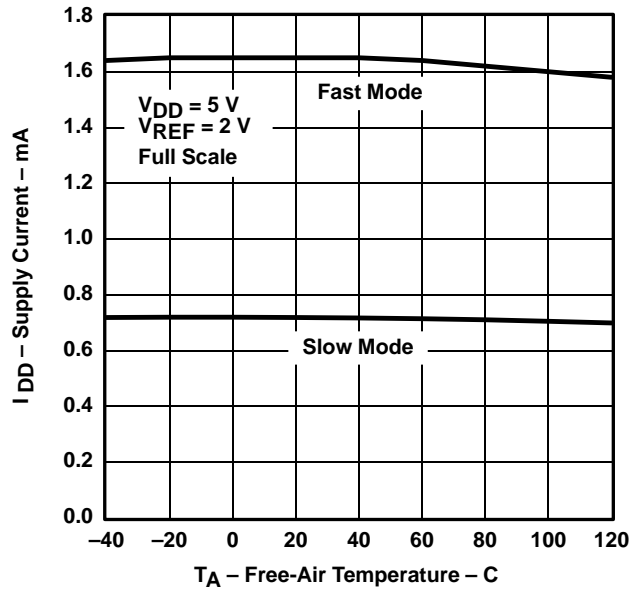


Figure 7

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

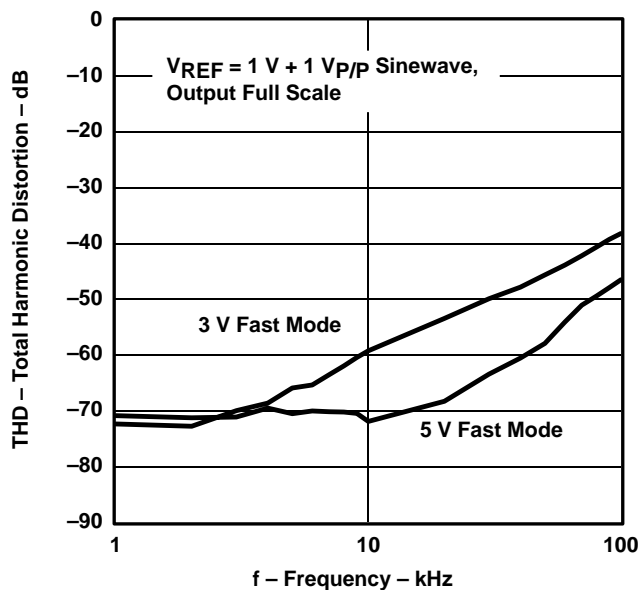


Figure 8

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

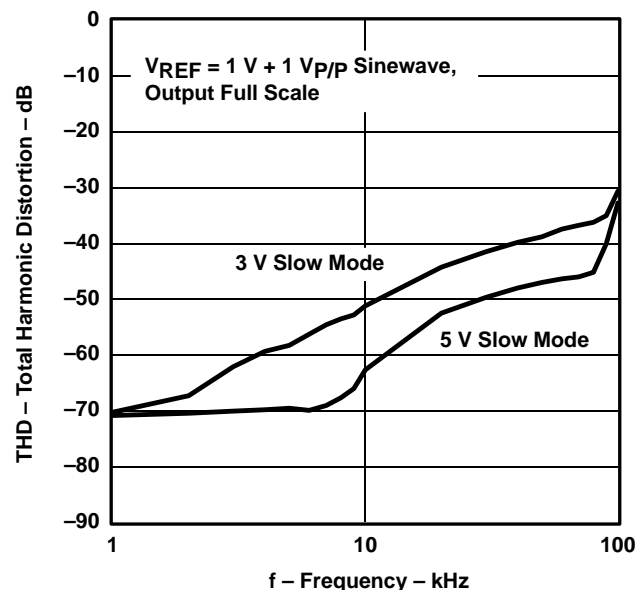


Figure 9



TYPICAL CHARACTERISTICS

INTEGRAL NONLINEARITY ERROR
vs
DIGITAL CODE

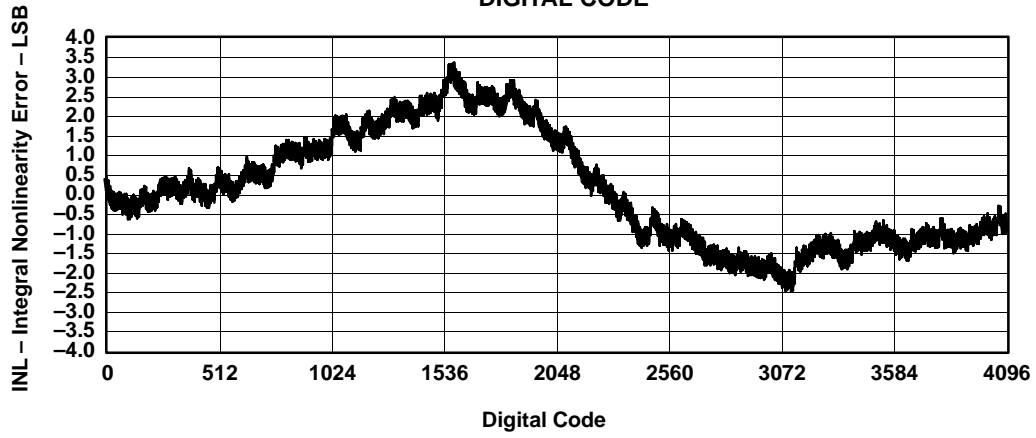


Figure 10

DIFFERENTIAL NONLINEARITY ERROR
vs
DIGITAL CODE

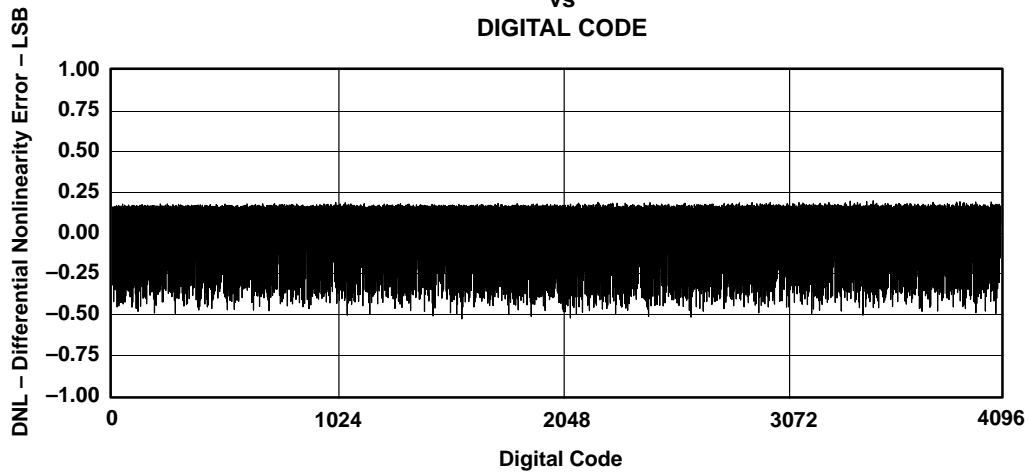


Figure 11

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APPLICATION INFORMATION

general function

The TLV5618A is a dual 12-bit, single-supply DAC, based on a resistor-string architecture. It consists of a serial interface, a speed and power down control logic, a resistor string, and a rail-to-rail output buffer.

The output voltage (full scale determined by the reference) is given by:

$$2 \text{ REF } \frac{\text{CODE}}{2^n} \text{ [V]}$$

Where REF is the reference voltage and CODE is the digital input value within the range of 0₁₀ to 2ⁿ–1, where n=12 (bits). The 16-bit data word, consisting of control bits and the new DAC value, is illustrated in the *data format* section. A power-on reset initially resets the internal latches to a defined state (all bits zero).

serial interface

A falling edge of $\overline{\text{CS}}$ starts shifting the data bit-per-bit (starting with the MSB) to the internal register on the falling edges of SCLK. After 16 bits have been transferred or $\overline{\text{CS}}$ rises, the content of the shift register is moved to the target latches (DAC A, DAC B, BUFFER, CONTROL), depending on the control bits within the data word.

Figure 12 shows examples of how to connect the TLV5618A to TMS320, SPI, and Microwire.

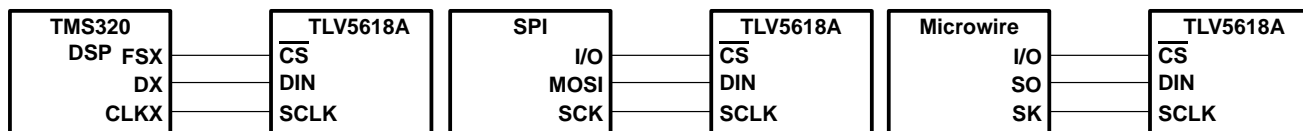


Figure 12. Three-Wire Interface

Notes on SPI and Microwire: Before the controller starts the data transfer, the software has to generate a falling edge on the pin connected to $\overline{\text{CS}}$. If the word width is 8 bits (SPI and Microwire) two write operations must be performed to program the TLV5618A. After the write operation(s), the holding registers or the control register are updated automatically on the next positive clock edge following the 16th falling clock edge.

serial clock frequency and update rate

The maximum serial clock frequency is given by:

$$f_{\text{sclkmax}} = \frac{1}{t_{\text{whmin}} + t_{\text{wlmin}}} = 20 \text{ MHz}$$

The maximum update rate is:

$$f_{\text{updatemax}} = \frac{1}{16 (t_{\text{whmin}} + t_{\text{wlmin}})} = 1.25 \text{ MHz}$$

Note that the maximum update rate is just a theoretical value for the serial interface, as the settling time of the TLV5618A should also be considered.



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APPLICATION INFORMATION

examples of operation (continued)

Both outputs are updated on the rising clock edge after D0 from the DAC A data word is sampled.

- Set power-down mode:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X

X = Don't care

linearity, offset, and gain error using single ended supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset, the output voltage may not change with the first code, depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage then remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 13.

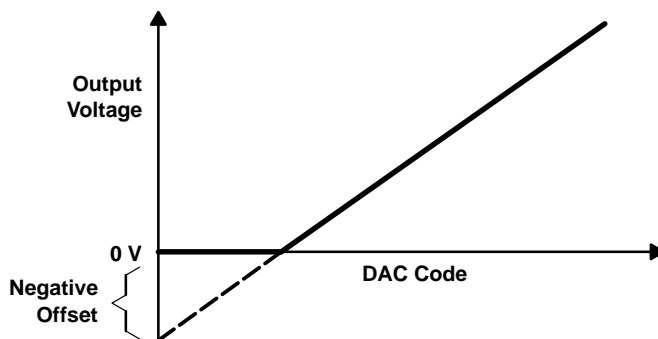


Figure 13. Effect of Negative Offset (Single Supply)

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

For a DAC, linearity is measured between zero-input code (all inputs 0) and full-scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage.

APPLICATION INFORMATION

definitions of specifications and terminology

integral nonlinearity (INL)

The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.

differential nonlinearity (DNL)

The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.

zero-scale error (E_{ZS})

Zero-scale error is defined as the deviation of the output from 0 V at a digital input value of 0.

gain error (E_G)

Gain error is the error in slope of the DAC transfer function.

total harmonic distortion (THD)

THD is the ratio of the rms value of the first six harmonic components to the value of the fundamental signal. The value for THD is expressed in decibels.

signal-to-noise ratio + distortion (S/N+D)

S/N+D is the ratio of the rms value of the output signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

spurious free dynamic range (SFDR)

Spurious free dynamic range is the difference between the rms value of the output signal and the rms value of the largest spurious signal within a specified bandwidth. The value for SFDR is expressed in decibels.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-9955701Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-9955701QPA	ACTIVE	CDIP	JG	8	1	TBD	Call TI	Call TI	
TLV5618ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV5618ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV5618ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV5618ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV5618ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLV5618ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLV5618AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV5618AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV5618AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV5618AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV5618AIP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLV5618AIPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLV5618AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
TLV5618AMJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
TLV5618AMJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
TLV5618AQD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV5618AQDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV5618AQDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV5618AQDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF TLV5618A, TLV5618AM :

- Catalog: [TLV5618A](#)
- Enhanced Product: [TLV5618A-EP](#), [TLV5618AM-EP](#)
- Military: [TLV5618AM](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV5618ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV5618AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV5618AQDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

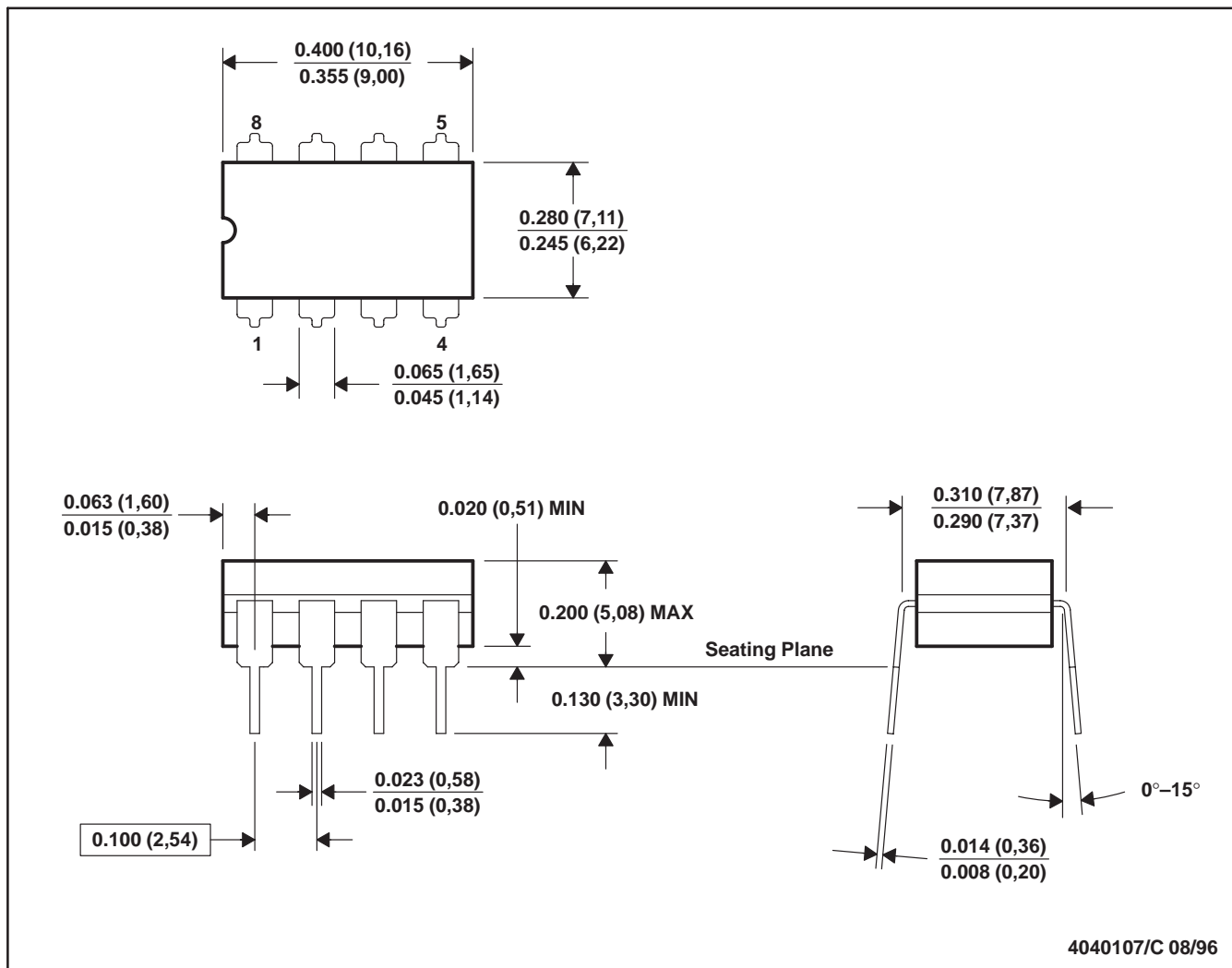


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV5618ACDR	SOIC	D	8	2500	367.0	367.0	35.0
TLV5618AIDR	SOIC	D	8	2500	367.0	367.0	35.0
TLV5618AQDR	SOIC	D	8	2500	367.0	367.0	35.0

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP1-T8

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

P (R-PDIP-T8)

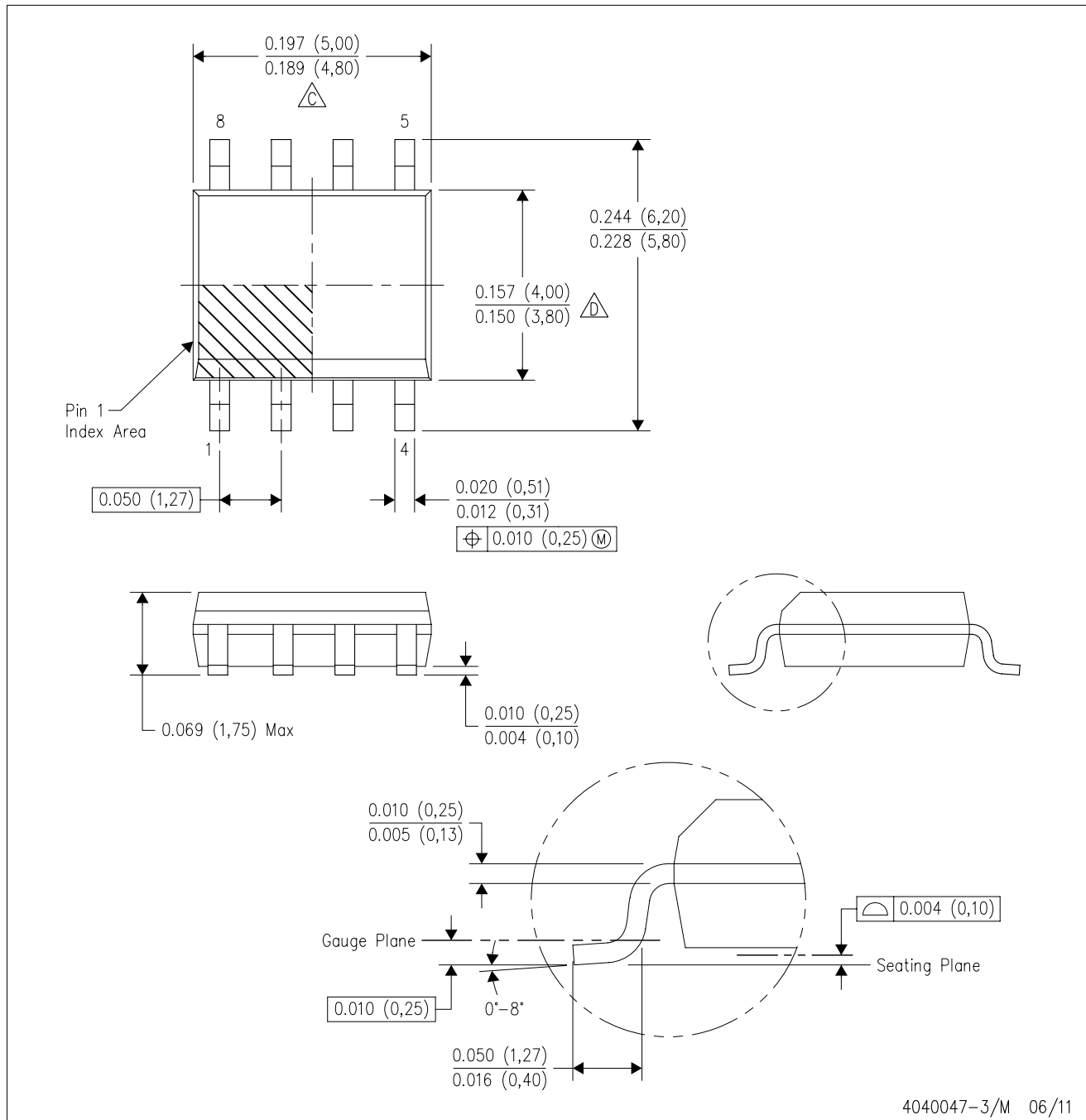
PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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