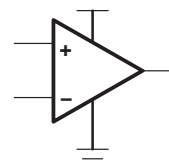


# TLV271-Q1, TLV272-Q1, TLV274-Q1 FAMILY OF 550- $\mu$ A/Ch 3-MHz RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

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- Qualification in Accordance With AEC-Q100†
- Qualified for Automotive Applications
- Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval
- Rail-To-Rail Output
- Wide Bandwidth . . . 3 MHz
- High Slew Rate . . . 2.4 V/ $\mu$ s
- Supply Voltage Range . . . 2.7 V to 16 V
- Supply Current . . . 550  $\mu$ A/Channel
- Input Noise Voltage . . . 39 nV/ $\sqrt{\text{Hz}}$
- Input Bias Current . . . 1 pA
- Specified Temperature Range –40°C to 125°C . . . Automotive Grade
- Ultrasmall Packaging – 5-Pin SOT-23 (TLV271)
- Ideal Upgrade for TLC27x Family

Operational Amplifier



† Contact Texas Instruments for details. Q100 qualification data available on request.

## description

The TLV27x takes the minimum operating supply voltage down to 2.7 V over the extended automotive temperature range while adding the rail-to-rail output swing feature. This makes it an ideal alternative to the TLC27x family for applications where rail-to-rail output swings are essential. The TLV27x also provides 3-MHz bandwidth from only 550  $\mu$ A.

Like the TLC27x, the TLV27x is fully specified for 5-V and  $\pm$ 5-V supplies. The maximum recommended supply voltage is 16 V, which allows the devices to be operated from a variety of rechargeable cells ( $\pm$ 8 V supplies down to  $\pm$ 1.35 V).

The CMOS inputs enable use in high-impedance sensor interfaces, with the lower voltage operation making an attractive alternative for the TLC27x in battery-powered applications.

The 2.7-V operation makes it compatible with Li-Ion powered systems and the operating supply voltage range of many micropower microcontrollers available today including Texas Instruments MSP430.

SELECTION OF SIGNAL AMPLIFIER PRODUCTS†

DEVICE	V <sub>DD</sub> (V)	V <sub>IO</sub> ( $\mu$ V)	I <sub>q</sub> /Ch ( $\mu$ A)	I <sub>B</sub> (pA)	GBW (MHz)	SR (V/ $\mu$ s)	SHUTDOWN	RAIL-TO-RAIL	SINGLES/DUALS/QUADS
TLV27x	2.7–16	500	550	1	3	2.4	—	O	S/D/Q
TLC27x	3–16	1100	675	1	1.7	3.6	—	—	S/D/Q
TLV237x	2.7–16	500	550	1	3	2.4	Yes	I/O	S/D/Q
TLC227x	4–16	300	1100	1	2.2	3.6	—	O	D/Q
TLV246x	2.7–6	150	550	1300	6.4	1.6	Yes	I/O	S/D/Q
TLV247x	2.7–6	250	600	2	2.8	1.5	Yes	I/O	S/D/Q
TLV244x	2.7–10	300	725	1	1.8	1.4	—	O	D/Q

† Typical values measured at 5 V, 25°C



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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# TLV271-Q1, TLV272-Q1, TLV274-Q1

## FAMILY OF 550- $\mu$ A/Ch 3-MHz RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

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FAMILY PACKAGE TABLE

DEVICE	NUMBER OF CHANNELS	PACKAGE TYPES				UNIVERSAL EVM BOARD
		SOIC	SOT-23	TSSOP	MSOP†	
TLV271	1	8	5	—	—	See the EVM Selection Guide (SLOU060)
TLV272	2	8	—	—	8	
TLV274	4	14	—	14	—	

† Product Preview

TLV271 AVAILABLE OPTIONS

T <sub>A</sub>	V <sub>IO</sub> MAX AT 25°C	PACKAGED DEVICES		
		SMALL OUTLINE (D)	SOT-23	
			(DBV)	SYMBOL
-40°C to 125°C	5 mV	TLV271QDRQ1	TLV271QDBVRQ1	271Q

TLV272 AVAILABLE OPTIONS

T <sub>A</sub>	V <sub>IO</sub> MAX AT 25°C	PACKAGED DEVICES		
		SMALL OUTLINE (D)	MSOP	
			(DGK)	SYMBOL
-40°C to 125°C	5 mV	TLV272QDRQ1	TLV272QDGKRQ1†	

† Product Preview

TLV274 AVAILABLE OPTIONS

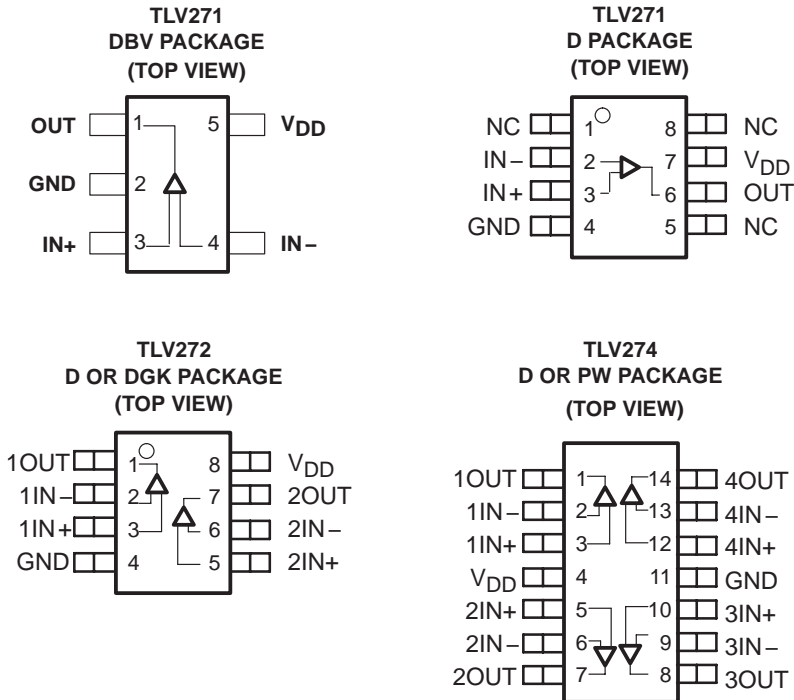
T <sub>A</sub>	V <sub>IO</sub> MAX AT 25°C	PACKAGED DEVICES	
		SMALL OUTLINE (D)	TSSOP (PW)
-40°C to 125°C	5 mV	TLV274QDRQ1	TLV274QPWRQ1



# TLV271-Q1, TLV272-Q1, TLV274-Q1 FAMILY OF 550- $\mu$ A/Ch 3-MHz RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

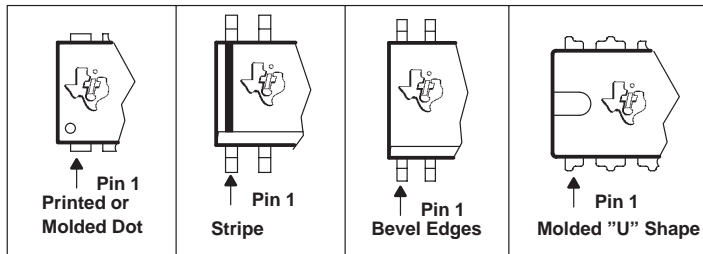
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## TLV27x PACKAGE PINOUTS(1)



NC – No internal connection  
(1) SOT-23 may or may not be indicated

## TYPICAL PIN 1 INDICATORS



# TLV271-Q1, TLV272-Q1, TLV274-Q1 FAMILY OF 550- $\mu$ A/Ch 3-MHz RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, $V_{DD}$ (see Note 1)	16.5 V
Differential input voltage, $V_{ID}$	$\pm V_{DD}$
Input voltage range, $V_I$ (see Note 1)	-0.2 V to $V_{DD} + 0.2$ V
Input current range, $I_I$	$\pm 10$ mA
Output current range, $I_O$	$\pm 100$ mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$	-40°C to 125°C
Maximum junction temperature, $T_J$	150°C
Storage temperature range, $T_{stg}$	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential voltages, are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$\theta_{JC}$ (°C/W)	$\theta_{JA}$ (°C/W)	$T_A \leq 25^\circ\text{C}$ POWER RATING	$T_A = 25^\circ\text{C}$ POWER RATING
D (8)	38.3	176	710 mW	396 mW
D (14)	26.9	122.3	1022 mW	531 mW
DBV (5)	55	324.1	385 mW	201 mW
DGK (8)	54.23	259.96	481 mW	250 mW
PW (14)	29.3	173.6	720 mW	374 mW

## recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, $V_{DD}$	Single supply	2.7	16	V
	Split supply	$\pm 1.35$	$\pm 8$	
Common-mode input voltage range, $V_{ICR}$		0	$V_{DD} - 1.35$	V
Operating free-air temperature, $T_A$	Q-suffix	-40	125	°C



**TLV271-Q1, TLV272-Q1, TLV274-Q1**  
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electrical characteristics at specified free-air temperature,  $V_{DD} = 2.7\text{ V}$ ,  $5\text{ V}$ , and  $15\text{ V}$  (unless otherwise noted)

**dc performance**

PARAMETER		TEST CONDITIONS		$T_A$ †	MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage	$V_{IC} = V_{DD}/2$ , $R_L = 10\text{ k}\Omega$ ,	$V_O = V_{DD}/2$ , $R_S = 50\ \Omega$	25°C	0.5		5	mV
				Full range			7	
$\alpha_{VIO}$	Offset voltage drift			25°C		2		$\mu\text{V}/^\circ\text{C}$
$CMRR$	Common-mode rejection ratio	$V_{IC} = 0\text{ to }V_{DD}-1.35\text{V}$ , $R_S = 50\ \Omega$	$V_{DD} = 2.7\text{ V}$	25°C	53		70	dB
				Full range		54		
		$V_{IC} = 0\text{ to }V_{DD}-1.35\text{V}$ , $R_S = 50\ \Omega$	$V_{DD} = 5\text{ V}$	25°C	58		80	
				Full range		57		
		$V_{IC} = 0\text{ to }V_{DD}-1.35\text{V}$ , $R_S = 50\ \Omega$	$V_{DD} = 15\text{ V}$	25°C	67		85	
				Full range		66		
$A_{VD}$	Large-signal differential voltage amplification	$V_{O(PP)} = V_{DD}/2$ , $R_L = 10\text{ k}\Omega$	$V_{DD} = 2.7\text{ V}$	25°C	95		106	dB
				Full range		76		
			$V_{DD} = 5\text{ V}$	25°C	80		110	
				Full range		82		
			$V_{DD} = 15\text{ V}$	25°C	77		115	
				Full range		79		

† Full range is  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ . If not specified, full range is  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ .

**input characteristics**

PARAMETER		TEST CONDITIONS		$T_A$	MIN	TYP	MAX	UNIT
$I_{IO}$	Input offset current	$V_{DD} = 15\text{ V}$ ,	$V_{IC} = V_{DD}/2$ ,	25°C		1	60	pA
				125°C			1000	
$I_{IB}$	Input bias current	$V_{IC} = V_{DD}/2$ ,	$R_S = 50\ \Omega$	25°C		1	60	pA
				125°C			1000	
$r_{i(d)}$	Differential input resistance			25°C		1000		$\text{G}\Omega$
$C_{IC}$	Common-mode input capacitance		$f = 21\text{ kHz}$	25°C		8		pF



**TLV271-Q1, TLV272-Q1, TLV274-Q1**  
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electrical characteristics at specified free-air temperature,  $V_{DD} = 2.7\text{ V}$ ,  $5\text{ V}$ , and  $15\text{ V}$  (unless otherwise noted)

**output characteristics**

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	MIN	TYP	MAX	UNIT
$V_{OH}$ High-level output voltage	$V_{IC} = V_{DD}/2, I_{OH} = -1\text{ mA}$	$V_{DD} = 2.7\text{ V}$	25°C	2.55	2.58	V
			Full range	2.48		
		$V_{DD} = 5\text{ V}$	25°C	4.9	4.93	
			Full range	4.85		
		$V_{DD} = 15\text{ V}$	25°C	14.92	14.96	
			Full range	14.9		
	$V_{IC} = V_{DD}/2, I_{OH} = -5\text{ mA}$	$V_{DD} = 2.7\text{ V}$	25°C	1.88	2.1	
			Full range	1.42		
		$V_{DD} = 5\text{ V}$	25°C	4.58	4.68	
			Full range	4.44		
		$V_{DD} = 15\text{ V}$	25°C	14.7	14.8	
			Full range	14.6		
$V_{OL}$ Low-level output voltage	$V_{IC} = V_{DD}/2, I_{OL} = 1\text{ mA}$	$V_{DD} = 2.7\text{ V}$	25°C	0.1	0.15	V
			Full range		0.22	
		$V_{DD} = 5\text{ V}$	25°C	0.05	0.1	
			Full range		0.15	
		$V_{DD} = 15\text{ V}$	25°C	0.05	0.08	
			Full range		0.1	
	$V_{IC} = V_{DD}/2, I_{OL} = 5\text{ mA}$	$V_{DD} = 2.7\text{ V}$	25°C	0.5	0.7	
			Full range		1.15	
		$V_{DD} = 5\text{ V}$	25°C	0.28	0.4	
			Full range		0.54	
		$V_{DD} = 15\text{ V}$	25°C	0.19	0.3	
			Full range		0.35	
$I_O$ Output current	$V_O = 0.5\text{ V from rail}, V_{DD} = 2.7\text{ V}$	Positive rail	25°C	4	mA	
		Negative rail	25°C	5		
	$V_O = 0.5\text{ V from rail}, V_{DD} = 5\text{ V}$	Positive rail	25°C	7		
		Negative rail	25°C	8		
	$V_O = 0.5\text{ V from rail}, V_{DD} = 15\text{ V}$	Positive rail	25°C	13		
		Negative rail	25°C	12		

$^\dagger$  Full range is  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ . If not specified, full range is  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ .

$^\ddagger$  Depending on package dissipation rating



**TLV271-Q1, TLV272-Q1, TLV274-Q1**  
**FAMILY OF 550- $\mu$ A/Ch 3-MHz RAIL-TO-RAIL OUTPUT**  
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electrical characteristics at specified free-air temperature,  $V_{DD} = 2.7\text{ V}$ ,  $5\text{ V}$ , and  $15\text{ V}$  (unless otherwise noted) (continued)

**power supply**

PARAMETER		TEST CONDITIONS	$T_A$ †	MIN	TYP	MAX	UNIT
$I_{DD}$	Supply current (per channel)	$V_O = V_{DD}/2$	$V_{DD} = 2.7\text{ V}$	25°C	470	560	$\mu\text{A}$
			$V_{DD} = 5\text{ V}$	25°C	550	660	
			$V_{DD} = 15\text{ V}$	25°C	750	900	
				Full range		1200	
PSRR	Supply voltage rejection ratio ( $\Delta V_{DD} / \Delta V_{IO}$ )	$V_{DD} = 2.7\text{ V to } 15\text{ V}$ , No load	$V_{IC} = V_{DD}/2$	25°C	70	80	dB
				Full range	65		

† Full range is  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ . If not specified, full range is  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ .

**dynamic performance**

PARAMETER		TEST CONDITIONS	$T_A$ †	MIN	TYP	MAX	UNIT
UGBW	Unity gain bandwidth	$R_L = 2\text{ k}\Omega$ , $C_L = 10\text{ pF}$	$V_{DD} = 2.7\text{ V}$	25°C	2.4		MHz
			$V_{DD} = 5\text{ V to } 15\text{ V}$	25°C	3		
SR	Slew rate at unity gain	$V_{O(PP)} = V_{DD}/2$ , $C_L = 50\text{ pF}$ , $R_L = 10\text{ k}\Omega$ ,	$V_{DD} = 2.7\text{ V}$	25°C	1.4	2.1	$\text{V}/\mu\text{s}$
				Full range	1		
			$V_{DD} = 5\text{ V}$	25°C	1.4	2.4	$\text{V}/\mu\text{s}$
				Full range	1.2		
			$V_{DD} = 15\text{ V}$	25°C	1.9	2.1	$\text{V}/\mu\text{s}$
				Full range	1.4		
$\phi_m$	Phase margin	$R_L = 2\text{ k}\Omega$	$C_L = 10\text{ pF}$	25°C	65		$^\circ$
	Gain margin	$R_L = 2\text{ k}\Omega$	$C_L = 10\text{ pF}$	25°C	18		dB
$t_s$	Settling time	$V_{DD} = 2.7\text{ V}$ , $V(\text{STEP})_{PP} = 1\text{ V}$ , $A_V = -1$ , $C_L = 10\text{ pF}$ , $R_L = 2\text{ k}\Omega$	0.1%	25°C	2.9		$\mu\text{s}$
		$V_{DD} = 5\text{ V, } 15\text{ V}$ , $V(\text{STEP})_{PP} = 1\text{ V}$ , $A_V = -1$ , $C_L = 47\text{ pF}$ , $R_L = 2\text{ k}\Omega$	0.1%		2		

† Full range is  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ . If not specified, full range is  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ .

**noise/distortion performance**

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
THD + N	Total harmonic distortion plus noise	$V_{DD} = 2.7\text{ V}$ , $V_{O(PP)} = V_{DD}/2\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $f = 10\text{ kHz}$	$A_V = 1$	25°C	0.02%		
			$A_V = 10$		0.05%		
			$A_V = 100$		0.18%		
		$V_{DD} = 5\text{ V, } \pm 5\text{ V}$ , $V_{O(PP)} = V_{DD}/2\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $f = 10\text{ K}$	$A_V = 1$	25°C	0.02%		
			$A_V = 10$		0.09%		
			$A_V = 100$		0.5%		
$V_n$	Equivalent input noise voltage	$f = 1\text{ kHz}$	25°C	39		$\text{nV}/\sqrt{\text{Hz}}$	
		$f = 10\text{ kHz}$		35			
$I_n$	Equivalent input noise current	$f = 1\text{ kHz}$	25°C	0.6		$\text{fA}/\sqrt{\text{Hz}}$	



**TLV271-Q1, TLV272-Q1, TLV274-Q1**  
**FAMILY OF 550- $\mu$ A/Ch 3-MHz RAIL-TO-RAIL OUTPUT**  
**OPERATIONAL AMPLIFIERS**

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**TYPICAL CHARACTERISTICS**

**Table of Graphs**

			<b>FIGURE</b>
CMRR	Common-mode rejection ratio	vs Frequency	1
	Input bias and offset current	vs Free-air temperature	2
V <sub>OL</sub>	Low-level output voltage	vs Low-level output current	3, 5, 7
V <sub>OH</sub>	High-level output voltage	vs High-level output current	4, 6, 8
V <sub>O(PP)</sub>	Peak-to-peak output voltage	vs Frequency	9
I <sub>DD</sub>	Supply current	vs Supply voltage	10
PSRR	Power supply rejection ratio	vs Frequency	11
A <sub>VD</sub>	Differential voltage gain & phase	vs Frequency	12
	Gain-bandwidth product	vs Free-air temperature	13
SR	Slew rate	vs Supply voltage	14
		vs Free-air temperature	15
$\phi_m$	Phase margin	vs Capacitive load	16
V <sub>n</sub>	Equivalent input noise voltage	vs Frequency	17
	Voltage-follower large-signal pulse response		18, 19
	Voltage-follower small-signal pulse response		20
	Inverting large-signal response		21, 22
	Inverting small-signal response		23
	Crosstalk	vs Frequency	24



TYPICAL CHARACTERISTICS

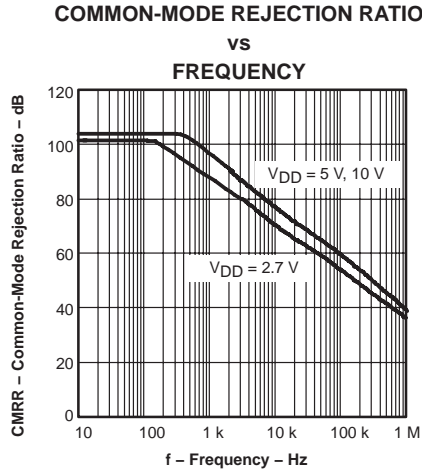


Figure 1

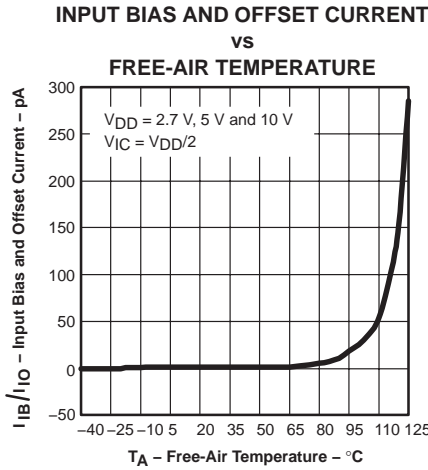


Figure 2

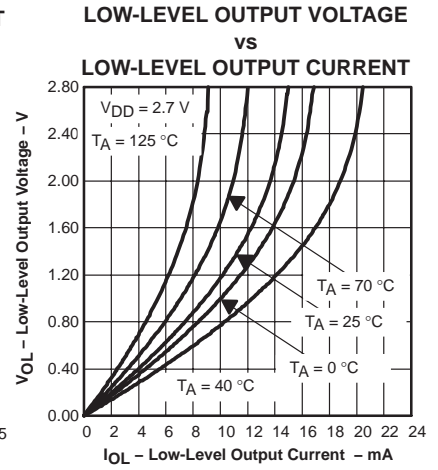


Figure 3

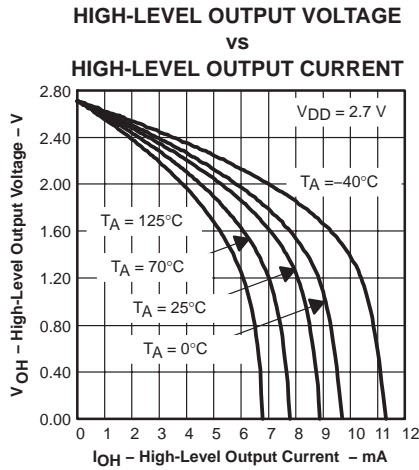


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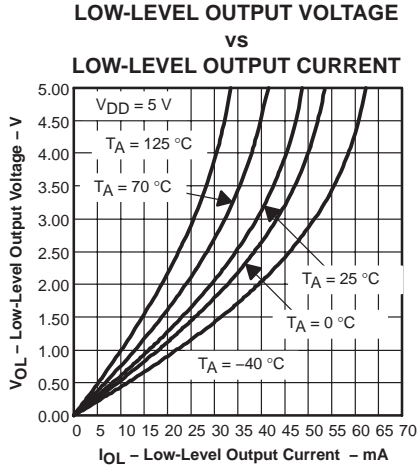


Figure 5

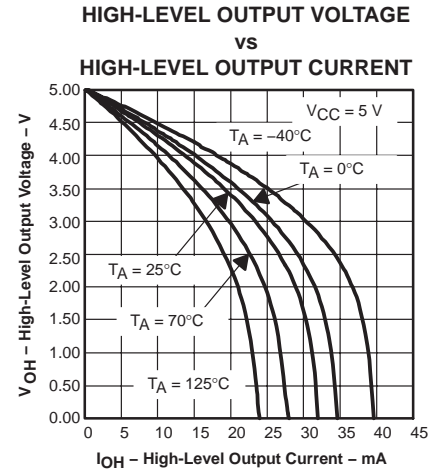


Figure 6

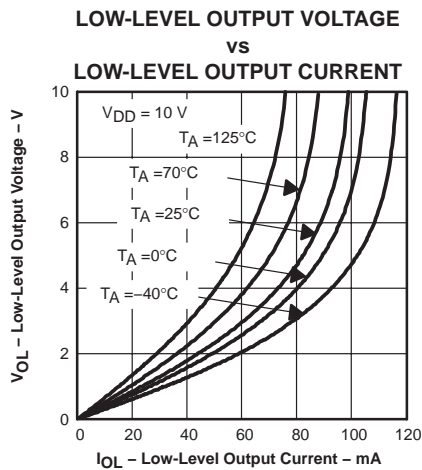


Figure 7

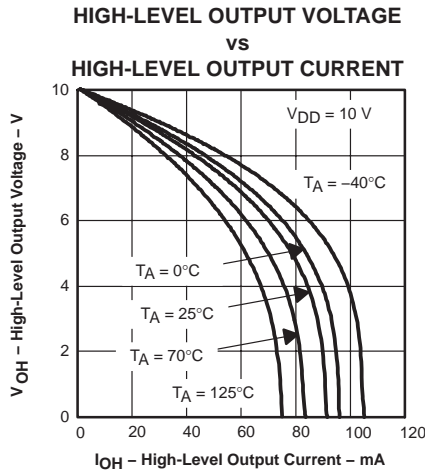


Figure 8

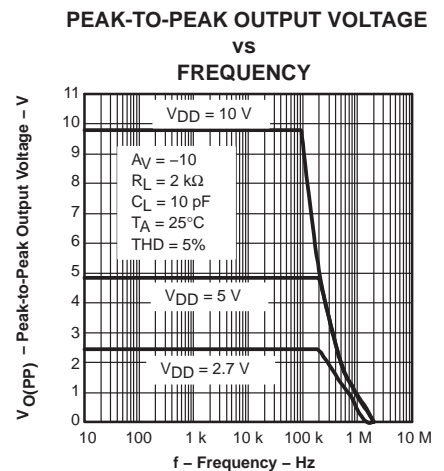
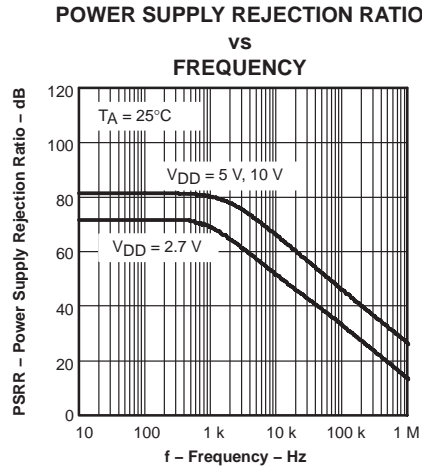
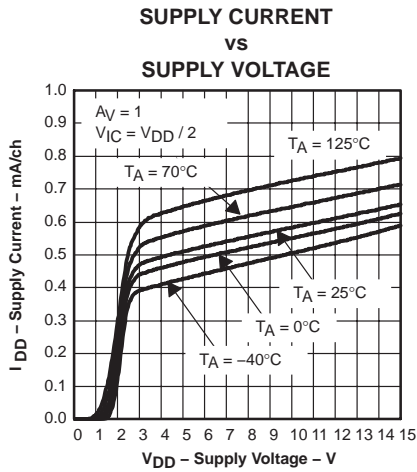


Figure 9

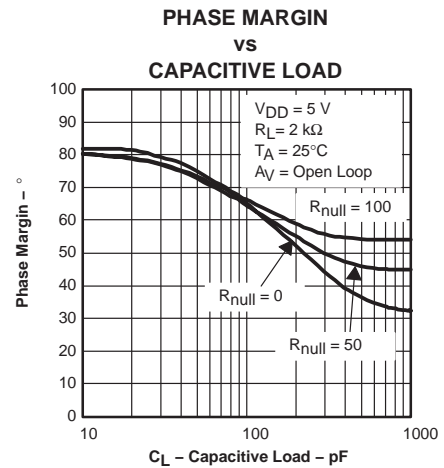
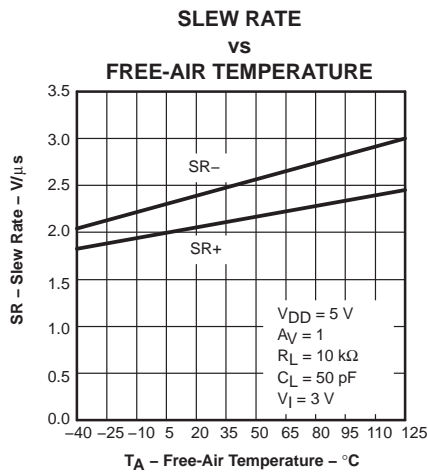
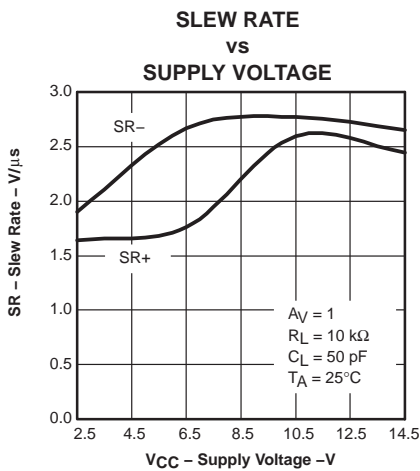
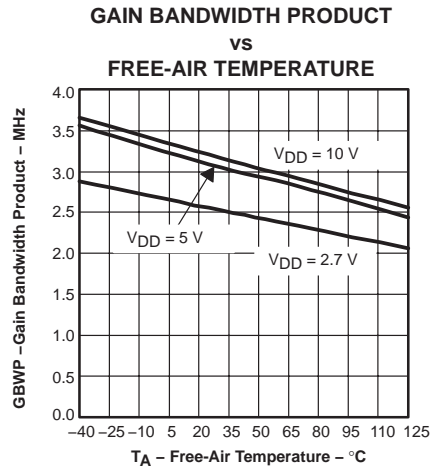
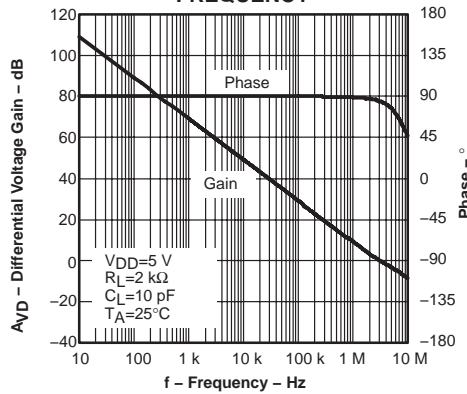
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## TYPICAL CHARACTERISTICS



**DIFFERENTIAL VOLTAGE GAIN AND PHASE  
vs  
FREQUENCY**



TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE

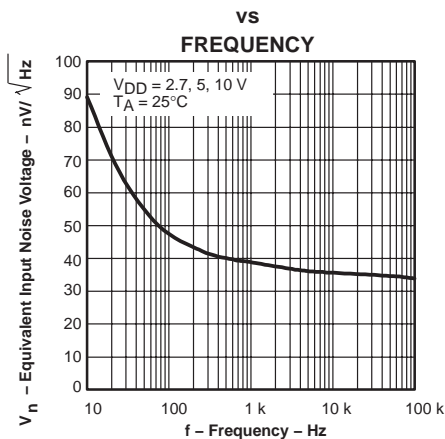


Figure 17

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

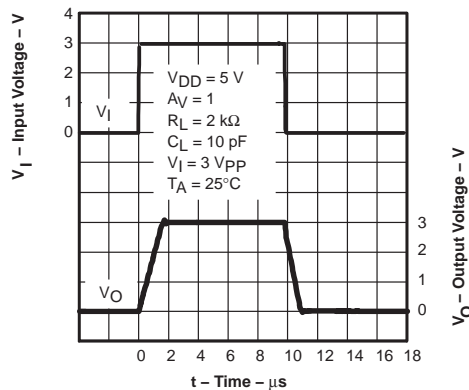


Figure 18

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

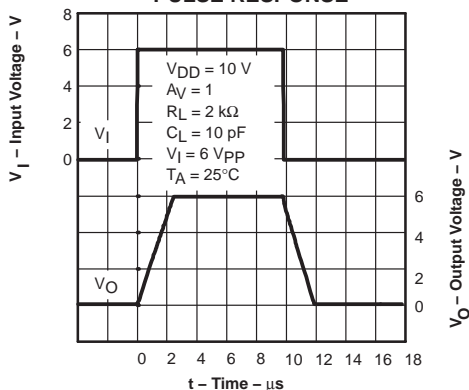


Figure 19

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

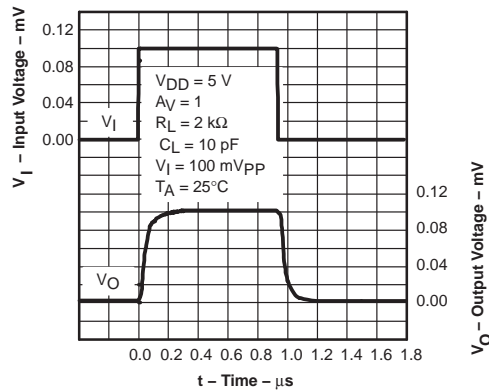


Figure 20

INVERTING LARGE-SIGNAL RESPONSE

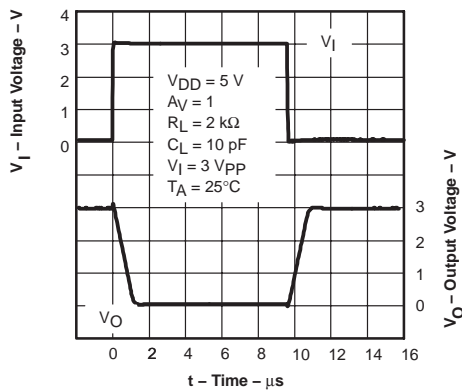


Figure 21

INVERTING LARGE-SIGNAL RESPONSE

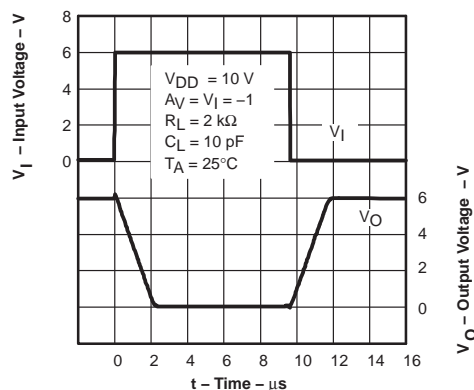


Figure 22

# TLV271-Q1, TLV272-Q1, TLV274-Q1 FAMILY OF 550- $\mu$ A/Ch 3-MHz RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

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## TYPICAL CHARACTERISTICS

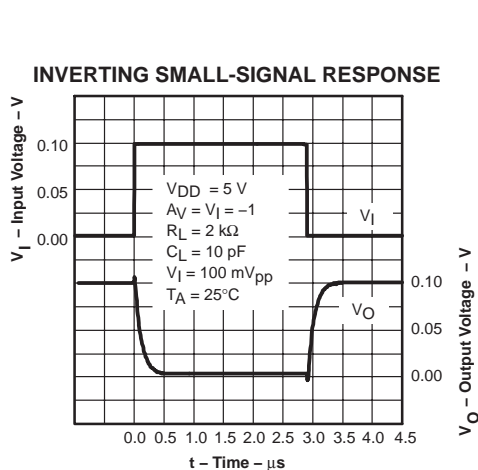


Figure 23

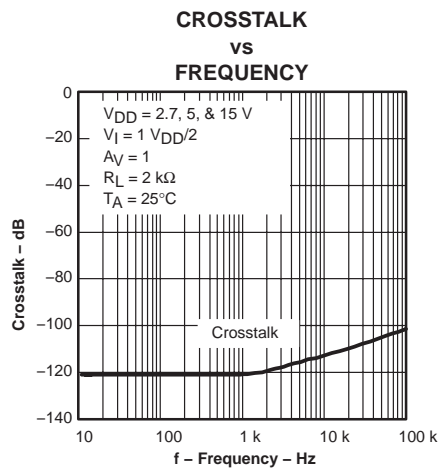


Figure 24

## APPLICATION INFORMATION

### driving a capacitive load

When the amplifier is configured in this manner, capacitive loading directly on the output decreases the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series ( $R_{NULL}$ ) with the output of the amplifier, as shown in Figure 25. A minimum value of 20  $\Omega$  should work well for most applications.

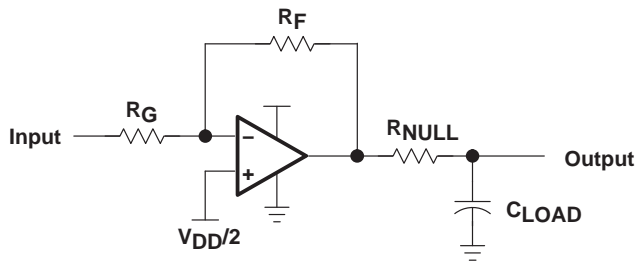


Figure 25. Driving a Capacitive Load

APPLICATION INFORMATION

offset voltage

The output offset voltage ( $V_{OO}$ ) is the sum of the input offset voltage ( $V_{IO}$ ) and both input bias currents ( $I_{IB}$ ) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

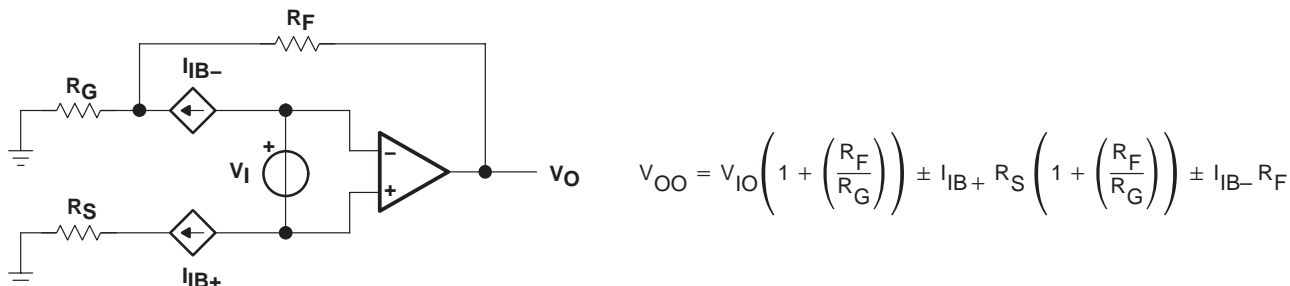


Figure 26. Output Offset Voltage Model

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 27).

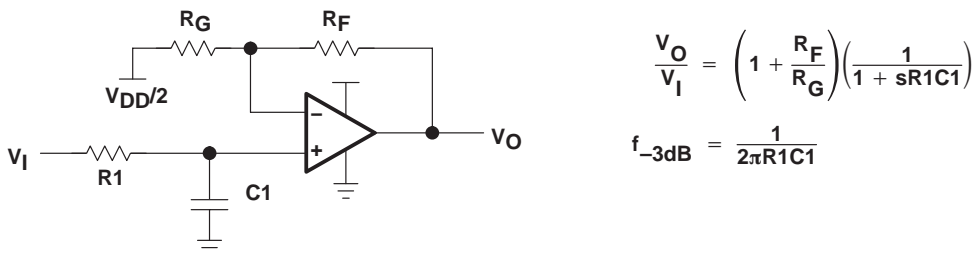


Figure 27. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For the best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

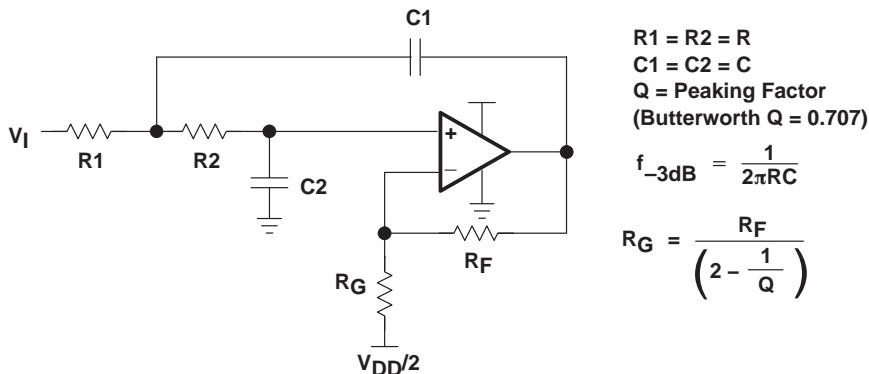


Figure 28. 2-Pole Low-Pass Sallen-Key Filter

# TLV271-Q1, TLV272-Q1, TLV274-Q1 FAMILY OF 550- $\mu$ A/Ch 3-MHz RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

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## APPLICATION INFORMATION

### circuit layout considerations

To achieve the levels of high performance of the TLV27x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes—It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling—Use a 6.8- $\mu$ F tantalum capacitor in parallel with a 0.1- $\mu$ F ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1- $\mu$ F ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1- $\mu$ F capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets—Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements—Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This helps to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components—Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

### APPLICATION INFORMATION

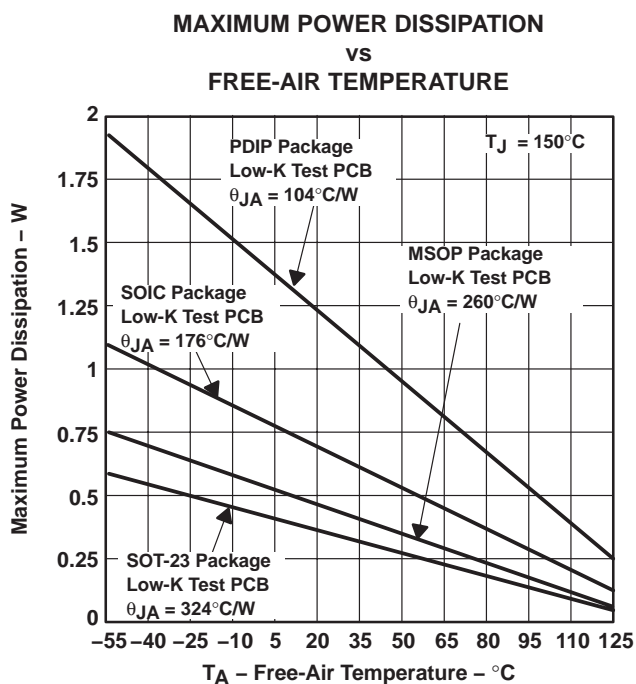
#### general power dissipation considerations

For a given  $\theta_{JA}$ , the maximum power dissipation is shown in Figure 29 and is calculated by the following formula:

$$P_D = \left( \frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

- $P_D$  = Maximum power dissipation of TLV27x IC (watts)
- $T_{MAX}$  = Absolute maximum junction temperature (150°C)
- $T_A$  = Free-ambient air temperature (°C)
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- $\theta_{JC}$  = Thermal coefficient from junction to case
- $\theta_{CA}$  = Thermal coefficient from case to ambient air (°C/W)



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

**Figure 29. Maximum Power Dissipation vs Free-Air Temperature**

# TLV271-Q1, TLV272-Q1, TLV274-Q1 FAMILY OF 550- $\mu$ A/Ch 3-MHz RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

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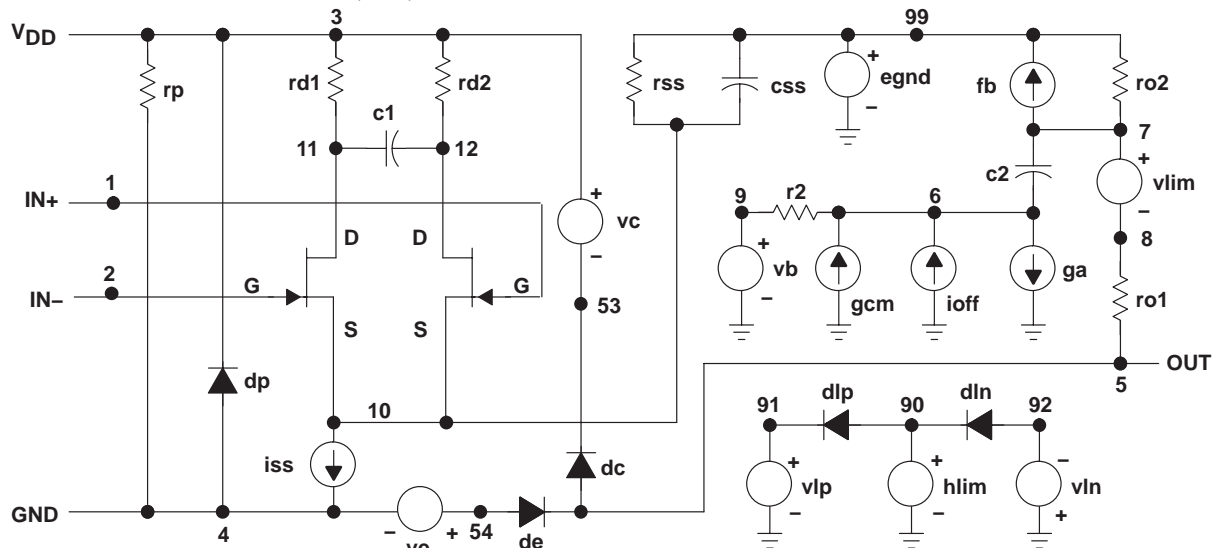
## APPLICATION INFORMATION

### macromodel information

Macromodel information provided was derived using Microsim *Parts*™ Release 9.1, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 2) and subcircuit in Figure 30 are generated using TLV27x typical electrical and operating characteristics at  $T_A = 25^\circ\text{C}$ . Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 2: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).



\*DEVICE=amp\_tlv27x\_highVdd,OP AMP,NJF,INT  
\* amp\_tlv\_27x\_highVdd operational amplifier "macromodel"  
\* subcircuit updated using Model Editor release 9.1 on 05/15/00  
\* at 14:40 Model Editor is an OrCAD product.

\* connections:

```

non-inverting input
inverting input
positive power supply
negative power supply
output
    
```

.subckt amp\_tlv27x\_highVdd

```

1 2 3 4 5
c1 11 12 457.48E-15
c2 6 7 5.0000E-12
css 10 99 1.1431E-12
dc 5 53 dy
de 54 5 dy
dip 90 91 dx
din 92 90 dx
dp 4 3 dx
egnd 99 0 poly(2) (3,0) (4,0) 0 .5 .5
fb 7 99 poly(5) vb vc ve vlp vln 0
176.02E6 -1E3 1E3 180E6
-180E6
    
```

```

ga 6 0 11 12 16.272E-6
gcm 0 6 10 99 6.8698E-9
iss 10 4 dc 1.3371E-6
hlim 90 0 vlim 1K
j1 11 2 10 jx1
J2 12 1 10 jx2
r2 6 9 100.00E3
rd1 3 11 61.456E3
rd2 3 12 61.456E3
ro1 8 5 10
ro2 7 99 10
rp 3 4 150.51E3
rss 10 99 149.58E6
vb 9 0 dc 0
vc 3 53 dc .78905
ve 54 4 dc .78905
vlim 7 8 dc 0
vlp 91 0 dc 14.200
vln 0 92 dc 14.200
.model dx D(Is=800.00E-18)
.model dy D(Is=800.00E-18 Rs=1m Cjo=10p)
.model jx1 NJF(Is=500.00E-15 Beta=198.03E-6 Vto=-1)
.model jx2 NJF(Is=500.00E-15 Beta=198.03E-6 Vto=-1)
.ends
    
```

Figure 30. Boyle Macromodel and Subcircuit

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POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TLV271QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV271QDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV271QDRQ1	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
TLV272QDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV272QDRQ1	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
TLV274QDRG4Q1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV274QDRQ1	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
TLV274QPWRQ1	ACTIVE	TSSOP	PW	14	2000	TBD	CU NIPDAU	Level-1-250C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

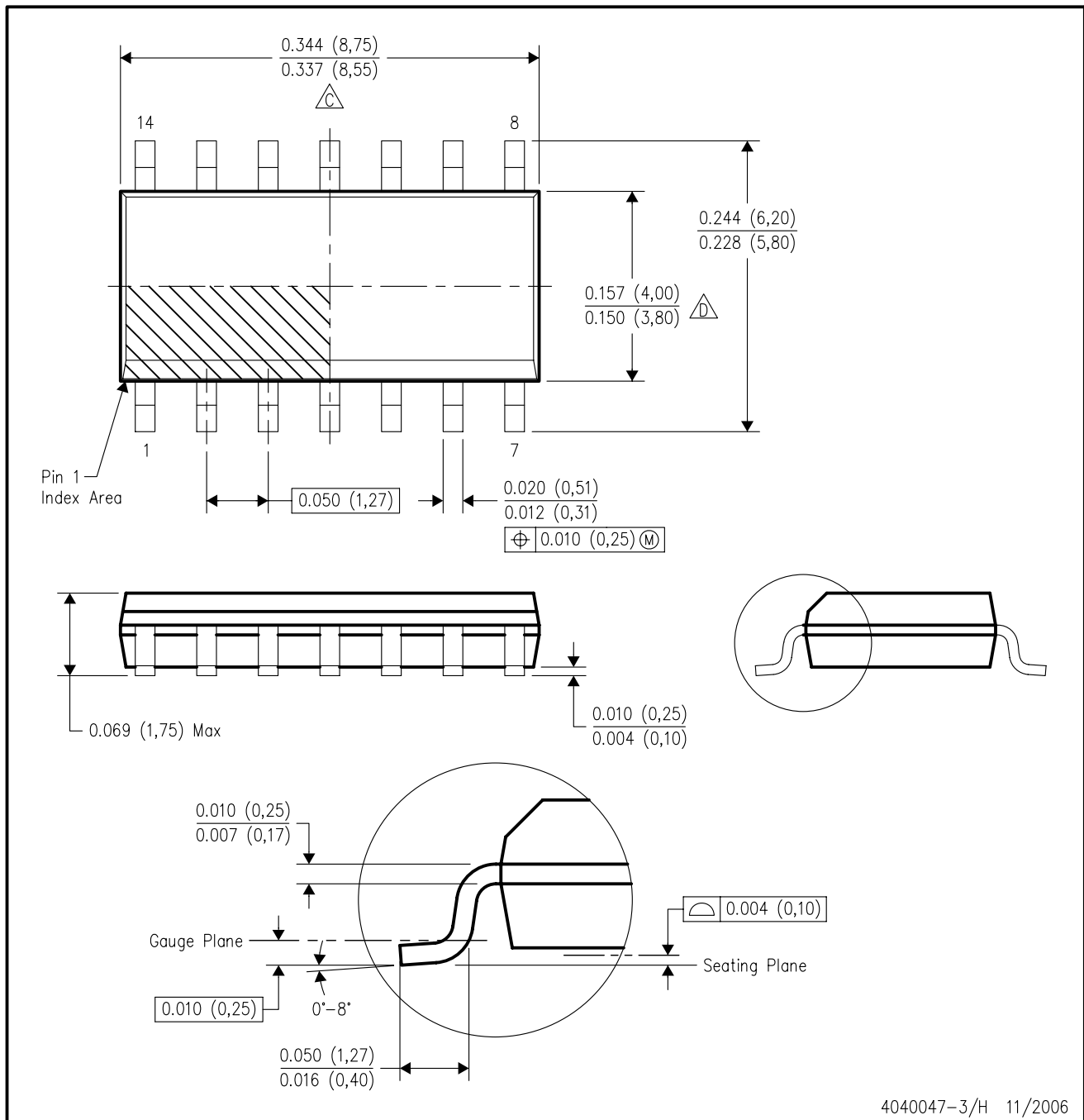
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D (R-PDSO-G14)

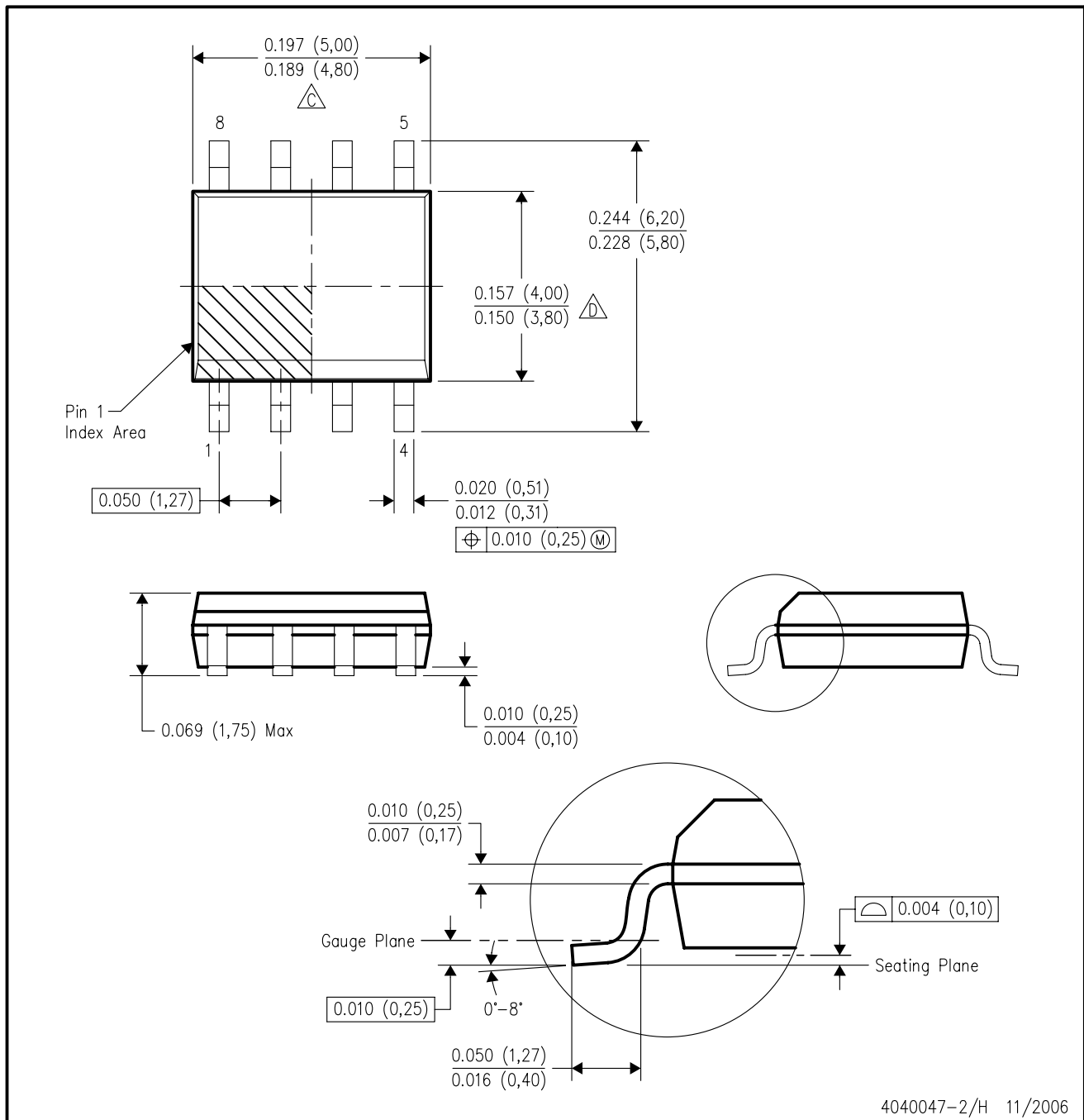
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



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  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AA.

PW (R-PDSO-G\*\*)

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14 PINS SHOWN



4040064/F 01/97

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Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
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