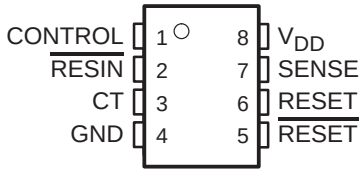
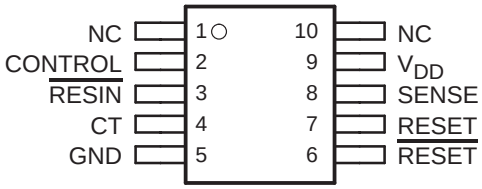
- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **Precision Voltage Sensor**
- **Temperature-Compensated Voltage Reference**
- **Programmable Delay Time by External Capacitor**
- **Supply Voltage Range . . . 2 V to 6 V**
- **Defined $\overline{\text{RESET}}$ Output from $V_{DD} \geq 1$ V**
- **Power-Down Control Support for Static RAM With Battery Backup**
- **Maximum Supply Current of 16 μA**
- **Power Saving Totem-Pole Outputs**
- **Temperature Range . . . Up to −55°C to 125°C**

D, JG, P OR PW PACKAGE
(TOP VIEW)



U PACKAGE
(TOP VIEW)



description

The TLC77xx family of micropower supply voltage supervisors provide reset control, primarily in microcomputer and microprocessor systems.

During power-on, $\overline{\text{RESET}}$ is asserted when V_{DD} reaches 1 V. After minimum V_{DD} (≥ 2 V) is established, the circuit monitors SENSE voltage and keeps the reset outputs active as long as SENSE voltage ($V_{I(SENSE)}$) remains below the threshold voltage. An internal timer delays return of the output to the inactive state to ensure proper system reset. The delay time, t_d, is determined by an external capacitor:

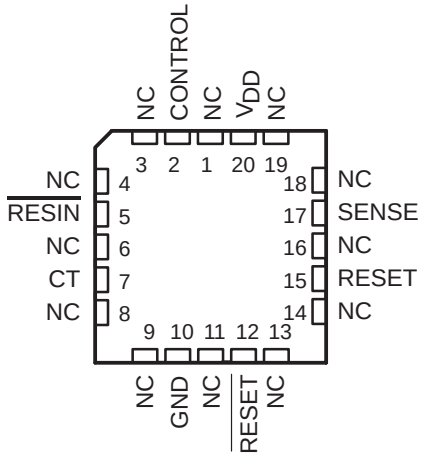
$$t_d = 2.1 \times 10^4 \times C_T$$

Where

C_T is in farads

t_d is in seconds

FK PACKAGE
(TOP VIEW)



Except for the TLC7701, which can be customized with two external resistors, each supervisor has a fixed SENSE threshold voltage set by an internal voltage divider. When SENSE voltage drops below the threshold voltage, the outputs become active and stay in that state until SENSE voltage returns above threshold voltage and the delay time, t_d, has expired.

description (continued)

In addition to the power-on-reset and undervoltage-supervisor function, the TLC77xx adds power-down control support for static RAM. When CONTROL is tied to GND, RESET will act as active high. The voltage monitor contains additional logic intended for control of static memories with battery backup during power failure. By driving the chip select ($\overline{CS}$) of the memory circuit with the RESET output of the TLC77xx and with the CONTROL driven by the memory bank select signal ($\overline{CSH1}$) of the microprocessor (see Figure 10), the memory circuit is automatically disabled during a power loss. (In this application the TLC77xx power has to be supplied by the battery.)

The TLC77xxI is characterized for operation over a temperature range of −40°C to 85°C; the TLC77xxQ is characterized for operation over a temperature range of −40°C to 125°C; and the TLC77xxM is characterized for operation over the full Military temperature range of −55°C to 125°C.

AVAILABLE OPTIONS

T_A	THRESHOLD VOLTAGE (V)	PACKAGED DEVICES					
		SMALL OUTLINE (D)†	CHIP CARRIER (FK)	CERAMIC DIP (JG)	CERAMIC DUAL FLATPACK (U)	PLASTIC DIP (P)	THIN SHRINK SMALL OUTLINE (PW)‡
−40°C to 85°C	1.1	TLC7701ID	—	—	—	TLC7701IP	TLC7701IPWR
	2.25	TLC7725ID	—	—	—	TLC7725IP	TLC7725IPWR
	2.63	TLC7703ID	—	—	—	TLC7703IP	TLC7703IPWR
	2.93	TLC7733ID	—	—	—	TLC7733IP	TLC7733IPWR
	4.55	TLC7705ID	—	—	—	TLC7705IP	TLC7705IPWR
−40°C to 125°C	1.1	TLC7701QD	—	—	—	TLC7701QP	TLC7701QPWR
	2.25	TLC7725QD	—	—	—	TLC7725QP	TLC7725QPWR
	2.63	TLC7703QD	—	—	—	TLC7703QP	TLC7703QPWR
	2.93	TLC7733QD	—	—	—	TLC7733QP	TLC7733QPWR
	4.55	TLC7705QD	—	—	—	TLC7705QP	TLC7705QPWR
−55°C to 125°C	2.93	—	TLC7733MFK	TLC7733MJG	—	—	—
	4.55	—	TLC7705MFK	TLC7705MJG	TLC7705MU	—	—

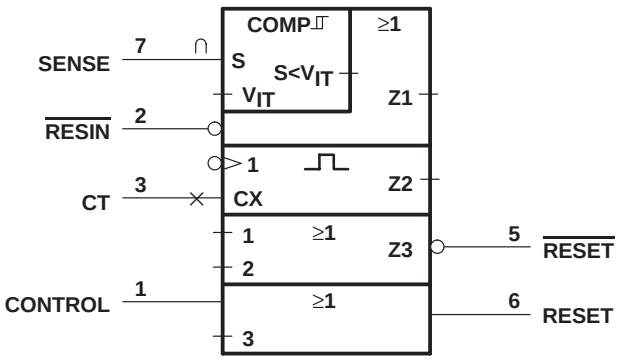
† The D package is available taped and reeled. Add the suffix R to the device type when ordering (e.g., TLC7705QDR).
‡ The PW package is only available left-end taped and reeled (indicated by the R suffix on the device type; e.g., TLC7705QPWR).

FUNCTION TABLE

CONTROL	$\overline{RESIN}$	$V_{I(SENSE)} > V_{IT+}$	RESET	$\overline{RESET}$
L	L	False	H	L
L	L	True	H	L
L	H	False	H	L
L	H	True	L§	H§
H	L	False	H	L
H	L	True	H	L
H	H	False	H	L
H	H	True	H	H§

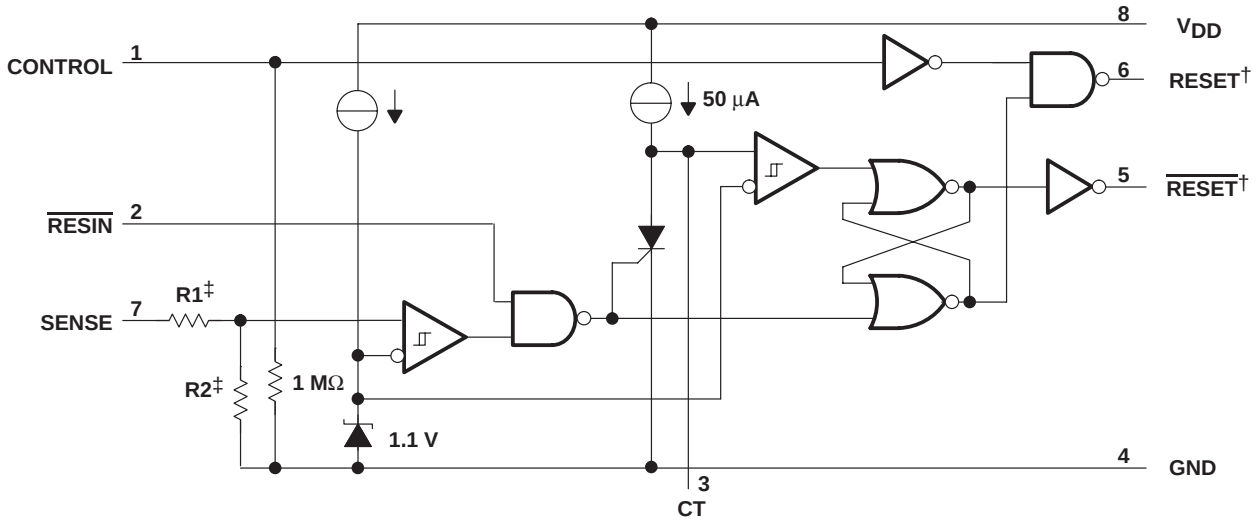
§ RESET and $\overline{RESET}$ states shown are valid for $t > t_d$.

logic symbol¶



¶ This symbol is in accordance with ANSI/IEEE Std 91−1984 and IEC Publication 617-12.

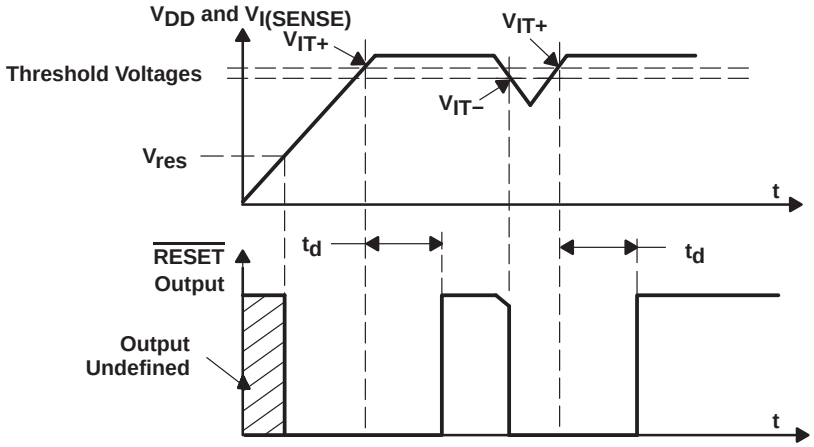
functional block diagram



† Outputs are totem-pole configuration. External pullup or pulldown resistors are not required.
‡ Nominal values:

	R1 (Typ)	R2 (Typ)
TLC7701	0	∞
TLC7725	600 kΩ	600 kΩ
TLC7703	698 kΩ	502 kΩ
TLC7733	750 kΩ	450 kΩ
TLC7705	910 kΩ	290 kΩ

timing diagram



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 7 V
Input voltage range, CONTROL, $\overline{\text{RESIN}}$, SENSE (see Note 1) . . . . . −0.3 V to 7 V
Maximum low output current, I_{OL} . . . . . 10 mA
Maximum high output current, I_{OH} . . . . . −10 mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$) . . . . . ±10 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) . . . . . ±10 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: TL77xxI . . . . . −40°C to 85°C
TL77xxQ . . . . . −40°C to 125°C
TL77xxM . . . . . −55°C to 125°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	546 mW	210 mW
P	1000 mW	8.0 mW/°C	520 mW	200 mW
PW	525 mW	4.2 mW/°C	273 mW	105 mW
U	700 mW	5.5 mW/°C	370 mW	150 mW

recommended operating conditions at specified temperature range

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	6	V
Input voltage, V_I		0	V_{DD}	V
High-level input voltage at $\overline{\text{RESIN}}$ and CONTROL‡, V_{IH}		$0.7\times V_{DD}$		V
Low-level input voltage at $\overline{\text{RESIN}}$ and CONTROL‡, V_{IL}			$0.2\times V_{DD}$	V
High-level output current, I_{OH}	$V_{DD} \ge 2.7$ V		−2	mA
Low-level output current, I_{OL}	$V_{DD} \ge 2.7$ V		2	mA
Input transition rise and fall rate at $\overline{\text{RESIN}}$ and CONTROL, $\Delta t/\Delta V$			100	ns/V
Operating free-air temperature range, T_A	TLC77xxI	−40	85	°C
	TLC77xxQ	−40	125	
Operating free-air temperature range, T_A	TLC77xxM	−55	125	°C

‡ To ensure a low supply current, V_{IL} should be kept < 0.3 V and $V_{IH} > V_{DD} - 0.3$ V.

electrical characteristics over recommended operating conditions (see Note 2) (unless otherwise noted)

PARAMETER				TEST CONDITIONS	TLC77xx			UNIT
					MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −20 μA		V_{DD} = 2 V	1.8			V
				V_{DD} = 2.7 V	2.5			
				V_{DD} = 4.5 V	4.3			
		I_{OH} = −2 mA		V_{DD} = 4.5 V	3.7			
V_{OL}	Low-level output voltage	I_{OL} = 20 μA		V_{DD} = 2 V			0.2	V
				V_{DD} = 2.7 V			0.2	
				V_{DD} = 4.5 V			0.2	
		I_{OL} = 2 mA		V_{DD} = 4.5 V			0.5	
V_{IT-}	Negative-going input threshold voltage, SENSE (see Note 3)		TLC7701	V_{DD} = 2 V to 6 V	1.04	1.1	1.16	V
			TLC7725		2.18	2.25	2.32	
			TLC7703		2.56	2.63	2.70	
			TLC7733		2.86	2.93	3	
			TLC7705		4.47	4.55	4.63	
V_{hys}	Hysteresis voltage, SENSE		TLC7701	V_{DD} = 2 V to 6 V		30		mV
			TLC7725	V_{DD} = 2 V to 6 V		70		mV
			TLC7703,					
			TLC7733,					
			TLC7705					
V_{res}	Power-up reset voltage‡			I_{OL} = 20 μA			1	V
I_I	Input current	$\overline{RESIN}$		V_I = 0 V to V_{DD}			2	μA
		CONTROL		V_I = V_{DD}		7	15	
		SENSE		V_I = 5 V		5	10	
		SENSE, TLC7701 only		V_I = 5 V			2	
I_{DD}	Supply current			$\overline{RESIN}$ = V_{DD}, SENSE = $V_{DD} \geq V_{IT}$max + 0.2 V CONTROL = 0 V, Outputs open		9	16	μA
$I_{DD(d)}$	Supply current during t_d			V_{DD} = 5 V, V_{CT} = 0 , $\overline{RESIN}$ = V_{DD}, SENSE = V_{DD}, CONTROL = 0 V, Outputs open		120	150	μA
C_I	Input capacitance, SENSE			V_I = 0 V to V_{DD}		50		pF

† Typical values apply at T_A = 25°C.

‡ The lowest supply voltage at which $\overline{RESET}$ becomes active. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology. Rise time of $V_{DD} \geq 15$ μs/V.

NOTES: 2. All characteristics are measured with C_T = 0.1 μF.

3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 μF) should be connected near the supply terminals.

electrical characteristics over recommended operating conditions (see Note 2) (unless otherwise noted)

PARAMETER				TEST CONDITIONS		TLC77xxM			UNIT
						MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −20 μA		V_{DD} = 2 V,	T_A = 25°C	1.8			V
					T_A = −55°C to 125°C	1.7			
				V_{DD} = 2.7 V	T_A = 25°C	2.5			
					T_A = −55°C to 125°C	2.3			
				V_{DD} = 4.5 V	T_A = 25°C	4.3			
					T_A = −55°C to 125°C	4.2			
		I_{OH} = −2 mA		V_{DD} = 4.5 V	T_A = 25°C	3.7			
					T_A = −55°C to 125°C	3.6			
V_{OL}	Low-level output voltage	I_{OL} = 20 μA		V_{DD} = 2 V	T_A = 25°C			0.2	V
					T_A = −55°C to 125°C			0.2	
				V_{DD} = 2.7 V	T_A = 25°C			0.2	
					T_A = −55°C to 125°C			0.2	
				V_{DD} = 4.5 V	T_A = 25°C			0.2	
					T_A = −55°C to 125°C			0.2	
		I_{OL} = 2 mA		V_{DD} = 4.5 V	T_A = 25°C			0.5	
					T_A = −55°C to 125°C			0.5	
V_{IT-}	Negative-going input threshold voltage, SENSE (see Note 3)		TLC7733	V_{DD} = 2 V to 6 V		2.86	2.93	3.1	V
			TLC7705			4.3	4.5	4.8	
V_{hys}	Hysteresis voltage, SENSE			V_{DD} = 2 V to 6 V	V_{DD} = 2 V to 6 V		70		mV
V_{res}	Power-up reset voltage‡			I_{OL} = 20 μA				1	V
I_I	Input current	$\overline{\text{RESIN}}$		V_I = 0 V to V_{DD}				2	μA
		CONTROL		V_I = V_{DD}			7	15	
		SENSE		V_I = 5 V			5	10	
		SENSE, TLC7701 only		V_I = 5 V				2	
I_{DD}	Supply current			$\overline{\text{RESIN}}$ = V_{DD}, SENSE = V_{DD} ≥ V_{IT}max + 0.2 V, CONTROL = 0 V, Outputs open			9	16	μA
$I_{DD(d)}$	Supply current during t_d		TLC7733	$\overline{V_{CT}}$ = 0, $\overline{\text{RESIN}}$ = V_{DD}, CONTROL = 0 V, SENSE = V_{DD}, Outputs open	V_{DD} = 3.3 V			250	μA
			TLC7705		V_{DD} = 5 V		120	150	
C_I	Input capacitance, SENSE			V_I = 0 V to V_{DD}			50		pF

† Typical values apply at T_A = 25°C.

‡ The lowest supply voltage at which $\overline{\text{RESET}}$ becomes active. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology. Rise time of V_{DD} ≥ 15 μs/V.

NOTES: 2. All characteristics are measured with C_T = 0.1 μF.

3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 μF) should be placed near the supply terminals.

switching characteristics at V_{DD} = 5 V, R_L = 2 kΩ, C_L = 50 pF, T_A = 25°C (unless otherwise noted)

PARAMETER		MEASURED		TEST CONDITIONS	TLC77xx			UNIT
		FROM (INPUT)	TO (OUTPUT)		MIN	TYP	MAX	
t_d	Delay time	$V_{I(SENSE)} \geq V_{IT+}$	RESET and $\overline{\text{RESET}}$	$\overline{\text{RESIN}}$ = 0.7 × V_{DD}, CONTROL = 0.2 × V_{DD}, C_T = 100 nF, T_A = Full range, See timing diagram	1.1	2.1	4.2	ms
t_{PLH}	Propagation delay time, low-to-high-level output	SENSE	$\overline{\text{RESET}}$	$V_{IH} = V_{IT+}$max + 0.2 V, $V_{IL} = V_{IT-}$min − 0.2 V, $\overline{\text{RESIN}}$ = 0.7 × V_{DD}, CONTROL = 0.2 × V_{DD}, CT = NC†			20	µs
t_{PHL}	Propagation delay time, high-to-low-level output						5	
t_{PLH}	Propagation delay time, low-to-high-level output		RESET				5	
t_{PHL}	Propagation delay time, high-to-low-level output						20	
t_{PLH}	Propagation delay time, low-to-high-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$	V_{IH} = 0.7 × V_{DD}, V_{IL} = 0.2 × V_{DD}, SENSE = V_{IT+}max + 0.2 V, CONTROL = 0.2 × V_{DD}, CT = NC†			20	µs
t_{PHL}	Propagation delay time, high-to-low-level output						40	ns
t_{PLH}	Propagation delay time, low-to-high-level output		RESET				45	ns
t_{PHL}	Propagation delay time, high-to-low-level output						20	µs
t_{PLH}	Propagation delay time, low-to-high-level output	CONTROL	RESET	V_{IH} = 0.7 × V_{DD}, V_{IL} = 0.2 × V_{DD}, SENSE = V_{IT+}max + 0.2 V, $\overline{\text{RESIN}}$ = 0.7 × V_{DD}, CT = NC†			38	ns
t_{PHL}	Propagation delay time, high-to-low-level output						38	ns
	Low-level minimum pulse duration to switch RESET and $\overline{\text{RESET}}$	SENSE		$V_{IH} = V_{IT+}$max + 0.2 V, $V_{IL} = V_{IT-}$min − 0.2 V,	3			µs
		$\overline{\text{RESIN}}$		V_{IL} = 0.2 × V_{DD}, V_{IH} = 0.7 × V_{DD}	1			
t_r	Rise time		RESET and $\overline{\text{RESET}}$	10% to 90%		8		ns/V
t_f	Fall time			90% to 10%		4		

† NC = No capacitor, and includes up to 100-pF probe and jig capacitance.

switching characteristics at V_{DD} = 5 V, R_L = 2 kΩ, C_L = 50 pF

PARAMETER		MEASURED FROM (INPUT)	MEASURED TO (OUTPUT)	TEST CONDITIONS	T_A	TLC77xxM MIN	TLC77xxM TYP	TLC77xxM MAX	UNIT
t_d	Delay time	$V_{I(SENSE)} \geq V_{IT+}$	RESET and $\overline{\text{RESET}}$	$\overline{\text{RESIN}}$ = 2.7 V, CONTROL = 0.4 V, C_T = 100 nF, See timing diagram	Full range	1.1	2.1	4.2	ms
t_{PLH}	Propagation delay time, low-to-high-level output	SENSE	$\overline{\text{RESET}}$	$V_{IH} = V_{IT+}$max + 0.2 V, $V_{IL} = V_{IT-}$min − 0.2 V, $\overline{\text{RESIN}}$ = 2.7 V, CONTROL = 0.4 V, CT = NC†	25°C			20	µs
					Full range			24	
			RESET		25°C			5	µs
					Full range			7	
t_{PHL}	Propagation delay time, high-to-low-level output	SENSE	$\overline{\text{RESET}}$	$V_{IH} = V_{IT+}$max + 0.2 V, $V_{IL} = V_{IT-}$min − 0.2 V, $\overline{\text{RESIN}}$ = 2.7 V, CONTROL = 0.4 V, CT = NC†	25°C			5	µs
					Full range			7	
			RESET		25°C			20	µs
					Full range			24	
t_{PLH}	Propagation delay time, low-to-high-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$	V_{IH} = 2.7 V, V_{IL} = 0.4 V, SENSE = V_{IT+}max + 0.2 V, CONTROL = 0.4 V, CT = NC†	25°C			20	µs
					Full range			24	
			RESET		25°C			45	ns
					Full range			65	
t_{PHL}	Propagation delay time, high-to-low-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$	V_{IH} = 2.7 V, V_{IL} = 0.4 V, SENSE = V_{IT+}max + 0.2 V, CONTROL = 0.4 V, CT = NC†	25°C			40	ns
					Full range			60	
			RESET		25°C			20	µs
					Full range			24	
t_{PLH}	Propagation delay time, low-to-high-level output	CONTROL	RESET	V_{IH} = 2.7 V, V_{IL} = 0.4 V, SENSE = V_{IT+}max + 0.2 V, $\overline{\text{RESIN}}$ = 2.7 V, CT = NC†	25°C			38	ns
					Full range			58	
t_{PHL}	Propagation delay time, high-to-low-level output				25°C			38	ns
					Full range			58	
	Low-level minimum pulse duration	SENSE		$V_{IH} = V_{IT+}$max + 0.2 V, $V_{IL} = V_{IT-}$min − 0.2 V,	Full range	3			µs
		$\overline{\text{RESIN}}$		V_{IL} = 0.4 V, V_{IH} = 2.7 V		1			
t_r	Rise time		RESET and $\overline{\text{RESET}}$	10% to 90%	Full range		8		ns/V
t_f	Fall time			90% to 10%			4		

† NC = No capacitor, and includes up to 100-pF probe and jig capacitance.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-9750901Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
5962-9750901QPA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
5962-9751301Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
5962-9751301QHA	ACTIVE	CFP	U	10	1	TBD	A42 SNPB	Level-NC-NC-NC
5962-9751301QPA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
TLC7701ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC7701IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC7701IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TLC7701IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TLC7701IPW	ACTIVE	TSSOP	PW	8	150	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC7701IPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI
TLC7701IPWR	ACTIVE	TSSOP	PW	8	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC7701QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC7701QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC7701QP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TLC7701QPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TLC7701QPW	ACTIVE	TSSOP	PW	8	150	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC7701QPWLE	PREVIEW	TSSOP	PW	8		TBD	Call TI	Call TI
TLC7701QPWR	ACTIVE	TSSOP	PW	8	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC7703ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC7703IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC7703IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TLC7703IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TLC7703IPW	ACTIVE	TSSOP	PW	8	150	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC7703IPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI
TLC7703IPWR	ACTIVE	TSSOP	PW	8	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC7703QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC7703QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC7703QP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TLC7703QPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TLC7703QPW	ACTIVE	TSSOP	PW	8	150	TBD	CU NIPDAU	Level-1-220C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TLC7703QPWR	ACTIVE	TSSOP	PW	8	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC7705ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC7705IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC7705IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TLC7705IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TLC7705IPW	ACTIVE	TSSOP	PW	8	150	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC7705IPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI
TLC7705IPWR	ACTIVE	TSSOP	PW	8	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC7705MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
TLC7705MJG	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
TLC7705MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
TLC7705MUB	ACTIVE	CFP	U	10	1	TBD	A42 SNPB	Level-NC-NC-NC
TLC7705QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC7705QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC7705QP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TLC7705QPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TLC7705QPW	ACTIVE	TSSOP	PW	8	150	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC7705QPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI
TLC7705QPWR	ACTIVE	TSSOP	PW	8	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC7725ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC7725IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC7725IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TLC7725IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TLC7725IPW	ACTIVE	TSSOP	PW	8	150	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC7725IPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI
TLC7725IPWR	ACTIVE	TSSOP	PW	8	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC7725IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC7725QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC7725QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC7725QP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TLC7725QPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TLC7725QPW	ACTIVE	TSSOP	PW	8	150	TBD	CU NIPDAU	Level-1-220C-UNLIM

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TLC7725QPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI
TLC7725QPWR	ACTIVE	TSSOP	PW	8	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC7733ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC7733IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC7733IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC7733IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC7733IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TLC7733IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TLC7733IPW	ACTIVE	TSSOP	PW	8	150	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC7733IPWR	ACTIVE	TSSOP	PW	8	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC7733IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC7733MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
TLC7733MJG	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
TLC7733MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
TLC7733QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC7733QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC7733QP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TLC7733QPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TLC7733QPW	ACTIVE	TSSOP	PW	8	150	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC7733QPWR	ACTIVE	TSSOP	PW	8	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is