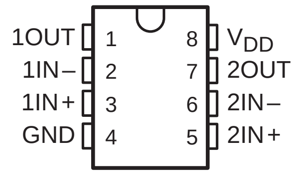
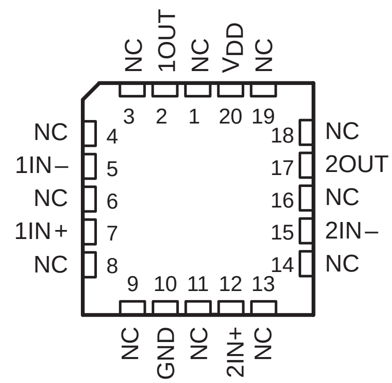
- **Push-Pull CMOS Output Drives Capacitive Loads Without Pullup Resistor, I_O = ± 8 mA**
- **Very Low Power . . . 100 μW Typ at 5 V**
- **Fast Response Time . . . t_{PLH} = 2.7 μs Typ With 5-mV Overdrive**
- **Single-Supply Operation . . . 3 V to 16 V**
  TLC3702M . . . 4 V to 16 V
- **On-Chip ESD Protection**

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



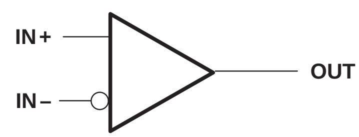
NC – No internal connection

description

The TLC3702 consists of two independent micropower voltage comparators designed to operate from a single supply and be compatible with modern HCMOS logic systems. They are functionally similar to the LM339 but use one-twentieth of the power for similar response times. The push-pull CMOS output stage drives capacitive loads directly without a power-consuming pullup resistor to achieve the stated response time. Eliminating the pullup resistor not only reduces power dissipation, but also saves board space and component cost. The output stage is also fully compatible with TTL requirements.

Texas Instruments LinCMOS™ process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS™ process offers extremely stable input offset voltages with large differential input voltages. This characteristic makes it possible to build reliable CMOS comparators.

symbol (each comparator)



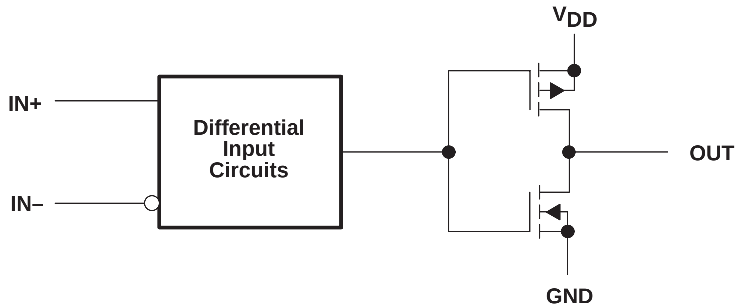
The TLC3702C is characterized for operation over the commercial temperature range of 0°C to 70°C. The TLC3702I is characterized for operation over the extended industrial temperature range of –40°C to 85°C. The TLC3702M is characterized for operation over the full military temperature range of –55°C to 125°C.

AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGES			
		SMALL OUTLINE (D)	CERAMIC (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	5 mV	TLC3702CD	—	—	TLC3702CP
–40°C to 85°C	5 mV	TLC3702ID	—	—	TLC3702IP
–55°C to 125°C	5 mV	TLC3702MD	TLC3702MFK	TLC3702MJG	—

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLC3702CDR).

functional block diagram (each comparator)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) . . . . . –0.3 V to 18 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±18 V
Input voltage range, V_I . . . . . –0.3 V to V_{DD}
Output voltage range, V_O . . . . . – 0.3 V to V_{DD}
Input current, I_I . . . . . ±5 mA
Output current, I_O (each output) . . . . . ±20 mA
Total supply current into V_{DD} . . . . . 40 mA
Total current out of GND . . . . . 40 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: TLC3702C . . . . . 0°C to 70°C
TLC3702I . . . . . –40°C to 85°C
TLC3702M . . . . . –55°C to 125°C
Storage temperature range . . . . . –65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN–.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	N/A

recommended operating conditions

	TLC3702C			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	– 0.2		V_{DD} – 1.5	V
High-level output current, I_{OH}			–20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A	TLC3702C			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{DD} = 5 V to 10 V, $V_{IC} = V_{ICR}$min, See Note 3	25°C		1.2	5	mV
			0°C to 70°C			6.5	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			70°C			0.3	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			70°C			0.6	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD} – 1			V
			0°C to 70°C	0 to V_{DD} – 1.5			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C		84		dB
			70°C		84		
			0°C		84		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			70°C		85		
			0°C		85		
V_{OH}	High-level output voltage	V_{ID} = 1 V, I_{OH} = –4 mA	25°C	4.5	4.7		V
			70°C	4.3			
V_{OL}	Low-level output voltage	V_{ID} = –1 V, I_{OH} = 4 mA	25°C		210	300	mV
			70°C			375	
I_{DD}	Supply current (both comparators)	Outputs low, No load	25°C		18	40	µA
			0°C to 70°C			50	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.
NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	TLC3702I MIN	TLC3702I NOM	TLC3702I MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	–0.2		V_{DD} – 1.5	V
High-level output current, I_{OH}			–20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	–40		85	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A	TLC3702I MIN	TLC3702I TYP	TLC3702I MAX	UNIT
V_{IO}	Input offset voltage	V_{DD} = 5 V to 10 V, V_{IC} = V_{ICR}min, See Note 3	25°C		1.2	5	mV
			–40°C to 85°C			7	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			85°C			1	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			85°C			2	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD} – 1			V
			–40°C to 85°C	0 to V_{DD} – 1.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C		84		dB
			85°C		84		
			–40°C		83		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			85°C		85		
			–40°C		83		
V_{OH}	High-level output voltage	V_{ID} = 1 V, I_{OH} = –4 mA	25°C	4.5	4.7		V
			85°C	4.3			
V_{OL}	Low-level output voltage	V_{ID} = –1 V, I_{OH} = –4 mA	25°C		210	300	mV
			85°C			400	
I_{DD}	Supply current (both comparators)	Outputs low, No load	25°C		18	40	µA
			–40°C to 85°C			65	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.
NOTE 3. The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	TLC3702M			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{DD}	4	5	16	V
Common-mode input voltage, V_{IC}	0		V_{DD} – 1.5	V
High-level output current, I_{OH}			– 20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	– 55		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A	TLC3702M			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{DD} = 5 V to 10 V, V_{IC} = V_{ICR}min, See Note 3	25°C		1.2	5	mV
			–55°C to 125°C			10	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			125°C			30	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD} – 1			V
			–55°C to 125°C	0 to V_{DD} – 1.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C		84		dB
			125°C		83		
			–55°C		82		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			125°C		85		
			– 55°C		82		
V_{OH}	High-level output voltage	V_{ID} = 1 V, I_{OH} = – 4 mA	25°C	4.5	4.7		V
			125°C	4.2			
V_{OL}	Low-level output voltage	V_{ID} = –1 V, I_{OH} = – 4 mA	25°C		210	300	mV
			125°C			500	
I_{DD}	Supply current (both comparators)	Outputs low, No load	25°C		18	40	µA
			–55°C to 125°C			90	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.
NOTE 3. The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLC3702C, TLC3702I TLC3702M			UNIT
				MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output†	f = 10 kHz, C_L = 50 pF	Overdrive = 2 mV		4.5		µs
			Overdrive = 5 mV		2.7		
			Overdrive = 10 mV		1.9		
			Overdrive = 20 mV		1.4		
			Overdrive = 40 mV		1.1		
		V_I = 1.4 V step at IN+			1.1		
t_{PHL}	Propagation delay time, high-to-low-level output†	f = 10 kHz, C_L = 50 pF	Overdrive = 2 mV		4		µs
			Overdrive = 5 mV		2.3		
			Overdrive = 10 mV		1.5		
			Overdrive = 20 mV		0.95		
			Overdrive = 40 mV		0.65		
		V_I = 1.4 V step at IN+			0.15		
t_f	Fall time	f = 10 kHz, C_L = 50 pF	Overdrive = 50 mV		50		ns
t_r	Rise time	f = 10 kHz, C_L = 50 pF	Overdrive = 50 mV		125		ns

† Simultaneous switching of inputs causes degradation in output response.

PRINCIPLES OF OPERATION

LinCMOS™ process

The LinCMOS™ process is a linear polysilicon-gate CMOS process. Primarily designed for single-supply applications, LinCMOS™ products facilitate the design of a wide range of high-performance analog functions from operational amplifiers to complex mixed-mode converters.

While digital designers are experienced with CMOS, MOS technologies are relatively new for analog designers. This short guide is intended to answer the most frequently asked questions related to the quality and reliability of LinCMOS™ products. Further questions should be directed to the nearest TI field sales office.

electrostatic discharge

CMOS circuits are prone to gate oxide breakdown when exposed to high voltages even if the exposure is only for very short periods of time. Electrostatic discharge (ESD) is one of the most common causes of damage to CMOS devices. It can occur when a device is handled without proper consideration for environmental electrostatic charges, e.g., during board assembly. If a circuit in which one amplifier from a dual op amp is being used and the unused pins are left open, high voltages tend to develop. If there is no provision for ESD protection, these voltages may eventually punch through the gate oxide and cause the device to fail. To prevent voltage buildup, each pin is protected by internal circuitry.

Standard ESD-protection circuits safely shunt the ESD current by providing a mechanism whereby one or more transistors break down at voltages higher than the normal operating voltages but lower than the breakdown voltage of the input gate. This type of protection scheme is limited by leakage currents which flow through the shunting transistors during normal operation after an ESD voltage has occurred. Although these currents are small, on the order of tens of nanoamps, CMOS amplifiers are often specified to draw input currents as low as tens of picoamps.

To overcome this limitation, TI design engineers developed the patented ESD-protection circuit shown in Figure 1. This circuit can withstand several successive 2-kV ESD pulses, while reducing or eliminating leakage currents that may be drawn through the input pins. A more detailed discussion of the operation of the TI ESD-protection circuit is presented on the next page.

All input and output pins on LinCMOS™ and Advanced LinCMOS™ products have associated ESD-protection circuitry that undergoes qualification testing to withstand 2000 V discharged from a 100-pF capacitor through a 1500-Ω resistor (human body model) and 200 V from a 100-pF capacitor with no current-limiting resistor (charged device model). These tests simulate both operator and machine handling of devices during normal test and assembly operations.

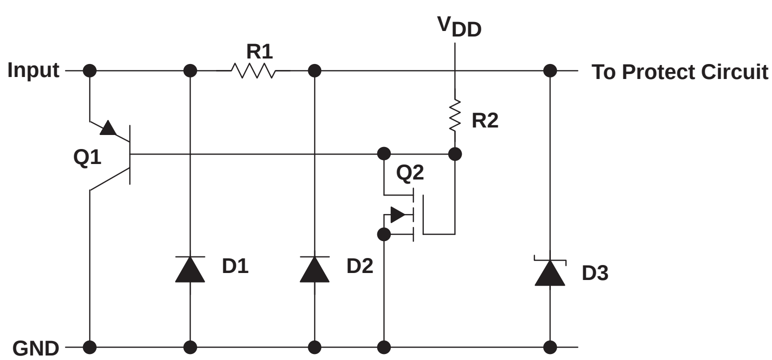


Figure 1. LinCMOS™ ESD-Protection Schematic

LinCMOS and Advanced LinCMOS are trademarks of Texas Instruments Incorporated.

PRINCIPLES OF OPERATION

input protection circuit operation

Texas Instruments patented protection circuitry allows for both positive- and negative-going ESD transients. These transients are characterized by extremely fast rise times and usually low energies, and can occur both when the device has all pins open and when it is installed in a circuit.

positive ESD transients

Initial positive charged energy is shunted through Q1 to V_{SS}. Q1 turns on when the voltage at the input rises above the voltage on the V_{DD} pin by a value equal to the V_{BE} of Q1. The base current increases through R2 with input current as Q1 saturates. The base current through R2 forces the voltage at the drain and gate of Q2 to exceed its threshold level (V_T ~ 22 to 26 V) and turn Q2 on. The shunted input current through Q1 to V_{SS} is now shunted through the n-channel enhancement-type MOSFET Q2 to V_{SS}. If the voltage on the input pin continues to rise, the breakdown voltage of the zener diode D3 is exceeded and all remaining energy is dissipated in R1 and D3. The breakdown voltage of D3 is designed to be 24 V to 27 V, which is well below the gate-oxide voltage of the circuit to be protected.

negative ESD transients

The negative charged ESD transients are shunted directly through D1. Additional energy is dissipated in R1 and D2 as D2 becomes forward biased. The voltage seen by the protected circuit is –0.3 V to –1 V (the forward voltage of D1 and D2).

circuit-design considerations

LinCMOS™ products are being used in actual circuit environments that have input voltages that exceed the recommended common-mode input voltage range and activate the input protection circuit. Even under normal operation, these conditions occur during circuit power up or power down, and in many cases, when the device is being used for a signal conditioning function. The input voltages can exceed V_{ICR} and not damage the device only if the inputs are current limited. The recommended current limit shown on most product data sheets is ±5 mA. Figure 2 and Figure 3 show typical characteristics for input voltage versus input current.

Normal operation and correct output state can be expected even when the input voltage exceeds the positive supply voltage. Again, the input current should be externally limited even though internal positive current limiting is achieved in the input protection circuit by the action of Q1. When Q1 is on, it saturates and limits the current to approximately 5-mA collector current by design. When saturated, Q1 base current increases with input current. This base current is forced into the V_{DD} pin and into the device I_{DD} or the V_{DD} supply through R2 producing the current limiting effects shown in Figure 2. This internal limiting lasts only as long as the input voltage is below the V_T of Q2.

When the input voltage exceeds the negative supply voltage, normal operation is affected and output voltage states may not be correct. Also, the isolation between channels of multiple devices (duals and quads) can be severely affected. External current limiting must be used since this current is directly shunted by D1 and D2 and no internal limiting is achieved. If normal output voltage states are required, an external input voltage clamp is required (see Figure 4).

PRINCIPLES OF OPERATION

circuit-design considerations (continued)

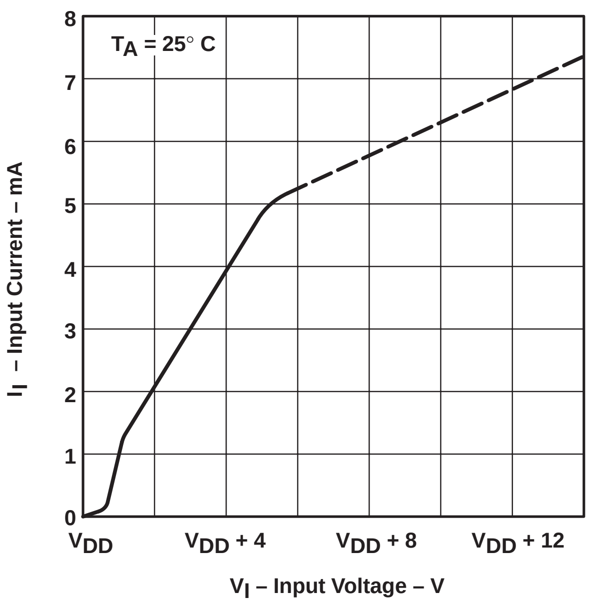


Figure 2

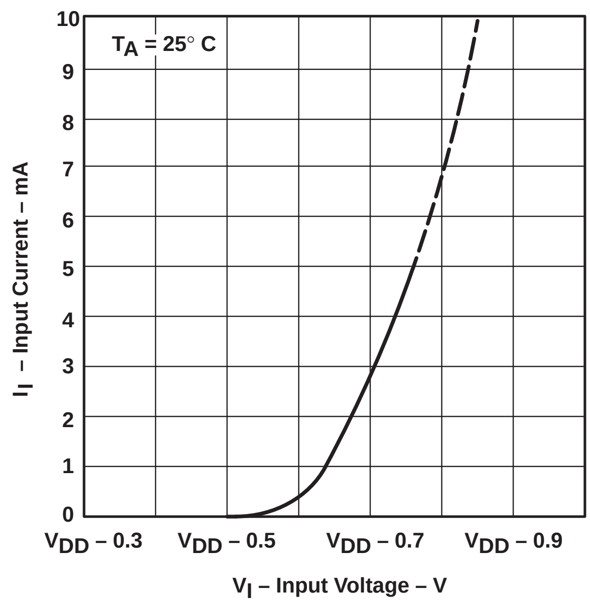
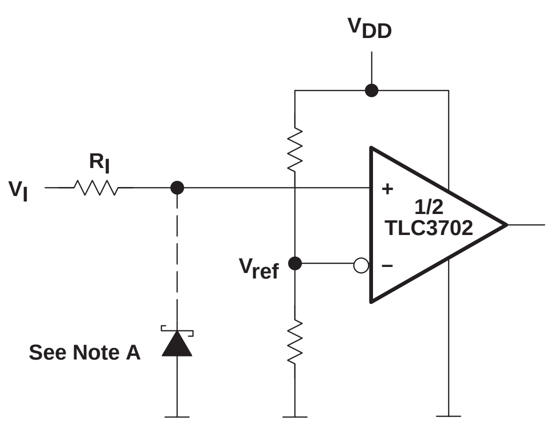


Figure 3



Positive Voltage Input Current Limit:

$$R_I = \frac{V_I - V_{DD} - 0.3\ V}{5\ mA}$$

Negative Voltage Input Current Limit:

$$R_I = \frac{-V_I - V_{DD} - (-0.3\ V)}{5\ mA}$$

NOTE A: If the correct input state is required when the negative input exceeds GND, a Schottky clamp is required.

Figure 4. Typical Input Current-Limiting Configuration for a LinCMOS™ Comparator

PARAMETER MEASUREMENT INFORMATION

The TLC3702 contains a digital output stage which, if held in the linear region of the transfer curve, can cause damage to the device. Conventional operational amplifier/comparator testing incorporates the use of a servo loop which is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, we offer the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, etc.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 5(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

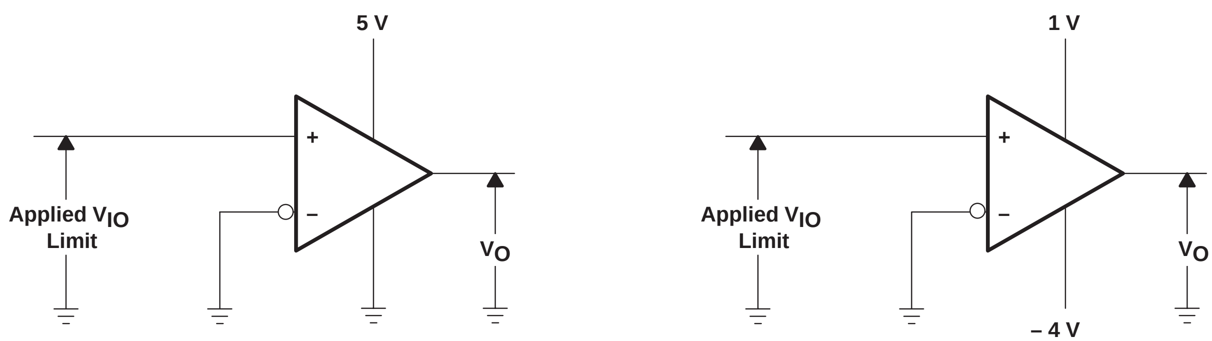
A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed to provide greater accuracy, as shown in Figure 5(b) for the V_{ICR} test. This slewing is done instead of changing the input voltages.

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output changes states.

Figure 6 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator in the linear region. The circuit consists of a switching mode servo loop in which IC1a generates a triangular waveform of approximately 20-mV amplitude. IC1b acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by IC1c through the voltage divider formed by R8 and R9. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage dividers R8 and R9 provide an increase in input offset voltage by a factor of 100 to make measurement easier. The values of R5, R7, R8, and R9 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be one percent or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.



(a) V_{IO} WITH V_{IC} = 0 V

(b) V_{IO} WITH V_{IC} = 4 V

Figure 5. Method for Verifying That Input Offset Voltage Is Within Specified Limits

PACKAGING INFORMATION

Orderable Device	Status [(1)]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [(2)]	Lead/Ball Finish	MSL Peak Temp [(3)]
5962-9153201Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
5962-9153201QHA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
5962-9153201QPA	ACTIVE	CDIP	JG	8		TBD	Call TI	Call TI
5962-9153202Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
5962-9153202QPA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
TLC3702CD	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
TLC3702CDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
TLC3702CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TLC3702CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TLC3702CPSLE	OBSOLETE	SO	PS	8		TBD	Call TI	Call TI
TLC3702CPSR	ACTIVE	SO	PS	8	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC3702CPW	ACTIVE	TSSOP	PW	8	150	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC3702CPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI
TLC3702CPWR	ACTIVE	TSSOP	PW	8	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC3702ID	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
TLC3702IDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
TLC3702IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TLC3702IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TLC3702IPW	ACTIVE	TSSOP	PW	8	150	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC3702IPWR	ACTIVE	TSSOP	PW	8	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC3702MD	ACTIVE	SOIC	D	8	75	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC3702MDR	ACTIVE	SOIC	D	8	2500	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLC3702MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
TLC3702MJG	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
TLC3702MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[(2)] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame

IMPORTANT NOTICE

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

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