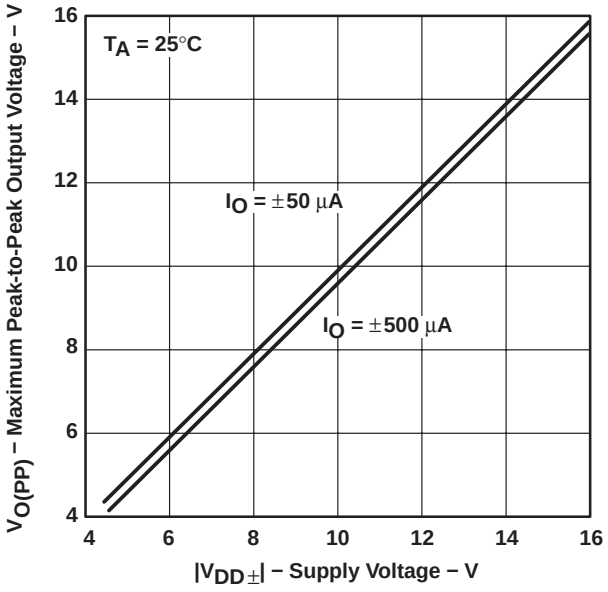
- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 9 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Both Single-Supply and Split-Supply Operation**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **High-Gain Bandwidth . . . 2.2 MHz Typ**
- **High Slew Rate . . . 3.6 V/μs Typ**
- **Low Input Offset Voltage 950 μV Max at T_A = 25°C**
- **Macromodel Included**
- **Performance Upgrades for the TS272, TS274, TLC272, and TLC274**
- **Available in Q-Temp Automotive**
  HighRel Automotive Applications
  Configuration Control / Print Support
  Qualification to Automotive Standards

description

The TLC2272 and TLC2274 are dual and quadruple operational amplifiers from Texas Instruments. Both devices exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLC227x family offers 2 MHz of bandwidth and 3 V/μs of slew rate for higher speed applications. These devices offer comparable ac performance while having better noise, input offset voltage, and power dissipation than existing CMOS operational amplifiers. The TLC227x has a noise voltage of 9 nV/√Hz, two times lower than competitive solutions.

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE



The TLC227x, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micro-power dissipation levels, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature, with single- or split-supplies, makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLC227xA family is available with a maximum input offset voltage of 950 μV. This family is fully characterized at 5 V and ±5 V.

The TLC2272/4 also makes great upgrades to the TLC272/4 or TS272/4 in standard designs. They offer increased output dynamic range, lower noise voltage, and lower input offset voltage. This enhanced feature set allows them to be used in a wider range of applications. For applications that require higher output drive and wider input voltage range, see the TLV2432 and TLV2442 devices.

If the design requires single amplifiers, see the TLV2211/21/31 family. These devices are single rail-to-rail operational amplifiers in the SOT-23 package. Their small size and low power consumption, make them ideal for high density, battery-powered equipment.

TLC2272 AVAILABLE OPTIONS

T_A	V_{IO}max At 25°C	PACKAGED DEVICES					
		SMALL OUTLINE† (D)	CERAMIC LCC (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP‡ (PW)	CERAMIC FLAT PACK (U)
0°C to 70°C	950 µV	TLC2272ACD	—	—	TLC2272ACP	TLC2272ACPW	—
	2.5 mV	TLC2272CD	—	—	TLC2272CP	TLC2272CPW	—
−40°C to 125°C	950 µV	TLC2272AID	—	—	TLC2272AIP	—	—
	2.5 mV	TLC2272ID	—	—	TLC2272IP	TLC2272IPW	—
	950 µV	TLC2272AQD	—	—	—	TLC2272AQPW	—
	2.5 mV	TLC2272QD	—	—		TLC2272QPW	—
−55°C to 125°C	950 µV	TLC2272AMD	TLC2272AMFK	TLC2272AMJG	TLC2272AMP	—	TLC2272AMU
	2.5 mV	TLC2272MD	TLC2272MFK	TLC2272MJG	TLC2272MP		TLC2272MU

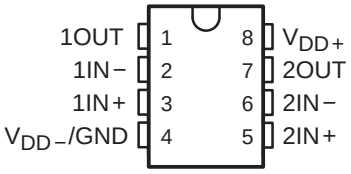
† The D packages are available taped and reeled. Add R suffix to the device type (e.g., TLC2272CDR).
‡ The PW package is available taped and reeled. Add R suffix to the device type (e.g., TLC2272PWR).
§ Chips are tested at 25°C.

TLC2274 AVAILABLE OPTIONS

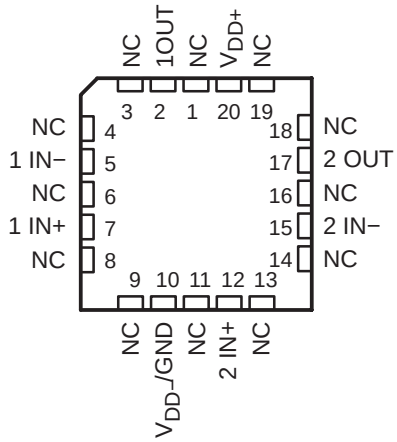
T_A	V_{IO}max AT 25°C	PACKAGED DEVICES					
		SMALL OUTLINE† (D)	CERAMIC LCC (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP‡ (PW)	CERAMIC FLAT PACK (W)
0°C to 70°C	950 µV	TLC2274ACD	—	—	TLC2274ACN	TLC2274ACPW	—
	2.5 mV	TLC2274CD			TLC2274CN	TLC2274CPW	
−40°C to 125°C	950 µV	TLC2274AID	—	—	TLC2274AIN	TLC2274AIPW	—
	2.5 mV	TLC2274ID			TLC2274IN	TLC2274IPW	
	950 µV	TLC2274AQD	—	—	—	—	—
	2.5 mV	TLC2274QD					
−55°C to 125°C	950 µV	TLC2274AMD	TLC2274AMFK	TLC2274AMJ	TLC2274AMN	—	TLC2274AMW
	2.5 mV	TLC2274MD	TLC2274MFK	TLC2274MJ	TLC2274MN		TLC2274MW

† The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC2274CDR).
‡ The PW package is available taped and reeled.
§ Chips are tested at 25°C.

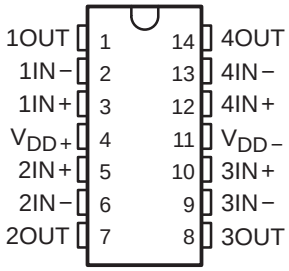
TLC2272
D, JG, P, OR PW PACKAGE
(TOP VIEW)



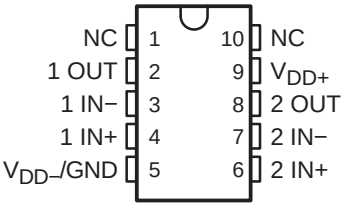
TLC2272
FK PACKAGE
(TOP VIEW)



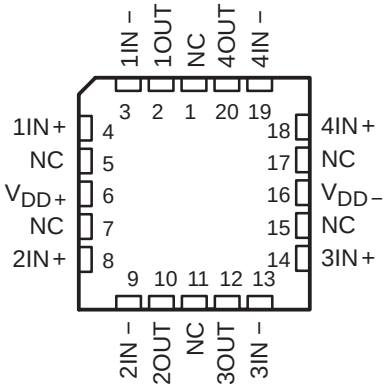
TLC2274
D, J, N, PW, OR W PACKAGE
(TOP VIEW)



TLC2272
U PACKAGE
(TOP VIEW)

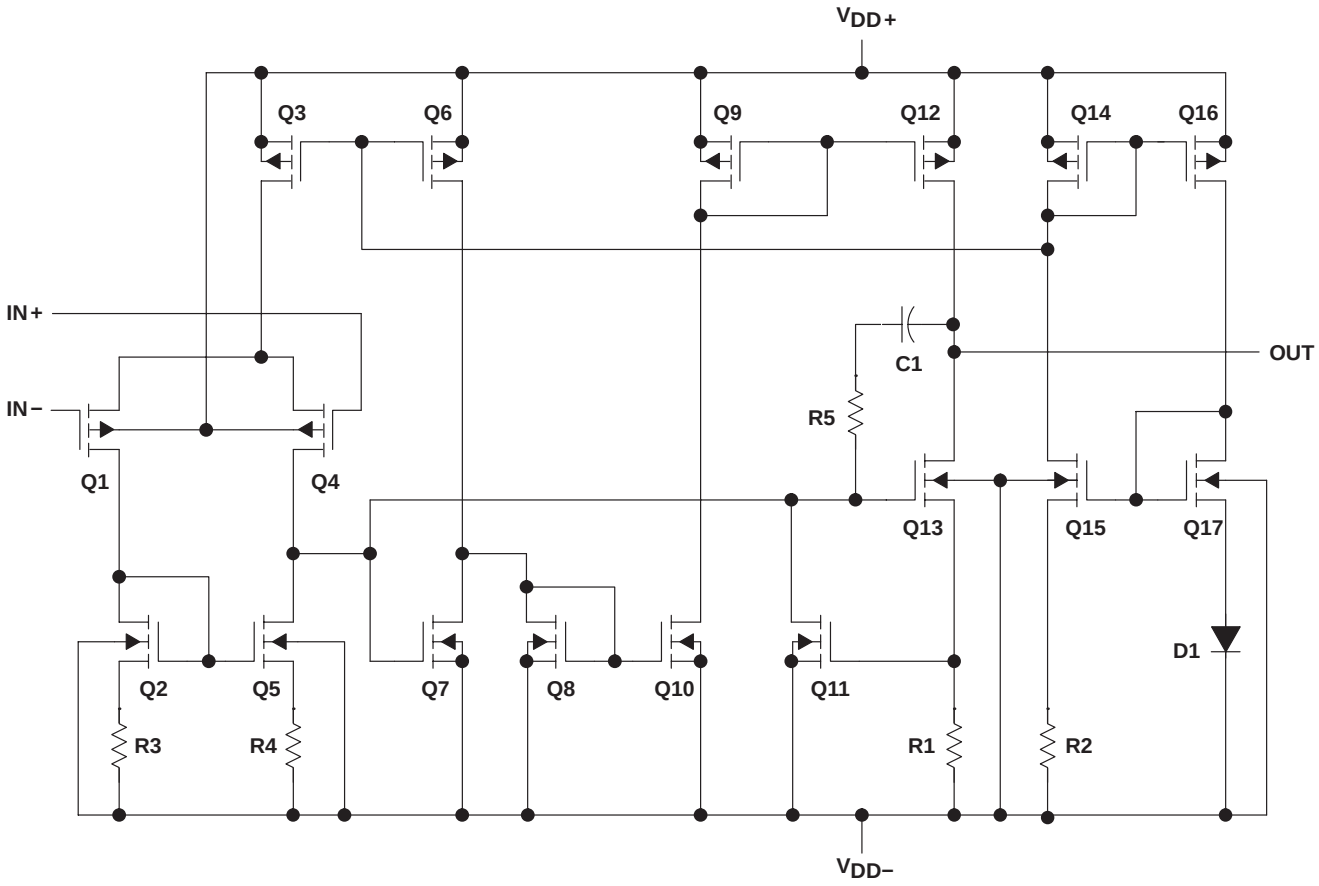


TLC2274
FK PACKAGE
(TOP VIEW)



NC − No internal connection

equivalent schematic (each amplifier)



ACTUAL DEVICE COMPONENT COUNT†		
COMPONENT	**TLC2272**	**TLC2274**
Transistors	38	76
Resistors	26	52
Diodes	9	18
Capacitors	3	6

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD+} (see Note 1) . . . . . 8 V
Supply voltage, V_{DD-} (see Note 1) . . . . . −8 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±16 V
Input voltage range, V_I (any input, see Note 1) . . . . . V_{DD-} − 0.3 V to V_{DD+}
Input current, I_I (any input) . . . . . ±5 mA
Output current, I_O . . . . . ±50 mA
Total current into V_{DD+} . . . . . ±50 mA
Total current out of V_{DD-} . . . . . ±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . . unlimited
Package thermal impedance, θ_{JA} (see Notes 4 and 5): D package (8 pin) . . . . . 97.1°C/W
D package (14 pin) . . . . . 86.2°C/W
N package . . . . . 79.7°C/W
P package . . . . . 84.6°C/W
PW package (8 pin) . . . . . 149°C/W
PW package (14 pin) . . . . . 113°C/W
Package thermal impedance, θ_{JC} (see Notes 4 and 5): FK package . . . . . 5.6°C/W
J package . . . . . 15.1°C/W
U package . . . . . 14.7°C/W
Operating free-air temperature range, T_A: C suffix . . . . . 0°C to 70°C
I, Q suffix . . . . . −40°C to 125°C
M suffix . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, P or PW package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or U package . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at IN+ with respect to IN−. Excessive current will flow if input is brought below V_{DD-} − 0.3 V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
4. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
5. The package thermal impedance is calculated in accordance with JESD 51-7 (plastic) or MIL-STD-883 Method 1012 (ceramic).

recommended operating conditions

	C SUFFIX		I SUFFIX		Q SUFFIX		M SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD\pm}$	±2.2	±8	±2.2	±8	±2.2	±8	±2.2	±8	V
Input voltage, V_I	V_{DD-}	V_{DD+} −1.5	V_{DD-}	V_{DD+} −1.5	V_{DD-}	V_{DD+} −1.5	V_{DD-}	V_{DD+} −1.5	V
Common-mode input voltage, V_{IC}	V_{DD-}	V_{DD+} −1.5	V_{DD-}	V_{DD+} −1.5	V_{DD-}	V_{DD+} −1.5	V_{DD-}	V_{DD+} −1.5	V
Operating free-air temperature, T_A	0	70	−40	125	−40	125	−55	125	°C

TLC2272C electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2272C			TLC2272AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0 V, $V_{DD}\pm$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω		25°C		300	2500		300	950	μV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 70°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.002			0.002		μV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				Full range			100			100	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				Full range			100			100	
V_{ICR}	Common-mode input voltage	R_S = 50 Ω,	$\lvert V_{IO}\rvert \le$ 5 mV	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		4.99			4.99		V
		I_{OH} = −200 μA		25°C	4.85	4.93		4.85	4.93		
				Full range	4.85			4.85			
		I_{OH} = −1 mA		25°C	4.25	4.65		4.25	4.65		
				Full range	4.25			4.25			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 5 mA	25°C		0.9	1.5		0.9	1.5	
				Full range			1.5			1.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 10 kΩ‡	25°C	15	35		15	35		V/mV
				Full range	15			15			
			R_L = 1 mΩ‡	25°C		175			175		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz,	A_V = 10	25°C		140			140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 V to 2.7 V, V_O = 2.5 V,	R_S = 50 Ω	25°C	70	75		70	75		dB
				Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD}/2, No load		25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		2.2	3		2.2	3	mA
				Full range			3			3	

† Full range is 0°C to 70°C.
‡ Referenced to 0 V

NOTE 6: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2272C operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2272C			TLC2272AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C	2.3	3.6		2.3	3.6		V/μs
				Full range	1.7			1.7			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		nV/√Hz
		f = 1 kHz		25°C		9			9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1			1		μV
		f = 0.1 Hz to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 10 kΩ‡,	A_V = 1	25°C		0.0013%			0.0013%		
			A_V = 10			0.004%			0.004%		
			A_V = 100			0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		2.18			2.18		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		1			1		MHz
t_s	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 10 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		1.5			1.5		μs
			To 0.01%			2.6			2.6		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		50°			50°		
	Gain margin			25°C		10			10		dB

† Full range is 0°C to 70°C.
‡ Referenced to 0 V

TLC2272C electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise specified)

PARAMETER		TEST CONDITIONS		T_A†	TLC2272C			TLC2272AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0 V, R_S = 50 Ω	V_O = 0 V,	25°C		300	2500		300	950	µV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 70°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.002			0.002		µV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				Full range			100			100	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				Full range			100			100	
V_{ICR}	Common-mode input voltage	R_S = 50 Ω,	$\|V_{IO}\| \le$ 5 mV	25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2		V
				Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	I_O = −20 µA		25°C		4.99			4.99		V
		I_O = −200 µA		25°C	4.85	4.93		4.85	4.93		
				Full range	4.85			4.85			
		I_O = −1 mA		25°C	4.25	4.65		4.25	4.65		
				Full range	4.25			4.25			
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0 V,	I_O = 50 µA	25°C		−4.99			−4.99		V
		V_{IC} = 0 V,	I_O = 500 µA	25°C	−4.85	−4.91		−4.85	−4.91		
				Full range	−4.85			−4.85			
		V_{IC} = 0 V,	I_O = 5 mA	25°C	−3.5	−4.1		−3.5	−4.1		
				Full range	−3.5			−3.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V	R_L = 10 kΩ	25°C	25	50		25	50		V/mV
				Full range	25			25			
			R_L = 1 mΩ	25°C		300			300		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz,	A_V = 10	25°C		130			130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = −5 V to 2.7 V, V_O = 0 V,	R_S = 50 Ω	25°C	75	80		75	80		dB
				Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ = 2.2 V to ±8 V, V_{IC} = 0 V,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 0 V	No load	25°C		2.4	3		2.4	3	mA
				Full range			3			3	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2272C operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2272C			TLC2272AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±2.3 V, C_L = 100 pF, R_L = 10 kΩ,		25°C	2.3	3.6		2.3	3.6		V/μs
				Full range	1.7			1.7			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		nV/√Hz
		f = 1 kHz		25°C		9			9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1			1		μV
		f = 0.1 Hz to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion pulse duration	V_O = ±2.3 V, f = 20 kHz, R_L = 10 kΩ	A_V = 1	25°C		0.0011%			0.0011%		
			A_V = 10			0.004%			0.004%		
			A_V = 100			0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF, R_L = 10 kΩ,		25°C		2.25			2.25		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, R_L = 10 kΩ, A_V = 1, C_L = 100 pF		25°C		0.54			0.54		MHz
t_s	Settling time	A_V = −1, Step = −2.3 V to 2.3 V, R_L = 10 kΩ, C_L = 100 pF	To 0.1%	25°C		1.5			1.5		μs
			To 0.01%			3.2			3.2		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF		25°C		52°			52°		
	Gain margin			25°C		10			10		dB

† Full range is 0°C to 70°C.

TLC2274C electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2274C			TLC2274AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_O = 0 V,	V_{IC} = 0 V, R_S = 50 Ω	25°C		300	2500		300	950	μV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 70°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.002			0.002		μV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				Full range			100			100	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				Full range			100			100	
V_{ICR}	Common-mode input voltage	R_S = 50 Ω,	$\lvert V_{IO}\rvert \le$ 5 mV,	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		4.99			4.99		V
		I_{OH} = −200 μA		25°C	4.85	4.93		4.85	4.93		
				Full range	4.85			4.85			
		I_{OH} = −1 mA		25°C	4.25	4.65		4.25	4.65		
				Full range	4.25			4.25			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 5 mA	25°C		0.9	1.5		0.9	1.5	
				Full range			1.5			1.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 10 kΩ‡	25°C	15	35		15	35		V/mV
				Full range	15			15			
			R_L = 1 mΩ‡	25°C		175			175		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz,	A_V = 10	25°C		140			140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 V to 2.7 V, V_O = 2.5 V,	R_S = 50 Ω	25°C	70	75		70	75		dB
				Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		4.4	6		4.4	6	mA
				Full range			6			6	

† Full range is 0°C to 70°C.
‡ Referenced to 0 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2274C operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2274C			TLC2274AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ‡,	C_L = 100 pF‡	25°C	2.3	3.6		2.3	3.6		V/μs
				Full range	1.7			1.7			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		nV/√Hz
		f = 1 kHz		25°C		9			9		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1			1		μV
		f = 0.1 Hz to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 10 kΩ‡	A_V = 1	25°C		0.0013%			0.0013%		
			A_V = 10			0.004%			0.004%		
			A_V = 100			0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF‡	R_L = 10 kΩ‡,	25°C		2.18			2.18		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		1			1		MHz
t_s	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 10 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		1.5			1.5		μs
			To 0.01%			2.6			2.6		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ‡,	C_L = 100 pF‡	25°C		50°			50°		
	Gain margin			25°C		10			10		dB

† Full range is 0°C to 70°C.
‡ Referenced to 0 V

TLC2274C electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2274C			TLC2274AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω		25°C		300	2500		300	950	µV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 70°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.002			0.002		µV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				Full range			100			100	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				Full range			100			100	
V_{ICR}	Common-mode input voltage	R_S = 50 Ω, $\|V_{IO}\| \le$ 5 mV		25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2		V
				Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	I_O = −20 µA		25°C		4.99			4.99		V
		I_O = −200 µA		25°C	4.85	4.93		4.85	4.93		
				Full range	4.85			4.85			
		I_O = −1 mA		25°C	4.25	4.65		4.25	4.65		
				Full range	4.25			4.25			
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0 V, I_O = 50 µA		25°C		−4.99			−4.99		V
		V_{IC} = 0 V, I_O = 500 µA		25°C	−4.85	−4.91		−4.85	−4.91		
				Full range	−4.85			−4.85			
		V_{IC} = 0 V, I_O = −5 mA		25°C	−3.5	−4.1		−3.5	−4.1		
				Full range	−3.5			−3.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V	R_L = 10 kΩ	25°C	25	50		25	50		V/mV
				Full range	25			25			
			R_L = 1 MΩ	25°C		300			300		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, N package		25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10		25°C		130			130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = −5 V to 2.7 V, V_O = 0 V, R_S = 50 Ω		25°C	75	80		75	80		dB
				Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ = ±2.2 V to ±8 V, V_{IC} = 0 V, No load		25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 0 V, No load		25°C		4.8	6		4.8	6	mA
				Full range			6			6	

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2274C operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2274C			TLC2274AC			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±2.3 V, C_L = 100 pF	R_L = 10 kΩ,	25°C	2.3	3.6		2.3	3.6		V/μs
				Full range	1.7			1.7			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		nV/√Hz
		f = 1 Hz		25°C		9			9		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1			1		μV
		f = 0.1 Hz to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = ±2.3 V, f = 20 kHz, R_L = 10 kΩ	A_V = 1	25°C		0.0011%			0.0011%		
			A_V = 10			0.004%			0.004%		
			A_V = 100			0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF	R_L = 10 kΩ,	25°C		2.25			2.25		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, R_L = 10 kΩ,	A_V = 1, C_L = 100 pF	25°C		0.54			0.54		MHz
t_s	Settling time	A_V = −1, Step = −2.3 V to 2.3 V, R_L = 10 kΩ, C_L = 100 pF	To 0.1%	25°C		1.5			1.5		μs
			To 0.01%			3.2			3.2		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ,	C_L = 100 pF	25°C		52°			52°		
	Gain margin			25°C		10			10		dB

† Full range is 0°C to 70°C.

TLC2272I electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2272I			TLC2272AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0 V, V_O = 0 V,	$V_{DD\pm}$ = ±2.5 V, R_S = 50 Ω	25°C		300	2500		300	950	μV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.002			0.002		μV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				−40°C to 85°C			150			150	
				Full range			800			800	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				−40°C to 85°C			150			150	
				Full range			800			800	
V_{ICR}	Common-mode input voltage	R_S = 50 Ω,	$\lvert V_{IO}\rvert \le$ 5 mV	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		4.99			4.99		V
		I_{OH} = −200 μA		25°C	4.85	4.93		4.85	4.93		
				Full range	4.85			4.85			
		I_{OH} = −1 mA		25°C	4.25	4.65		4.25	4.65		
				Full range	4.25			4.25			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 5 mA	25°C		0.9	1.5		0.9	1.5	
				Full range			1.5			1.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 10 kΩ‡	25°C	15	35		15	35		V/mV
				Full range	15			15			
			R_L = 1 mΩ‡	25°C		175			175		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz,	A_V = 10	25°C		140			140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 V to 2.7 V, V_O = 2.5 V,	R_S = 50 Ω	25°C	70	75		70	75		dB
				Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		2.2	3		2.2	3	mA
				Full range			3			3	

† Full range is − 40°C to 125°C.
‡ Referenced to 0 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2272I operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2272I			TLC2272AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C	2.3	3.6		2.3	3.6		V/μs
				Full range	1.7			1.7			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		nV/√Hz
		f = 1 kHz		25°C		9			9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1			1		μV
		f = 0.1 Hz to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 10 kΩ‡	A_V = 1	25°C		0.0013%			0.0013%		
			A_V = 10			0.004%			0.004%		
			A_V = 100			0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		2.18			2.18		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		1			1		MHz
t_s	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 10 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		1.5			1.5		μs
			To 0.01%			2.6			2.6		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		50°			50°		
	Gain margin			25°C		10			10		dB

† Full range is − 40°C to 125°C.
‡ Referenced to 0 V

TLC2272I electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2272I			TLC2272AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω		25°C		300	2500		300	950	μV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.002			0.002		μV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				−40°C to 85°C			150			150	
				Full range			800			800	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				−40°C to 85°C			150			150	
				Full range			800			800	
V_{ICR}	Common-mode input voltage	R_S = 50 Ω,	$\lvert V_{IO}\rvert \le$ 5 mV	25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2		V
				Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	I_O = −20 μA		25°C		4.99			4.99		V
		I_O = −200 μA		25°C	4.85	4.93		4.85	4.93		
				Full range	4.85			4.85			
		I_O = −1 mA		25°C	4.25	4.65		4.25	4.65		
				Full range	4.25			4.25			
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0 V,	I_O = 50 μA	25°C		−4.99			−4.99		V
		V_{IC} = 0 V,	I_O = 500 μA	25°C	−4.85	−4.91		−4.85	−4.91		
				Full range	−4.85			−4.85			
		V_{IC} = 0 V,	I_O = 5 mA	25°C	−3.5	−4.1		−3.5	−4.1		
				Full range	−3.5			−3.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V	R_L = 10 kΩ	25°C	25	50		25	50		V/mV
				Full range	25			25			
			R_L = 1 mΩ	25°C		300			300		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz,	A_V = 10	25°C		130			130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = −5 V to 2.7 V, V_O = 0 V, R_S = 50 Ω		25°C	75	80		75	80		dB
				Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 0 V,	No load	25°C		2.4	3		2.4	3	mA
				Full range			3			3	

† Full range is − 40°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2272I operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2272I			TLC2272AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±2.3 V, C_L = 100 pF, R_L = 10 kΩ,		25°C	2.3	3.6		2.3	3.6		V/μs
				Full range	1.7			1.7			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		nV/√Hz
		f = 1 kHz		25°C		9			9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1			1		μV
		f = 0.1 Hz to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = ±2.3 V, R_L = 10 kΩ, f = 20 kHz	A_V = 1	25°C		0.0011%			0.0011%		
			A_V = 10			0.004%			0.004%		
			A_V = 100			0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF, R_L = 10 kΩ,		25°C		2.25			2.25		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, R_L = 10 kΩ, A_V = 1, C_L = 100 pF		25°C		0.54			0.54		MHz
t_s	Settling time	A_V = −1, Step = −2.3 V to 2.3 V, R_L = 10 kΩ, C_L = 100 pF	To 0.1%	25°C		1.5			1.5		μs
			To 0.01%			3.2			3.2		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF		25°C		52°			52°		
	Gain margin			25°C		10			10		dB

† Full range is −40°C to 125°C.

TLC2274I electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2274I			TLC2274AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_O = 0 V,	V_{IC} = 0 V, R_S = 50 Ω	25°C		300	2500		300	950	µV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.002			0.002		µV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				−40°C to 85°C			150			150	
				Full range			800			800	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				−40°C to 85°C			150			150	
				Full range			800			800	
V_{ICR}	Common-mode input voltage	R_S = 50 Ω,	$\lvert V_{IO}\rvert \le$ 5 mV	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 µA		25°C		4.99			4.99		V
		I_{OH} = −200 µA		25°C	4.85	4.93		4.85	4.93		
				Full range	4.85			4.85			
		I_{OH} = −1 mA		25°C	4.25	4.65		4.25	4.65		
				Full range	4.25			4.25			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 µA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 µA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 5 mA	25°C		0.9	1.5		0.9	1.5	
				Full range			1.5			1.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 10 kΩ‡	25°C	15	35		15	35		V/mV
				Full range	15			15			
			R_L = 1 MΩ‡	25°C		175			175		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz,	A_V = 10	25°C		140			140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 V to 2.7 V, V_O = 2.5 V,	R_S = 50 Ω	25°C	70	75		70	75		dB
				Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		4.4	6		4.4	6	mA
				Full range			6			6	

† Full range is − 40°C to 125°C.
‡ Referenced to 0 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2274I operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2274I			TLC2274AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C	2.3	3.6		2.3	3.6		V/μs
				Full range	1.7			1.7			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		nV/√Hz
		f = 1 kHz		25°C		9			9		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1			1		μV
		f = 0.1 Hz to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 10 kΩ‡	A_V = 1	25°C		0.0013%			0.0013%		
			A_V = 10			0.004%			0.004%		
			A_V = 100			0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		2.18			2.18		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		1			1		MHz
t_s	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 10 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		1.5			1.5		μs
			To 0.01%			2.6			2.6		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		50°			50°		
	Gain margin			25°C		10			10		dB

† Full range is − 40°C to 125°C.
‡ Referenced to 0 V

TLC2274I electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2274I			TLC2274AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω		25°C		300	2500		300	950	µV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.002			0.002		µV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				−40°C to 85°C			150			150	
				Full range			800			800	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				−40°C to 85°C			150			150	
				Full range			800			800	
V_{ICR}	Common-mode input voltage	R_S = 50 Ω, $\lvert V_{IO}\rvert \le$ 5 mV		25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2		V
				Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	I_O = −20 µA		25°C		4.99			4.99		V
		I_O = −200 µA		25°C	4.85	4.93		4.85	4.93		
				Full range	4.85			4.85			
		I_O = −1 mA		25°C	4.25	4.65		4.25	4.65		
				Full range	4.25			4.25			
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0 V, I_O = 50 µA		25°C		−4.99			−4.99		V
		V_{IC} = 0 V, I_O = 500 µA		25°C	−4.85	−4.91		−4.85	−4.91		
				Full range	−4.85			−4.85			
		V_{IC} = 0 V, I_O = 5 mA		25°C	−3.5	−4.1		−3.5	−4.1		
				Full range	−3.5			−3.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V	R_L = 10 kΩ	25°C	25	50		25	50		V/mV
				Full range	25			25			
			R_L = 1 MΩ	25°C		300			300		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, N package		25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10		25°C		130			130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = −5 V to 2.7 V, V_O = 0 V, R_S = 50 Ω		25°C	75	80		75	80		dB
				Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ = ±2.2 V to ±8 V, V_{IC} = 0 V, No load		25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 0 V, No load		25°C		4.8	6		4.8	6	mA
				Full range			6			6	

† Full range is − 40°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2274I operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2274I			TLC2274AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±2.3 V, C_L = 100 pF	R_L = 10 kΩ,	25°C	2.3	3.6		2.3	3.6		V/μs
				Full range	1.7			1.7			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		nV/√Hz
		f = 1 kHz		25°C		9			9		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1			1		μV
		f = 0.1 Hz to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = ±2.3 V, R_L = 10 kΩ, f = 20 kHz	A_V = 1	25°C		0.0011%			0.0011%		
			A_V = 10			0.004%			0.004%		
			A_V = 100			0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF	R_L = 10 kΩ,	25°C		2.25			2.25		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, R_L = 10 kΩ,	A_V = 1, C_L = 100 pF	25°C		0.54			0.54		MHz
t_s	Settling time	A_V = −1, Step = −2.3 V to 2.3 V, R_L = 10 kΩ, C_L = 100 pF	To 0.1%	25°C		1.5			1.5		μs
			To 0.01%			3.2			3.2		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ,	C_L = 100 pF	25°C		52°			52°		
	Gain margin			25°C		10			10		dB

† Full range is −40°C to 125°C.

TLC2272Q and TLC2272M electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2272Q, TLC2272M			TLC2272AQ, TLC2272AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0 V, V_O = 0 V,	$V_{DD\pm}$ = ±2.5 V, R_S = 50 Ω	25°C		300	2500		300	950	μV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.002			0.002		μV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				Full range			800			800	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				Full range			800			800	
V_{ICR}	Common-mode input voltage	R_S = 50 Ω,	$\lvert V_{IO}\rvert \le$ 5 mV	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		4.99			4.99		V
		I_{OH} = −200 μA		25°C	4.85	4.93		4.85	4.93		
				Full range	4.85			4.85			
		I_{OH} = −1 mA		25°C	4.25	4.65		4.25	4.65		
				Full range	4.25			4.25			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 5 mA	25°C		0.9	1.5		0.9	1.5	
				Full range			1.5			1.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 10 kΩ‡	25°C	10	35		10	35		V/mV
				Full range	10			10			
			R_L = 1 mΩ‡	25°C		175			175		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz,	A_V = 10	25°C		140			140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 V to 2.7 V, V_O = 2.5 V,	R_S = 50 Ω	25°C	70	75		70	75		dB
				Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		2.2	3		2.2	3	mA
				Full range			3			3	

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2272Q and TLC2272M operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2272Q, TLC2272M			TLC2272AQ, TLC2272AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.25 V to 2.75 V, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C	2.3	3.6		2.3	3.6		V/μs
				Full range	1.7			1.7			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		nV/√Hz
		f = 1 kHz		25°C		9			9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1			1		μV
		f = 0.1 Hz to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 10 kΩ‡,	A_V = 1	25°C		0.0013%			0.0013%		
			A_V = 10			0.004%			0.004%		
			A_V = 100			0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		2.18			2.18		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		1			1		MHz
t_s	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 10 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		1.5			1.5		μs
			To 0.01%			2.6			2.6		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ‡, C_L = 100 pF‡		25°C		50°			50°		
	Gain margin			25°C		10			10		dB

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.
‡ Referenced to 2.5 V

TLC2272Q and TLC2272M electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2272Q, TLC2272M			TLC2272AQ, TLC2272AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω		25°C		300	2500		300	950	μV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.002			0.002		μV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				Full range			800			800	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				Full range			800			800	
V_{ICR}	Common-mode input voltage	R_S = 50 Ω,	$\lvert V_{IO}\rvert \le$ 5 mV	25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2		V
				Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	I_O = −20 μA		25°C		4.99			4.99		V
		I_O = −200 μA		25°C	4.85	4.93		4.85	4.93		
				Full range	4.85			4.85			
		I_O = −1 mA		25°C	4.25	4.65		4.25	4.65		
				Full range	4.25			4.25			
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0 V,	I_O = 50 μA	25°C		−4.99			−4.99		V
		V_{IC} = 0 V,	I_O = 500 μA	25°C	−4.85	−4.91		−4.85	−4.91		
				Full range	−4.85			−4.85			
		V_{IC} = 0 V,	I_O = 5 mA	25°C	−3.5	−4.1		−3.5	−4.1		
				Full range	−3.5			−3.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V	R_L = 10 kΩ	25°C	20	50		20	50		V/mV
				Full range	20			20			
			R_L = 1 mΩ	25°C		300			300		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz,	A_V = 10	25°C		130			130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = −5 V to 2.7 V, V_O = 0 V,	R_S = 50 Ω	25°C	75	80		75	80		dB
				Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = ±2.2 V to ±8 V, V_{IC} = 0 V,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		2.4	3		2.4	3	mA
				Full range			3			3	

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2272Q and TLC2272M operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2272Q, TLC2272M			TLC2272AQ, TLC2272AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±1 V, C_L = 100 pF	R_L = 10 kΩ,	25°C	2.3	3.6		2.3	3.6		V/μs
				Full range	1.7			1.7			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		nV/√Hz
		f = 1 kHz		25°C		9			9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1			1		μV
		f = 0.1 Hz to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = ±2.3 V, R_L = 10 kΩ, f = 20 kHz	A_V = 1	25°C		0.0011%			0.0011%		
			A_V = 10			0.004%			0.004%		
			A_V = 100			0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF	R_L = 10 kΩ,	25°C		2.25			2.25		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, R_L = 10 kΩ,	A_V = 1, C_L = 100 pF	25°C		0.54			0.54		MHz
t_s	Settling time	A_V = −1, Step = −2.3 V to 2.3 V, R_L = 10 kΩ, C_L = 100 pF	To 0.1%	25°C		1.5			1.5		μs
			To 0.01%			3.2			3.2		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ,	C_L = 100 pF	25°C		52°			52°		
	Gain margin			25°C		10			10		dB

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.

TLC2274Q and TLC2274M electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2274Q, TLC2274M			TLC2274AQ, TLC2274AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_O = 0 V,	V_{IC} = 0 V, R_S = 50 Ω	25°C		300	2500		300	950	μV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.002			0.002		μV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				Full range			800			800	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				Full range			800			800	
V_{ICR}	Common-mode input voltage	R_S = 50 Ω,	$\lvert V_{IO}\rvert \le$ 5 mV	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		4.99			4.99		V
		I_{OH} = −200 μA		25°C	4.85	4.93		4.85	4.93		
				Full range	4.85			4.85			
		I_{OH} = −1 mA		25°C	4.25	4.65		4.25	4.65		
				Full range	4.25			4.25			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V, I_{OL} = 500 μA		25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 5 mA	25°C		0.9	1.5		0.9	1.5	
				Full range			1.5			1.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 10 kΩ‡	25°C	10	35		10	35		V/mV
				Full range	10			10			
			R_L = 1 MΩ‡	25°C		175			175		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz,	A_V = 10	25°C		140			140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 V to 2.7 V, V_O = 2.5 V,	R_S = 50 Ω	25°C	70	75		70	75		dB
				Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		4.4	6		4.4	6	mA
				Full range			6			6	

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.
‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2274Q and TLC2274M operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2274Q, TLC2274M			TLC2274AQ, TLC2274AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ‡,	C_L = 100 pF‡	25°C	2.3	3.6		2.3	3.6		V/μs
				Full range	1.7			1.7			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		nV/√Hz
		f = 1 kHz		25°C		9			9		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1			1		μV
		f = 0.1 Hz to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 10 kΩ‡	A_V = 1	25°C		0.0013%			0.0013%		
			A_V = 10			0.004%			0.004%		
			A_V = 100			0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF‡	R_L = 10 kΩ‡,	25°C		2.18			2.18		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		1			1		MHz
t_s	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 10 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		1.5			1.5		μs
			To 0.01%			2.6			2.6		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ‡,	C_L = 100 pF‡	25°C		50°			50°		
	Gain margin			25°C		10			10		dB

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.
‡ Referenced to 2.5 V

TLC2274Q and TLC2274M electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLC2274Q, TLC2274M			TLC2274AQ, TLC2274AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω		25°C		300	2500		300	950	µV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.002			0.002		µV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				Full range			800			800	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				Full range			800			800	
V_{ICR}	Common-mode input voltage	R_S = 50 Ω, $\|V_{IO}\| \le$ 5 mV		25°C	−5 to 4	−5.3 to 4.2		−5 to 4	−5.3 to 4.2		V
				Full range	−5 to 3.5			−5 to 3.5			
V_{OM+}	Maximum positive peak output voltage	I_O = −20 µA		25°C		4.99			4.99		V
		I_O = −200 µA		25°C	4.85	4.93		4.85	4.93		
				Full range	4.85			4.85			
		I_O = −1 mA		25°C	4.25	4.65		4.25	4.65		
				Full range	4.25			4.25			
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0 V, I_O = 50 µA		25°C		−4.99			−4.99		V
		V_{IC} = 0 V, I_O = 500 µA		25°C	−4.85	−4.91		−4.85	−4.91		
				Full range	−4.85			−4.85			
		V_{IC} = 0 V, I_O = 5 mA		25°C	−3.5	−4.1		−3.5	−4.1		
				Full range	−3.5			−3.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V	R_L = 10 kΩ	25°C	20	50		20	50		V/mV
				Full range	20			20			
			R_L = 1 MΩ	25°C		300			300		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_i	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, N package		25°C		8			8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10		25°C		130			130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = −5 V to 2.7 V, V_O = 0 V, R_S = 50 Ω		25°C	75	80		75	80		dB
				Full range	75			75			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ = ± 2.2 V to ±8 V, V_{IC} = 0 V, No load		25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 0 V, No load		25°C		4.8	6		4.8	6	mA
				Full range			6			6	

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2274Q and TLC2274M operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V

PARAMETER		TEST CONDITIONS		T_A†	TLC2274Q, TLC2274M			TLC2274AQ, TLC2274AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±2.3 V, C_L = 100 pF	R_L = 10 kΩ,	25°C	2.3	3.6		2.3	3.6		V/μs
				Full range	1.7			1.7			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		50			50		nV/√Hz
		f = 1 kHz		25°C		9			9		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1			1		μV
		f = 0.1 Hz to 10 Hz		25°C		1.4			1.4		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = ±2.3 V, R_L = 10 kΩ, f = 20 kHz	A_V = 1	25°C		0.0011%			0.0011%		
			A_V = 10			0.004%			0.004%		
			A_V = 100			0.03%			0.03%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF	R_L = 10 kΩ,	25°C		2.25			2.25		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, R_L = 10 kΩ,	A_V = 1, C_L = 100 pF	25°C		0.54			0.54		MHz
t_s	Settling time	A_V = −1, Step = −2.3 V to 2.3 V, R_L = 10 kΩ, C_L = 100 pF	To 0.1%	25°C		1.5			1.5		μs
			To 0.01%			3.2			3.2		
ϕ_m	Phase margin at unit gain	R_L = 10 kΩ,	C_L = 100 pF	25°C		52°			52°		
	Gain margin			25°C		10			10		dB

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.

TYPICAL CHARACTERISTICS

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NOTE: For all graphs where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC2272
INPUT OFFSET VOLTAGE

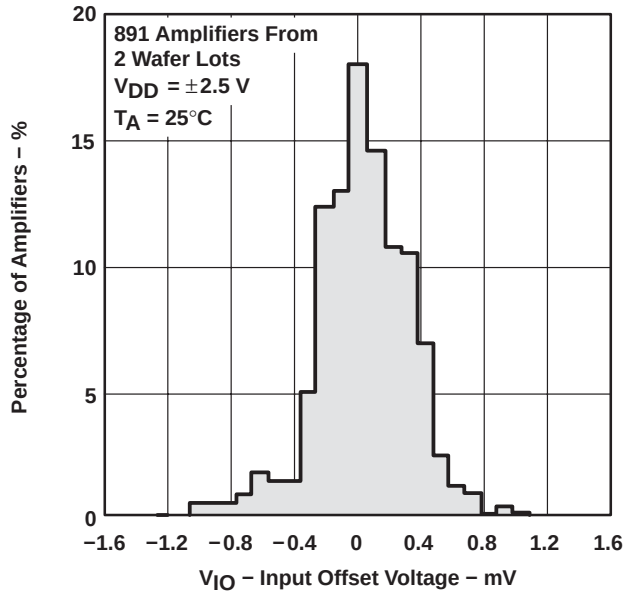


Figure 1

DISTRIBUTION OF TLC2272
INPUT OFFSET VOLTAGE

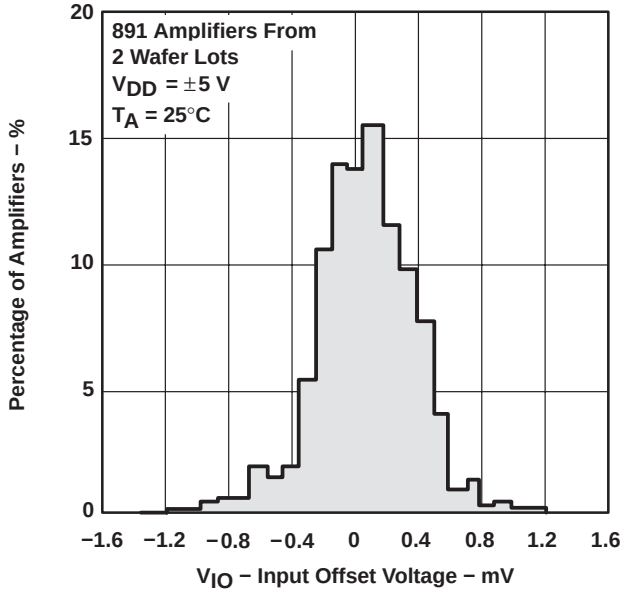


Figure 2

DISTRIBUTION OF TLC2274
INPUT OFFSET VOLTAGE

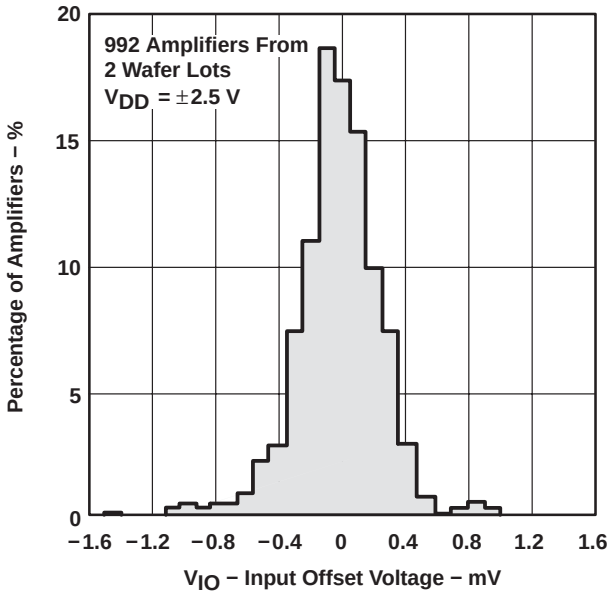


Figure 3

DISTRIBUTION OF TLC2274
INPUT OFFSET VOLTAGE

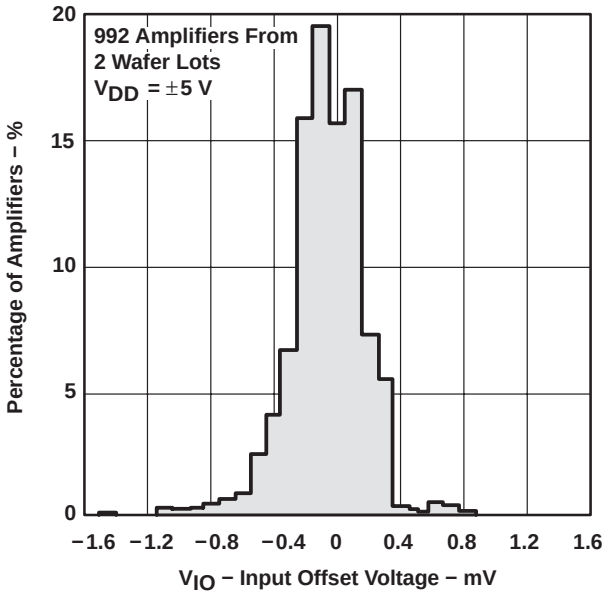


Figure 4

TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE
vs
COMMON-MODE VOLTAGE

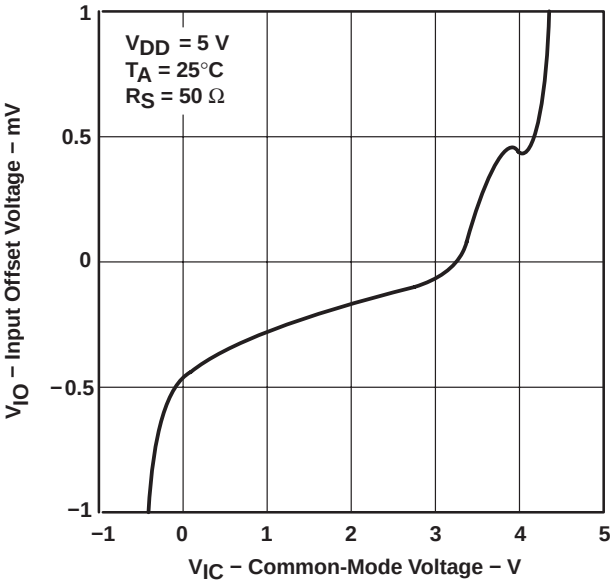


Figure 5

INPUT OFFSET VOLTAGE
vs
COMMON-MODE VOLTAGE

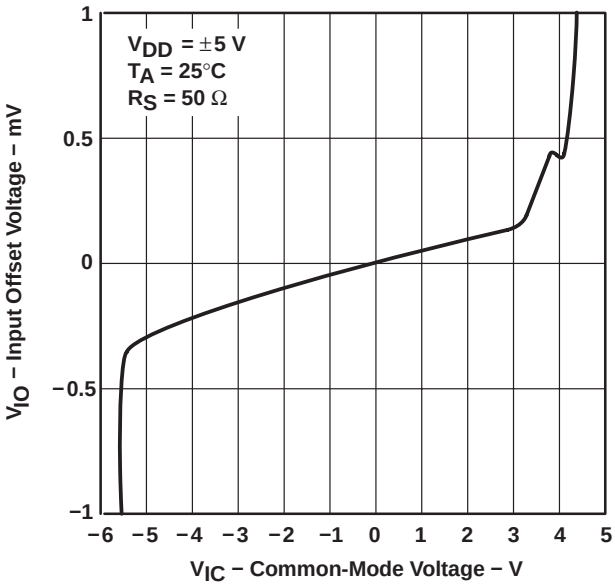


Figure 6

DISTRIBUTION OF TLC2272
vs
INPUT OFFSET VOLTAGE TEMPERATURE
COEFFICIENT†

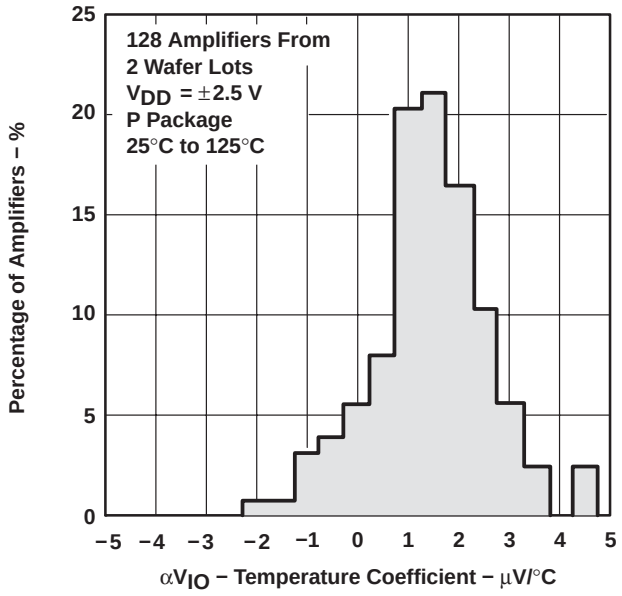


Figure 7

DISTRIBUTION OF TLC2272
vs
INPUT OFFSET VOLTAGE TEMPERATURE
COEFFICIENT†

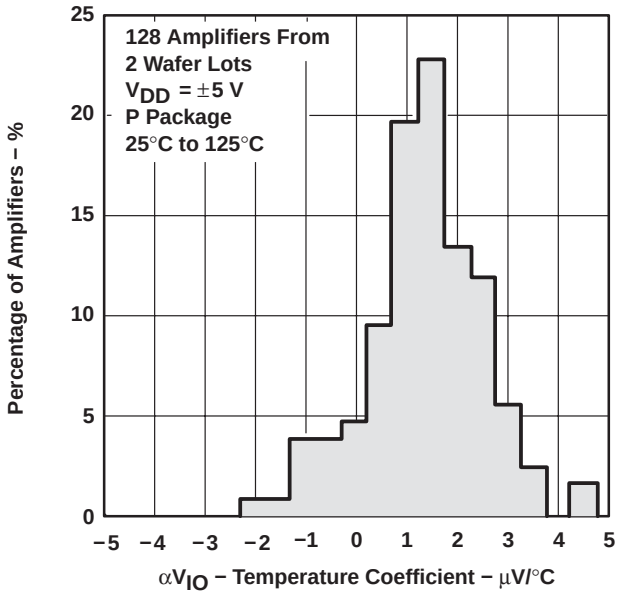


Figure 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC2274
vs
INPUT OFFSET VOLTAGE TEMPERATURE
COEFFICIENT†

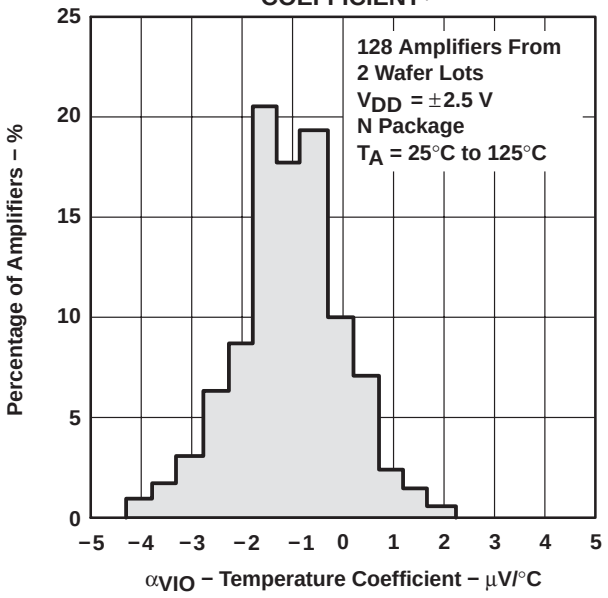


Figure 9

DISTRIBUTION OF TLC2274
vs
INPUT OFFSET VOLTAGE TEMPERATURE
COEFFICIENT†

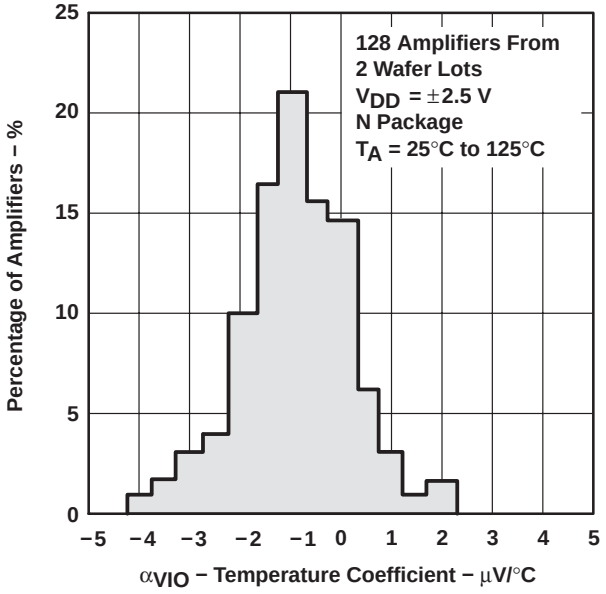


Figure 10

INPUT BIAS AND INPUT OFFSET CURRENT†
vs
FREE-AIR TEMPERATURE

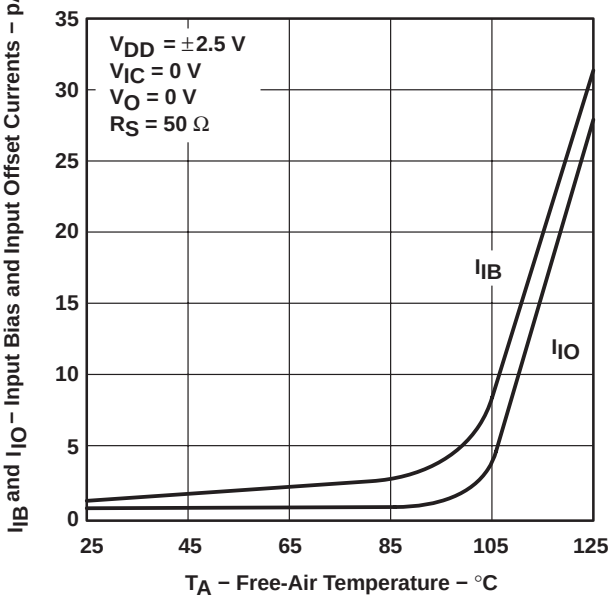


Figure 11

INPUT VOLTAGE
vs
SUPPLY VOLTAGE

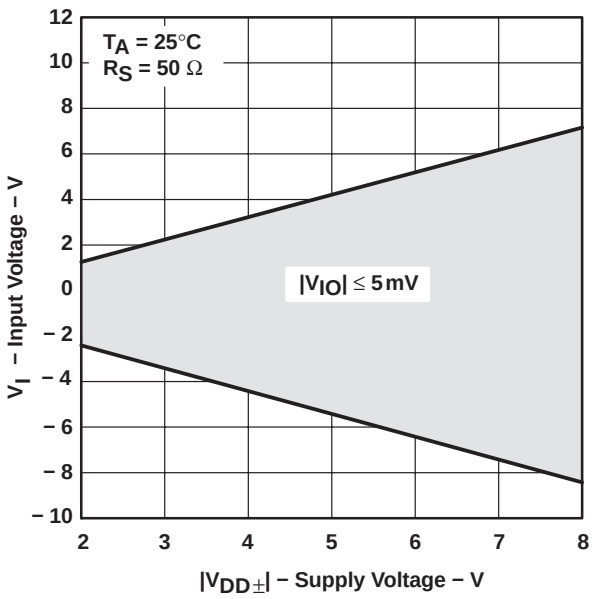


Figure 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

INPUT VOLTAGE† vs FREE-AIR TEMPERATURE

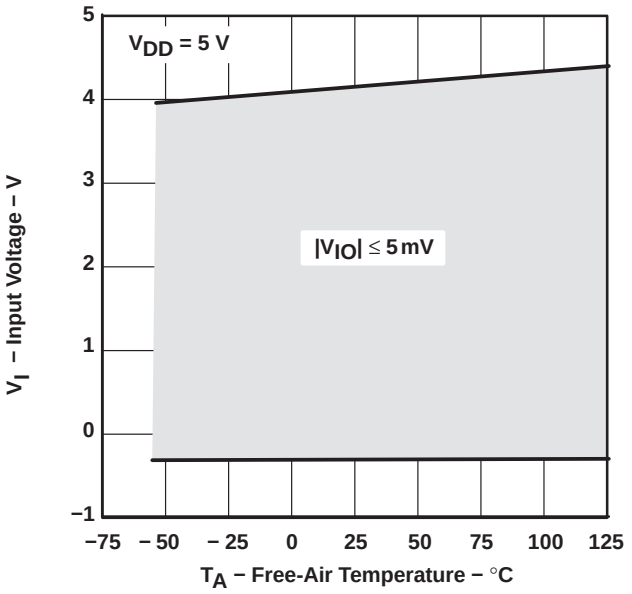


Figure 13

HIGH-LEVEL OUTPUT VOLTAGE† vs HIGH-LEVEL OUTPUT CURRENT

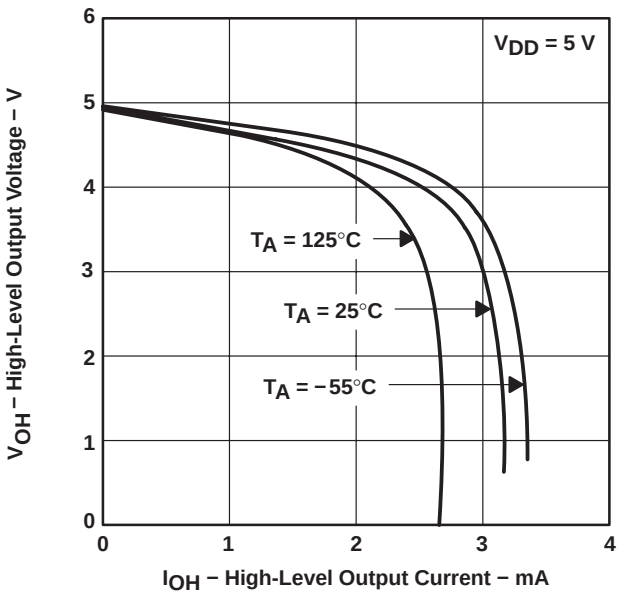


Figure 14

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

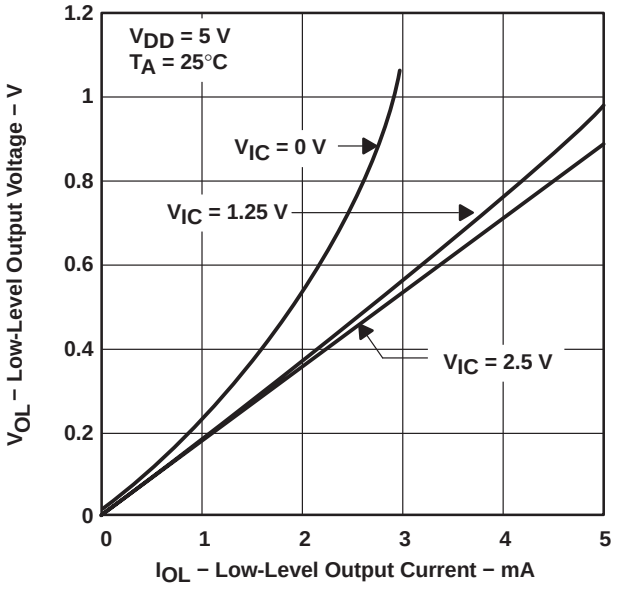


Figure 15

LOW-LEVEL OUTPUT VOLTAGE† vs LOW-LEVEL OUTPUT CURRENT

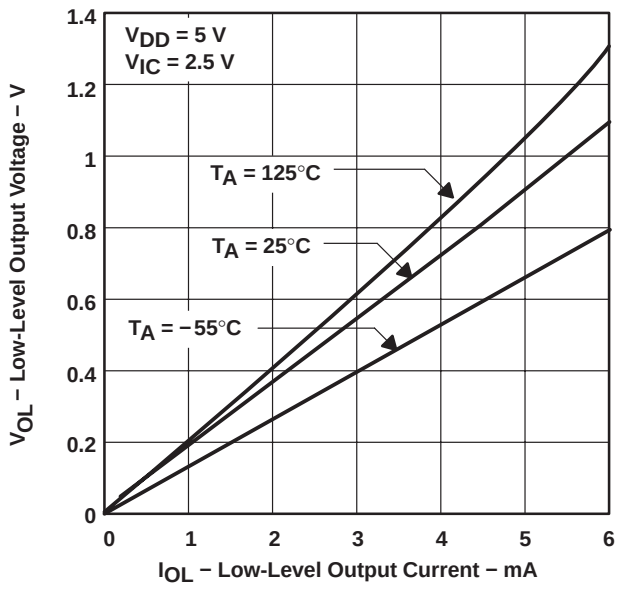


Figure 16

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE† vs OUTPUT CURRENT

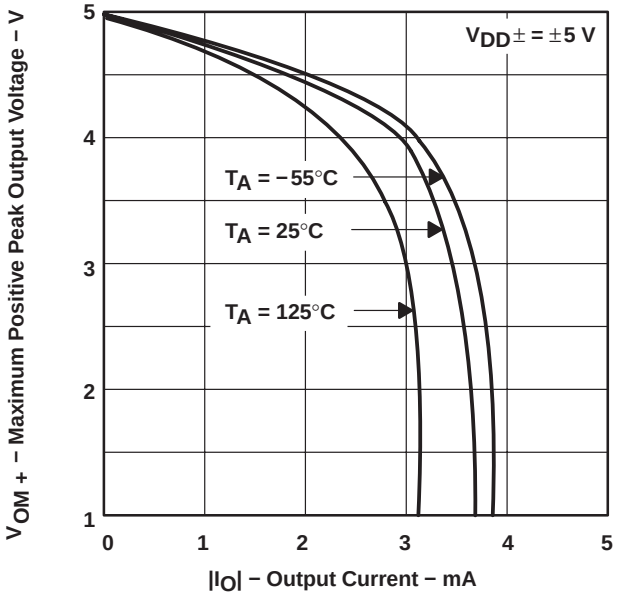


Figure 17

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE† vs OUTPUT CURRENT

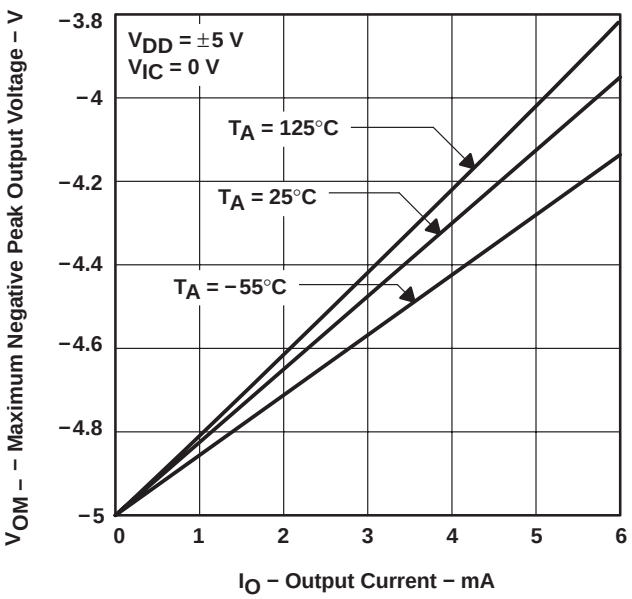


Figure 18

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

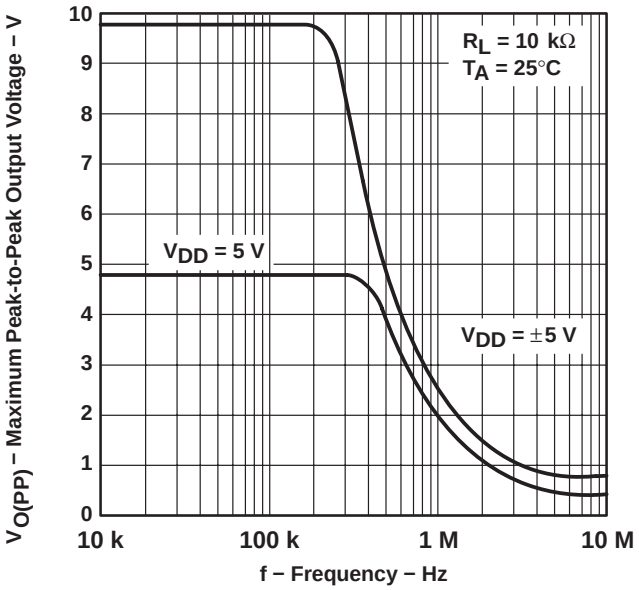


Figure 19

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

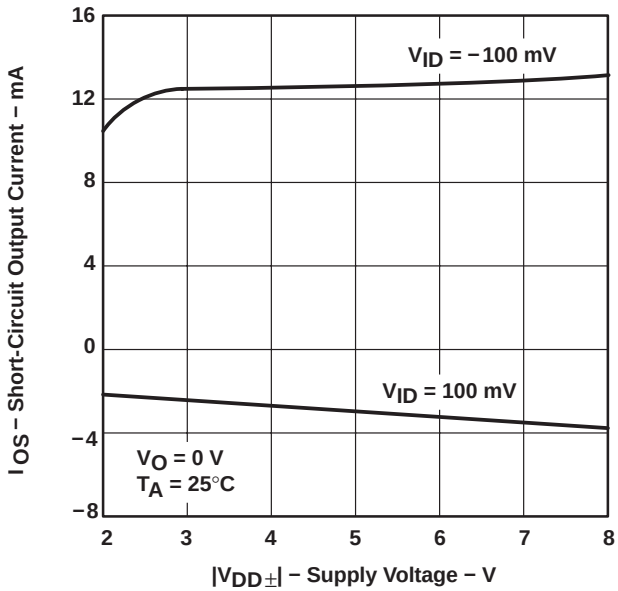


Figure 20

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT† vs FREE-AIR TEMPERATURE

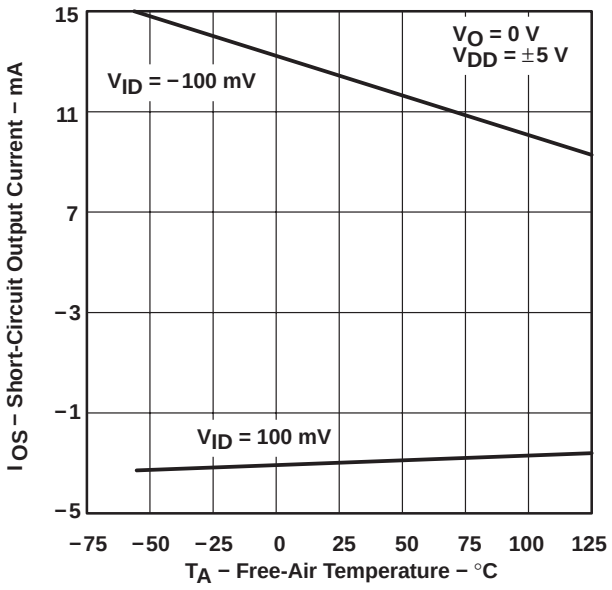


Figure 21

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

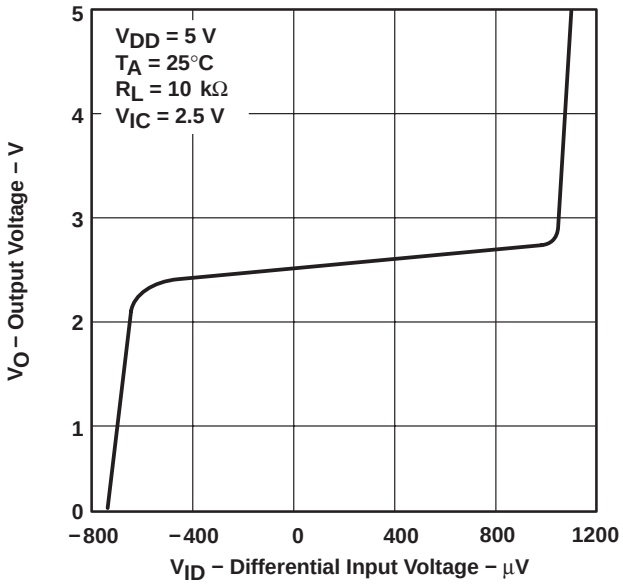


Figure 22

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

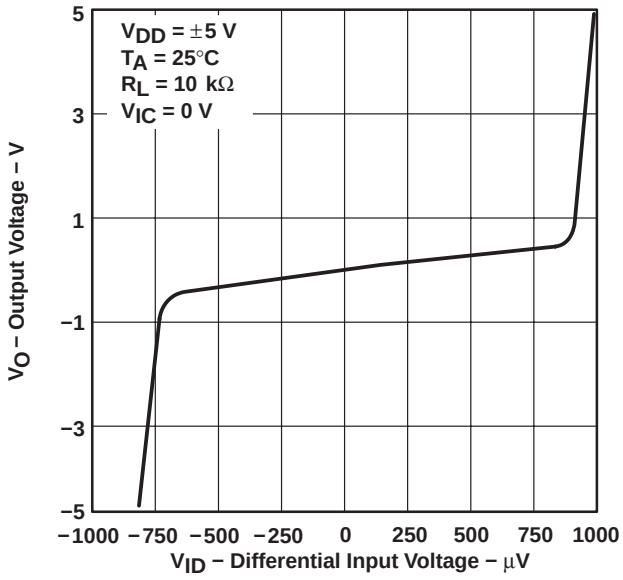


Figure 23

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs LOAD RESISTANCE

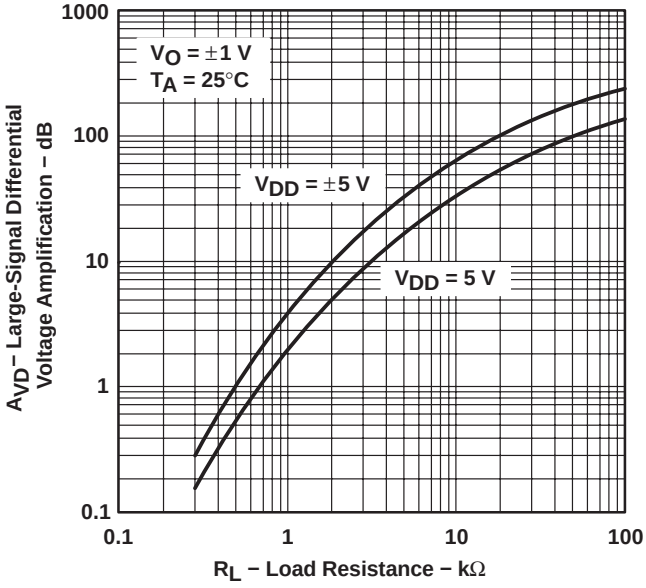


Figure 24

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

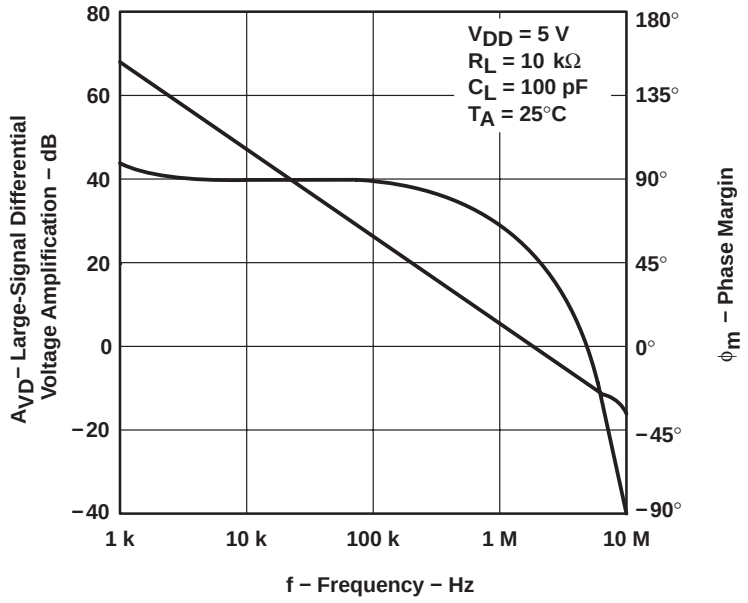


Figure 25

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

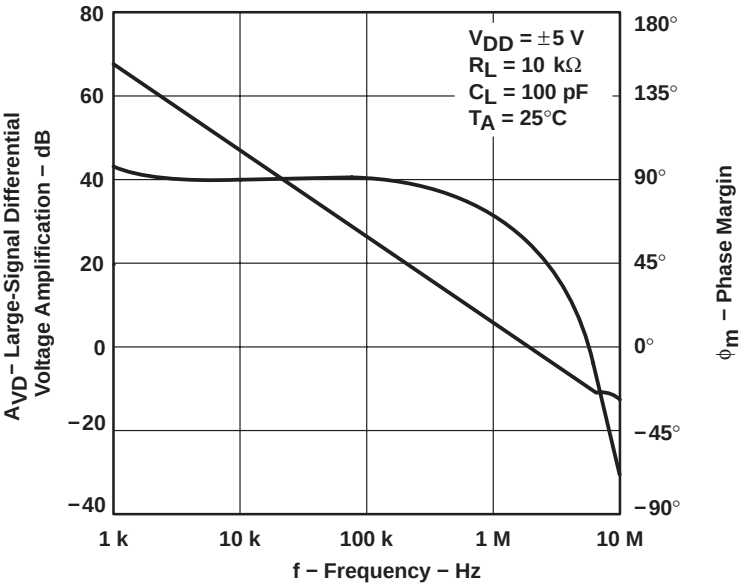


Figure 26

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION† vs FREE-AIR TEMPERATURE

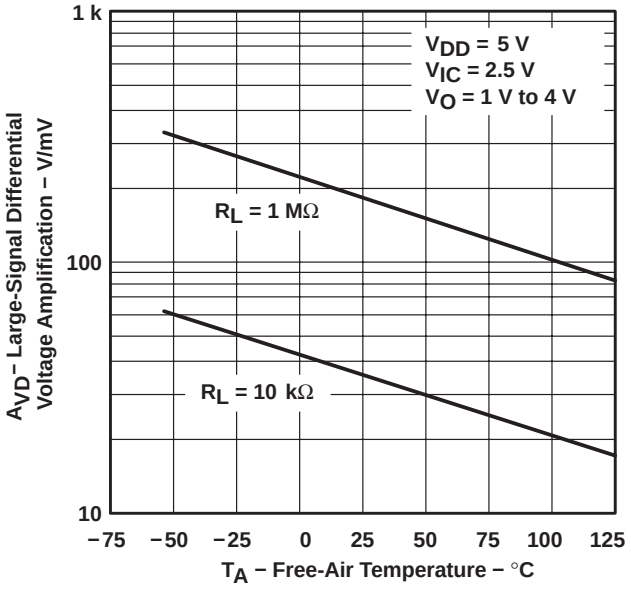


Figure 27

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION† vs FREE-AIR TEMPERATURE

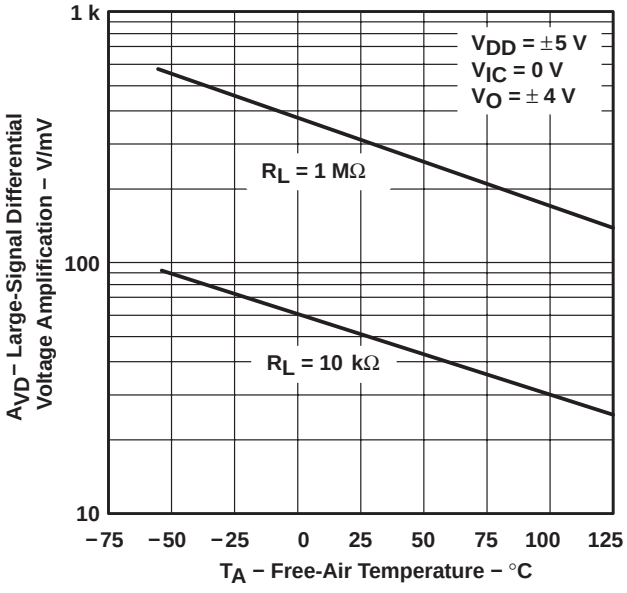


Figure 28

OUTPUT IMPEDANCE vs FREQUENCY

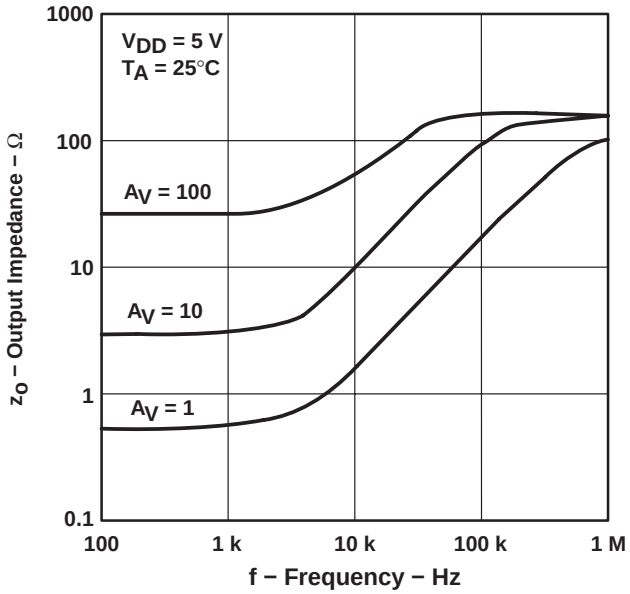


Figure 29

OUTPUT IMPEDANCE vs FREQUENCY

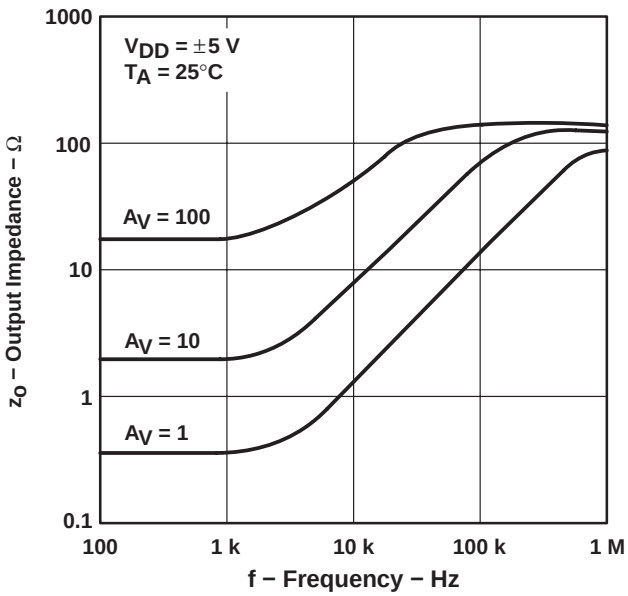


Figure 30

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO vs FREQUENCY

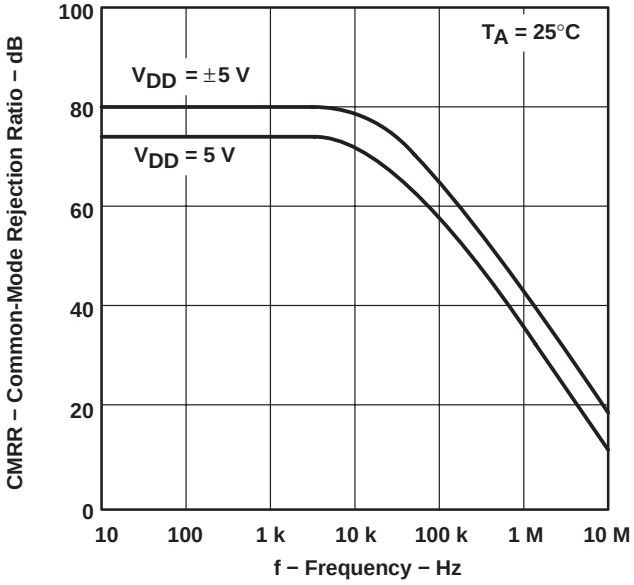


Figure 31

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

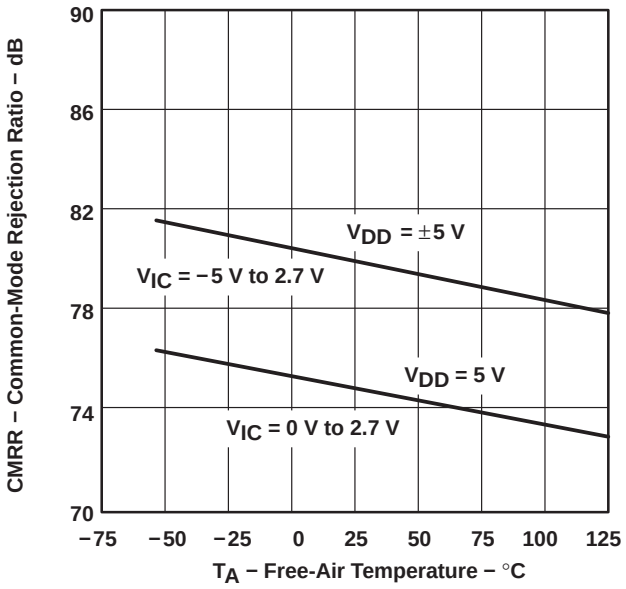


Figure 32

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

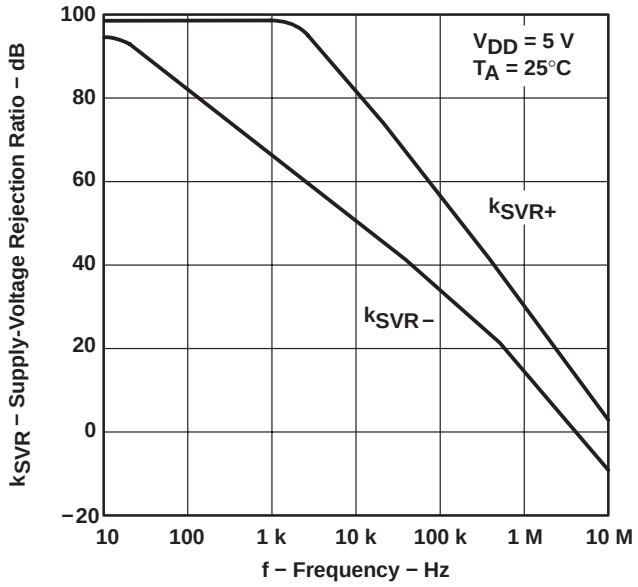


Figure 33

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

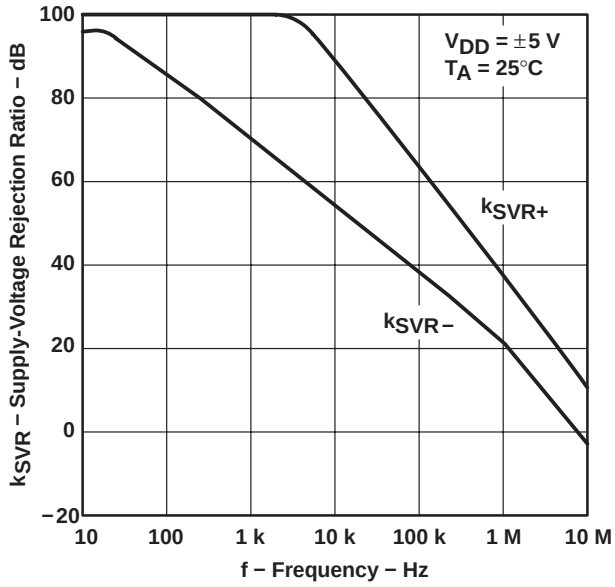


Figure 34

TYPICAL CHARACTERISTICS

SUPPLY VOLTAGE REJECTION RATIO† vs FREE-AIR TEMPERATURE

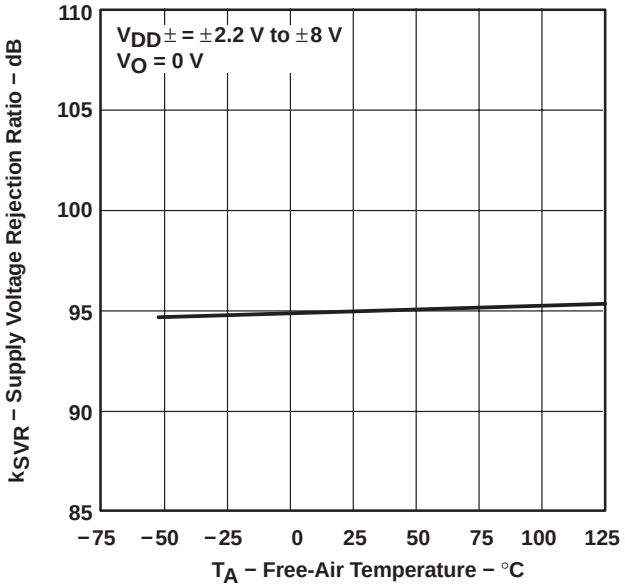


Figure 35

TLC2272 SUPPLY CURRENT† vs SUPPLY VOLTAGE

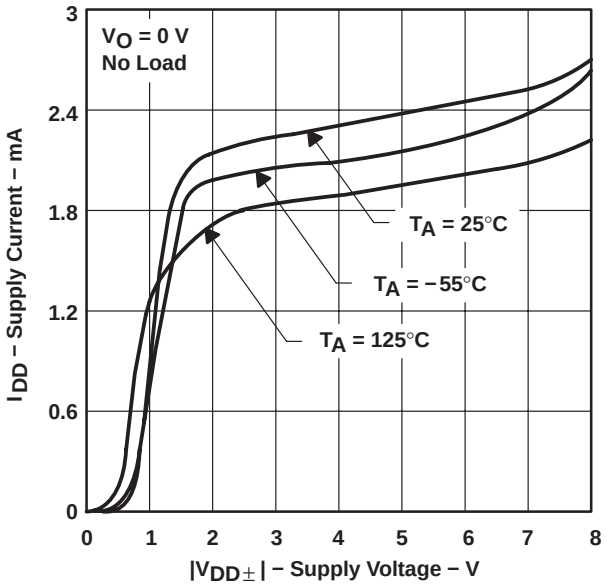


Figure 36

TLC2274 SUPPLY CURRENT† vs SUPPLY VOLTAGE

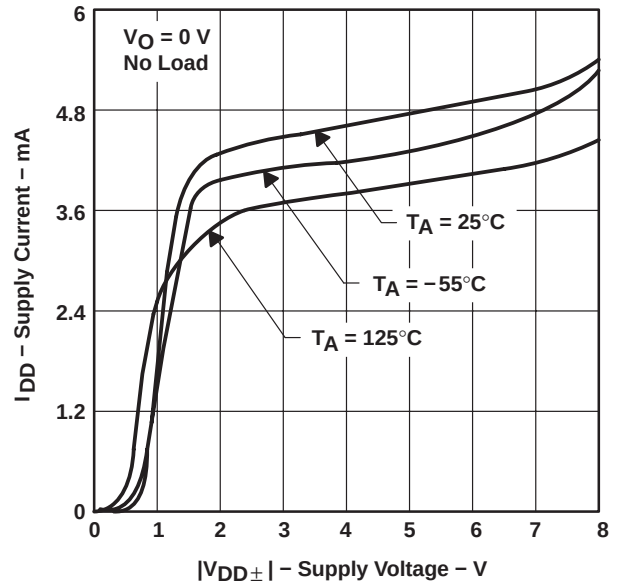


Figure 37

TLC2272 SUPPLY CURRENT† vs FREE-AIR TEMPERATURE

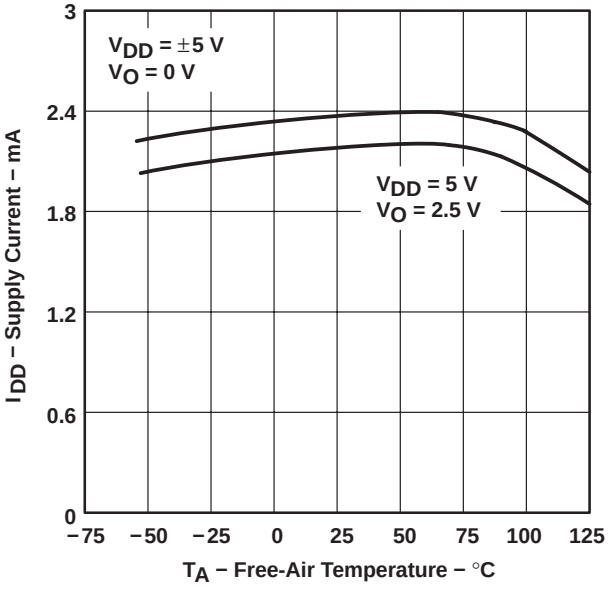


Figure 38

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

TLC2274
SUPPLY CURRENT†
vs
FREE-AIR TEMPERATURE

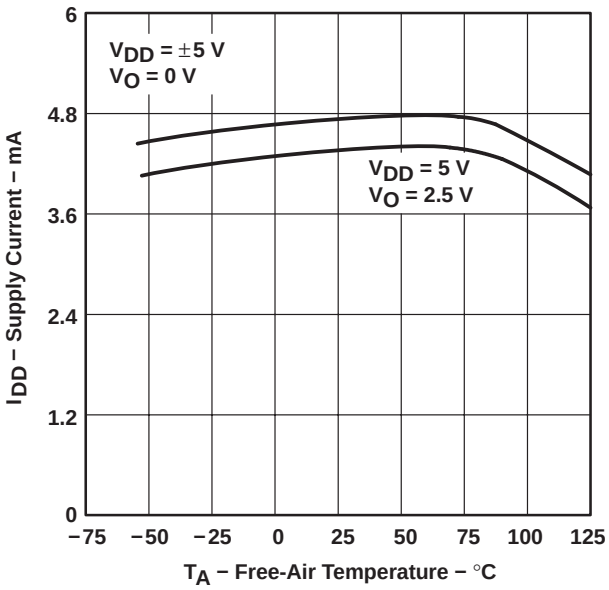


Figure 39

SLEW RATE
vs
LOAD CAPACITANCE

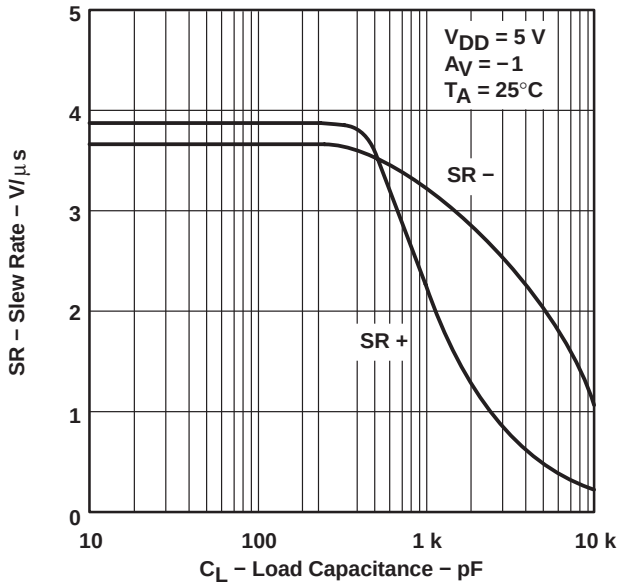


Figure 40

SLEW RATE†
vs
FREE-AIR TEMPERATURE

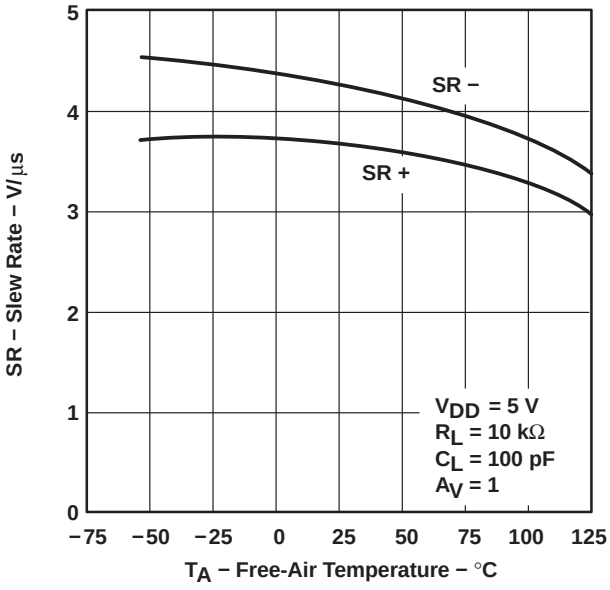


Figure 41

INVERTING LARGE-SIGNAL PULSE RESPONSE

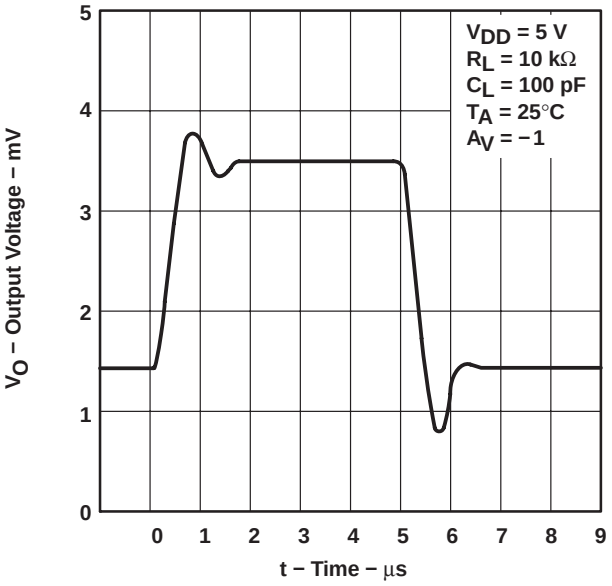


Figure 42

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

INVERTING LARGE-SIGNAL PULSE RESPONSE

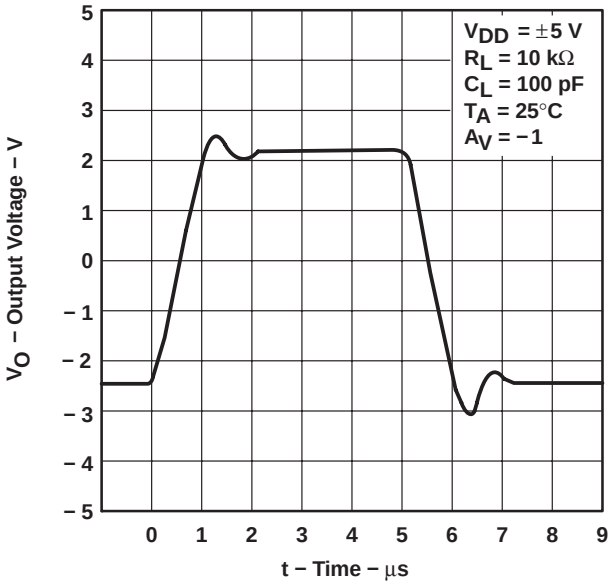


Figure 43

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

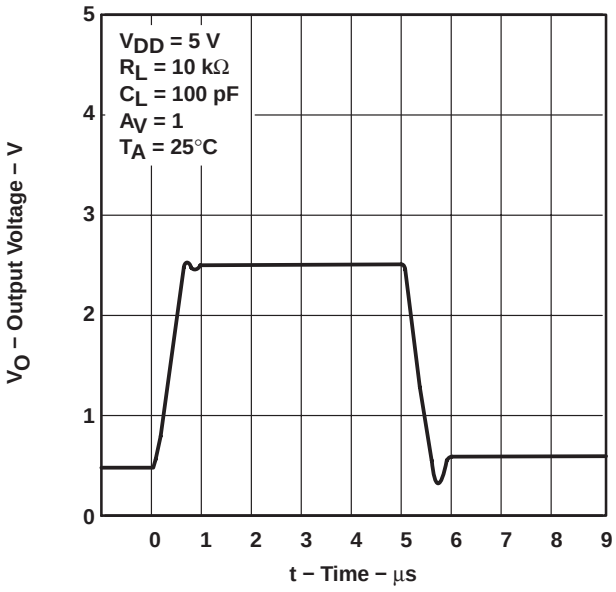


Figure 44

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

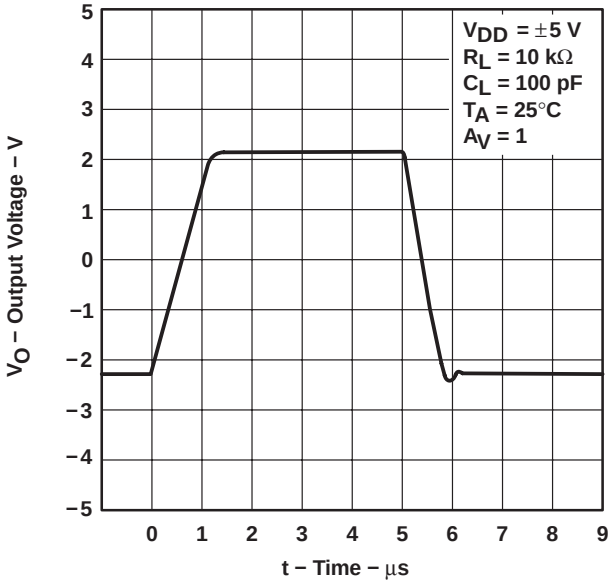


Figure 45

INVERTING SMALL-SIGNAL PULSE RESPONSE

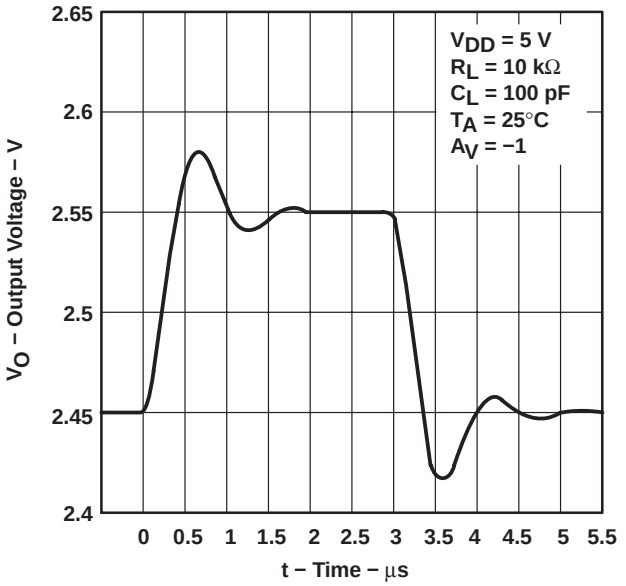


Figure 46

TYPICAL CHARACTERISTICS

INVERTING SMALL-SIGNAL PULSE RESPONSE

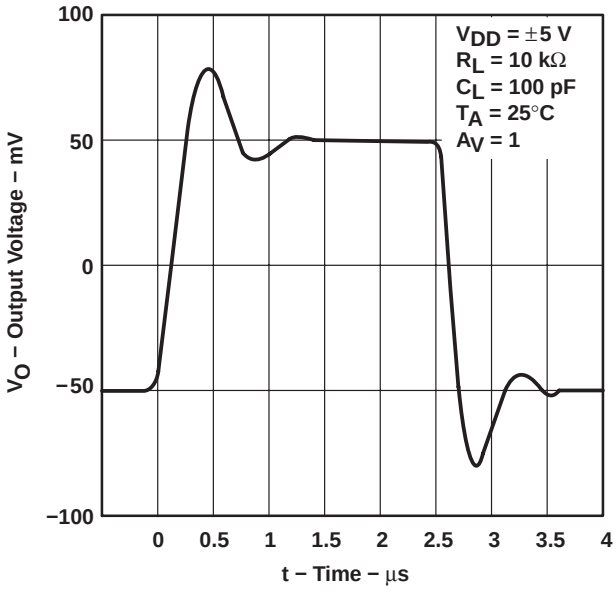


Figure 47

VOLTAGE-FOLLOWER
SMALL-SIGNAL PULSE RESPONSE

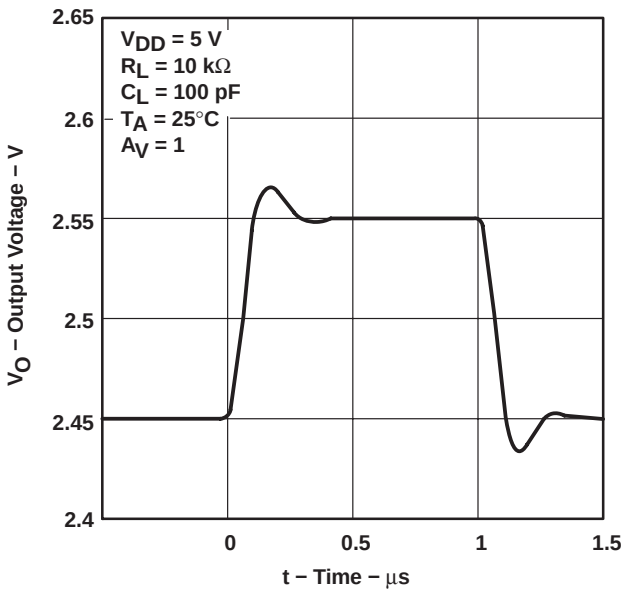


Figure 48

VOLTAGE-FOLLOWER
SMALL-SIGNAL PULSE RESPONSE

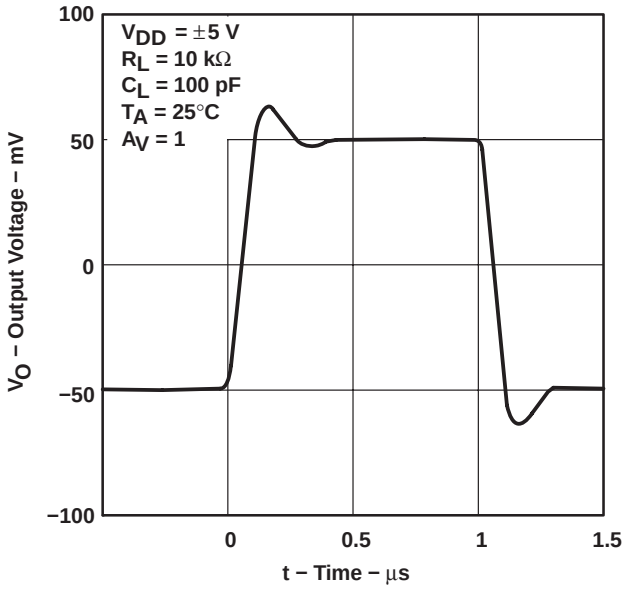


Figure 49

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

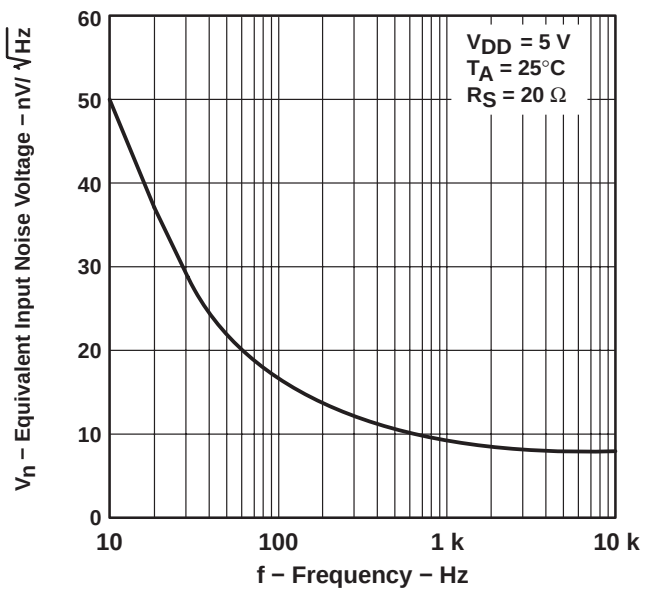


Figure 50

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

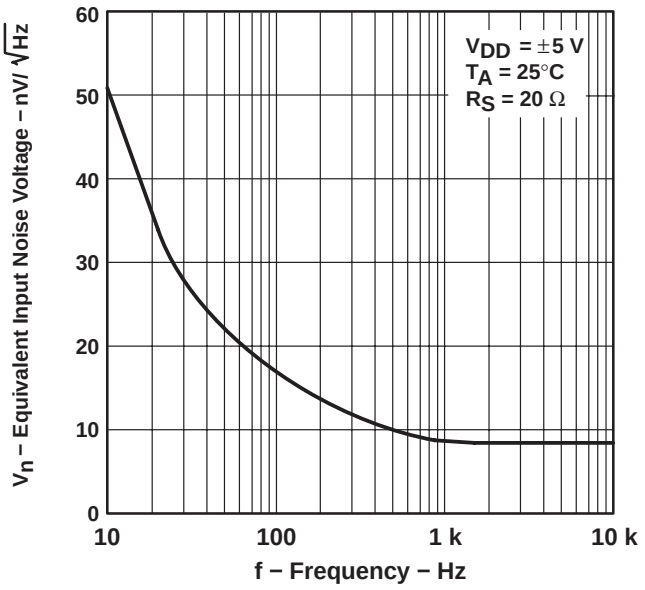


Figure 51

NOISE VOLTAGE OVER A 10 SECOND PERIOD

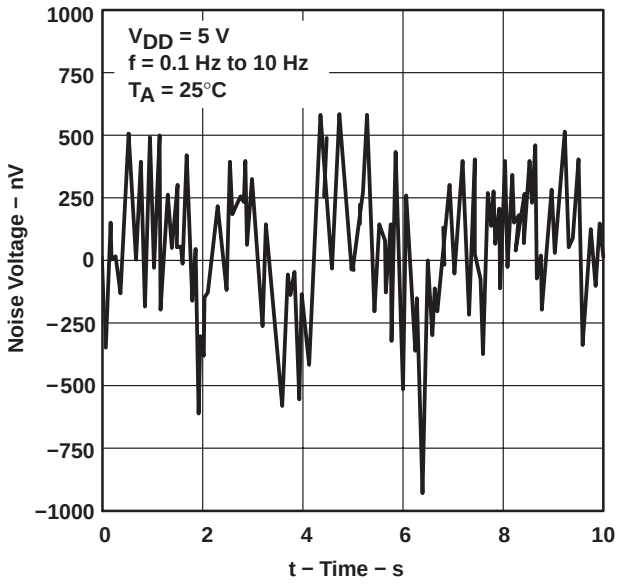


Figure 52

INTEGRATED NOISE VOLTAGE vs FREQUENCY

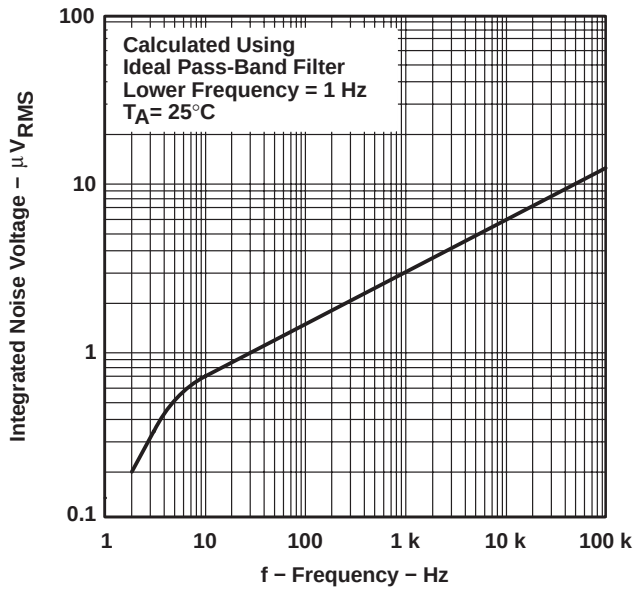


Figure 53

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

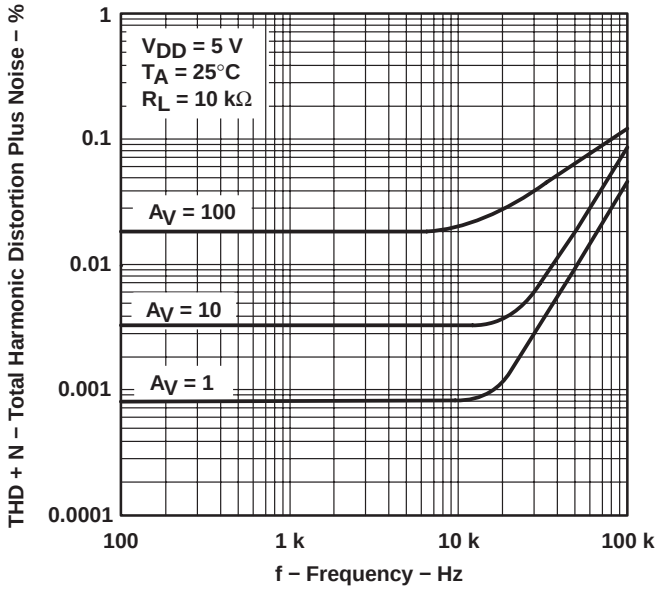


Figure 54

TYPICAL CHARACTERISTICS

GAIN-BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

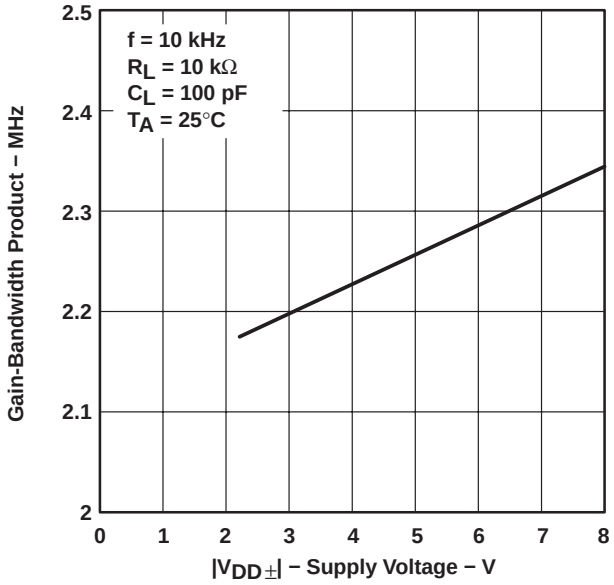


Figure 55

GAIN-BANDWIDTH PRODUCT† vs FREE-AIR TEMPERATURE

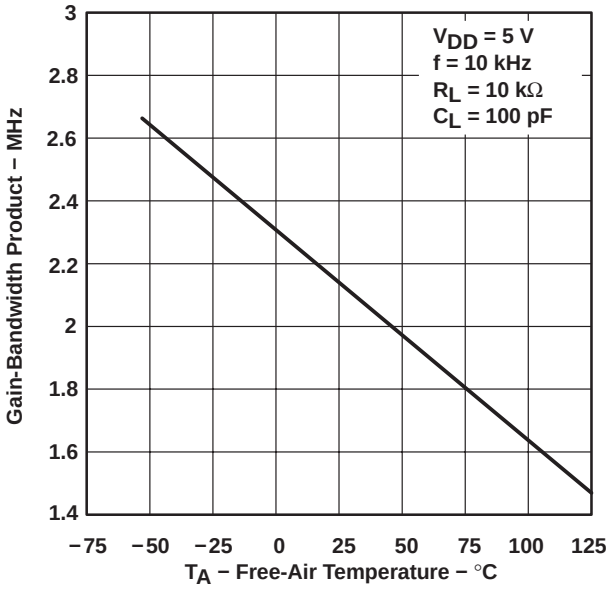


Figure 56

PHASE MARGIN vs LOAD CAPACITANCE

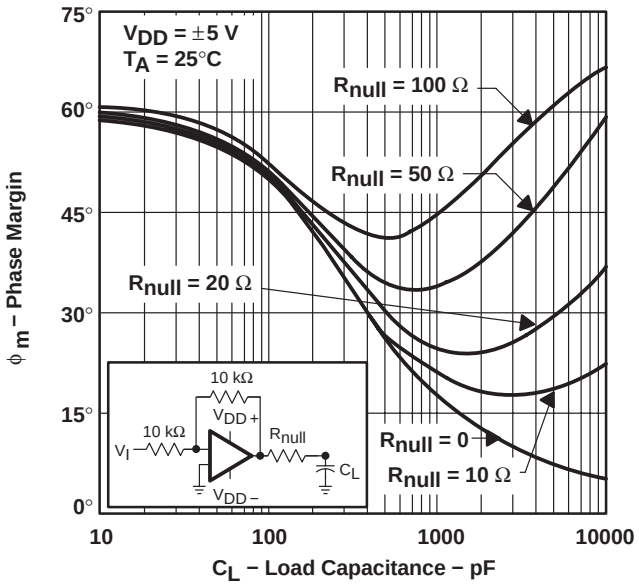


Figure 57

GAIN MARGIN vs LOAD CAPACITANCE

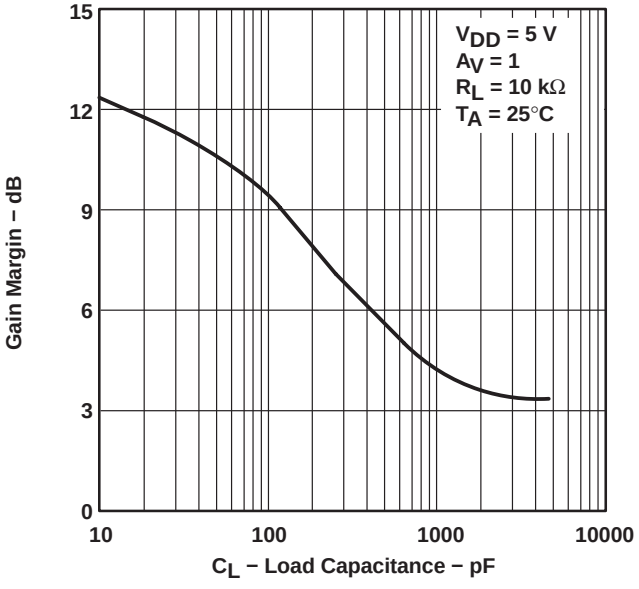


Figure 58

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

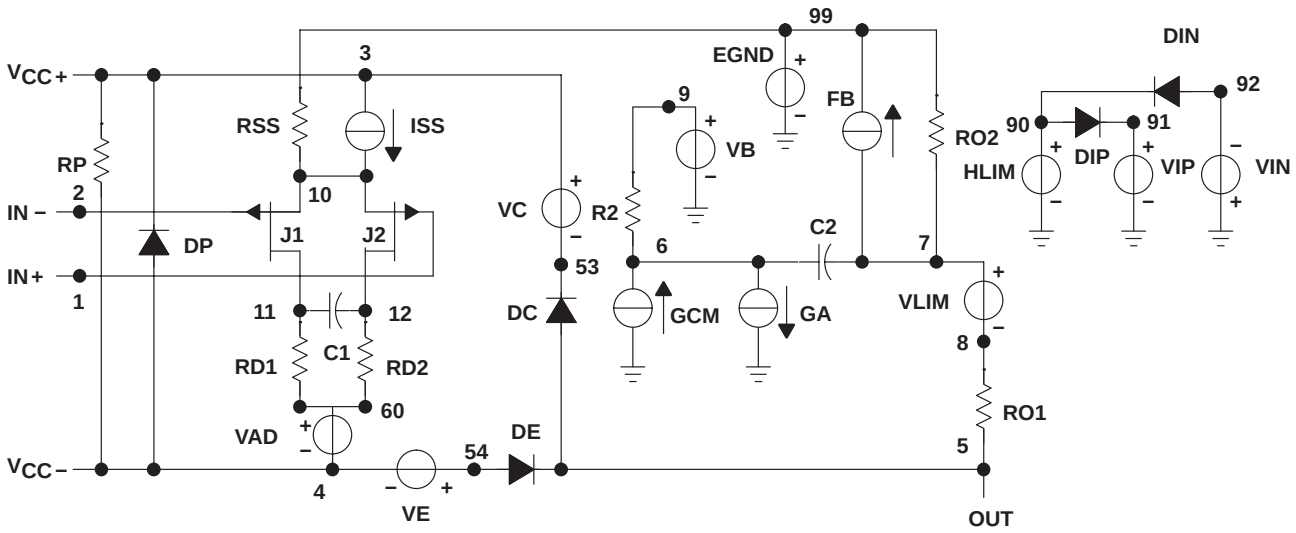
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 5) and subcircuit in Figure 59 were generated using the TLC227x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, “Macromodeling of Integrated Circuit Operational Amplifiers”, *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).




```
.SUBCKT TLC227x 1 2 3 4 5
C1      11      12      1214E−12
C2      6       7       760.00E−12
DC      5       53      DX
DE      54      5       DX
DLP     90      91      DX
DLN     92      90      DX
DP      4       3       DX
EGND    99      0       POLY (2) (3,0) (4,) 0 .5 .5
FB      99      0       POLY (5) VB VC VE VLP VLN 0
+ 984.9E3 −1E6 1E6 1E6 −1E6
GA      6       0       11 12 377.0E−6
GCM 0 6 10 99 134E−9
ISS     3       10      DC 216.OE−6
HLIM    90      0       VLIM 1K
J1      11      1       210 JX
J2      12      1       110 JX
R2      6       9       100.OE3
RD1     60      11      2.653E3
RD2     60      12      2.653E3
R01     8       5       50
R02     7       99      50
RP      3       4       4.310E3
RSS     10      99      925.9E3
VAD     60      4       −.5
VB      9       0       DC 0
VC 3 53 DC .78
VE      54      4       DC .78
VLIM    7       8       DC 0
VLP     91      0       DC 1.9
VLN     0       92      DC 9.4
.MODEL DX D (IS=800.0E−18)
.MODEL JX PJF (IS=1.500E−12BETA=1.316E-3
+ VTO=−.270)
.ENDS
```

Figure 59. Boyle Macromodel and Subcircuit

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9318201M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9318201M2A TLC2274 MFKB	Samples
5962-9318201MCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9318201MCA TLC2274MJB	Samples
5962-9318201QDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9318201QDA TLC2274MWB	Samples
5962-9318202Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9318202Q2A TLC2274 AMFKB	Samples
5962-9318202QCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9318202QCA TLC2274AMJB	Samples
5962-9318202QDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9318202QDA TLC2274AMWB	Samples
5962-9555201NXD	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	Q2272M	Samples
5962-9555201NXDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	Q2272M	Samples
5962-9555201Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9555201Q2A TLC2272 MFKB	Samples
5962-9555201QHA	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	9555201QHA TLC2272M	Samples
5962-9555201QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9555201QPA TLC2272M	Samples
5962-9555202Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9555202Q2A TLC2272 AMFKB	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9555202QHA	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	9555202QHA TLC2272AM	Samples
5962-9555202QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9555202QPA TLC2272AM	Samples
TLC2272ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2272AC	Samples
TLC2272ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2272AC	Samples
TLC2272ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2272AC	Samples
TLC2272ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2272AC	Samples
TLC2272ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC2272AC	Samples
TLC2272ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC2272AC	Samples
TLC2272ACPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		P2272A	Samples
TLC2272ACPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		P2272A	Samples
TLC2272ACPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI			
TLC2272ACPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		P2272A	Samples
TLC2272ACPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		P2272A	Samples
TLC2272AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2272AI	Samples
TLC2272AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2272AI	Samples
TLC2272AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2272AI	Samples
TLC2272AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2272AI	Samples
TLC2272AIP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC2272AI	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC2272AIPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC2272AI	Samples
TLC2272AMD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2272AM	Samples
TLC2272AMDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2272AM	Samples
TLC2272AMDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2272AM	Samples
TLC2272AMDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2272AM	Samples
TLC2272AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9555202Q2A TLC2272 AMFKB	Samples
TLC2272AMJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9555202QPA TLC2272AM	Samples
TLC2272AMP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	-55 to 125		
TLC2272AMUB	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	9555202QHA TLC2272AM	Samples
TLC2272AQD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C2272A	Samples
TLC2272AQDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		C2272A	Samples
TLC2272AQDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C2272A	Samples
TLC2272AQDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		C2272A	Samples
TLC2272CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2272C	Samples
TLC2272CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2272C	Samples
TLC2272CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2272C	Samples
TLC2272CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2272C	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC2272CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC2272CP	Samples
TLC2272CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC2272CP	Samples
TLC2272CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P2272	Samples
TLC2272CPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P2272	Samples
TLC2272CPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P2272	Samples
TLC2272CPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	0 to 70		
TLC2272CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P2272	Samples
TLC2272CPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P2272	Samples
TLC2272ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2272I	Samples
TLC2272IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2272I	Samples
TLC2272IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2272I	Samples
TLC2272IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2272I	Samples
TLC2272IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC2272IP	Samples
TLC2272IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC2272IP	Samples
TLC2272IPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		Y2272	Samples
TLC2272IPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		Y2272	Samples
TLC2272IPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI			
TLC2272IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		Y2272	Samples
TLC2272IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		Y2272	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC2272MD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2272M	Samples
TLC2272MDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2272M	Samples
TLC2272MDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2272M	Samples
TLC2272MDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2272M	Samples
TLC2272MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9555201Q2A TLC2272 MFKB	Samples
TLC2272MJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	TLC2272MJG	Samples
TLC2272MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9555201QPA TLC2272M	Samples
TLC2272MP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	-55 to 125		
TLC2272MUB	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	-55 to 125	9555201QHA TLC2272M	Samples
TLC2272QDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		C2272Q	Samples
TLC2272QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C2272Q	Samples
TLC2272QPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		T2272Q	Samples
TLC2274ACD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2274AC	Samples
TLC2274ACDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2274AC	Samples
TLC2274ACDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2274AC	Samples
TLC2274ACDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	2274AC	Samples
TLC2274ACN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC2274ACN	Samples
TLC2274ACNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC2274ACN	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC2274ACPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P2274A	Samples
TLC2274ACPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P2274A	Samples
TLC2274ACPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P2274A	Samples
TLC2274ACPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P2274A	Samples
TLC2274AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274AI	Samples
TLC2274AIDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274AI	Samples
TLC2274AIDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274AI	Samples
TLC2274AIDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274AI	Samples
TLC2274AIN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLC2274AIN	Samples
TLC2274AINE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	TLC2274AIN	Samples
TLC2274AIPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y2274A	Samples
TLC2274AIPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y2274A	Samples
TLC2274AIPWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125		
TLC2274AIPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y2274A	Samples
TLC2274AIPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y2274A	Samples
TLC2274AMD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2274AM	Samples
TLC2274AMDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2274AM	Samples
TLC2274AMDR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125		
TLC2274AMDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		2274AM	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC2274AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9318202Q2A TLC2274 AMFKB	Samples
TLC2274AMJB	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9318202QC A TLC2274AMJB	Samples
TLC2274AMWB	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9318202QD A TLC2274AMWB	Samples
TLC2274AQD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC2274A	Samples
TLC2274AQDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PJ2274A	Samples
TLC2274AQDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC2274A	Samples
TLC2274AQDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PJ2274A	Samples
TLC2274CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC2274C	Samples
TLC2274CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC2274C	Samples
TLC2274CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC2274C	Samples
TLC2274CDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC2274C	Samples
TLC2274CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC2274CN	Samples
TLC2274CNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC2274CN	Samples
TLC2274CNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC2274	Samples
TLC2274CPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		P2274	Samples
TLC2274CPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		P2274	Samples
TLC2274CPWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI			

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC2274CPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		P2274	Samples
TLC2274CPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	P2274	Samples
TLC2274ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC2274I	Samples
TLC2274IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC2274I	Samples
TLC2274IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC2274I	Samples
TLC2274IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC2274I	Samples
TLC2274IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC2274IN	Samples
TLC2274IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		Y2274	Samples
TLC2274IPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		Y2274	Samples
TLC2274IPWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI			
TLC2274IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		Y2274	Samples
TLC2274IPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		Y2274	Samples
TLC2274MD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLC2274M	Samples
TLC2274MDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PJ2274M	Samples
TLC2274MDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	TLC2274M	Samples
TLC2274MDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PJ2274M	Samples
TLC2274MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9318201M2A TLC2274 MFKB	Samples
TLC2274MJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	TLC2274MJ	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC2274MJB	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9318201MC A TLC2274MJB	Samples
TLC2274MN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	TLC2274MN	Samples
TLC2274MWB	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9318201QD A TLC2274MWB	Samples
TLC2274QD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC2274	Samples
TLC2274QDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC2274	Samples
TLC2274QDR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125	TLC2274	
TLC2274QDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC2274	Samples
TLC2274Y	PREVIEW	DIESALE	Y	0		TBD	Call TI	Call TI			

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TLC2272, TLC2272A, TLC2272AM, TLC2272M, TLC2274, TLC2274A, TLC2274AM, TLC2274M :

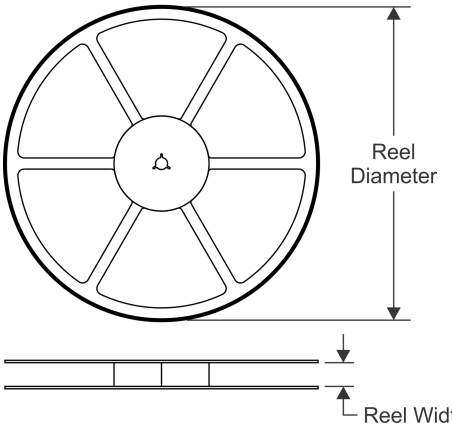
- Catalog: TLC2272A, TLC2272, TLC2274A, TLC2274
- Automotive: TLC2272-Q1, TLC2272A-Q1, TLC2272A-Q1, TLC2272-Q1, TLC2274-Q1, TLC2274A-Q1, TLC2274A-Q1, TLC2274-Q1
- Enhanced Product: TLC2272A-EP, TLC2272A-EP, TLC2274-EP, TLC2274A-EP, TLC2274A-EP, TLC2274-EP
- Military: TLC2272M, TLC2272AM, TLC2274M, TLC2274AM

NOTE: Qualified Version Definitions:

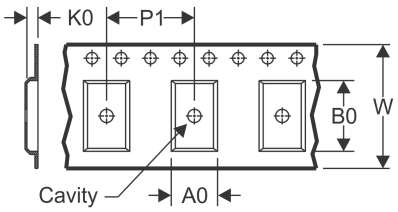
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

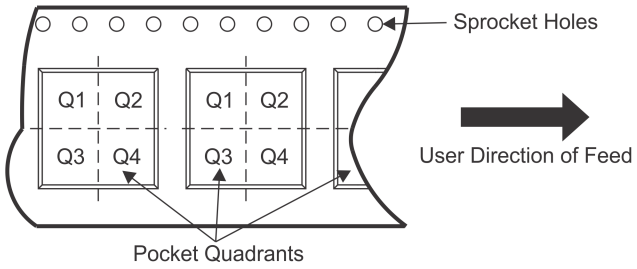


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

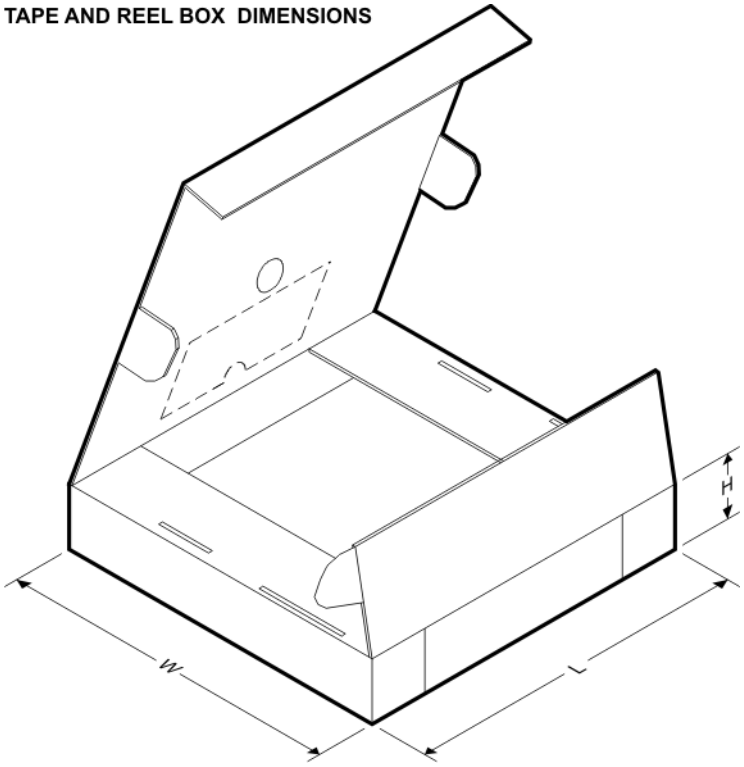


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
5962-9555201NXDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2272ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2272ACPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC2272AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2272AMDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2272AMDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2272CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2272CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC2272IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2272IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC2272MDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2274ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2274ACPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2274AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2274AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2274AQDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2274CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2274CNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC2274CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2274IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2274IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2274MDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2274MDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2274QDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



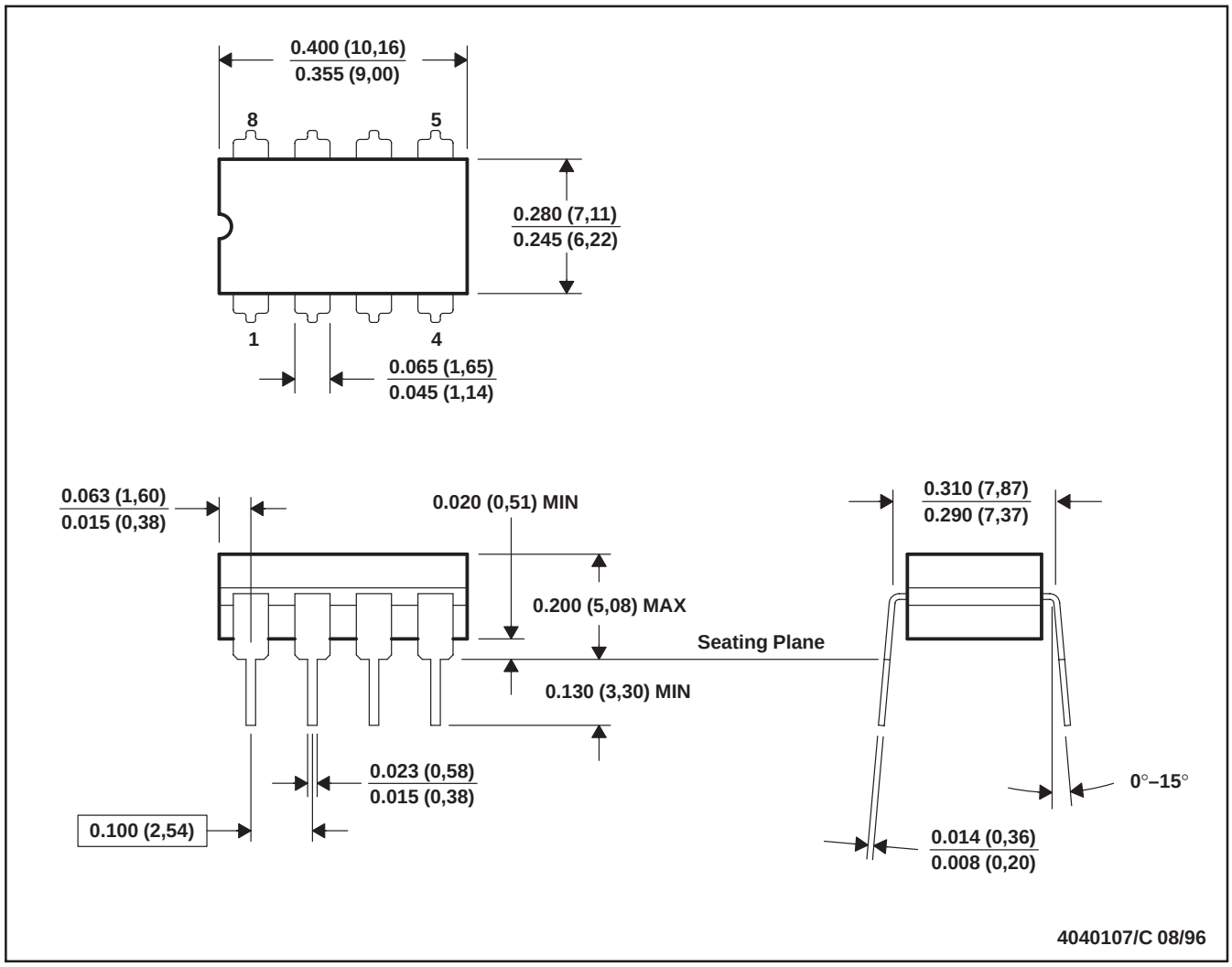
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
5962-9555201NXDR	SOIC	D	8	2500	367.0	367.0	35.0
TLC2272ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC2272ACPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TLC2272AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC2272AMDR	SOIC	D	8	2500	367.0	367.0	38.0
TLC2272AMDRG4	SOIC	D	8	2500	367.0	367.0	38.0
TLC2272CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC2272CPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TLC2272IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC2272IPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TLC2272MDR	SOIC	D	8	2500	367.0	367.0	38.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC2274ACDR	SOIC	D	14	2500	333.2	345.9	28.6
TLC2274ACPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TLC2274AIDR	SOIC	D	14	2500	333.2	345.9	28.6
TLC2274AIPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TLC2274AQDR	SOIC	D	14	2500	367.0	367.0	38.0
TLC2274CDR	SOIC	D	14	2500	333.2	345.9	28.6
TLC2274CNSR	SO	NS	14	2000	367.0	367.0	38.0
TLC2274CPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TLC2274IDR	SOIC	D	14	2500	333.2	345.9	28.6
TLC2274IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TLC2274MDR	SOIC	D	14	2500	367.0	367.0	38.0
TLC2274MDRG4	SOIC	D	14	2500	367.0	367.0	38.0
TLC2274QDRG4	SOIC	D	14	2500	367.0	367.0	38.0

MCER001A – JANUARY 1995 – REVISED JANUARY 1997

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**

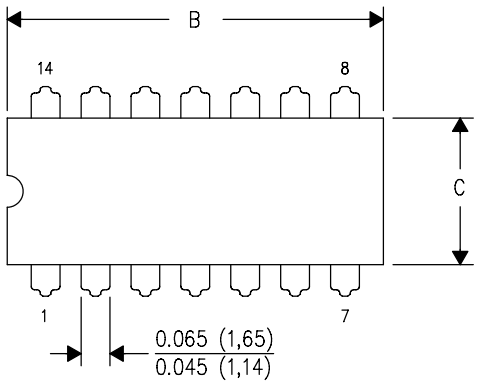


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

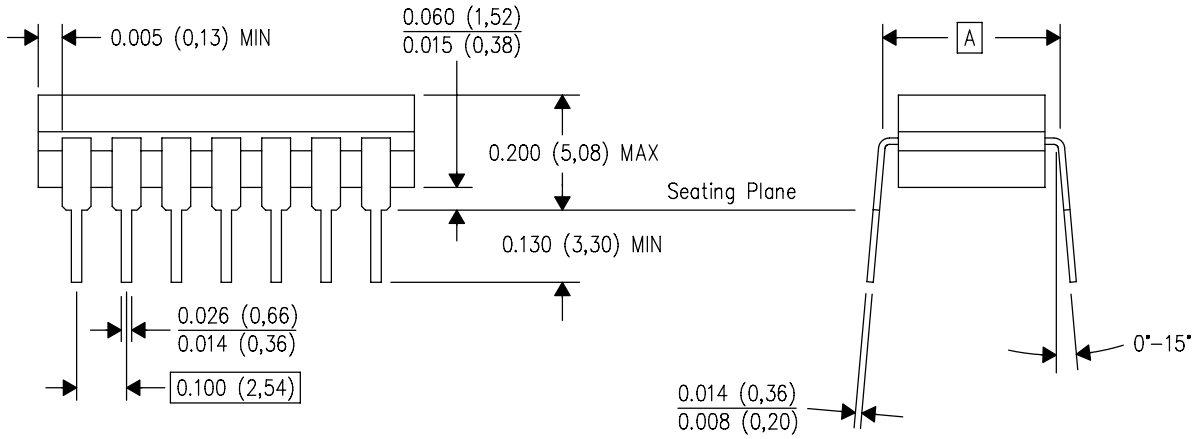
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



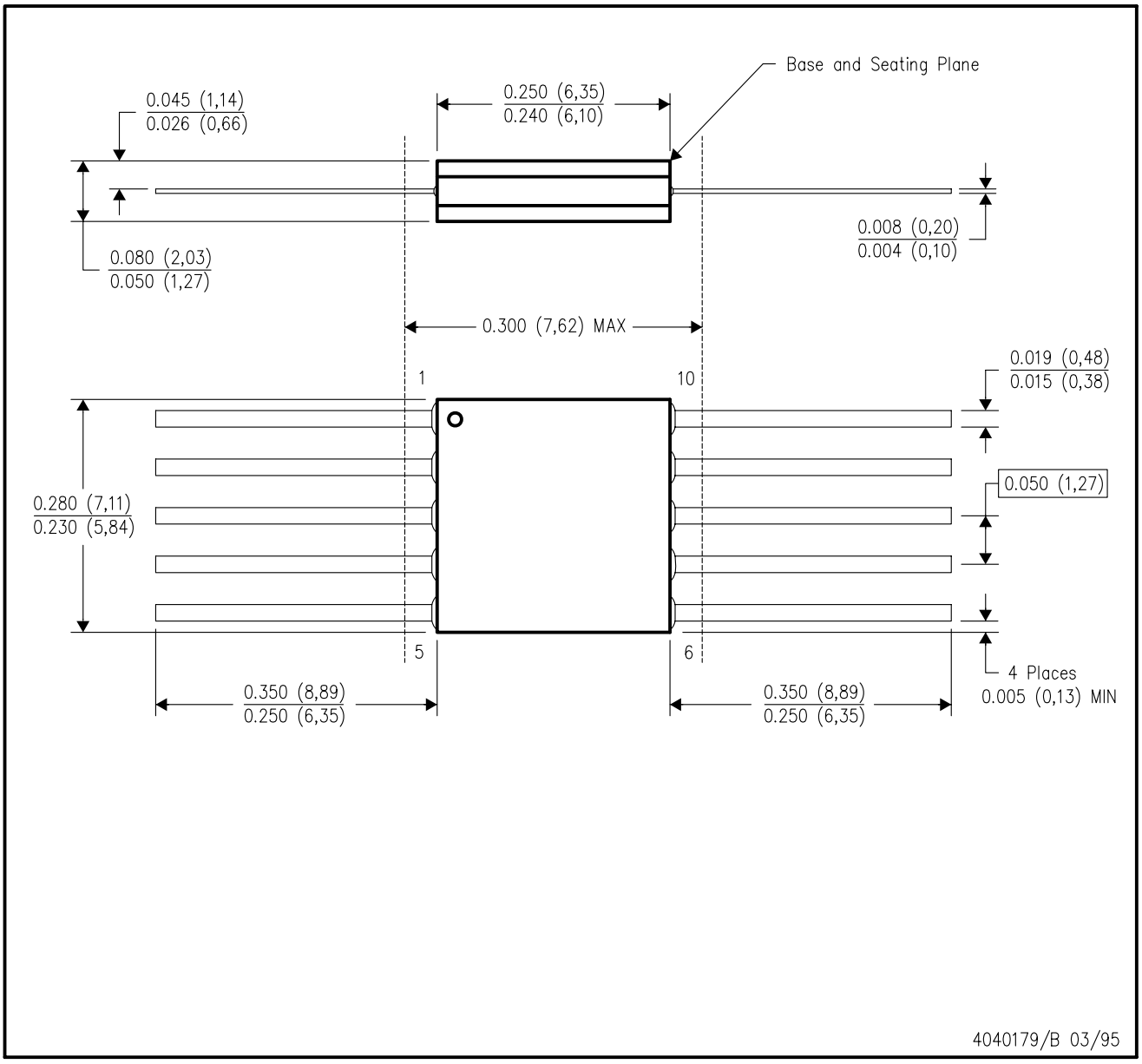
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

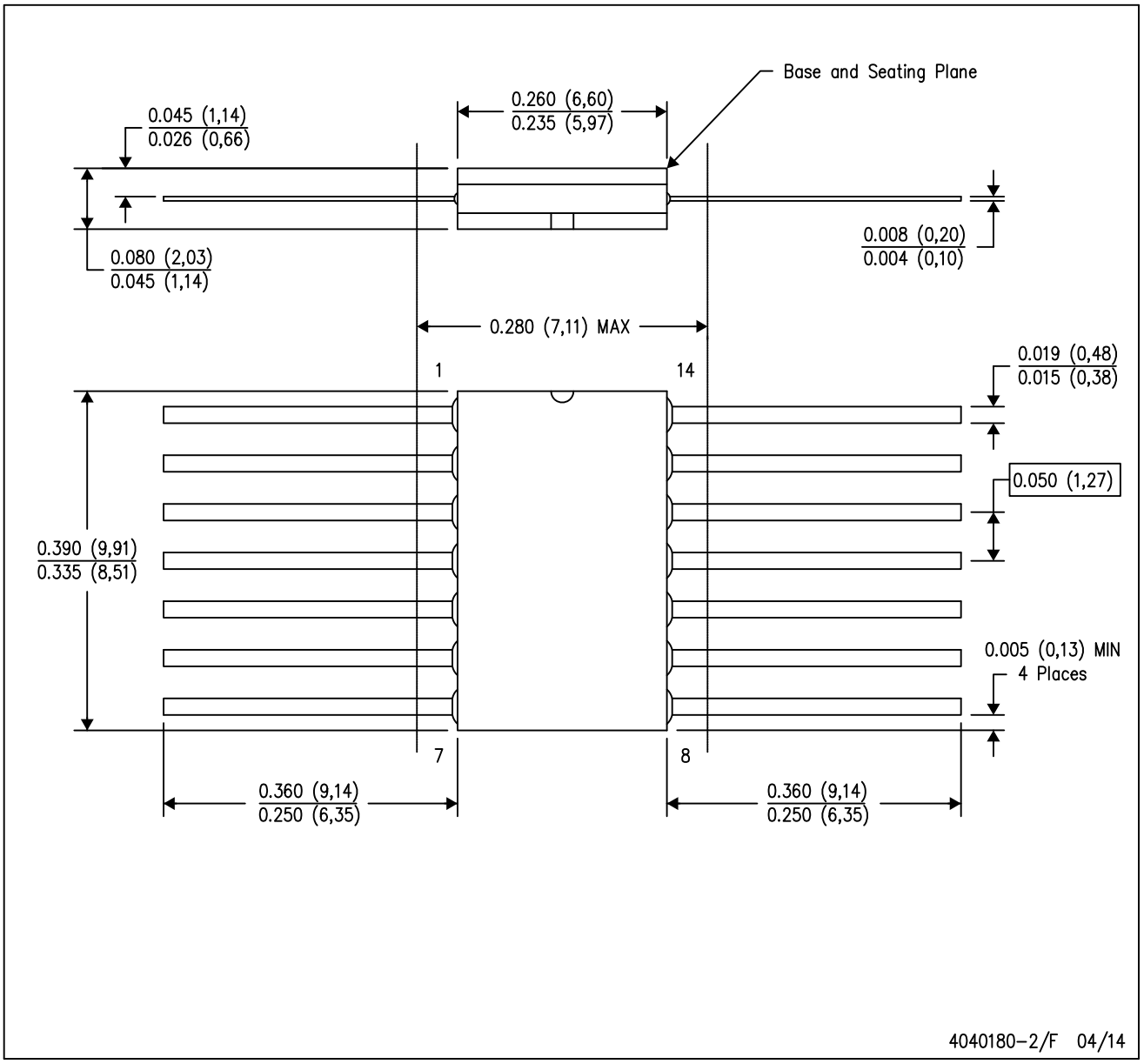
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

U (S–GDFP–F10) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F10 and JEDEC MO–092AA

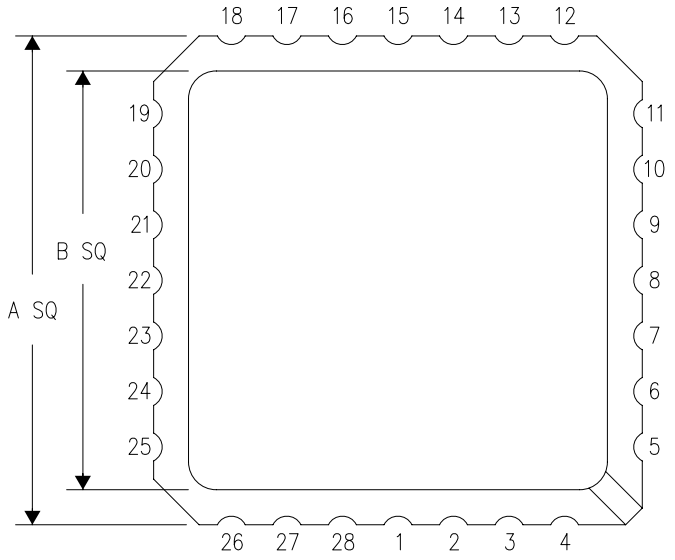
W (R–GDFP–F14) CERAMIC DUAL FLATPACK



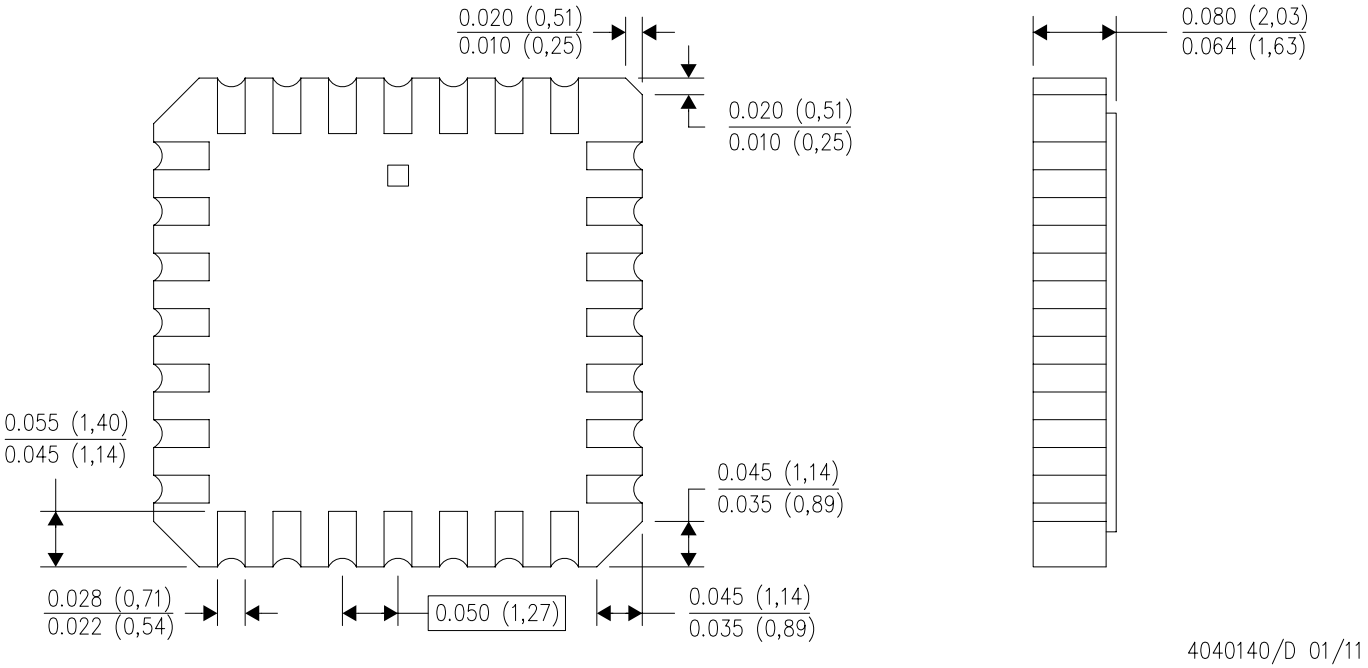
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



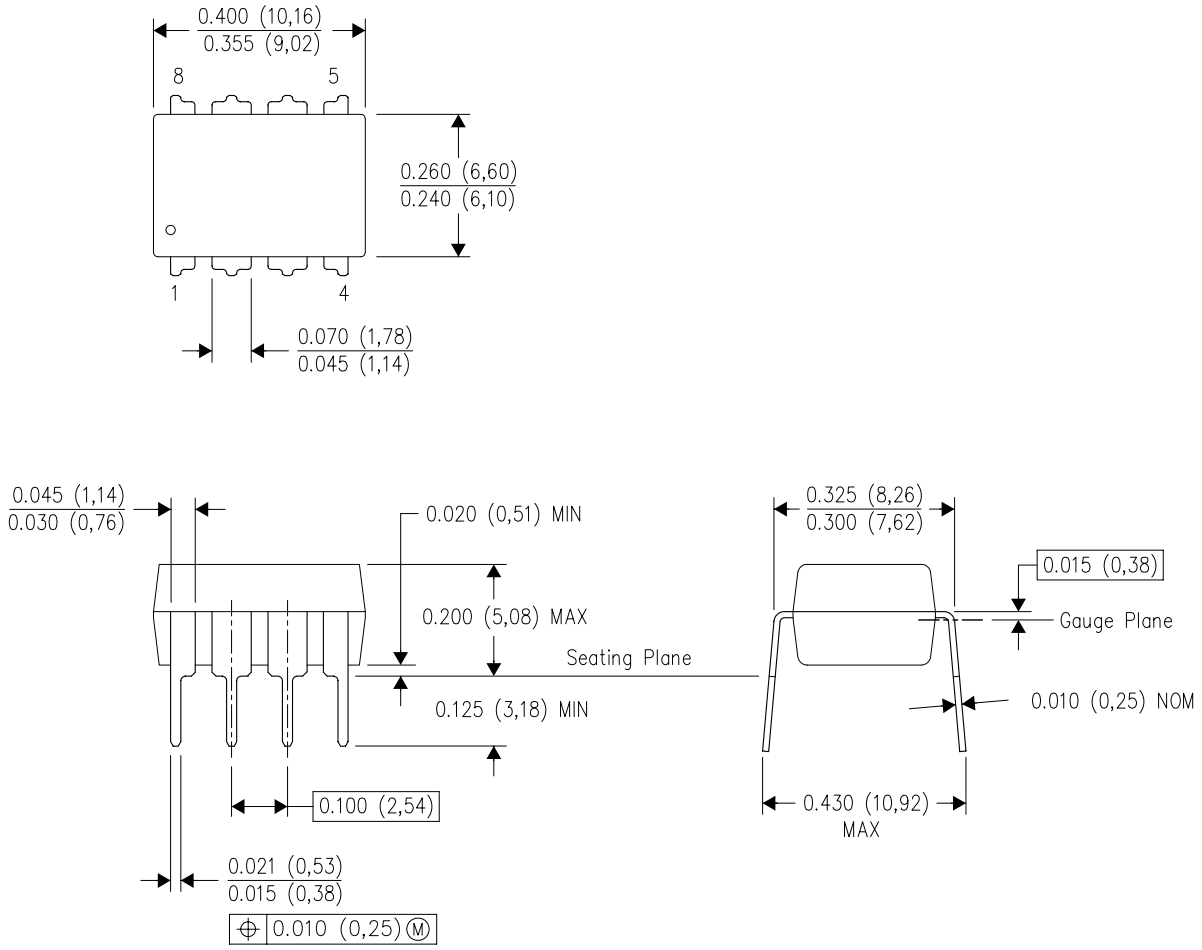
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

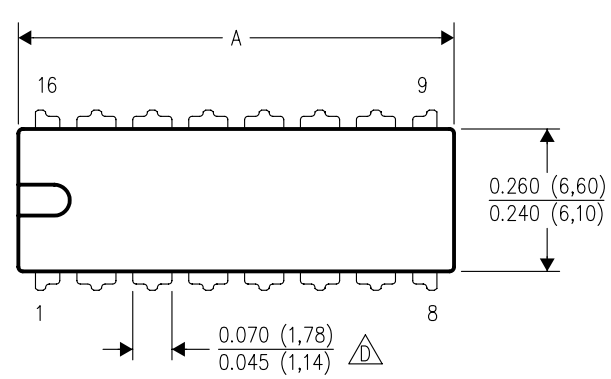


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

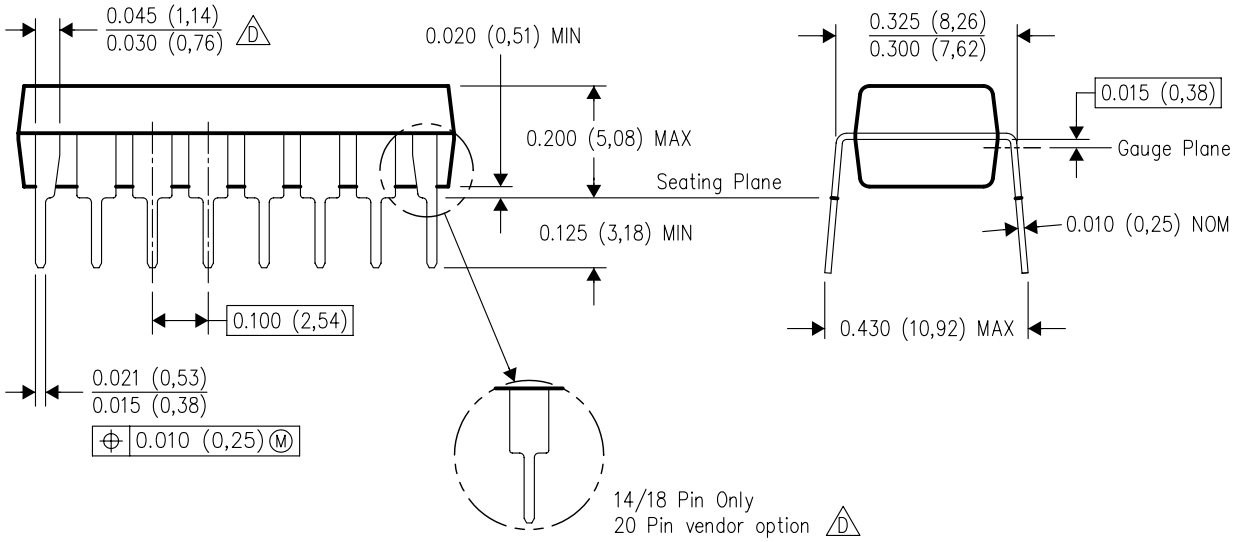
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



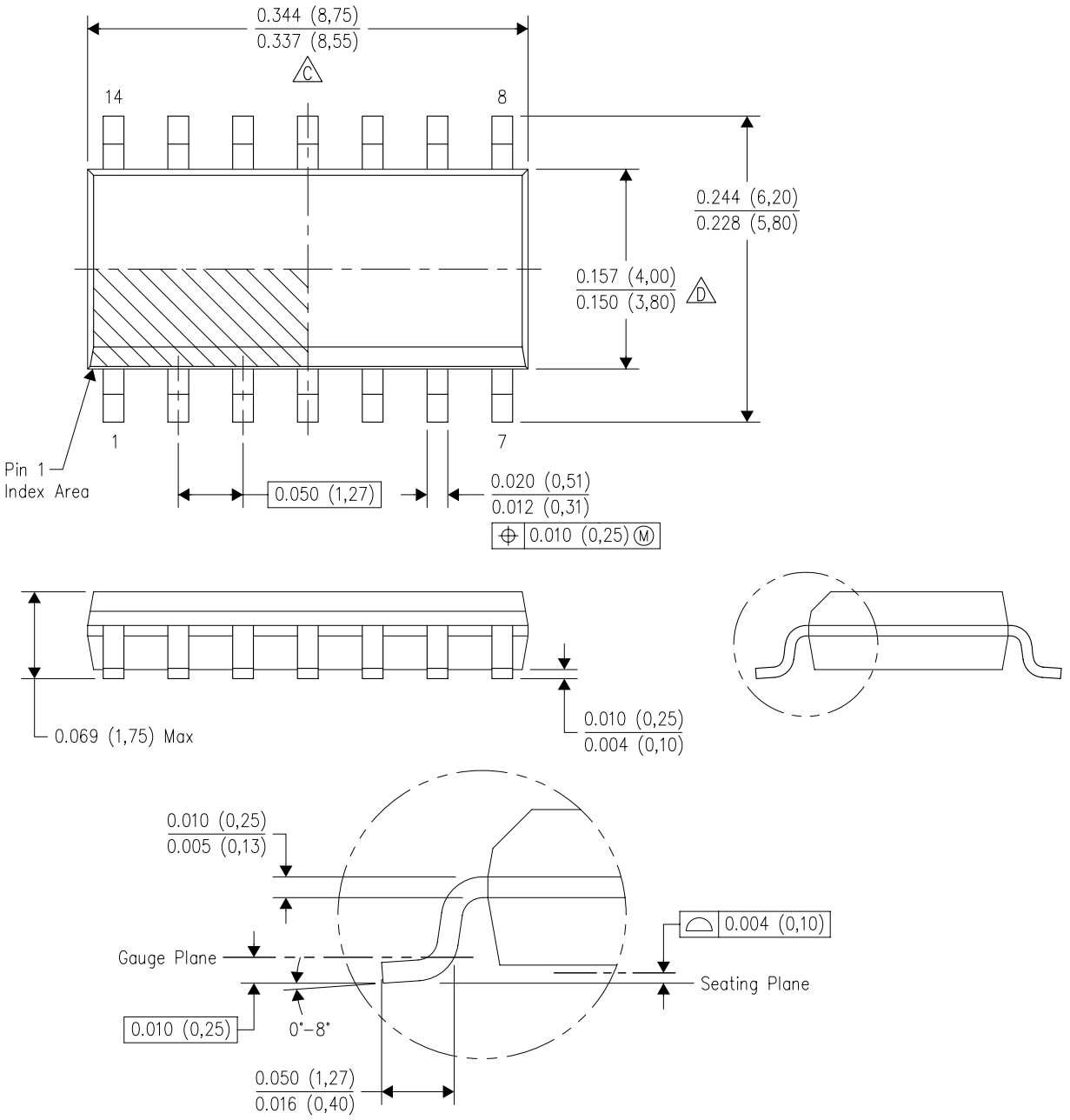
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

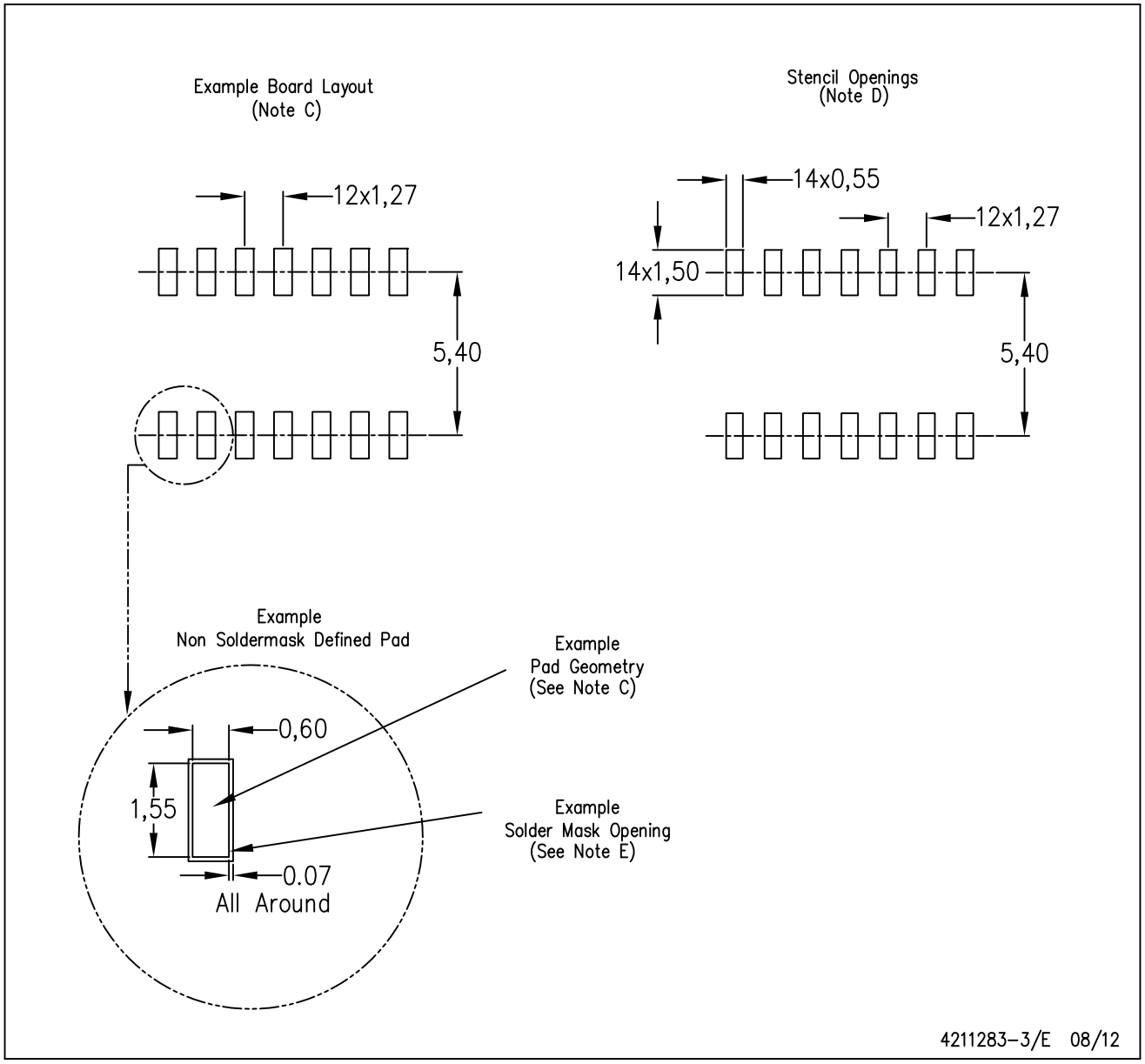
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

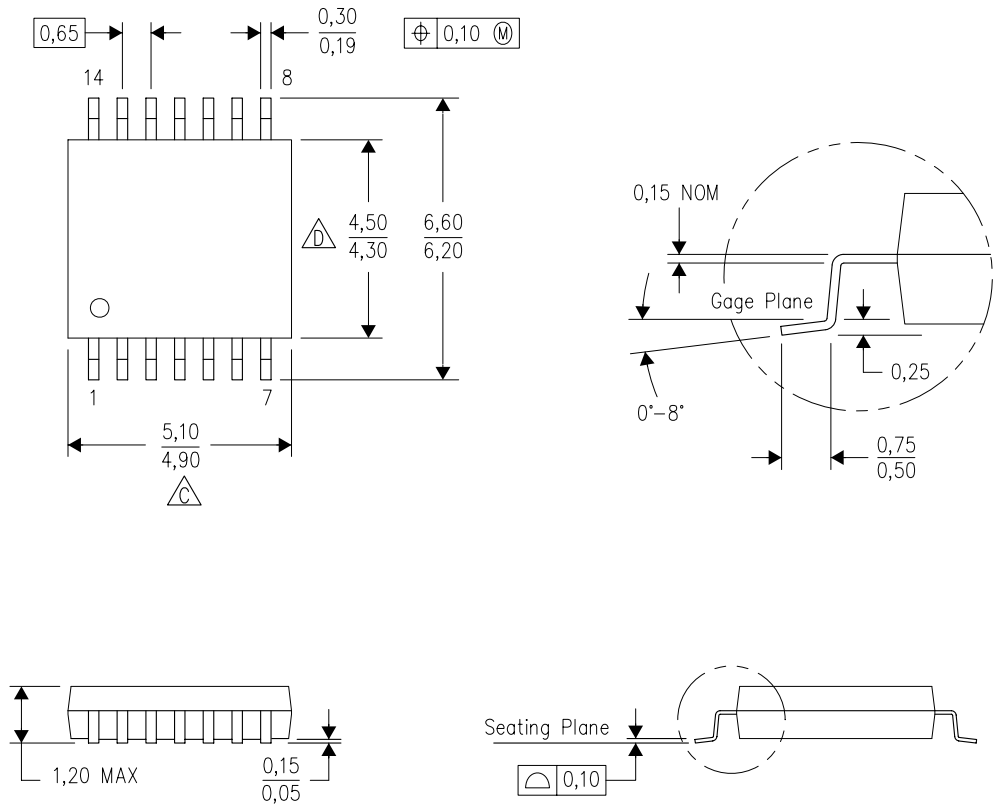
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

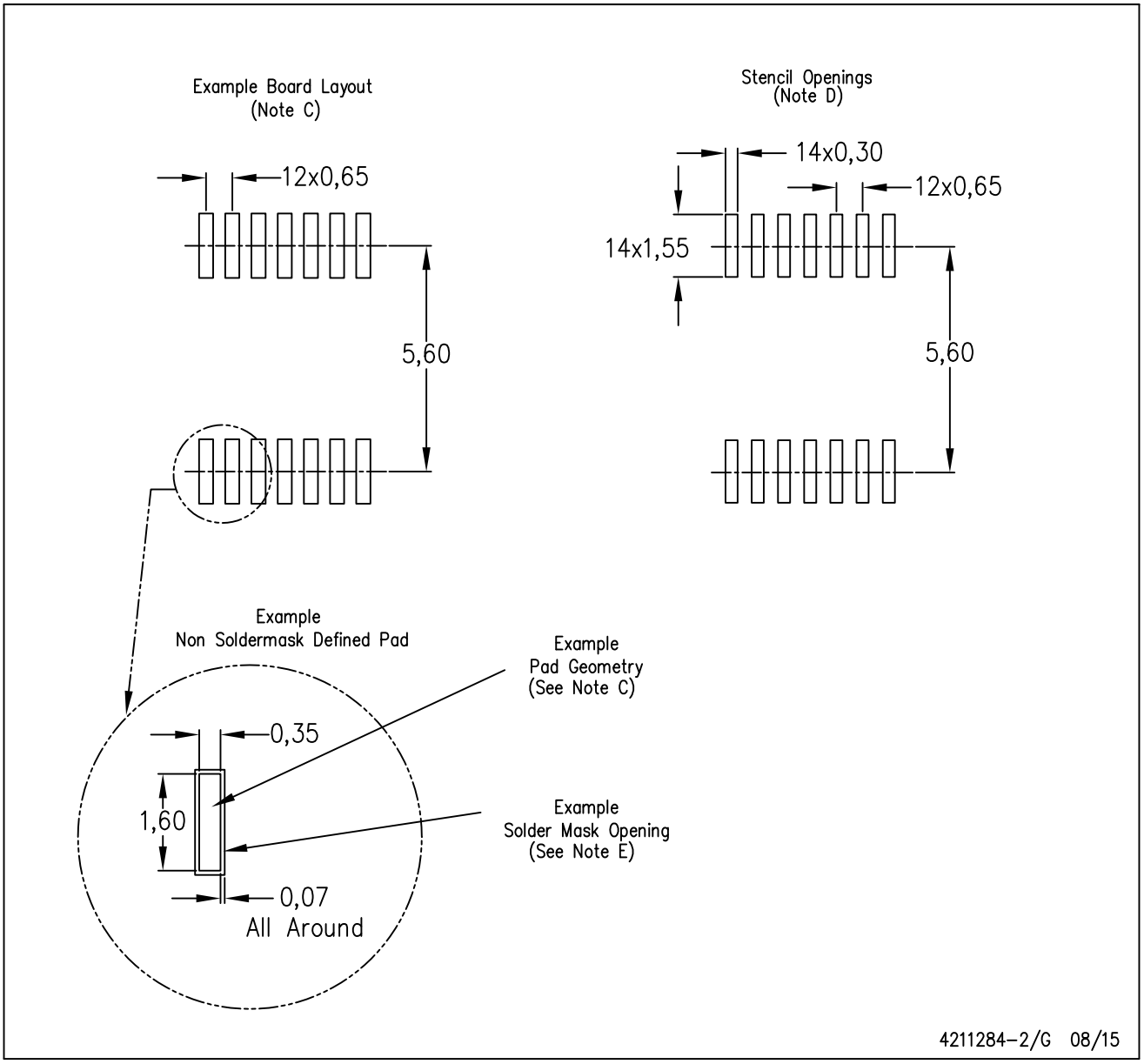
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



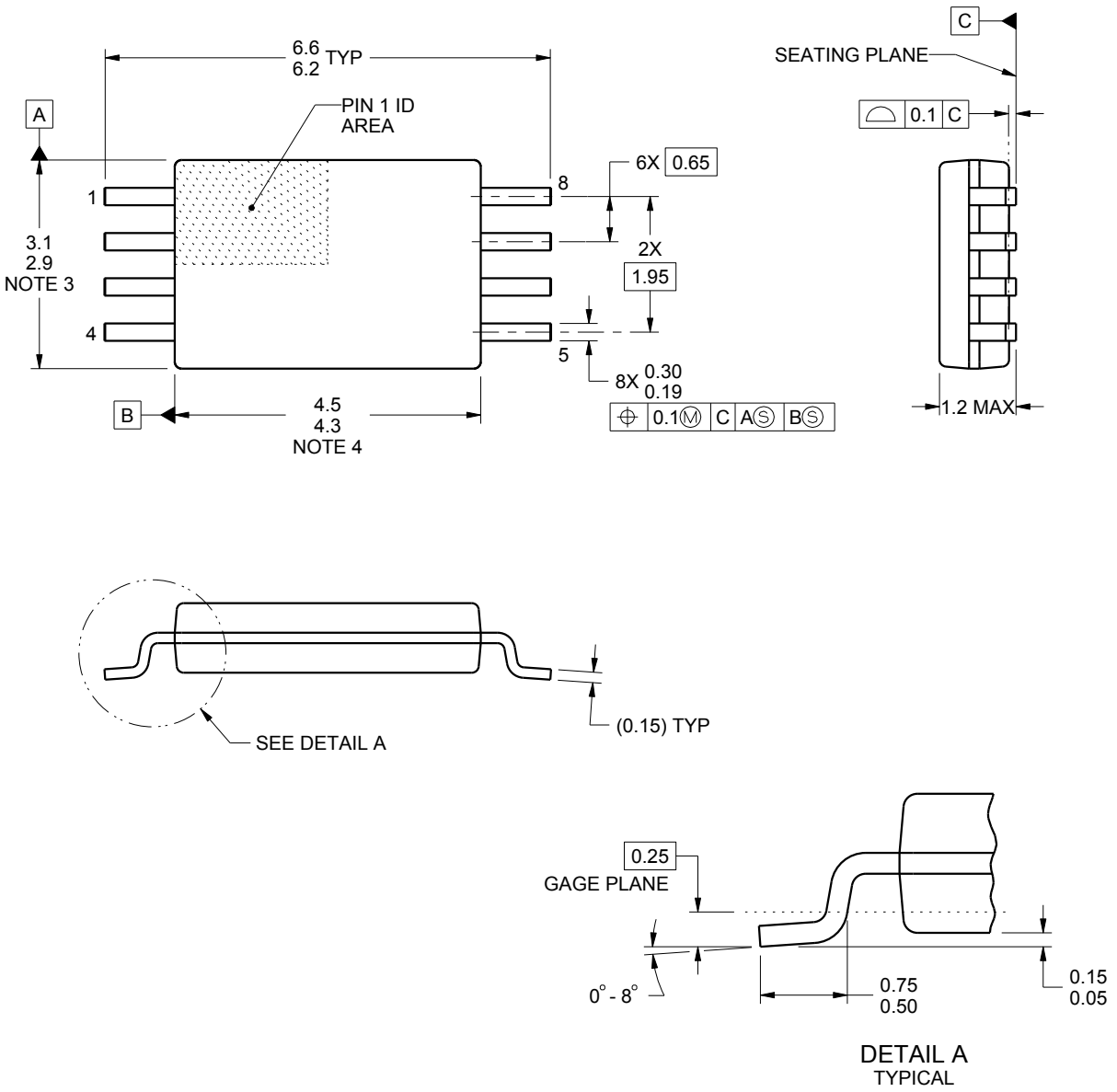
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0008A

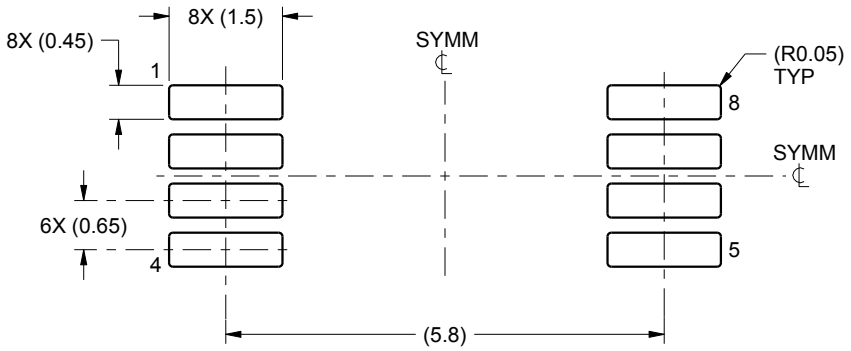
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

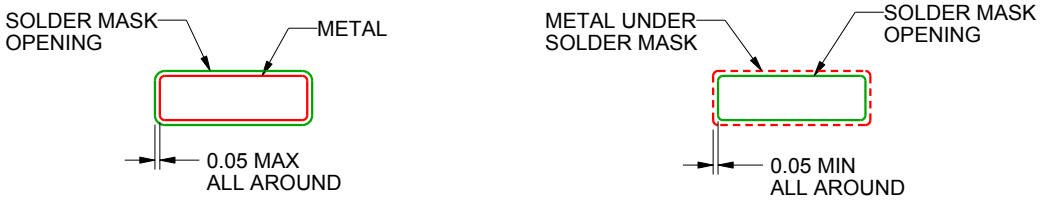


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

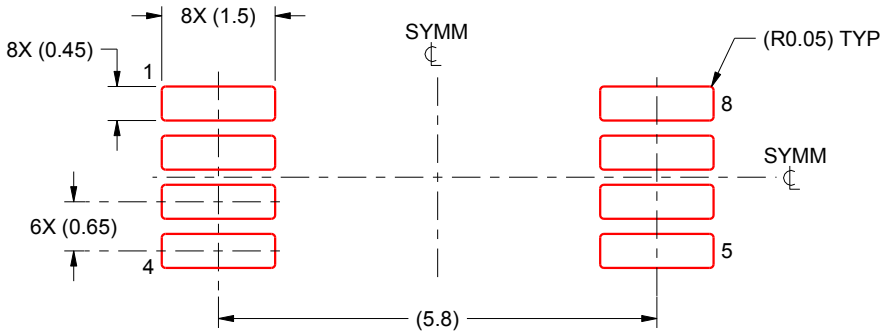


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



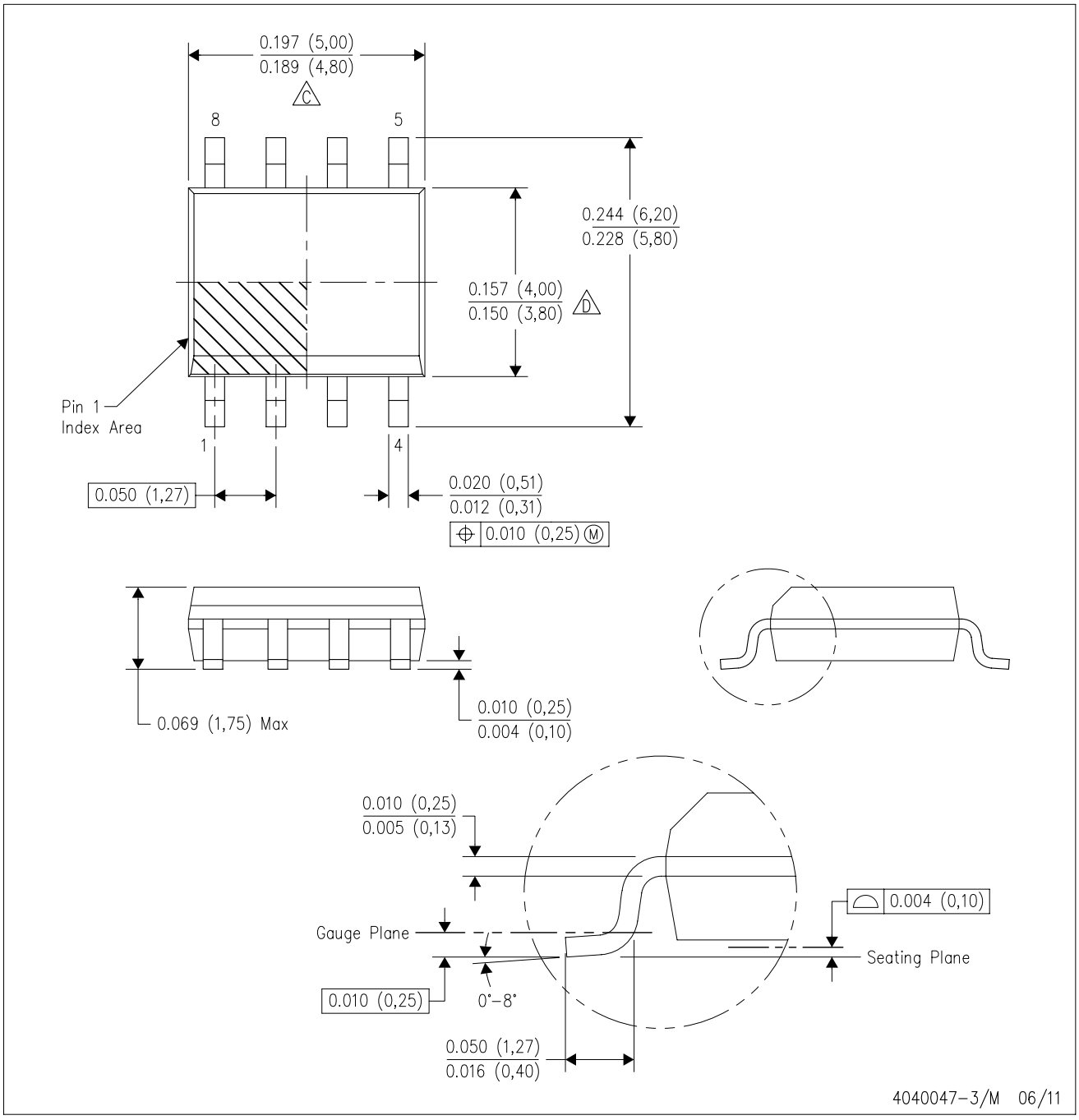
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

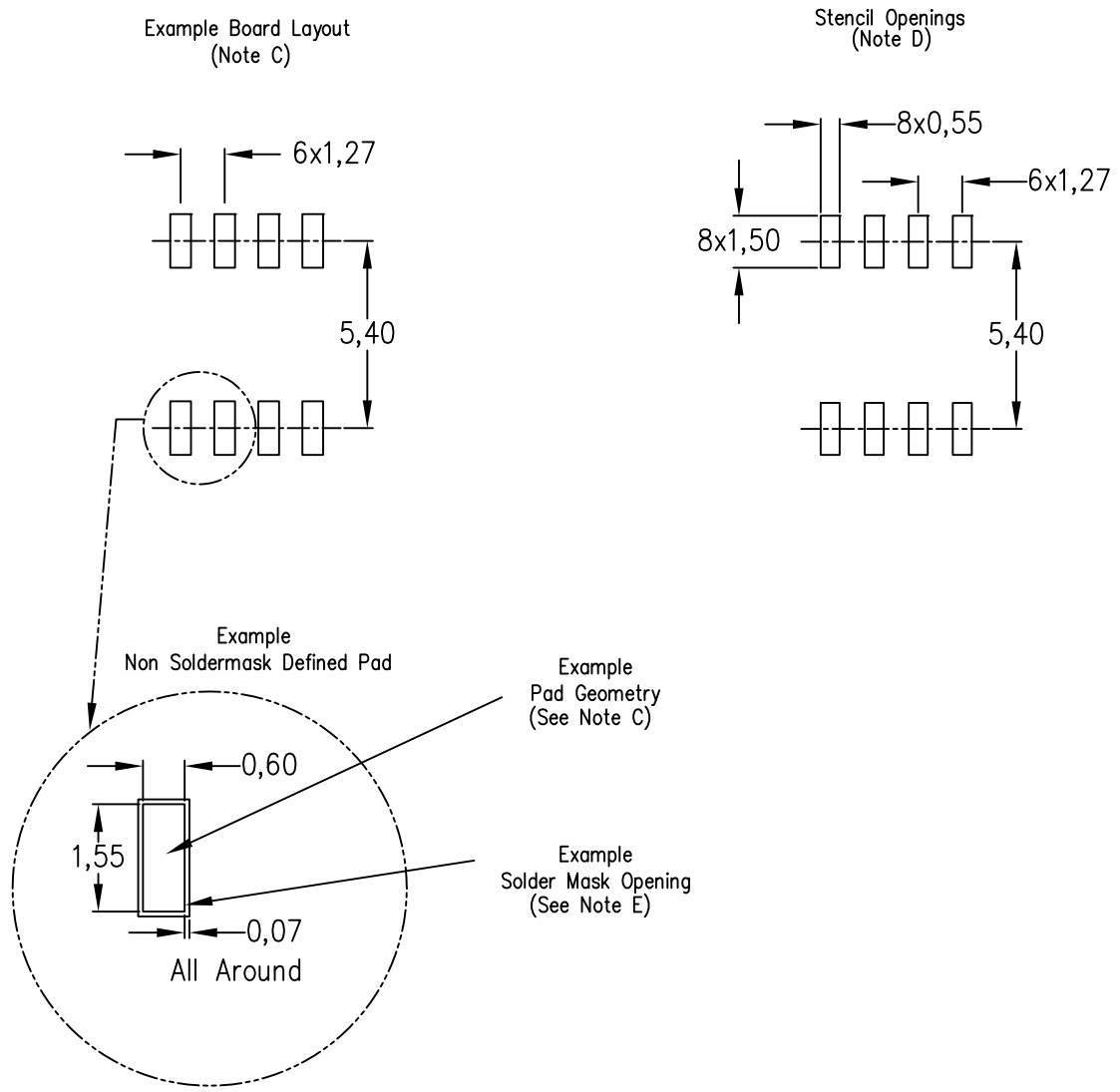
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

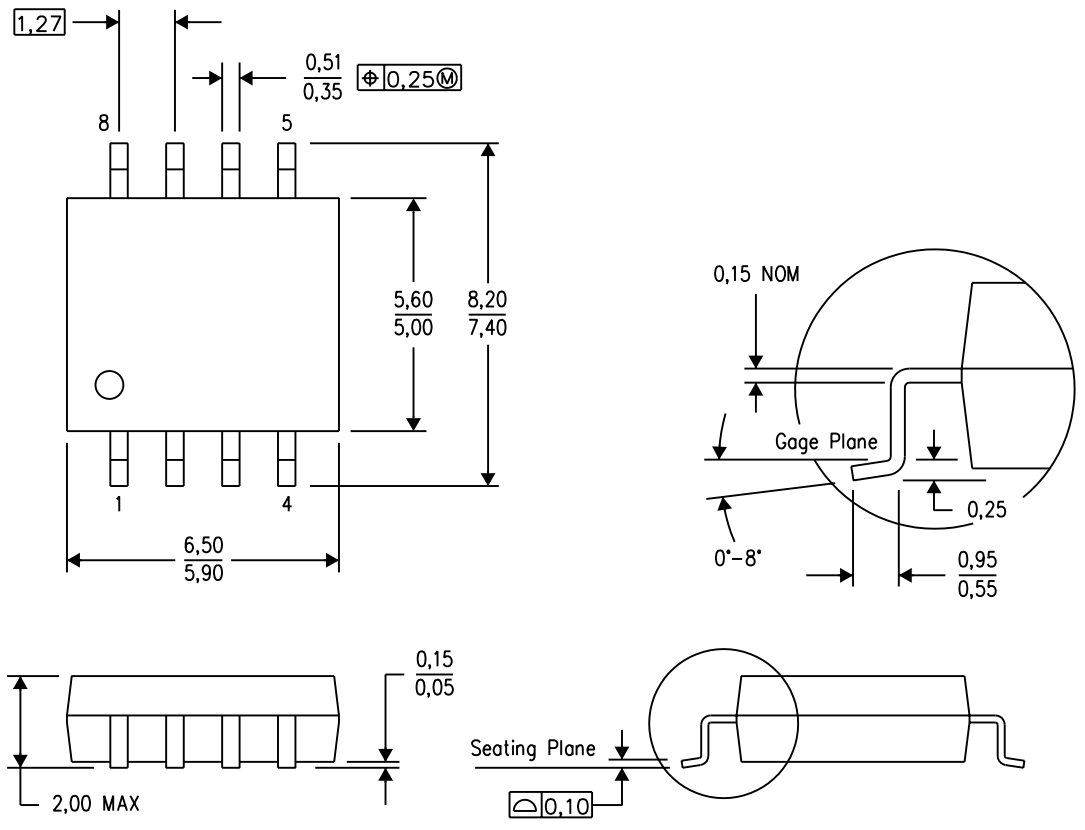
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

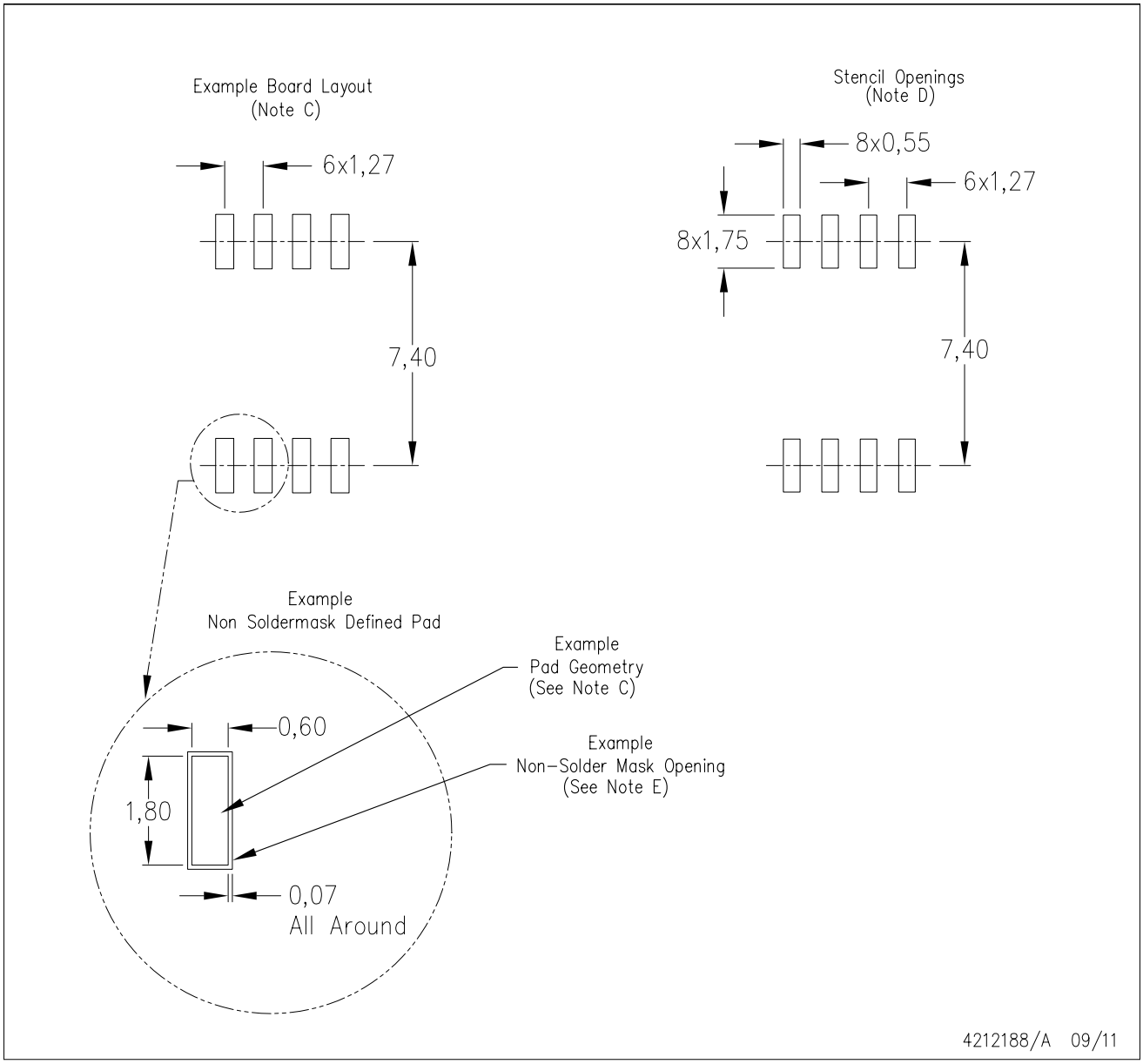
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE

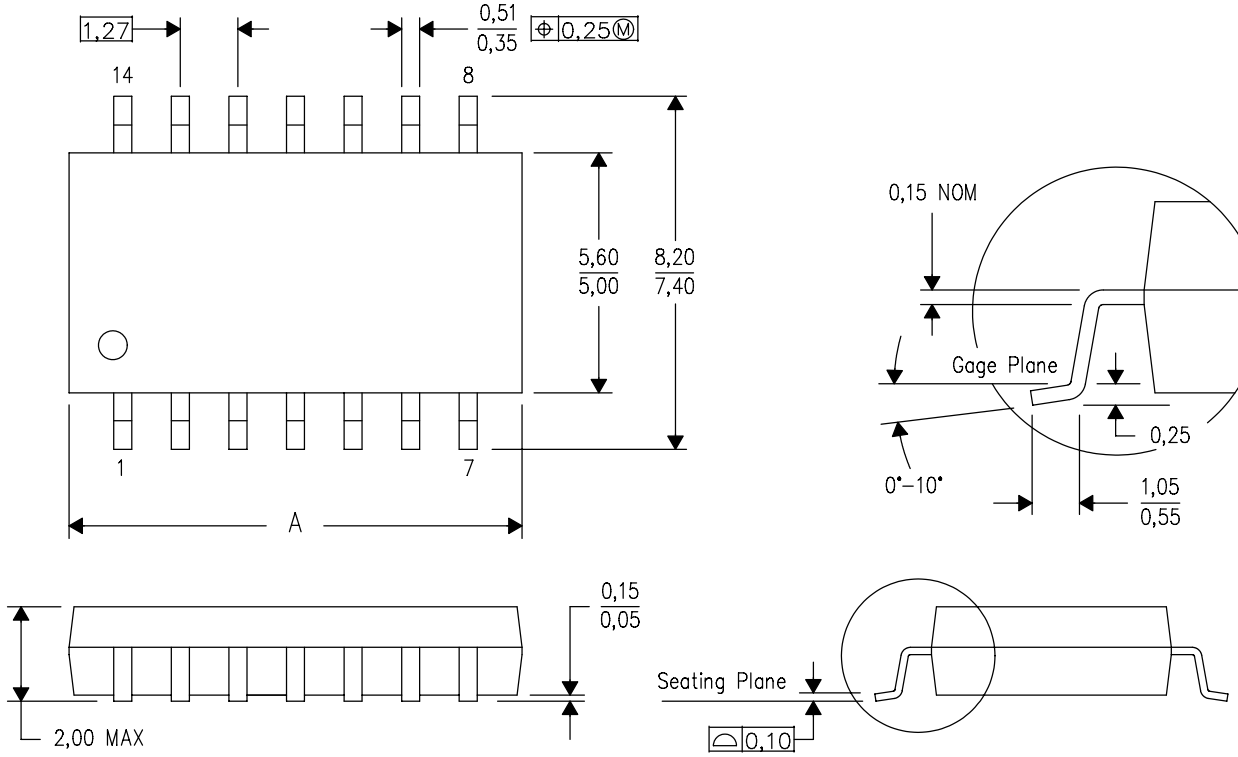


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE

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