

## TL77xxA Supply-Voltage Supervisors

### 1 Features

- Power-On Reset Generator
- Automatic Reset Generation After Voltage Drop
- Wide Supply-Voltage Range
- Precision Voltage Sensor
- Temperature-Compensated Voltage Reference
- Externally Adjustable Pulse Duration

### 2 Applications

- Computers
- Tablets
- Smart Phones
- Servers
- Music Players

### 3 Description

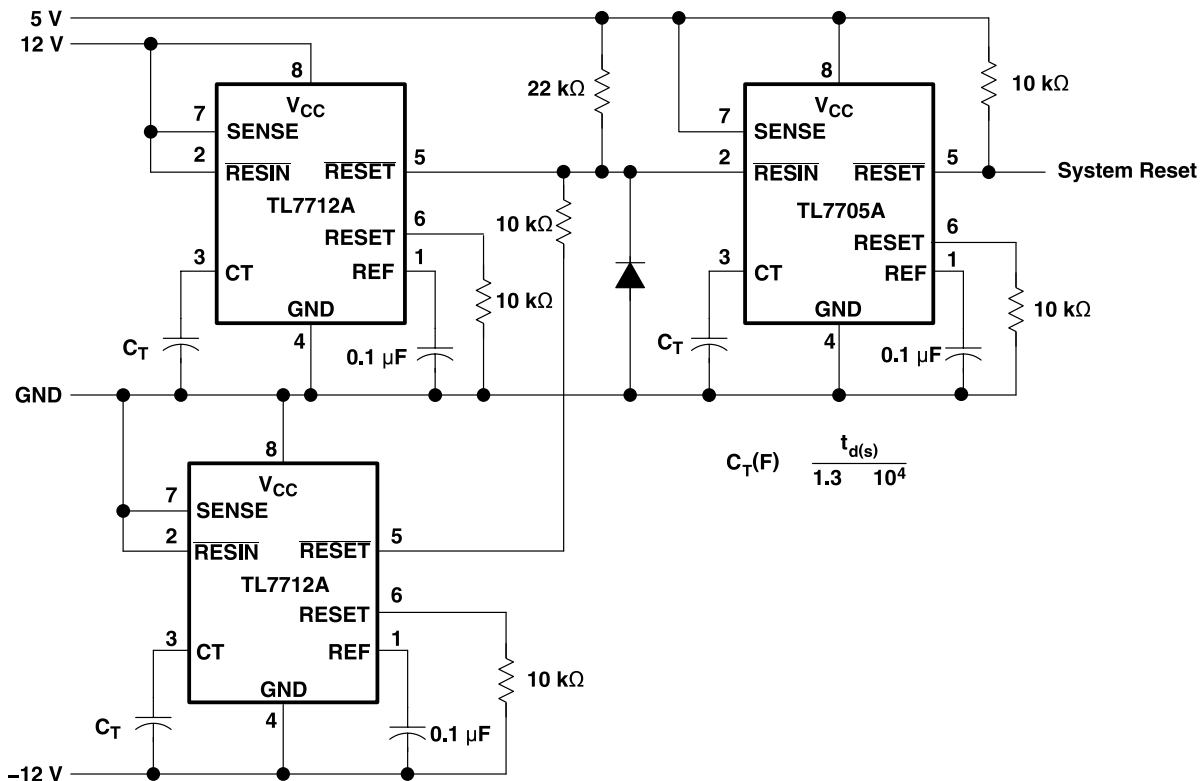
The TL77xxA family of integrated-circuit supply-voltage supervisors is designed specifically for use as reset controllers in microcomputer and microprocessor systems. The supply-voltage supervisor monitors the supply for undervoltage conditions at the SENSE input. During power up, the RESET output becomes active (low) when  $V_{CC}$  attains a value approaching 3.6 V. At this point (assuming that SENSE is above  $V_{IT+}$ ), the delay timer function activates a time delay, after which outputs  $\overline{\text{RESET}}$  and RESET go inactive (high and low, respectively). When an undervoltage condition occurs during normal operation,  $\overline{\text{RESET}}$  and RESET go active.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TL77xxA	SOIC (8)	4.90 mm x 3.91 mm
	PDIP (8)	9.81 mm x 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

### 4 Three-Supply Monitoring



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## 5 Revision History

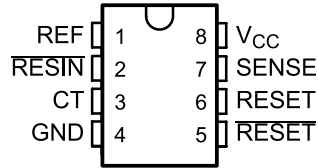
### Changes from Revision I (July 2009) to Revision J

Page

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. .... 1
- Deleted *Ordering Information* table. .... 1

## 6 Pin Configuration and Functions

TL7702A, TL7709A, TL7712A, TL7715A . . . D OR P PACKAGE  
 TL7705A . . . D, P, OR PS PACKAGE,  
 (TOP VIEW)



### Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
CT	3	I/O	External timing-capacitor pin
GND	4	—	Device ground
REF	1	O	Voltage reference output
RESET	6	O	Supervisor reset signal output
$\overline{\text{RESET}}$	5	O	Supervisor reset signal output (inverted)
$\overline{\text{RESIN}}$	2	I	Reset input
SENSE	7	I	Sense input
$V_{CC}$	8	—	Power Supply

## 7 Specifications

### 7.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply Voltage <sup>(2)</sup>		20	V	
V <sub>I</sub>	Input Voltage Range, $\overline{\text{RESIN}}$	-0.3	20	V	
V <sub>I</sub>	Input Voltage Range SENSE	TL7702A <sup>(3)</sup>	-0.3	6	V
		TL7705A	-0.3	20	V
		TL7709A	-0.3	20	V
		TL7712A, TL7715A	-0.3	20	V
I <sub>OH</sub>	High-level output current, I <sub>OH</sub> , $\overline{\text{RESET}}$		-30	mA	
I <sub>OL</sub>	Low-level output current, I <sub>OL</sub> , $\overline{\text{RESET}}$		30	mA	
T <sub>J</sub>	Operating virtual junction temperature		150	°C	
T <sub>stg</sub>	Storage temperature range	-65	150	°C	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) For proper operation of the TL7702A, the voltage applied to the SENSE terminal should not exceed V<sub>CC</sub> - 1 V or 6 V, whichever is less.
- (3) All voltage values are with respect to GND.

### 7.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply Voltage	3.5	18	V	
V <sub>IH</sub>	High-level input voltage at $\overline{\text{RESIN}}$	2		V	
V <sub>IL</sub>	Low-level input voltage at $\overline{\text{RESIN}}$		0.6	V	
V <sub>I</sub>	Input voltage, SENSE	TL7702A	0	See <sup>(1)</sup>	V
		TL7705A	0	10	
		TL7709A	0	15	
		TL7712A	0	20	
		TL7715A	0	20	
I <sub>OH</sub>	High-level output current, $\overline{\text{RESET}}$		-16	mA	
I <sub>OL</sub>	Low-level output current, $\overline{\text{RESET}}$		16	mA	
T <sub>A</sub>	Operating free-air temperature	TL77xxAC	0	70	°C
		TL77xxAI	-40	85	

- (1) For proper operation of the TL7702A, the voltage applied to the SENSE terminal should not exceed V<sub>CC</sub> - 1 V or 6 V, whichever is less.

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	TL77xxA			UNIT
	D	P	PS	
	8 PINS	8 PINS	8 PINS	
R <sub>θJA</sub> Junction-to-ambient thermal resistance	97	85	95	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

### 7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>(1)</sup>	TL77xxAC TL77xxAI			UNIT
		MIN	TYP	MAX	
V <sub>OH</sub> High-level output voltage, RESET	I <sub>OH</sub> = -16 mA	V <sub>CC</sub> - 1.5			V
V <sub>OL</sub> Low-level output voltage, RESET	I <sub>OL</sub> = 16 mA	0.4			V
V <sub>ref</sub> Reference Voltage	T <sub>A</sub> = 25°C	2.48	2.53	2.58	V
V <sub>IT-</sub> Negative-going input threshold voltage, SENSE	TL7702A	2.48	2.53	2.58	V
	TL7705A	4.5	4.55	4.6	
	TL7709A	7.5	7.6	7.7	
	TL7712A	10.6	10.8	11	
	TL7715A	13.2	13.5	13.8	
V <sub>hys</sub> Hysteresis, SENS (V <sub>IT+</sub> - V <sub>IT-</sub> )	TL7702A	10			mV
	TL7705A	15			
	TL7709A	20			
	TL7712A	35			
	TL7715A	45			
I <sub>I</sub> Input current	RESIN	20			μA
		-100			
	SENSE TL7702A	0.5			
I <sub>OH</sub> High-level output current, RESET	V <sub>O</sub> = 18 V	50			μA
I <sub>OL</sub> Low-level output current, RESET	V <sub>O</sub> = 0	-50			μA
I <sub>CC</sub> Supply current	All inputs and outputs open	1.8			3 mA

(1) All electrical characteristics are measured with 0.1-μF capacitors connected at REF, CT, and V<sub>CC</sub> to GND.

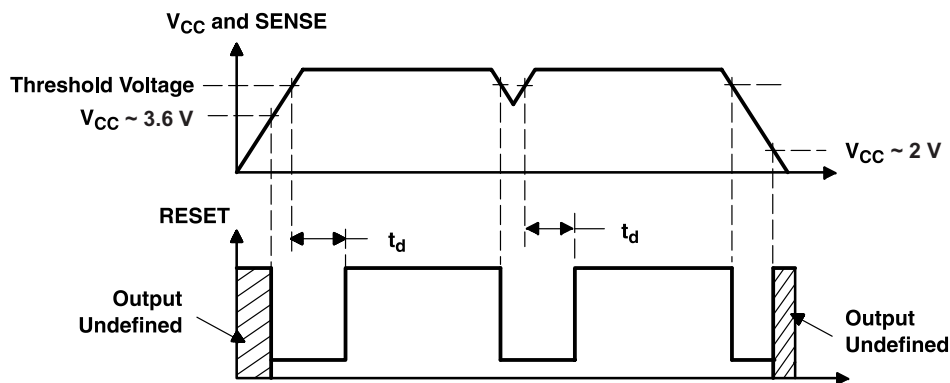


Figure 1. Timing Diagram

## 7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>(1)</sup>	TL77xxAC TL77xxAI			UNIT
		MIN	TYP	MAX	
Output pulse duration	$C_T = 0.1 \mu\text{F}$	0.65	1.2	2.6	msec
Input pulse duration at $\overline{\text{RESIN}}$		0.4			$\mu\text{s}$
$t_{w(S)}$ Pulse duration at sense input to switch outputs	$V_{IH} = V_{IT-} + 200 \text{ mV}, V_{IL} = V_{IT-} - 200 \text{ mV}$	2			$\mu\text{s}$
$t_{pd}$ propagation delay time, $\overline{\text{RESIN}}$ to $\overline{\text{RESET}}$	$V_{CC} = 5\text{V}$			1	$\mu\text{s}$
$t_r$ Rise time	RESET	$V_{CC} = 5 \text{ V}^{(2)}$			$\mu\text{s}$
	$\overline{\text{RESET}}$				
$t_f$ Fall time	RESET	$V_{CC} = 5 \text{ V}^{(2)}$			$\mu\text{s}$
	$\overline{\text{RESET}}$				

(1) All switching characteristics are measured with 0.1- $\mu\text{F}$  capacitors connected at REF and  $V_{CC}$  to GND.

(2) The rise and fall times are measured with a 4.7-k $\Omega$  load resistor at RESET and  $\overline{\text{RESET}}$ .

## 7.7 Typical Characteristics

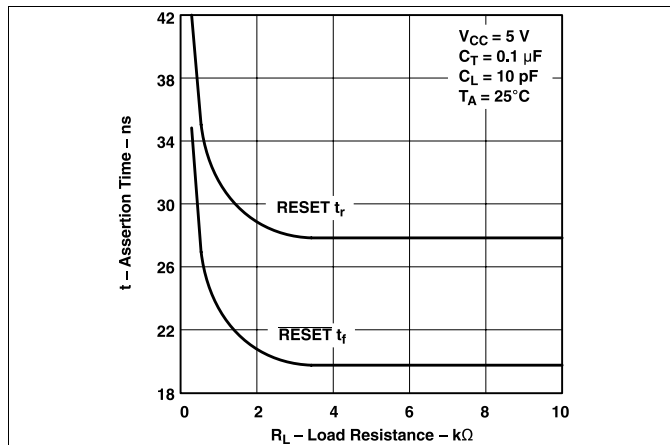


Figure 2. Assertion Time vs Load Resistance

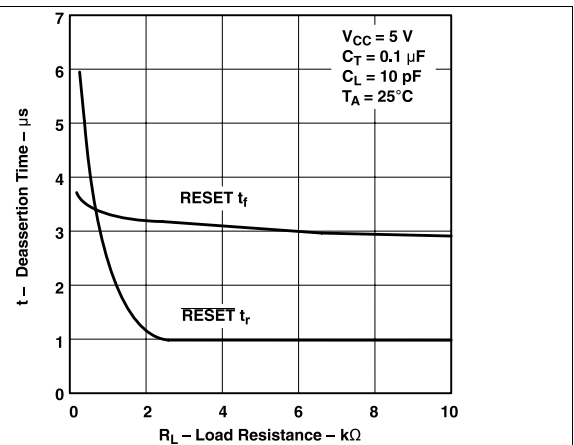


Figure 3. Deassertion Time vs Load Resistance

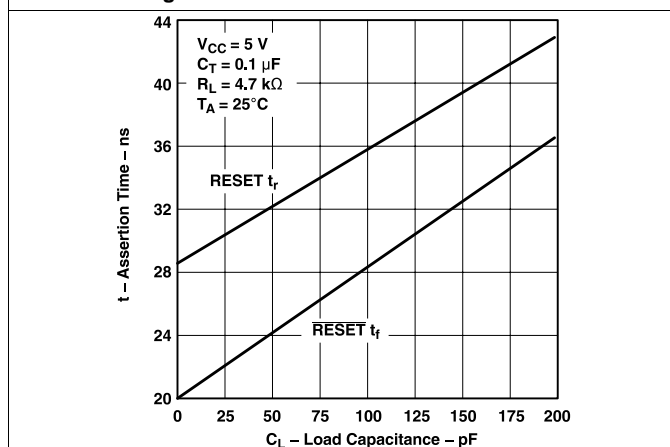


Figure 4. Assertion Time vs Load Capacitance

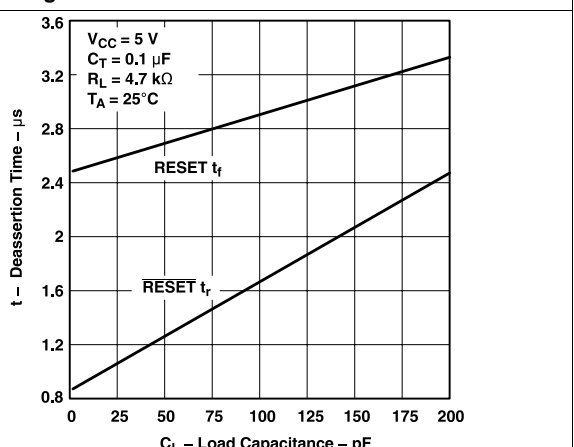


Figure 5. De-assertion Time vs Load Capacitance

## 8 Parameter Measurement Information

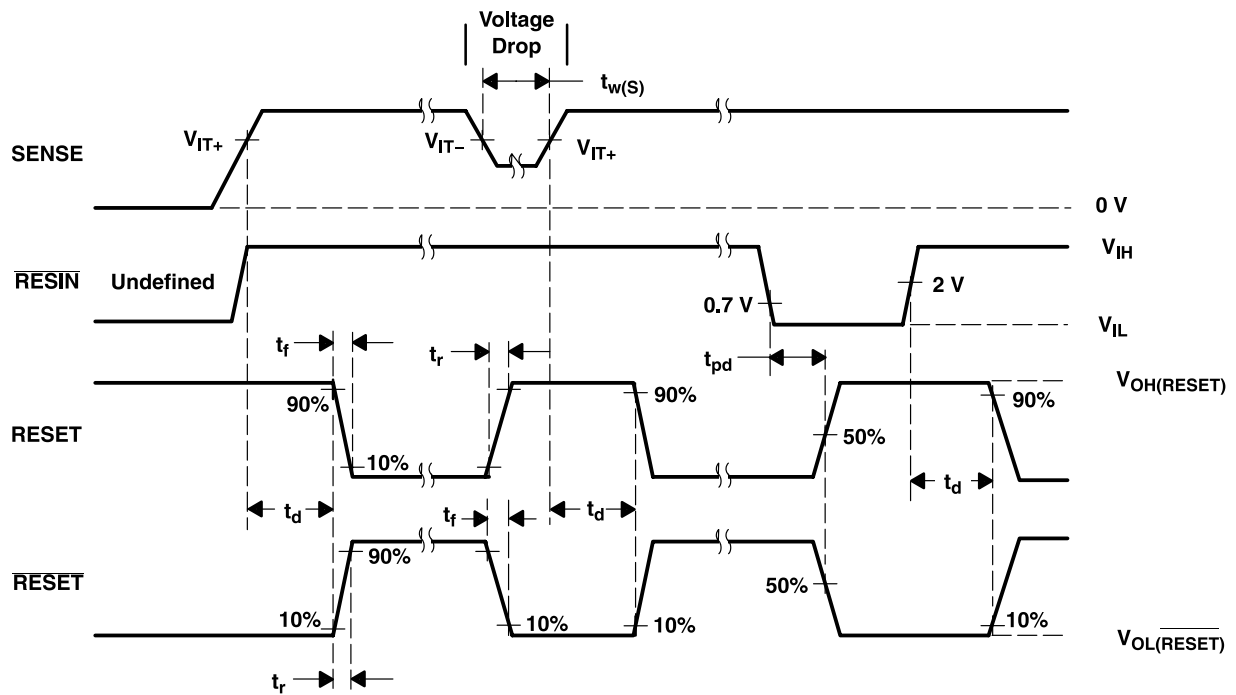


Figure 6. Voltage Waveform

## 9 Detailed Description

### 9.1 Overview

The TL77xxA family of integrated-circuit supply-voltage supervisors is designed specifically for use as reset controllers in microcomputer and microprocessor systems. The supply-voltage supervisor monitors the supply for undervoltage conditions at the SENSE input. During power up, the RESET output becomes active (low) when  $V_{CC}$  attains a value approaching 3.6 V. At this point (assuming that SENSE is above  $V_{IT+}$ ), the delay timer function activates a time delay, after which outputs  $\overline{\text{RESET}}$  and  $\text{RESET}$  go inactive (high and low, respectively). When an undervoltage condition occurs during normal operation,  $\overline{\text{RESET}}$  and  $\text{RESET}$  go active. To ensure that a complete reset occurs, the reset outputs remain active for a time delay after the voltage at the SENSE input exceeds the positive-going threshold value.

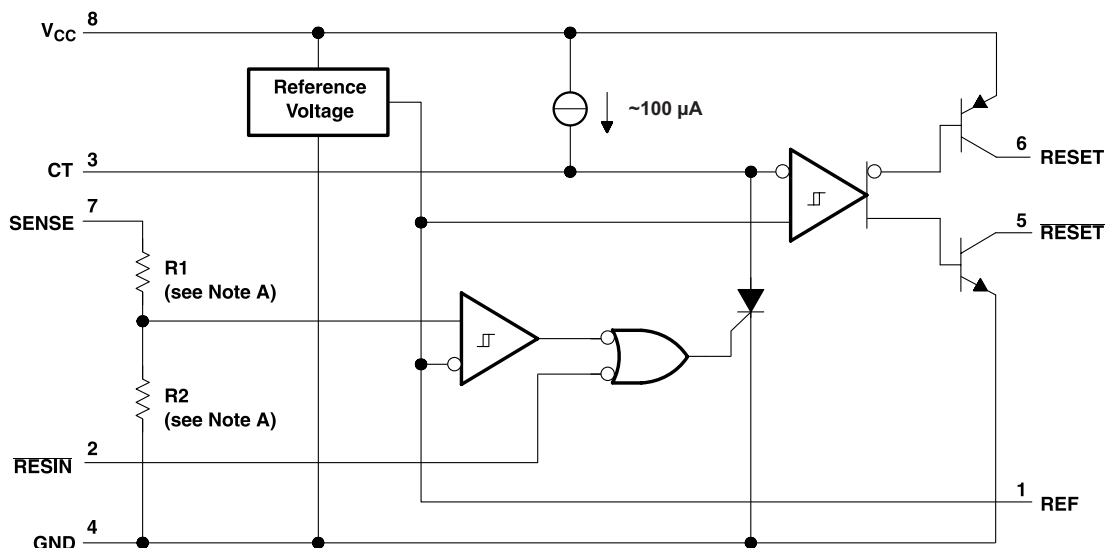
During power down and when SENSE is below  $V_{IT-}$ , the outputs remain active until  $V_{CC}$  falls below 2 V. After this, the outputs are undefined. An external capacitor (typically 0.1  $\mu\text{F}$ ) must be connected to REF to reduce the influence of fast transients in the supply voltage.

Five versions of this circuit are available:

- TL7705A ( $V_t = 4.55 \text{ V}$ ): Application in TTL-systems and microcomputer systems which require a 5 volt supply (e.g. TMS7000)
- TL7709A ( $V_t = 7.6 \text{ V}$ ): Application in microcomputer systems using the TMS1XXXNLL
- TL7712A ( $V_t = 10.8 \text{ V}$ ): Application in CMOS, microprocessor, and memory circuits with a 12 volt supply.
- TL7715A ( $V_t = 13.5 \text{ V}$ ): Application in circuits which operate with a supply voltage of 15 V, as is found often in analog circuits.
- TL7702A ( $V_t = 2.5 \text{ V}$ ): Application in systems where other supply voltages are used. The required trigger level may be adjusted with an external resistor divider at the SENSE input.

### 9.2 Functional Block Diagram

The functional block diagram is shown for illustrative purposes only; the actual circuit includes a trimming network to adjust the reference voltage and sense-comparator trip point.



- A. TL7702A:  $R_1 = 0 \Omega$ ,  $R_2 = \text{open}$   
 TL7705A:  $R_1 = 7.8 \text{ k}\Omega$ ,  $R_2 = 10 \text{ k}\Omega$   
 TL7709A:  $R_1 = 19.7 \text{ k}\Omega$ ,  $R_2 = 10 \text{ k}\Omega$   
 TL7712A:  $R_1 = 32.7 \text{ k}\Omega$ ,  $R_2 = 10 \text{ k}\Omega$   
 TL7715A:  $R_1 = 43.4 \text{ k}\Omega$ ,  $R_2 = 10 \text{ k}\Omega$
- B. Resistor values shown are nominal.

## 9.3 Feature Description

### 9.3.1 Wide Supply-Voltage Range

The TL77xxA family operates over a wide supply voltage range of 3.5 V to 18 V.

### 9.3.2 Externally Adjustable Pulse Duration

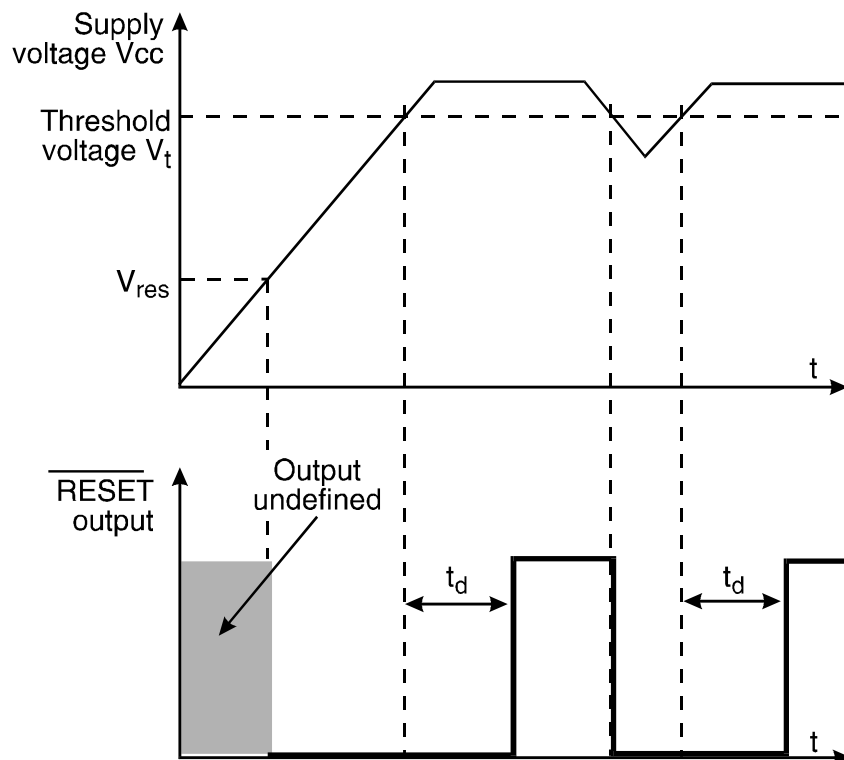
The time delay is determined by the value of the external capacitor  $C_T$ :  $t_d = 1.3 \times 10^4 \times C_T$ , where  $C_T$  is in farads (F) and  $t_d$  is in seconds (s).

### 9.3.3 Temperature-Compensated Voltage Reference

The series TL77xxA incorporates an extremely stable reference voltage source. This voltage source can also be used in applications where a constant voltage source is required. The reference voltage varies less than 10 mV over the supply voltage range of 3.5 V to 18 V. The same stability of the reference voltage is maintained, when the ambient temperature is changed. The reference's voltage varies only 16 mV when the ambient temperature is changed from -40 °C to 85 °C.

## 9.4 Device Functional Modes

Figure 7 shows the timing of the various signals. In this example the SENSE input is connected to the supply voltage  $V_{CC}$  as in typical applications of this device. The minimum supply voltage for which the function of this device is guaranteed is 3.6 V. After power-on, the outputs are undefined until the minimum supply voltage  $V_{res}$  is reached. For the TL77xxA the minimum supply voltage is  $V_{res} = 3.0$  V (typical 2.5 V). Beyond the voltage  $V_{res}$  the capacitor  $C_T$  is first kept discharged, and the outputs stay in the active state (RESET = High, RESET = Low). When the input voltage becomes higher than the threshold voltage  $V_t$ , the thyristor is turned off and the capacitor is charged. After a delay,  $t_d$ , the voltage at the capacitor passes the trigger level of the output comparator and the outputs become inactive. The circuit to be initialized is now set to a defined state and starts the correct operation.



A. Note: SENSE Input connected to  $V_{CC}$

Figure 7. Timing Diagram

## 10 Application and Implementation

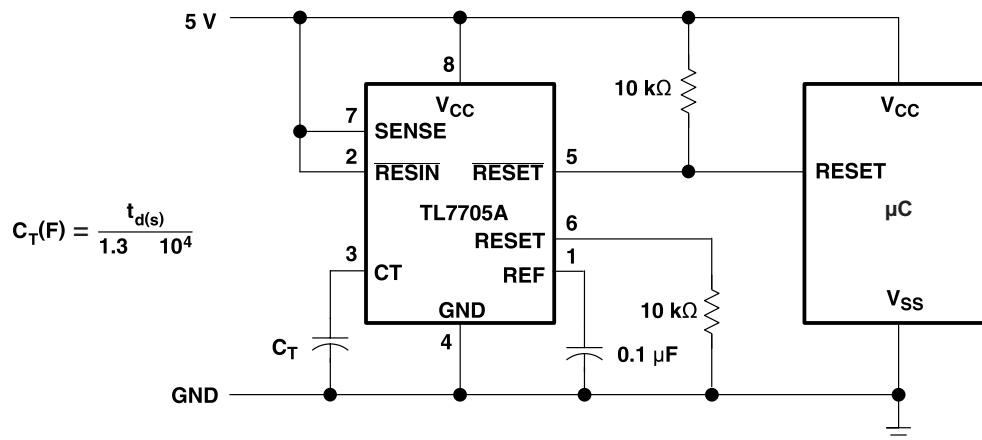
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

This application shows the initialization circuit diagrams for a microprocessor system with supply voltage  $V_{CC} = 5$  V. The external components required are the decoupling capacitor  $C_{ref}$  for the reference voltage and the timing capacitor  $C_T$ . The outputs of the TL77xxA are open collector outputs. In [Figure 8](#) therefore a pull-up resistor is shown at the RESET output to ensure the correct HIGH level.

### 10.2 Typical Application



**Figure 8. Reset Controller Schematic for a Microprocessor**

#### 10.2.1 Design Requirements

- 5-V microprocessor supply voltage
- $t_d = 1.3$  ms

#### 10.2.2 Detailed Design Procedure

- Select reasonable values for pull-up/pull-down resistors for RESET and  $\overline{\text{RESET}}$ . This design will use 10 kΩ.
- Choose  $C_T = 0.1$  μF to achieve  $t_d = 1.3$  ms
- This design will use only the active-low reset output ( $\overline{\text{RESET}}$ ) because the example microcontroller resets when the input is Low.

Typical Application (continued)

10.2.3 Application Curves

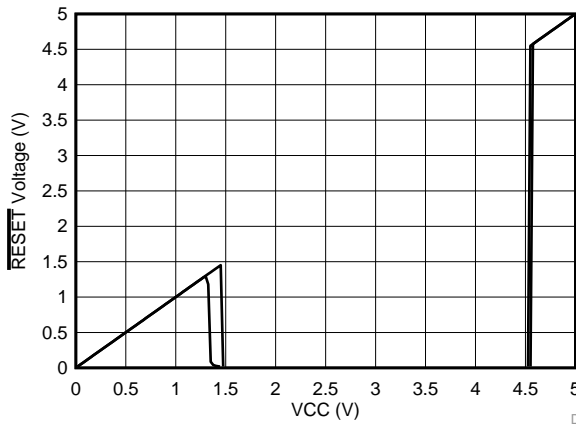


Figure 9. Supervisor  $\overline{\text{RESET}}$  Output Voltage vs  $V_{CC}$

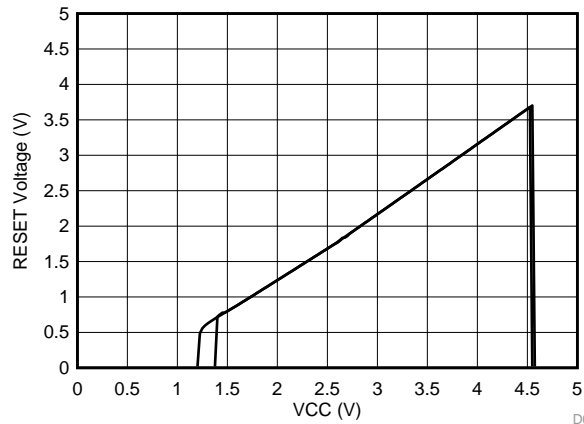


Figure 10. Supervisor RESET Output Voltage vs  $V_{CC}$

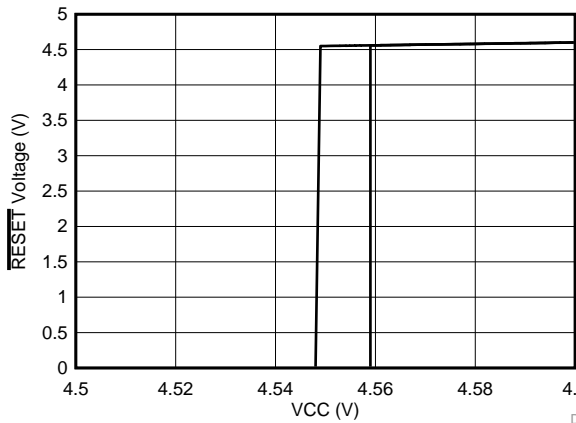


Figure 11. Supervisor  $\overline{\text{RESET}}$  Output Voltage vs  $V_{CC}$  at Transition

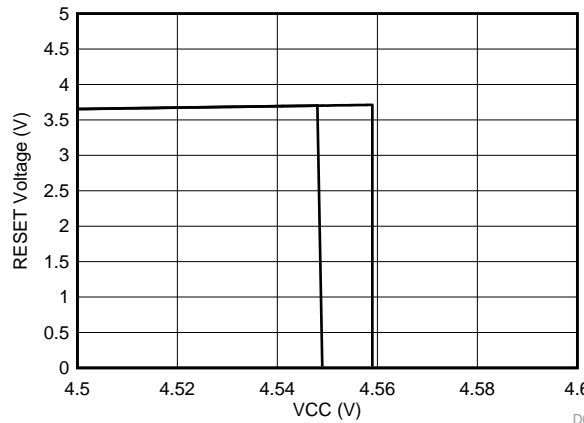


Figure 12. Supervisor RESET Output Voltage vs  $V_{CC}$  at Transition



System Examples (continued)

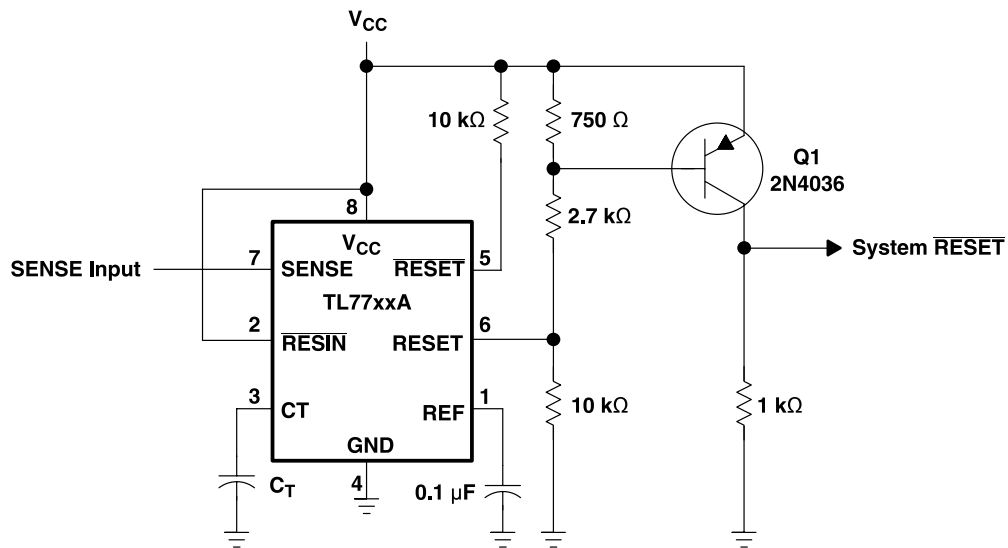


Figure 15. Eliminating Undefined States Using PNP Transistor Schematic

## 11 Power Supply Recommendations

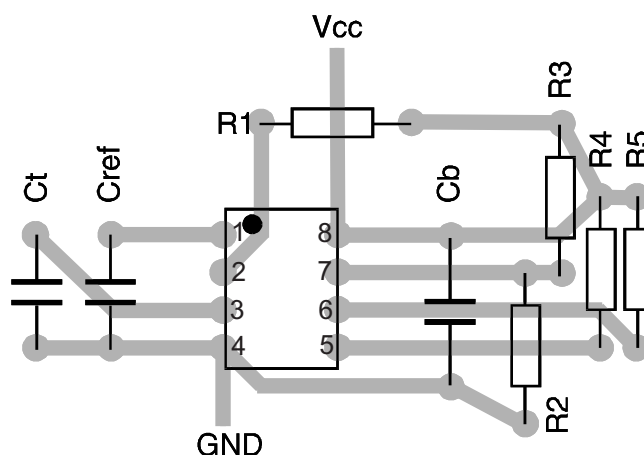
The TL77xxA devices will operate within the above specifications between 3.5 V and 18 V. These devices will risk being damaged when powered by more than 20 V.

## 12 Layout

### 12.1 Layout Guidelines

The voltage monitor should be placed on the printed circuit board, where there are no neighboring circuits in the which switch high currents (like bus interface circuits and power switches). When laying out the layout of the printed circuit board special care should taken with the interconnects which carry analog signals. Beside the SENSE input these are the  $C_T$  and  $V_{ref}$  terminals. Noise coupled into the  $C_T$  input will lead to a reduction of the output pulse width. Noise coupled into the  $V_{ref}$  input or into the filter capacitor at this input may lead to undesired triggering of the circuit and by this to an undesired RESET pulse. Practice shows, that this malfunction when high currents flow over the interconnects of these capacitors to the GND terminal of the voltage monitor. To avoid these effects, the GND terminals of these capacitors must be connected by the shortest way to the GND terminal of the voltage monitor in so that no currents caused by other circuits flow over these wires. [Figure 16](#) show a layout proposal for the printed circuit board. Furthermore the resistors of the voltage divider at the SENSE input of the TL7702 (R2 and R3 in [Figure 16](#)) have to be placed in so, that no noise may be coupled into this circuit.

### 12.2 Layout Example



**Figure 16. Printed Circuit Layout for the Supply Voltage Supervisor**

## 13 Device and Documentation Support

### 13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 1. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TL7702A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TL7705A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TL7709A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TL7712A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TL7715A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 13.2 Trademarks

All trademarks are the property of their respective owners.

### 13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL7702ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7702AC	<a href="#">Samples</a>
TL7702ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7702AC	<a href="#">Samples</a>
TL7702ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7702AC	<a href="#">Samples</a>
TL7702ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7702AC	<a href="#">Samples</a>
TL7702ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7702AC	<a href="#">Samples</a>
TL7702ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL7702ACP	<a href="#">Samples</a>
TL7702AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7702AI	<a href="#">Samples</a>
TL7702AIDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7702AI	<a href="#">Samples</a>
TL7702AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7702AI	<a href="#">Samples</a>
TL7702AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7702AI	<a href="#">Samples</a>
TL7702AIDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7702AI	<a href="#">Samples</a>
TL7702AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7702AI	<a href="#">Samples</a>
TL7702AIP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL7702AIP	<a href="#">Samples</a>
TL7702AIPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL7702AIP	<a href="#">Samples</a>
TL7702AMFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
TL7702AMJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	-55 to 125		
TL7702AMJGB	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	-55 to 125		
TL7705ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7705AC	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL7705ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7705AC	<a href="#">Samples</a>
TL7705ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7705AC	<a href="#">Samples</a>
TL7705ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7705AC	<a href="#">Samples</a>
TL7705ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7705AC	<a href="#">Samples</a>
TL7705ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7705AC	<a href="#">Samples</a>
TL7705ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL7705ACP	<a href="#">Samples</a>
TL7705ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL7705ACP	<a href="#">Samples</a>
TL7705ACPSLE	OBSOLETE	SO	PS	8		TBD	Call TI	Call TI	0 to 70		
TL7705ACPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T7705A	<a href="#">Samples</a>
TL7705AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7705AI	<a href="#">Samples</a>
TL7705AIDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7705AI	<a href="#">Samples</a>
TL7705AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7705AI	<a href="#">Samples</a>
TL7705AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7705AI	<a href="#">Samples</a>
TL7705AIDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7705AI	<a href="#">Samples</a>
TL7705AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7705AI	<a href="#">Samples</a>
TL7705AIP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL7705AIP	<a href="#">Samples</a>
TL7705AIPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TL7705AIP	<a href="#">Samples</a>
TL7709ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7709AC	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL7709ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7709AC	<a href="#">Samples</a>
TL7709ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7709AC	<a href="#">Samples</a>
TL7709ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL7709ACP	<a href="#">Samples</a>
TL7709ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL7709ACP	<a href="#">Samples</a>
TL7709AID	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85		
TL7709AIP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	-40 to 85		
TL7712ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7712AC	<a href="#">Samples</a>
TL7712ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7712AC	<a href="#">Samples</a>
TL7712ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7712AC	<a href="#">Samples</a>
TL7712ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7712AC	<a href="#">Samples</a>
TL7712ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7712AC	<a href="#">Samples</a>
TL7712ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7712AC	<a href="#">Samples</a>
TL7712ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL7712ACP	<a href="#">Samples</a>
TL7712ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL7712ACP	<a href="#">Samples</a>
TL7712AID	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85		
TL7712AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		7712AI	<a href="#">Samples</a>
TL7712AIP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	-40 to 85		
TL7715ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7715AC	<a href="#">Samples</a>
TL7715ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7715AC	<a href="#">Samples</a>
TL7715ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7715AC	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL7715ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL7715ACP	<a href="#">Samples</a>
TL7715ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TL7715ACP	<a href="#">Samples</a>
TL7715AID	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85		
TL7715AIP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL7702ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7702ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7702AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7705ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7705ACPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL7705AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7709ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7712ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7712AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL7702ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL7702ACDR	SOIC	D	8	2500	367.0	367.0	35.0
TL7702AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TL7705ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL7705ACPSR	SO	PS	8	2000	367.0	367.0	38.0
TL7705AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TL7709ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL7712ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL7712AIDR	SOIC	D	8	2500	340.5	338.1	20.6

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