

TL071, TL071A, TL071B, TL072  
TL072A, TL072B, TL074, TL074A, TL074B  
**LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS**

SLOS080J – SEPTEMBER 1978 – REVISED MARCH 2005

- Low Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- Low Total Harmonic Distortion . . . 0.003% Typ
- Low Noise  
 $V_n = 18 \text{ nV}/\sqrt{\text{Hz}}$  Typ at  $f = 1 \text{ kHz}$
- High Input Impedance . . . JFET Input Stage
- Internal Frequency Compensation
- Latch-Up-Free Operation
- High Slew Rate . . . 13 V/ $\mu\text{s}$  Typ
- Common-Mode Input Voltage Range Includes  $V_{CC+}$

### description/ordering information

The JFET-input operational amplifiers in the TL07x series are similar to the TL08x series, with low input bias and offset currents and fast slew rate. The low harmonic distortion and low noise make the TL07x series ideally suited for high-fidelity and audio preamplifier applications. Each amplifier features JFET inputs (for high input impedance) coupled with bipolar output stages integrated on a single monolithic chip.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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**description/ordering information (continued)**

**ORDERING INFORMATION**

TA	V <sub>IO</sub> max AT 25°C	PACKAGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING		
0°C to 70°C	10 mV	PDIP (P)	Tube of 50	TL071CP	TL071CP	
			Tube of 50	TL072CP	TL072CP	
		PDIP (N)	Tube of 25	TL074CN	TL074CN	
		SOIC (D)	Tube of 75	TL071CD	TL071C	
			Reel of 2500	TL071CDR		
			Tube of 75	TL072CD	TL072C	
			Reel of 2500	TL072CDR		
			Tube of 50	TL074CD	TL074C	
			Reel of 2500	TL074CDR		
		SOP (NS)	Reel of 2000	TL074CNSR	TL074	
		SOP (PS)	Reel of 2000	TL071CPSR	TL071	
			Reel of 2000	TL072CPSR	T072	
		TSSOP (PW)	Reel of 2000	TL072CPWR	T072	
			Tube of 90	TL074CPW	T074	
			Reel of 2000	TL074CPWR		
		6 mV	PDIP (P)	Tube of 50	TL071ACP	TL071ACP
				Tube of 50	TL072ACP	TL072ACP
			PDIP (N)	Tube of 25	TL074ACN	TL074ACN
	SOIC (D)		Tube of 75	TL071ACD	071AC	
			Reel of 2500	TL071ACDR		
			Tube of 75	TL072ACD	072AC	
			Reel of 2500	TL072ACDR		
			Tube of 50	TL074ACD	TL074AC	
			Reel of 2500	TL074ACDR		
	SOP (PS)		Reel of 2000	TL072ACPSR	T072A	
	SOP (NS)		Reel of 2000	TL074ACNSR	TL074A	
	3 mV		PDIP (P)	Tube of 50	TL071BCP	TL071BCP
		Tube of 50		TL072BCP	TL072BCP	
		PDIP (N)	Tube of 25	TL074BCN	TL074BCN	
		SOIC (D)	Tube of 75	TL071BCD	071BC	
			Reel of 2500	TL071BCDR		
			Tube of 75	TL072BCD	072BC	
			Reel of 2500	TL072BCDR		
Tube of 50			TL074BCD	TL074BC		
Reel of 2500			TL074BCDR			
SOP (NS)		Reel of 2000	TL074BCNSR	TL074B		

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**description/ordering information (continued)**

**ORDERING INFORMATION**

T <sub>A</sub>	V <sub>IOMax</sub> AT 25°C	PACKAGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
-40°C to 85°C	6 mV	PDIP (P)	Tube of 50	TL071IP	TL071IP
			Tube of 50	TL072IP	TL072IP
		PDIP (N)	Tube of 25	TL074IN	TL074IN
		SOIC (D)	Tube of 75	TL071ID	TL071I
			Reel of 2500	TL071IDR	
			Tube of 75	TL072ID	TL072I
			Reel of 2500	TL072IDR	
			Tube of 50	TL074ID	TL074I
			Reel of 2500	TL074IDR	
		-55°C to 125°C	6 mV	CDIP (JG)	Tube of 50
CFP (U)	Tube of 150			TL072MUB	TL072MUB
LCCC (FK)	Tube of 55			TL072MFKB	TL072MFKB
9 mV	CDIP (J)		Tube of 25	TL074MJB	TL074MJB
	CFP (W)		Tube of 25	TL074MWB	TL074MWB
	LCCC (FK)		Tube of 55	TL074MFKB	TL074MFKB

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage (see Note 1): $V_{CC+}$ .....	18 V
$V_{CC-}$ .....	-18 V
Differential input voltage, $V_{ID}$ (see Note 2) .....	$\pm 30$ V
Input voltage, $V_I$ (see Notes 1 and 3) .....	$\pm 15$ V
Duration of output short circuit (see Note 4) .....	Unlimited
Package thermal impedance, $\theta_{JA}$ (see Notes 5 and 6): D package (8 pin) .....	97°C/W
D package (14 pin) .....	86°C/W
N package .....	80°C/W
NS package .....	76°C/W
P package .....	85°C/W
PS package .....	95°C/W
PW package (8 pin) .....	149°C/W
PW package (14 pin) .....	113°C/W
U package .....	185°C/W
Package thermal impedance, $\theta_{JC}$ (see Notes 7 and 8): FK package .....	5.61°C/W
J package .....	15.05°C/W
JG package .....	14.5°C/W
W package .....	14.65°C/W
Operating virtual junction temperature, $T_J$ .....	150°C
Case temperature for 60 seconds: FK package .....	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: J, JG, or W package .....	300°C
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between  $V_{CC+}$  and  $V_{CC-}$ .
  2. Differential voltages are at  $IN+$ , with respect to  $IN-$ .
  3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
  4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
  5. Maximum power dissipation is a function of  $T_J(max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(max) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
  6. The package thermal impedance is calculated in accordance with JESD 51-7.
  7. Maximum power dissipation is a function of  $T_J(max)$ ,  $\theta_{JC}$ , and  $T_C$ . The maximum allowable power dissipation at any allowable case temperature is  $P_D = (T_J(max) - T_C)/\theta_{JC}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
  8. The package thermal impedance is calculated in accordance with MIL-STD-883.



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**electrical characteristics,  $V_{CC\pm} = \pm 15\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS†	T <sub>A</sub> ‡	TL071C TL072C TL074C			TL071AC TL072AC TL074AC			TL071BC TL072BC TL074BC			TL071I TL072I TL074I			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub>	V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω	25°C Full range	3	10	13	3	3	6	2	2	3	3	3	6	mV
αV <sub>IO</sub>	V <sub>O</sub> = 0, R <sub>S</sub> = 50 Ω	Full range	18			18			18			18			μV/°C
I <sub>IO</sub>	V <sub>O</sub> = 0	25°C Full range	5	100	10	5	100	2	5	100	2	5	100	pA	
I <sub>IB</sub>	V <sub>O</sub> = 0	25°C Full range	65	200	7	65	200	7	65	200	7	65	200	pA	
V <sub>ICR</sub>	Common-mode input voltage range	25°C	±11	-12 to 15		±11	-12 to 15		±11	-12 to 15		±11	-12 to 15	V	
V <sub>OM</sub>	Maximum peak output voltage	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5	V	
	output voltage swing	Full range	±12			±12			±12			±12			
			±10			±10			±10			±10			
A <sub>VD</sub>	Large-signal differential voltage amplification	25°C Full range	25	200	15	50	200	25	50	200	25	50	200	V/mV	
B <sub>1</sub>	Unity-gain bandwidth	25°C	3			3			3			3		MHz	
r <sub>i</sub>	Input resistance	25°C	10 <sup>12</sup>			10 <sup>12</sup>			10 <sup>12</sup>			10 <sup>12</sup>		Ω	
CMRR	Common-mode rejection ratio	25°C	70	100		75	100		75	100		75	100	dB	
kSVR	Supply-voltage rejection ratio (ΔV <sub>CC±</sub> /ΔV <sub>IO</sub> )	25°C	70	100		80	100		80	100		80	100	dB	
I <sub>CC</sub>	Supply current (each amplifier)	25°C	1.4	2.5		1.4	2.5		1.4	2.5		1.4	2.5	mA	
V <sub>O1</sub> /V <sub>O2</sub>	Crosstalk attenuation	25°C	120			120			120			120		dB	

† All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified.

‡ Full range is T<sub>A</sub> = 0°C to 70°C for TL07\_C, TL07\_AC, TL07\_BC and is T<sub>A</sub> = -40°C to 85°C for TL07\_I.

§ Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 4. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.



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**electrical characteristics,  $V_{CC\pm} = \pm 15\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS†	$T_A$ ‡	TL071M TL072M			TL074M			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_O = 0, R_S = 50\ \Omega$	25°C		3	6		3	9	mV
		Full range			9			15	
$\alpha V_{IO}$ Temperature coefficient of input offset voltage	$V_O = 0, R_S = 50\ \Omega$	Full range		18			18		$\mu\text{V}/^\circ\text{C}$
$I_{IO}$ Input offset current	$V_O = 0$	25°C		5	100		5	100	pA
		Full range			20			20	nA
$I_{IB}$ Input bias current‡	$V_O = 0$	25°C		65	200		65	200	pA
		Full range			50			50	nA
$V_{ICR}$ Common-mode input voltage range		25°C	$\pm 11$	-12 to 15		$\pm 11$	-12 to 15		V
$V_{OM}$ Maximum peak output voltage swing	$R_L = 10\ \text{k}\Omega$	25°C	$\pm 12$	$\pm 13.5$		$\pm 12$	$\pm 13.5$		V
	$R_L \geq 10\ \text{k}\Omega$	Full range	$\pm 12$			$\pm 12$			
	$R_L \geq 2\ \text{k}\Omega$		$\pm 10$			$\pm 10$			
$A_{VD}$ Large-signal differential voltage amplification	$V_O = \pm 10\ \text{V}, R_L \geq 2\ \text{k}\Omega$	25°C	35	200		35	200		V/mV
		Full range	15			15			
$B_1$ Unity-gain bandwidth	$T_A = 25^\circ\text{C}$			3			3		MHz
$r_i$ Input resistance	$T_A = 25^\circ\text{C}$			$10^{12}$			$10^{12}$		$\Omega$
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, V_O = 0, R_S = 50\ \Omega$	25°C	80	86		80	86		dB
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC} = \pm 9\ \text{V to } \pm 15\ \text{V}, V_O = 0, R_S = 50\ \Omega$	25°C	80	86		80	86		dB
$I_{CC}$ Supply current (each amplifier)	$V_O = 0, \text{ No load}$	25°C		1.4	2.5		1.4	2.5	mA
$V_{O1}/V_{O2}$ Crosstalk attenuation	$A_{VD} = 100$	25°C		120			120		dB

† Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 4. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

‡ All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified. Full range is  $T_A = -55^\circ\text{C to } 125^\circ\text{C}$ .

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operating characteristics,  $V_{CC\pm} = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TL07xM			ALL OTHERS			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain $V_I = 10\text{ V}$ , $C_L = 100\text{ pF}$ , $R_L = 2\text{ k}\Omega$ , See Figure 1	5	13		8	13		$\text{V}/\mu\text{s}$
$t_r$	Rise-time overshoot factor $V_I = 20\text{ mV}$ , $C_L = 100\text{ pF}$ , $R_L = 2\text{ k}\Omega$ , See Figure 1	0.1			0.1			$\mu\text{s}$
		20%			20%			
$V_n$	Equivalent input noise voltage $R_S = 20\ \Omega$	$f = 1\text{ kHz}$			18			$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{ Hz to } 10\text{ kHz}$			4			$\mu\text{V}$
$I_n$	Equivalent input noise current $R_S = 20\ \Omega$ , $f = 1\text{ kHz}$	0.01			0.01			$\text{pA}/\sqrt{\text{Hz}}$
THD	Total harmonic distortion $V_{\text{rms}} = 6\text{ V}$ , $R_L \geq 2\text{ k}\Omega$ , $f = 1\text{ kHz}$ , $A_{VD} = 1$ , $R_S \leq 1\text{ k}\Omega$	0.003%			0.003%			

**PARAMETER MEASUREMENT INFORMATION**

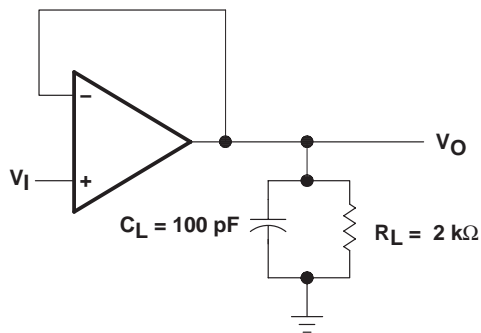


Figure 1. Unity-Gain Amplifier

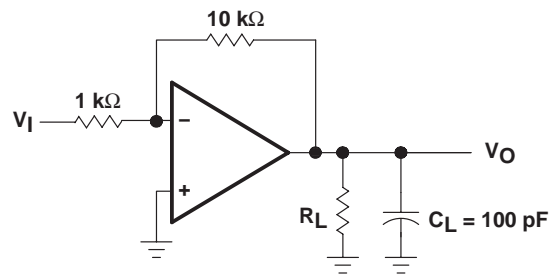


Figure 2. Gain-of-10 Inverting Amplifier

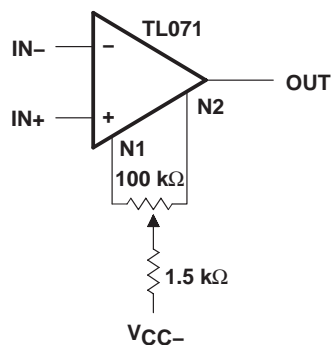


Figure 3. Input Offset-Voltage Null Circuit

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**TYPICAL CHARACTERISTICS**

**Table of Graphs**

		<b>FIGURE</b>	
$I_{IB}$	Input bias current	vs Free-air temperature	4
$V_{OM}$	Maximum output voltage	vs Frequency	5, 6, 7
		vs Free-air temperature	8
		vs Load resistance	9
		vs Supply voltage	10
$A_{VD}$	Large-signal differential voltage amplification	vs Free-air temperature	11
		vs Frequency	12
	Phase shift	vs Frequency	12
	Normalized unity-gain bandwidth	vs Free-air temperature	13
	Normalized phase shift	vs Free-air temperature	13
$CMRR$	Common-mode rejection ratio	vs Free-air temperature	14
$I_{CC}$	Supply current	vs Supply voltage	15
		vs Free-air temperature	16
$P_D$	Total power dissipation	vs Free-air temperature	17
		Normalized slew rate	vs Free-air temperature
$V_n$	Equivalent input noise voltage	vs Frequency	19
THD	Total harmonic distortion	vs Frequency	20
		Large-signal pulse response	vs Time
$V_O$	Output voltage	vs Elapsed time	22



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
8102304HA	OBSOLETE			10		TBD	Call TI	Call TI
81023052A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
8102305HA	ACTIVE	CFP	U	10	1	TBD	A42 SNPB	Level-NC-NC-NC
8102305PA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
81023062A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
8102306CA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	Level-NC-NC-NC
8102306DA	ACTIVE	CFP	W	14	1	TBD	A42 SNPB	Level-NC-NC-NC
JM38510/11905BPA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
JM38510/11906BCA	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
TL071ACD	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL071ACDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL071ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL071BCD	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL071BCDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL071BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL071CD	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL071CDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL071CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL071CPSR	ACTIVE	SO	PS	8	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL071CPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI
TL071ID	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL071IDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL071IJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
TL071IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL071MFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
TL071MJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
TL071MJGB	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
TL072ACD	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL072ACDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL072ACJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
TL072ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TL072ACPSR	ACTIVE	SO	PS	8	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL072BCD	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL072BCDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL072BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL072CD	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL072CDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL072CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL072CPSLE	OBSOLETE	SO	PS	8		TBD	Call TI	Call TI
TL072CPSR	ACTIVE	SO	PS	8	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL072CPWR	ACTIVE	TSSOP	PW	8	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
TL072CPWRE4	ACTIVE	TSSOP	PW	8	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
TL072ID	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL072IDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL072IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL072MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
TL072MJG	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
TL072MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
TL072MUB	ACTIVE	CFP	U	10	1	TBD	A42 SNPB	Level-NC-NC-NC
TL074ACD	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL074ACDR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL074ACJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
TL074ACN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL074ACNSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	Call TI	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL074ACNSRE4	ACTIVE	SO	NS	14	2000	TBD	Call TI	Call TI
TL074BCD	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL074BCDR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL074BCN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL074BCNSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	Call TI	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL074BCNSRE4	ACTIVE	SO	NS	14	2000	TBD	Call TI	Call TI

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TL074CD	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL074CDR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL074CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL074CNSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL074CNSRE4	ACTIVE	SO	NS	14	2000	TBD	Call TI	Call TI
TL074CPW	ACTIVE	TSSOP	PW	14	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
TL074CPWE4	ACTIVE	TSSOP	PW	14	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
TL074CPWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI
TL074CPWR	ACTIVE	TSSOP	PW	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
TL074CPWRE4	ACTIVE	TSSOP	PW	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
TL074ID	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL074IDR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL074IJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
TL074IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL074MFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
TL074MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
TL074MJ	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	Level-NC-NC-NC
TL074MJB	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	Level-NC-NC-NC
TL074MWB	ACTIVE	CFP	W	14	1	TBD	A42 SNPB	Level-NC-NC-NC

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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