Errata to TFP410, Datasheet Literature Number SLDS145A

This document describes errata to the TFP410 and its datasheet.

Revision history:

Version	Date	Description
1.0	Initial	DE generator
1.1	1/22/03	Items 2-4
1.2	5/20/03	V_{IH}, V_{IL} clarification, CTL3 encoding, pad size update, revision history

1. DE Generator:
The DE generator function has a limitation which limits its use in high pixel count formats. The DE_DLY and DE_CNT values are limited by DE_DLY + DE_CNT $\leq$ 2047.

For resolutions where the timing allows, it may be possible to work around this limitation by using the inactive edge of HSYNC as the starting point for DE_DLY. Appropriate timing allowances may be needed for the vertical count starting location.

Changes in the document text:

In the "register descriptions" section, under the pictorial for DE_DLY (Page 20), add after the existing sentence: The value must be less than or equal to (2047 - DE_CNT).

In the "register descriptions" section, under the pictorial for DE_CNT (Page 21), add after the existing sentence: The value must be less than or equal to (2047 - DE_DLY).

2. MSEN output:
The MSEN output description is incorrect in the "Terminal Functions" table. MSEN behavior of the 410 with manual configuration is to output the receiver connected status as a high, receiver not connected as a low.

Changes in the document text:

In the "Terminal Functions" table, page 4, for the MSEN/PO1 pin, middle paragraph of the "Description" column, change the second paragraph
FROM:

> When I2C is disabled (ISEL = low), a low level indicates a powered on receiver is detected at the differential outputs. A high level indicates a powered on receiver is not detected. This function is only valid in dc-coupled systems.

TO:

> When I2C is disabled (ISEL = low), a high level indicates a powered on receiver is detected at the differential outputs. A low level indicates a powered on receiver is not detected. This function is only valid in dc-coupled systems.

3. Error in register capability:
Sheet 17, in the register map for sub-address 0B, change the RW column value FROM: RW TO: R

4. Error in default value:
Sheet 18, Reg sub-address 08 Change register default FROM: FE TO: BE

5. CTL3 not encoded in output:
The CTL3 input from the device pin or register value is not encoded into the DVI stream. The current TFP410 is aware of HDCP and encodes the CTL3 signal as 0 in the output. When the device is configured for manual input with pins 6-8 selected as CTL[3:1], pin 6 is not encoded. When the device is configured for I2C operation, bit 3 of the CTL_# MODE register at Sub-Address 0A can be written and read, but the bit is not encoded.

Changes in the document text:
Sheet 2, change pin 6 label FROM: CTL3/A3/DK3 TO: A3/DK3

Sheet 4, in the Terminal Functions table, change the name of pin 6 FROM: CTL3/A3/DK3 TO: A3/DK3 and in the Description column, change the second paragraph
FROM:
When the I2C bus is disabled (ISEL = low) and the de-skew mode is disabled (DKEN = low), these three inputs become the control inputs, CTL[3:1], which can be used to send additional information across the DVI link during the blanking interval (DE = low). The CTL3 input is reserved for HDCP compliant DVI TXs (TFP510) and the CTL[2:1] inputs are reserved for future use.
TO:
When the I2C bus is disabled (ISEL = low) and the de-skew mode is disabled (DKEN = low), pins 7 and 8 become the control inputs, CTL[2:1], which can be used to send additional information across the DVI link during the blanking interval (DE = low). Pin 6 is not used.

Sheet 10, in the first paragraph of the T.M.D.S. pixel data and control signal encoding section, change the sentence
FROM:
These same three channels are also used to transmit HSYNC, VSYNC, and three user definable control signals, CTL[3:1], during the inactive display or blanking interval (DE = Low).
TO:
These same three channels are also used to transmit HSYNC, VSYNC, and the control signals, CTL[3:1], during the inactive display or blanking interval (DE = Low).

Sheet 10, in note 8, change the second sentence
FROM:
The CTL3 input is reserved for HDCP compliant DVI TXs and the CTL[2:1] inputs are reserved for future use.
TO:
CTL3 is reserved for HDCP and is always encoded as 0. The CTL[2:1] inputs are reserved for future use.

Sheet 19, register CTL_3_MODE, change definition of bits 3:1 in the diagram
FROM:

3	2	1
CTL[3:1]		

TO:

3	2	1
RSVD	CTL[2:1]	

In the text below the diagram, change the CTL bit definition name
FROM:
CTL[3:1]:This read/write register contains the values of the three CTL[3:1] bits that are output on the DVI port during the blanking interval.
TO:
CTL[2:1]:This read/write register contains the values of the three CTL[2:1] bits that are output on the DVI port during the blanking interval.

6. Input voltage clarifications

In the DC specification table, V_{IH} and V_{IL} are not clear for signals that are not part of the video input bus.

Changes in the document text:
Sheet 7, in the dc specifications table, change the V_{IH} and V_{IL} specifications to contain the following information:

PARAMETERS			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	Data, DE, VSYNC, HSYNC and IDCK+/-	$V_{REF} = DV_{DD}$	$0.7V_{DD}$			V
			$0.5V \le V_{REF} \le 0.95V$	$V_{REF} + 0.2$			V
		Other inputs		$0.7V_{DD}$			V
V_{IL}	Low-level input voltage	Data, DE, VSYNC, HSYNC and IDCK+/-	$V_{REF} = DV_{DD}$			$0.3V_{DD}$	V
			$0.5V \le V_{REF} \le 0.95V$			$V_{REF} - 0.2$	V
		Other inputs				$0.3V_{DD}$	V

7. PowerPad size and routing consideration:

The size of the exposed metal on the PowerPad package figure is shown as larger than on production devices. When providing a thermal land, it may be smaller than assumed from the package drawing. If routing traces under the power pad, some method of protection from shorts between the traces or vias and the PowerPad should be used.

Changes to document:

Sheet 24, change the package figure as described:
a) Re-size the thermal pad dashed box from its present size to 5.35mm, centered in the package.
b) Note the dimensions and change note D by either:

Add dimensions to re-sized pad showing: 5.35 SQ
4.25

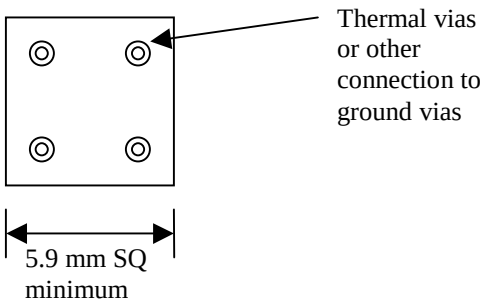
and
Change note D to read:
The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is centered on the package and is electrically and thermally connected to the backside of the die.

Sheet 23, add sentence to paragraph 1, correct typographical error in paragraph 2 and add figure and paragraphs between existing paragraphs 2 &3 to read:

… soldering the back side of the TFP410 to the application board is not required thermally as the device power dissipation is well within the package capability when not soldered. If traces or vias are located under the back side pad, they should be protected by suitable solder mask or other assembly technique to prevent inadvertent shorting to the exposed back side pad.

Soldering the backside of the device to a thermal land connected to the PCB ground plane is recommended for electrical and EMI considerations. The thermal land may be soldered to the exposed PowerPAD using standard reflow soldering techniques.

The recommended pad size for the grounded thermal land is 5.9mm minimum, centered in the device land pattern. When vias are required to ground the land, multiple vias are recommended for a low impedance connection to the ground plane. Vias in the exposed pad should be small enough or filled to prevent wicking the solder away from the interface between the package body and the thermal land on the surface of the board during solder reflow.



More information on this package and other requirements for using thermal lands and thermal vias are detailed in the TI application note *PowerPAD Thermally Enhanced Package Application Report*, TI literature number SLMA002, available via the TI Web pages beginning at URL: http://www.ti.com

Table 2 outlines the thermal properties…

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