



STF8NK100Z STP8NK100Z

N-CHANNEL 1000V - 1.60Ω - 6.5A - TO-220 - TO-220FP
Zener-Protected SuperMESH™ MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D	P _w
STF8NK100Z	1000 V	<1.85Ω	6.5 A ^{Note 1}	40 W
STP8NK100Z	1000 V	<1.85Ω	6.5 A	160 W

- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE RATED
- IMPROVED ESD CAPABILITY
- VERY LOW INTRINSIC CAPACITANCE

Description

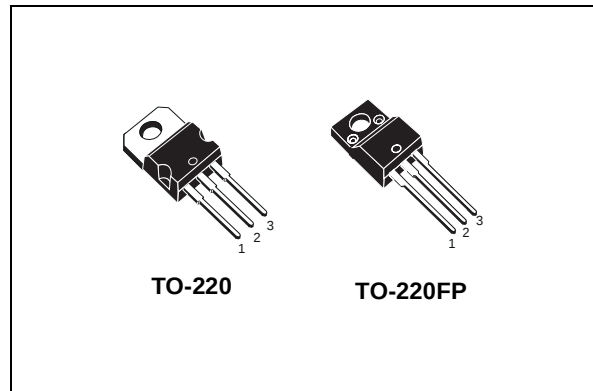
The SuperMESH™ series is obtained through an extreme optimization of ST's well established stripbased PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

Applications

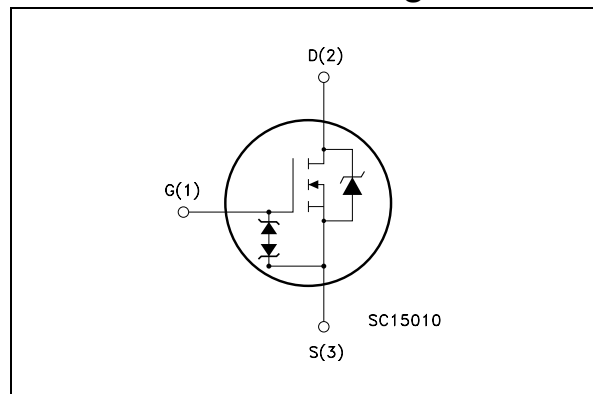
- HIGH CURRENT, SWITCHING APPLICATION
- IDEAL FOR OFF-LINE POWER SUPPLIES

Order codes

Sales Type	Marking	Package	Packaging
STF8NK100Z	F8NK100Z	TO-220FP	TUBE
STP8NK100Z	P8NK100Z	TO-220	TUBE



Internal schematic diagram



1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
V_{DS}	Drain-source Voltage ($V_{GS}=0$)	1000		V
V_{DGR}	Drain-gate Voltage	1000		V
V_{GS}	Gate-Source Voltage	± 30		V
I_D <i>Note 1</i>	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	6.5	6.5	A
I_D	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	4.3	4.3	A
I_{DM} <i>Note 2</i>	Drain Current (pulsed)	16	16	A
P_{TOT}	Total Dissipation at $T_C = 25^\circ\text{C}$	160	40	W
	Derating Factor	1.28	0.32	W/°C
$V_{ESD(G-S)}$	Gate source ESD (HBM-C=100pF, R=1.5K Ω)	4000		V
dv/dt <i>Note 3</i>	Peak Diode Recovery voltage slope	4.5		V/ns
V_{ISO}	Insulation Withstand Voltage (DC)	--	2500	V
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 150		°C

Table 2. Thermal data

		TO-220	TO-220FP	
Rthj-case	Thermal Resistance Junction-case Max	0.78	3.1	°C/W
Rthj-a	Thermal Resistance Junction-ambient Max	62.5		°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300		°C

Table 3. Avalanche Characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	6.5	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{V}$)	320	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-Source Breakdown Voltage	I _D = 1mA, V _{GS} = 0	1000			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating, V _{DS} = Max Rating, T _c = 125°C			1 50	μA μA
I _{GSS}	Gate Body Leakage Current (V _{DS} = 0)	V _{GS} = ±20V			±10	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 100 μA	3	3.75	4.5	V
R _{DS(on)}	Static Drain-Source On Resistance	V _{GS} = 10 V, I _D = 3.15 A		1.60	1.85	Ω

Table 5. Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} <i>Note 6</i>	Forward Transconductance	V _{DS} = 15V, I _D = 3.15 A		7		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		2180 174 36		pF pF pF
C _{oss eq.} <i>Note 5</i>	Equivalent Output Capacitance	V _{GS} = 0V, V _{DS} = 0 to 800V		83		pF
Q _g Q _{gs} Q _{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V _{DD} = 800V, I _D = 6.3A V _{GS} = 10V (see Figure 17)		73 12 40	102	nC nC nC

Table 6. Switching times

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD}=500\text{ V}$, $I_D=3.15\text{ A}$, $R_G=4.7\Omega$, $V_{GS}=10\text{ V}$ (see Figure 18)		28 19		ns ns
$t_{d(off)}$ t_f	Turn-off Delay Time FallTime	$V_{DD}=500\text{ V}$, $I_D=3.15\text{ A}$, $R_G=4.7\Omega$, $V_{GS}=10\text{ V}$ (see Figure 18)		59 30		ns ns

Table 7. Source drain diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} <i>Note 3</i>	Source-drain Current Source-drain Current (pulsed)				6.5 26	A A
V_{SD} <i>Note 2</i>	Forward on Voltage	$I_{SD}=6.3\text{ A}$, $V_{GS}=0$			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD}=6.3\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=50\text{ V}$, $T_J=25^\circ\text{C}$		620 5.3 17		ns μC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD}=6.3\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=50\text{ V}$, $T_J=150^\circ\text{C}$		840 7.5 18		ns μC A

Table 8. Gate-source zener diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO} <i>Note 4</i>	Gate-Source Breakdown Voltage	$I_{gs} = \pm 1\text{ mA}$ (Open Drain)	30			V

(1) Limited only by maximum temperature allowed

(2) $I_{SD} \leq 6.5\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DS} \leq V_{(BR)DSS}$, $T_J \leq T_{Jmax}$

(3) Pulse width limited by safe operating area

(4) The built-in-back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

(5) $C_{oss,eq}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} (6) Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe Operating Area for TO-220

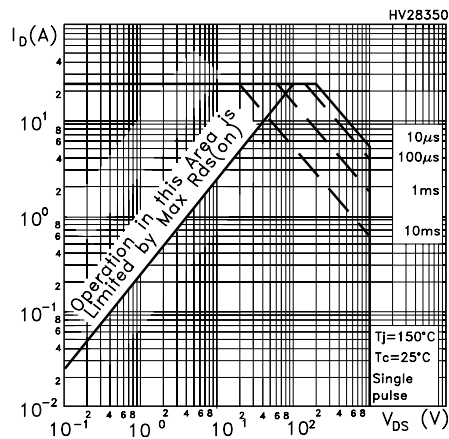


Figure 2. Thermal Impedance for TO-220

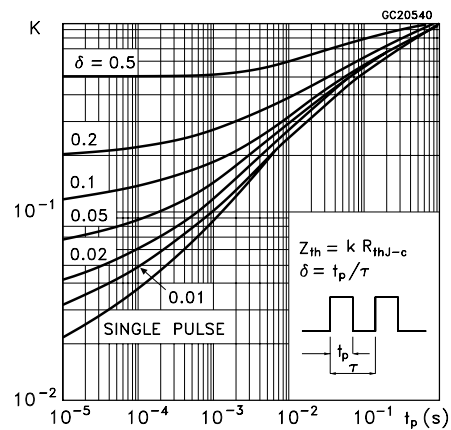


Figure 3. Safe Operating Area for TO-220FP

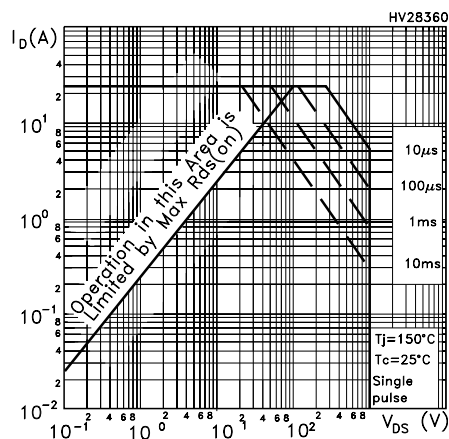


Figure 4. Thermal Impedance for TO-220FP

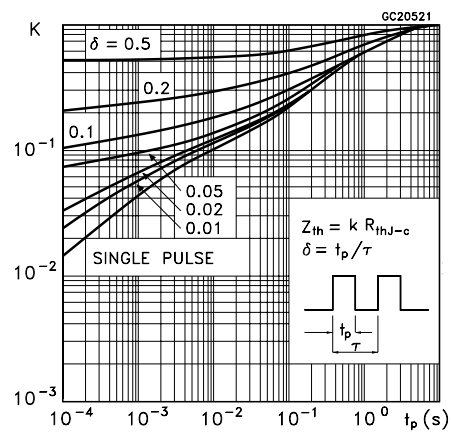


Figure 5. Output Characteristics

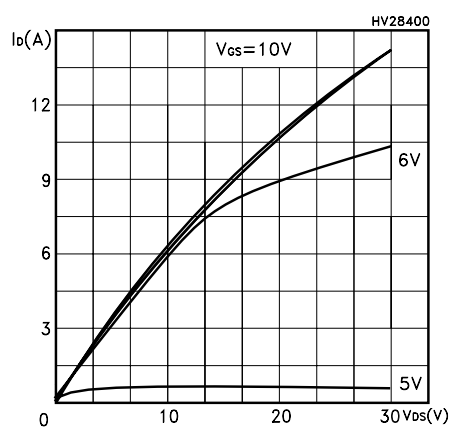


Figure 6. Transfer Characteristics

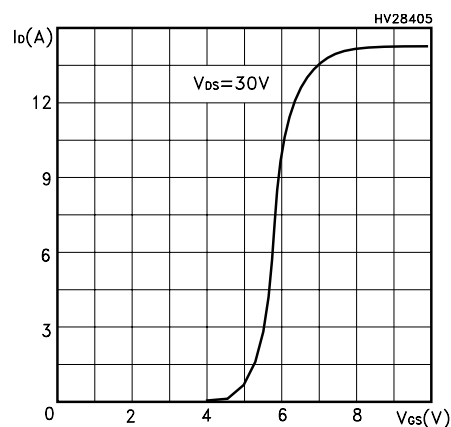


Figure 7. Transconductance

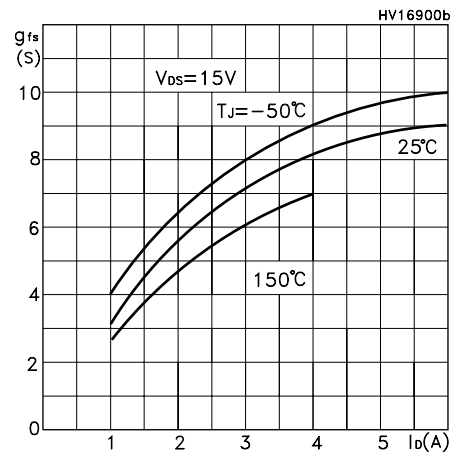


Figure 8. Static Drain-source on Resistance

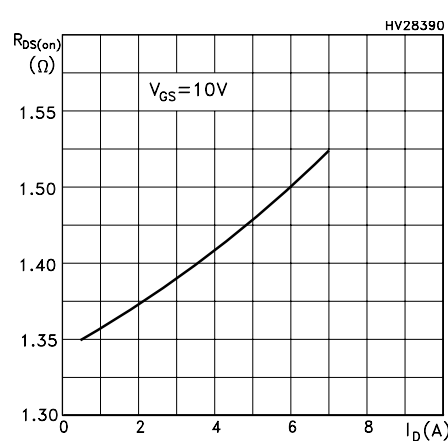


Figure 9. Gate Charge vs Gate-source Voltage Figure 10. Capacitance Variations

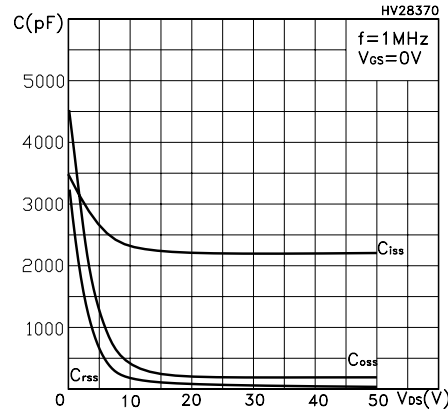
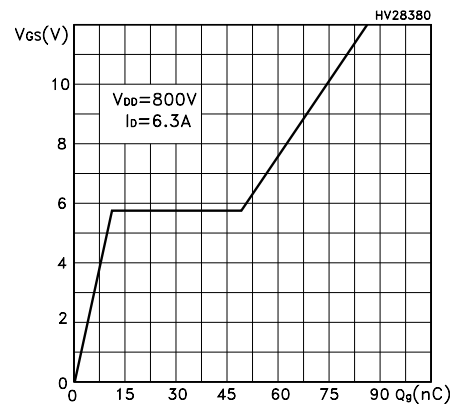


Figure 11. Normalized Gate Threshold Voltage vs. Temperature Figure 12. Normalized On Resistance vs. Temperature

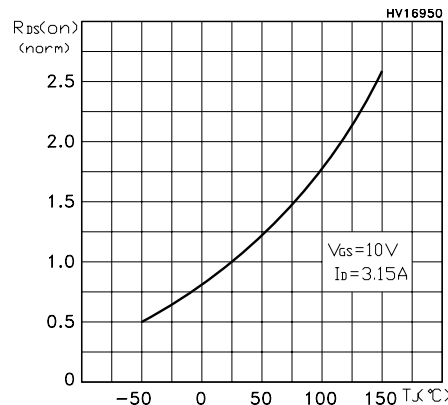
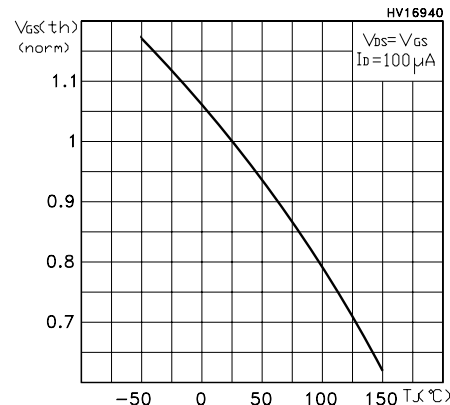


Figure 13. Source-drain Diode Forward Characteristics

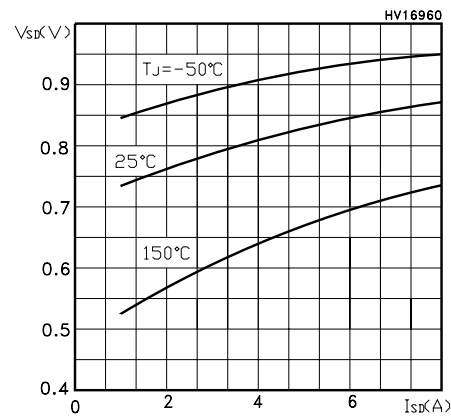


Figure 14. Normalized BVDSS vs Temperature

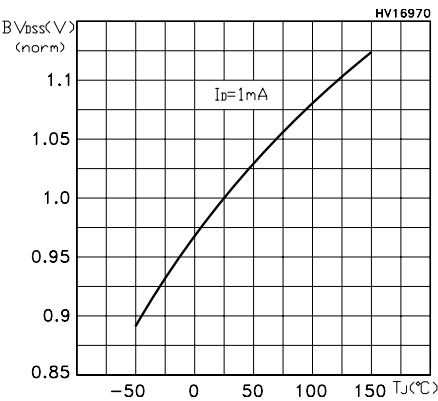
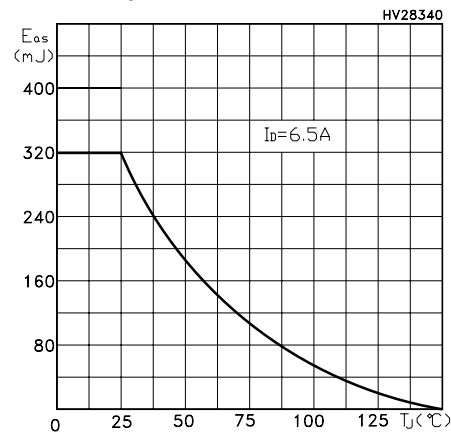


Figure 15. Maximum Avalanche Energy vs Temperature



3 Test circuits

Figure 16. Switching Times Test Circuit For Resistive Load

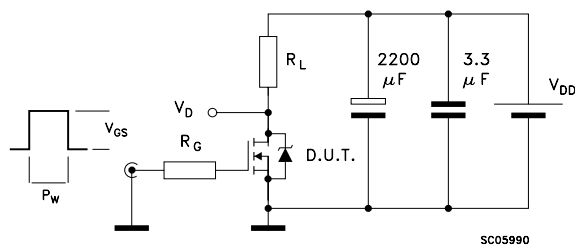


Figure 17. Gate Charge Test Circuit

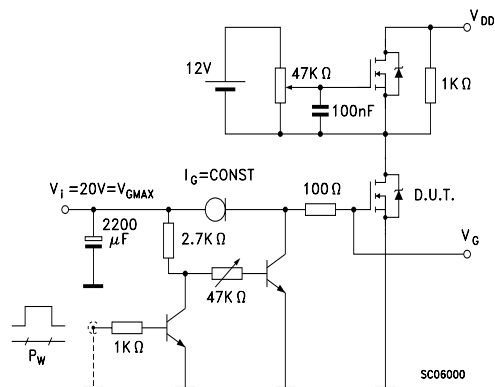


Figure 18. Test Circuit For Inductive Load Switching and Diode Recovery Times

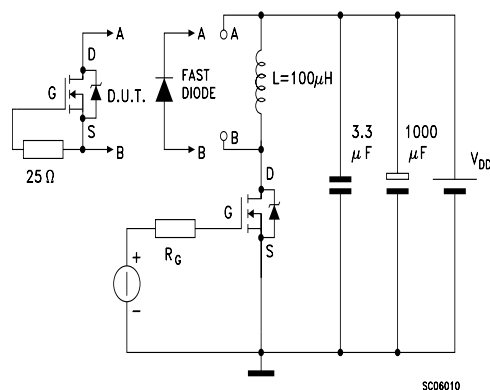


Figure 20. Unclamped Inductive Load Test Circuit

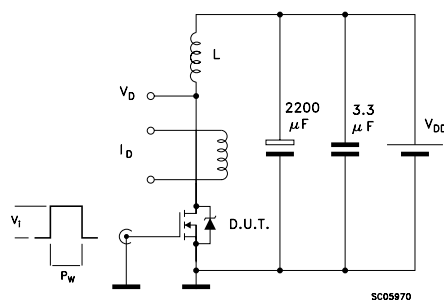
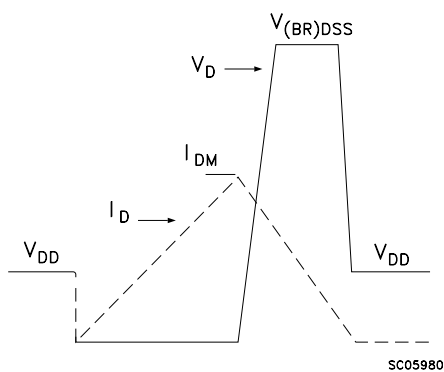


Figure 19. Unclamped Inductive Waveform

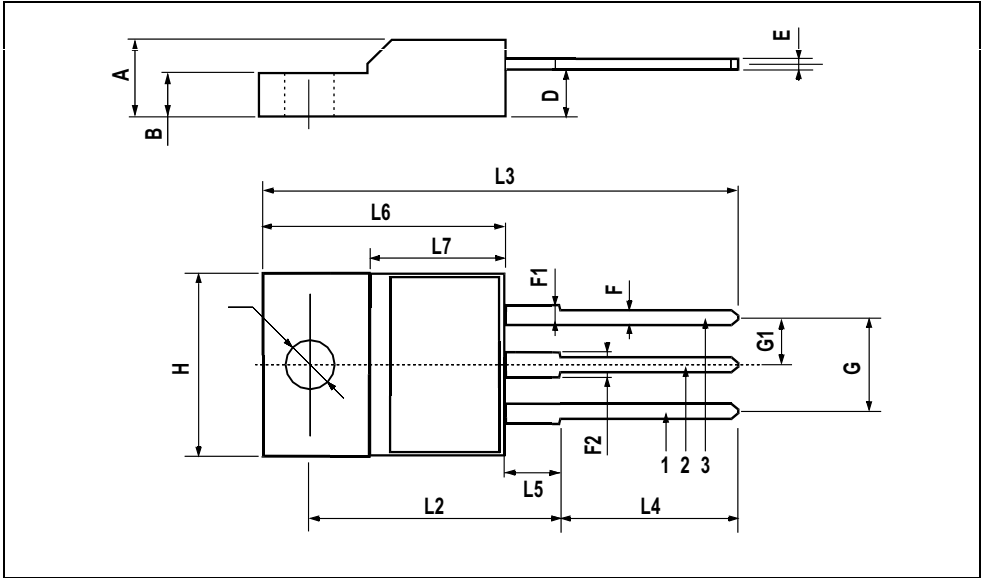


4 Package mechanical data

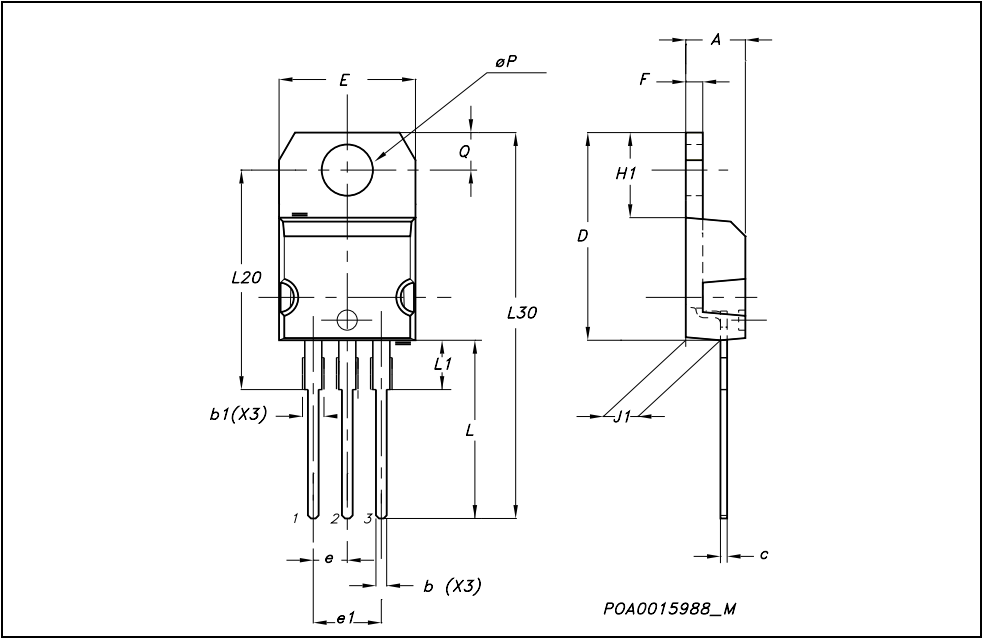
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



TO-220 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



5 Revision History

Date	Revision	Changes
04-Nov-2005	1	First release

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics.
All other names are the property of their respective owners

© 2005 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan -
Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

