



STP60NF06 STP60NF06FP

N-channel 60V - 0.014Ω - 60A TO-220/TO-220FP
STripFET II™ Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D
STP60NF06	60V	<0.016Ω	60A
STP60NF06FP	60V	<0.016Ω	60A

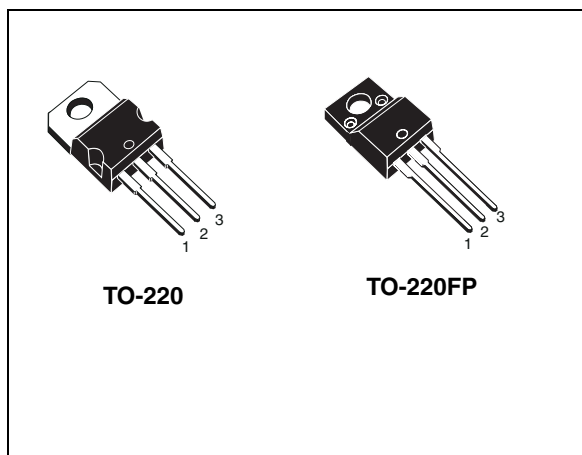
- Exceptional dv/dt capability
- 100% avalanche tested
- Application oriented characterization

Description

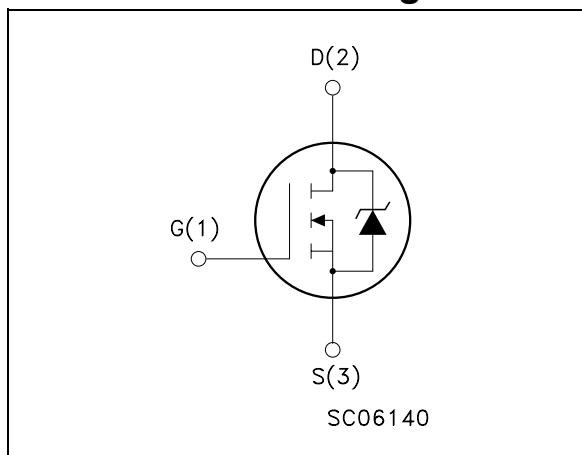
This Power Mosfet series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC converters for Telecom and Computer application. It is also intended for any application with low gate charge drive requirements.

Applications

- Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STP60NF06	P60NF06	TO-220	Tube
STP60NF06FP	P60NF06	TO-220FP	Tube

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	60		V
V_{GS}	Gate- source voltage	± 20		V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	60	30	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	42	21	A
$I_{DM}^{(1)}$	Drain current (pulsed)	240	120	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	110	30	W
	Derating factor	0.74	0.2	W/ $^\circ\text{C}$
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t=1\text{s}$; $T_C=25^\circ\text{C}$)	--	2500	V
T_{stg}	Storage temperature	- 55 to 175		$^\circ\text{C}$
T_j	Max. operating junction temperature			

1. Pulse width limited by safe operating area

2. $I_{SD} \leq 60\text{A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DD} \leq 24\text{V}$, $T_j \leq T_{jmax}$

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case max	1.36	5	$^\circ\text{C}/\text{W}$
R_{thj-a}	Thermal resistance junction-ambient max	62.5		$^\circ\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purpose	300		$^\circ\text{C}$

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j Max)	30	A
E_{AS}	Single pulse avalanche energy (starting $T_j=25^\circ\text{C}$, $I_d=I_{AR}$, $V_{DD}=30\text{V}$)	370	mJ

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	60			V
I_{DSS}	Zero gate voltage Drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}, T_C = 125^{\circ}C$			1 10	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20V$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 30A$		0.014	0.016	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15V, I_D = 30A$		20		S
C_{iss}	Input capacitance			1810		pF
C_{oss}	Output capacitance	$V_{DS} = 25V, f = 1 \text{ MHz},$ $V_{GS} = 0$		360		pF
C_{rss}	Reverse transfer capacitance			125		pF
Q_g	Total gate charge	$V_{DD} = 48V, I_D = 60A,$ $V_{GS} = 10V$		49	66	nC
Q_{gs}	Gate-source charge	$V_{GS} = 10V$		18		nC
Q_{gd}	Gate-drain charge	(see Figure 15)		14		nC

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD} = 30V, I_D = 30A$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see Figure 14)		16 108		ns ns
$t_{d(off)}$ t_f	Turn-off-delay time Fall time	$V_{DD} = 30V, I_D = 30A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see Figure 14)		43 20		ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage rise time Fall time Cross-over time	$V_{clamp} = 48V, I_D = 60A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see Figure 14)		40 12 21		ns ns ns

Table 7. Source drain diode

Symbol	Parameter		Test conditions	Min	Typ.	Max	Unit	
I_{SD}	Source-drain current	TO-220				60	A	
$I_{SDM}^{(1)}$	Source-drain current (pulsed)					240	A	
I_{SD}	Source-drain current	TO-220FP				30	A	
I_{SDM}	Source-drain current (pulsed)					120	A	
$V_{SD}^{(2)}$	Forward on voltage		$I_{SD} = 60A, V_{GS} = 0$			1.3	V	
t_{rr}	Reverse recovery time		$I_{SD} = 60A, V_{DD}=25V$ $di/dt = 100A/\mu s,$ $T_j = 150^\circ C$ <i>(see Figure 19)</i>		75		ns	
Q_{rr}	Reverse recovery charge					182		nC
I_{RRM}	Reverse recovery current					5		A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220

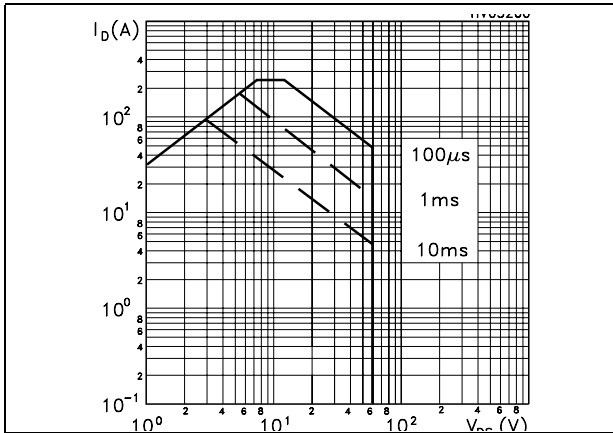


Figure 2. Thermal impedance for TO-220

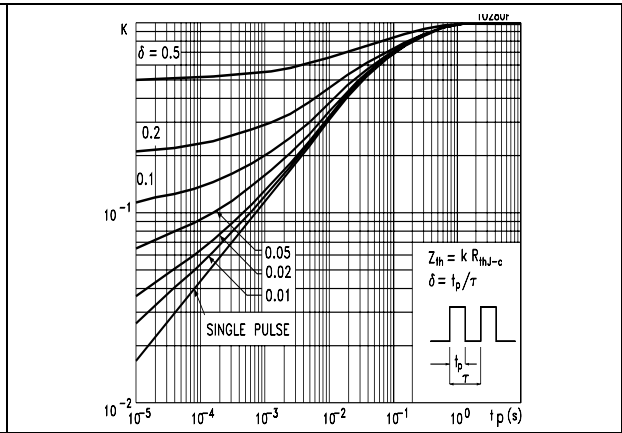


Figure 3. Safe operating area for TO-220FP

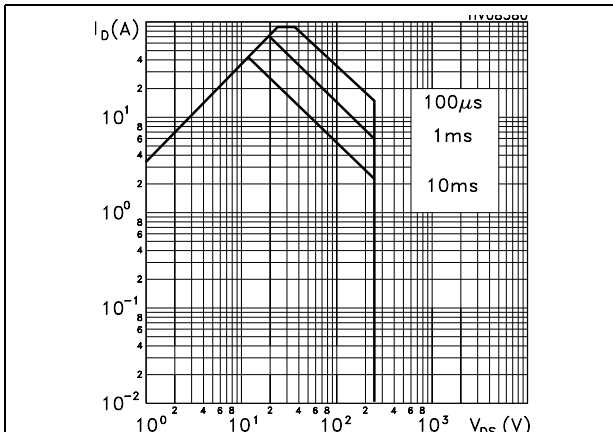


Figure 4. Thermal impedance for TO-220FP

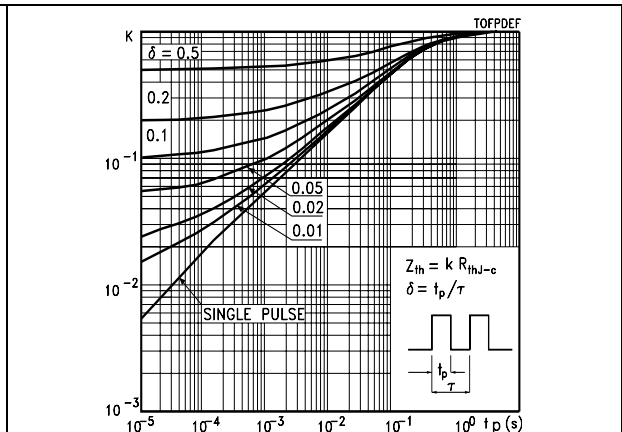


Figure 5. Output characteristics

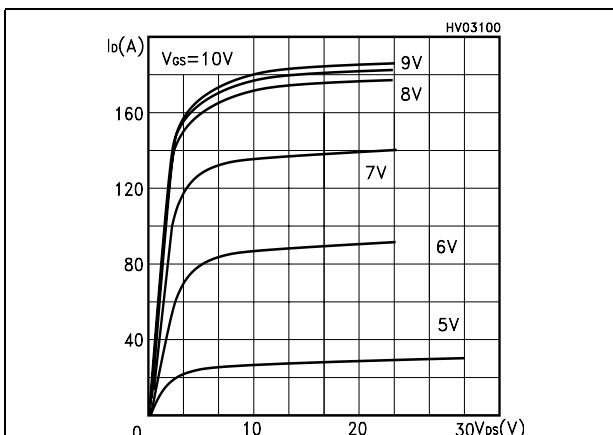


Figure 6. Transfer characteristics

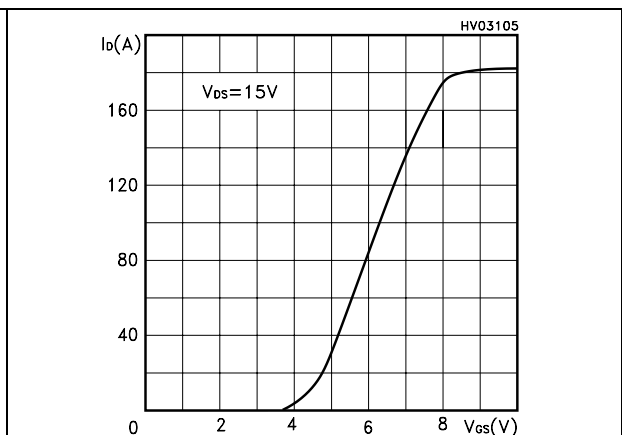


Figure 7. Transconductance

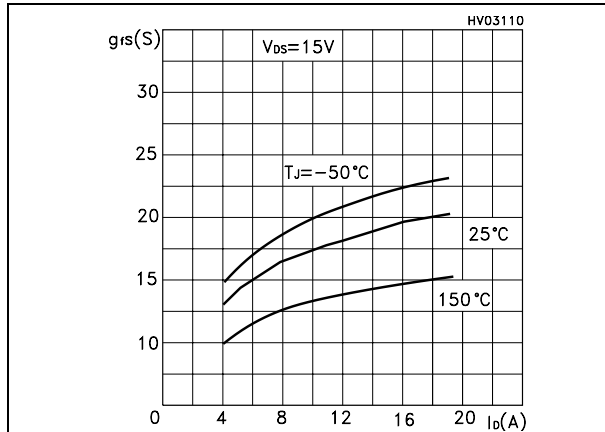


Figure 8. Static drain-source on resistance

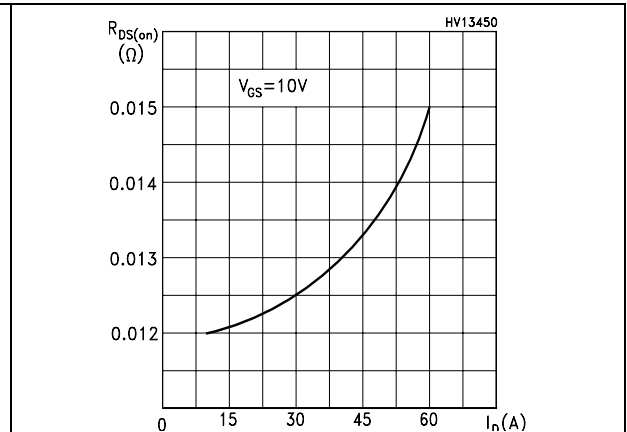


Figure 9. Gate charge vs gate-source voltage

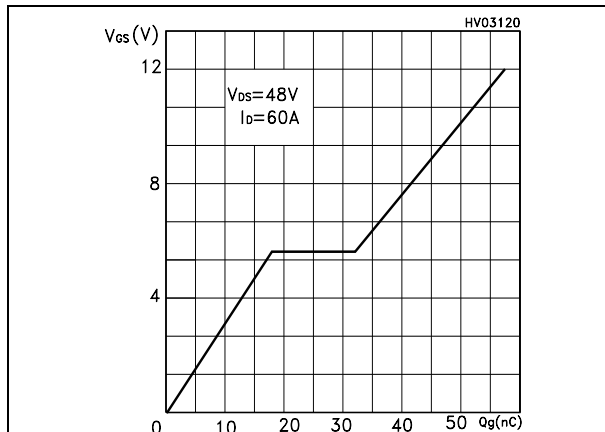


Figure 10. Capacitance variations

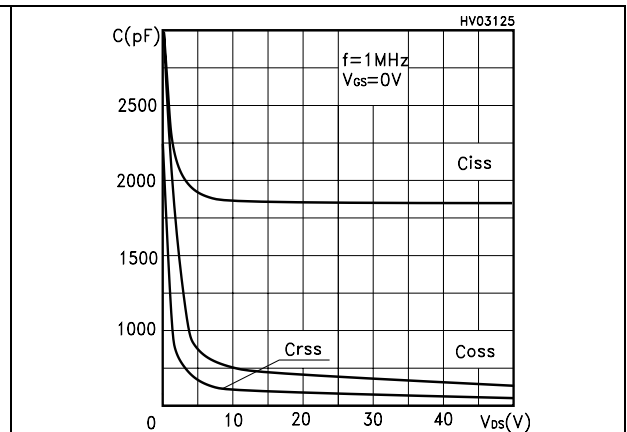


Figure 11. Normalized gate threshold voltage vs temperature

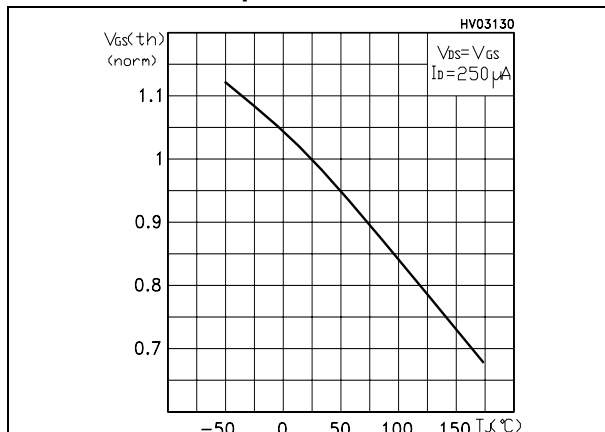


Figure 12. Normalized on resistance vs temperature

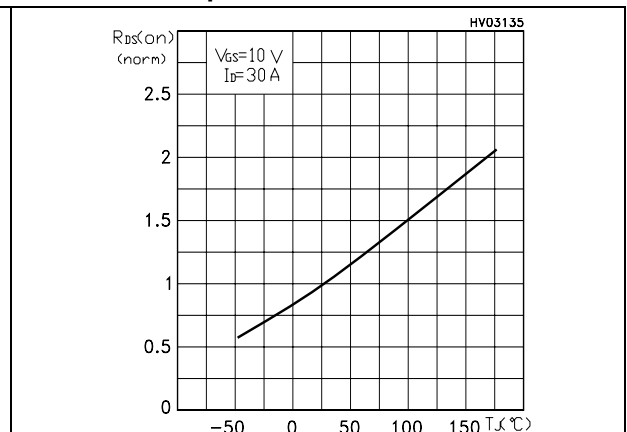
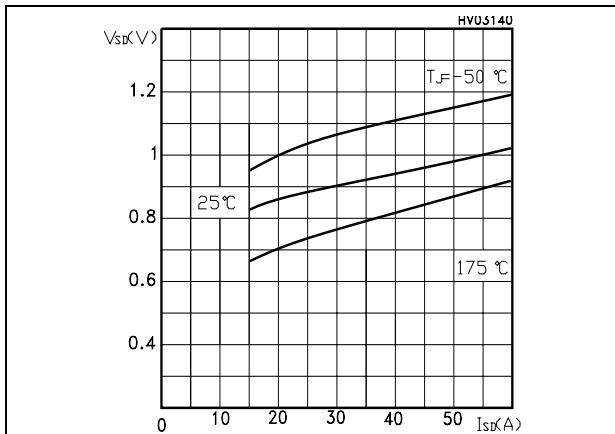


Figure 13. Source-drain diode forward characteristics



3 Test circuit

Figure 14. Switching times test circuit for resistive load

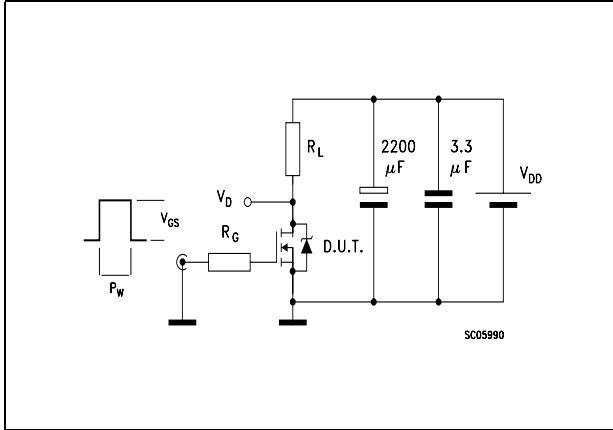


Figure 15. Gate charge test circuit

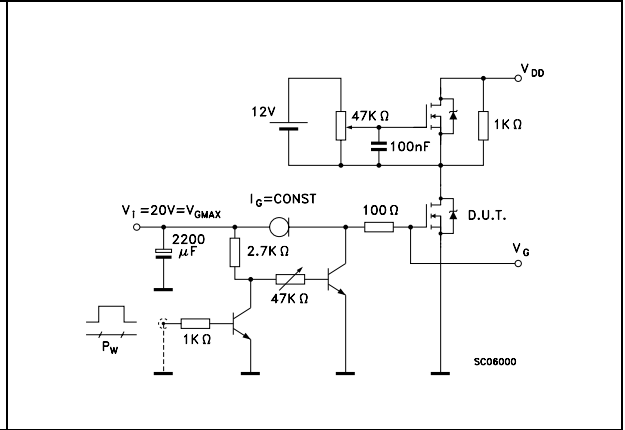


Figure 16. Test circuit for inductive load switching and diode recovery times

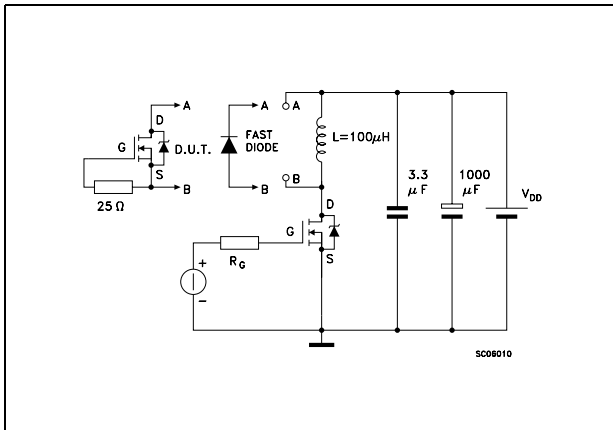


Figure 17. Unclamped Inductive load test circuit

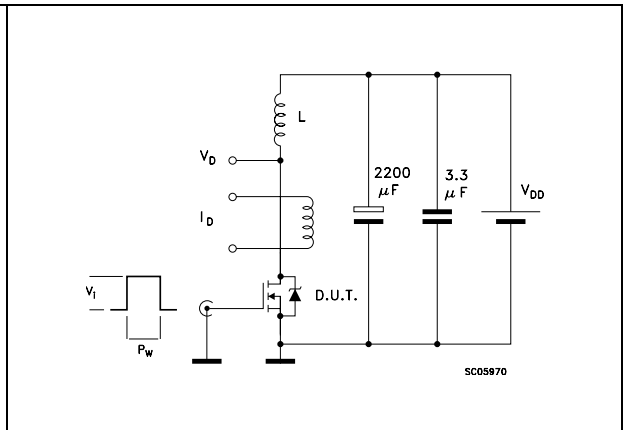


Figure 18. Unclamped inductive waveform

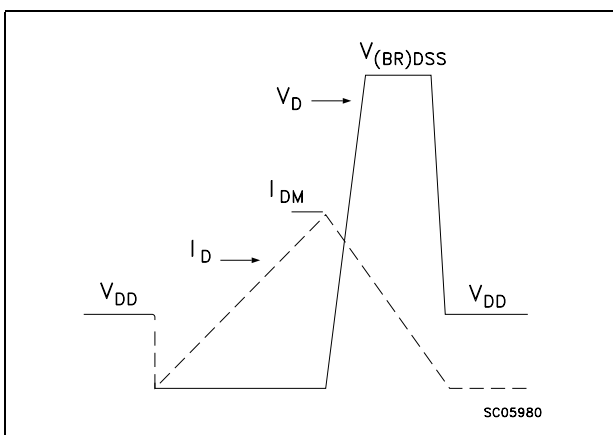
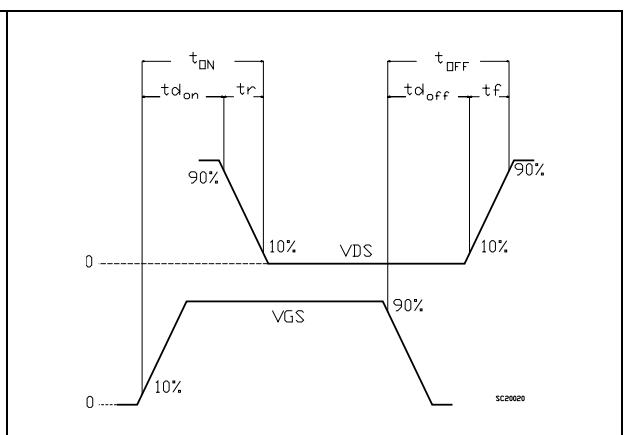


Figure 19. Switching time waveform

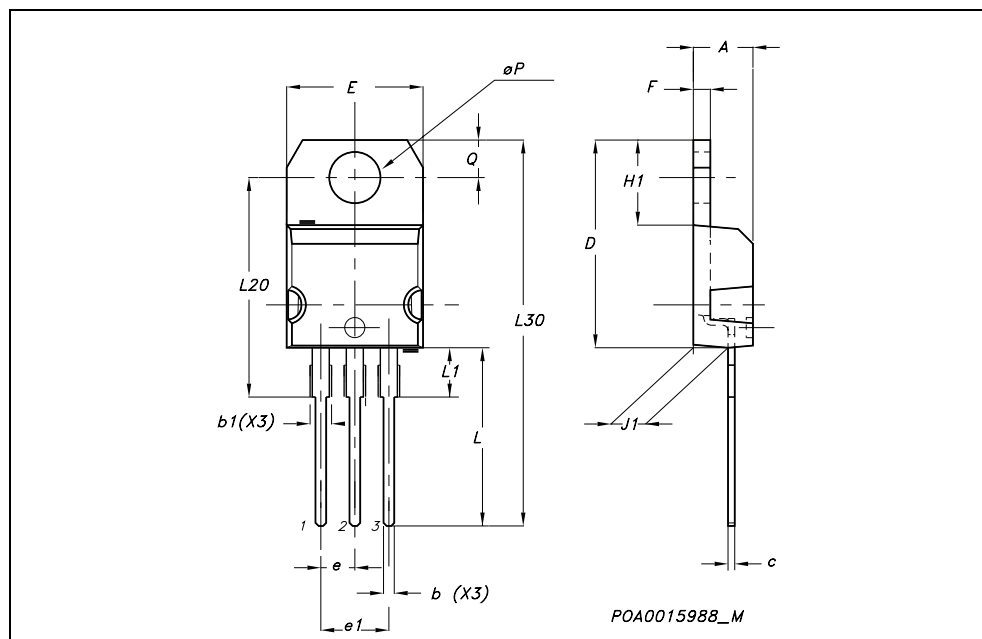


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at : www.st.com

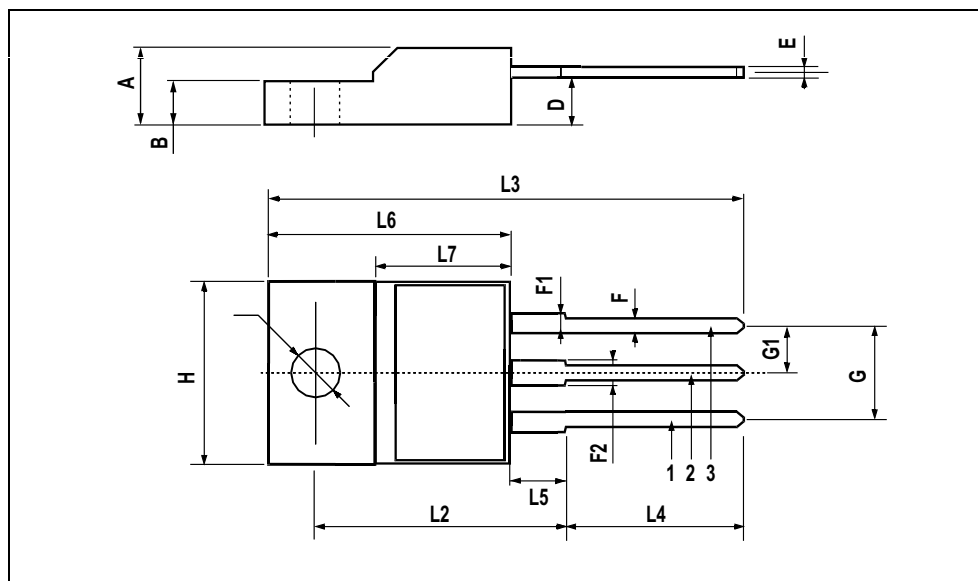
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



5 Revision history

Table 8. Revision history

Date	Revision	Changes
09-Sep-2004	3	Complete version
17-Aug-2006	4	New template, no content change
04-Oct-2006	5	Changes in <i>Dynamic</i>

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