
PIC16F684 Rev. A Silicon/Data Sheet Errata

The PIC16F684 parts you have received conform functionally to the Device Data Sheet (DS41202D), except for the anomalies described below.

Microchip intends to address all issues listed here in future revisions of the **PIC16F684 silicon**.

1. Module: Resets (when WDT times out)

If the OPTION_REG bits, PS<2:0>, are clear, multiple spurious Resets can occur when the WDT times out. These Resets can occur even when the PSA bit is clear, assigning the prescaler to the Timer0.

Work around

If a CLRWDT instruction is issued before the WDT times out and before the OPTION register is modified, this problem is eliminated.

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: Data EEPROM Memory

The EEIF flag may be cleared inadvertently when performing operations on the PIR1 register simultaneously with the completion of an EEPROM write. This condition occurs when the EEPROM write timer completes at the same moment that the PIR1 register operation is executed. Register operations are those that have the PIR1 register as the destination and include, but are not limited to, BSF, BCF, ANDWF, IORWF and XORWF.

Work around

1. Avoid operations on the PIR1 register when writing to the EEPROM memory.
2. Poll the WR bit (EECON1<1>) to determine when the write is complete.
3. Use a timer interrupt to catch any instances when the EEIF flag is inadvertently cleared. The timer interrupt should be set longer than 8 ms. If EEIF fails, then the timer interrupt occurs as a default time out. The WR and WRERR flags are checked as part of the timer interrupt service routine to verify the EEPROM write success.

4. If periodic interrupts are occurring in addition to the EEIF interrupts, then use a secondary flag to sense write completion. The secondary flag is set whenever EEPROM writes are active. An EEPROM write completion is indicated when the secondary flag is set and the WR flag is clear.

3. Module: ECCP with Auto-Shutdown (Silicon Rev. A4 and B2)

The PIC16F684 Rev. A4 silicon for the ECCP Auto-Shutdown is connected to the C1IF and C2IF flags. See Figures 8-2 and 8-3 on the following page.

Rev. A4's auto-shutdown connection to C1IF and C2IF causes the auto-shutdown to incorrectly operate synchronously. Additionally, reads of CMCON0 will incorrectly clear an auto-shutdown event.

Work around

Rev. A4 Silicon

- 1) Poll the CxOUT bit until it is low.
- 2) Read CMCON1 to precondition CxIF.
- 3) If CMCON0 is read while CxOUT is changing, repeat steps 1 and 2.

Fix

Rev. B2 Silicon

The Silicon Rev. B2 device (now shipping) has moved the auto-shutdown connection from CxIF to CxOUT. This will eliminate the synchronous shutdown and simplify the use of the comparator for a shutdown event. Figure 1 shows the function of auto-shutdown before and after the device revision.

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FIGURE 8-2: COMPARATOR C1 OUTPUT BLOCK DIAGRAM

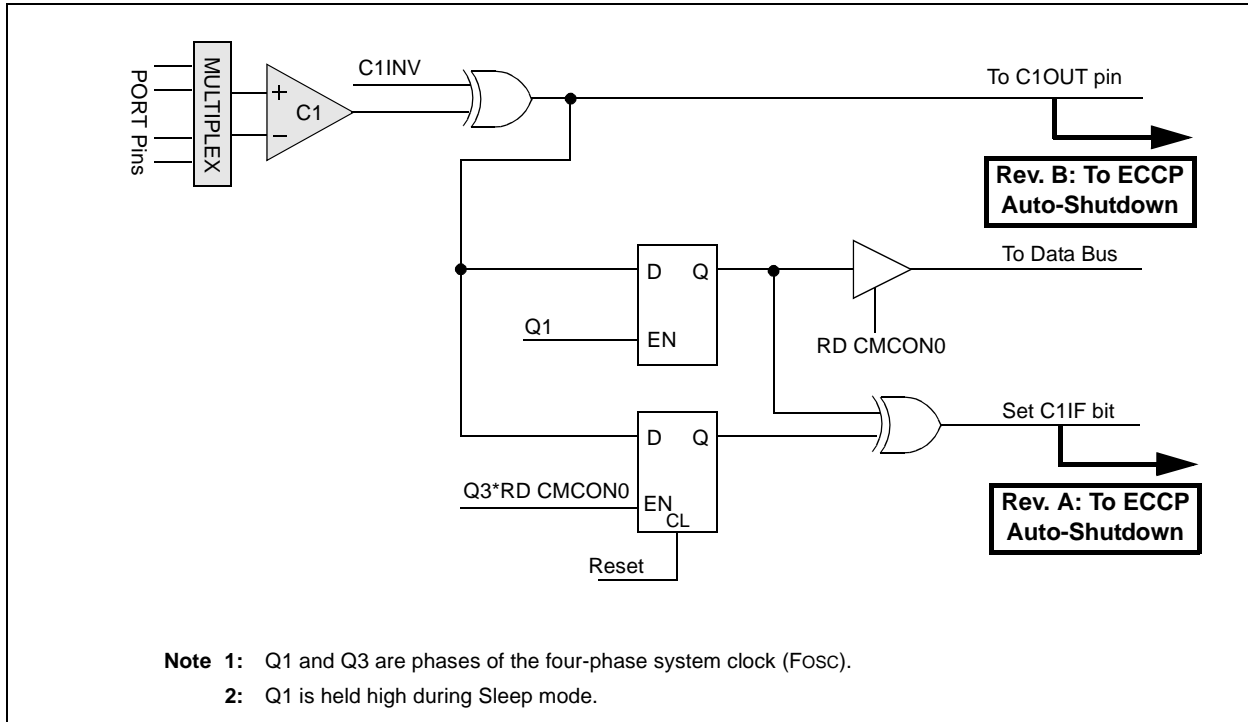


FIGURE 8-3: COMPARATOR C2 OUTPUT BLOCK DIAGRAM

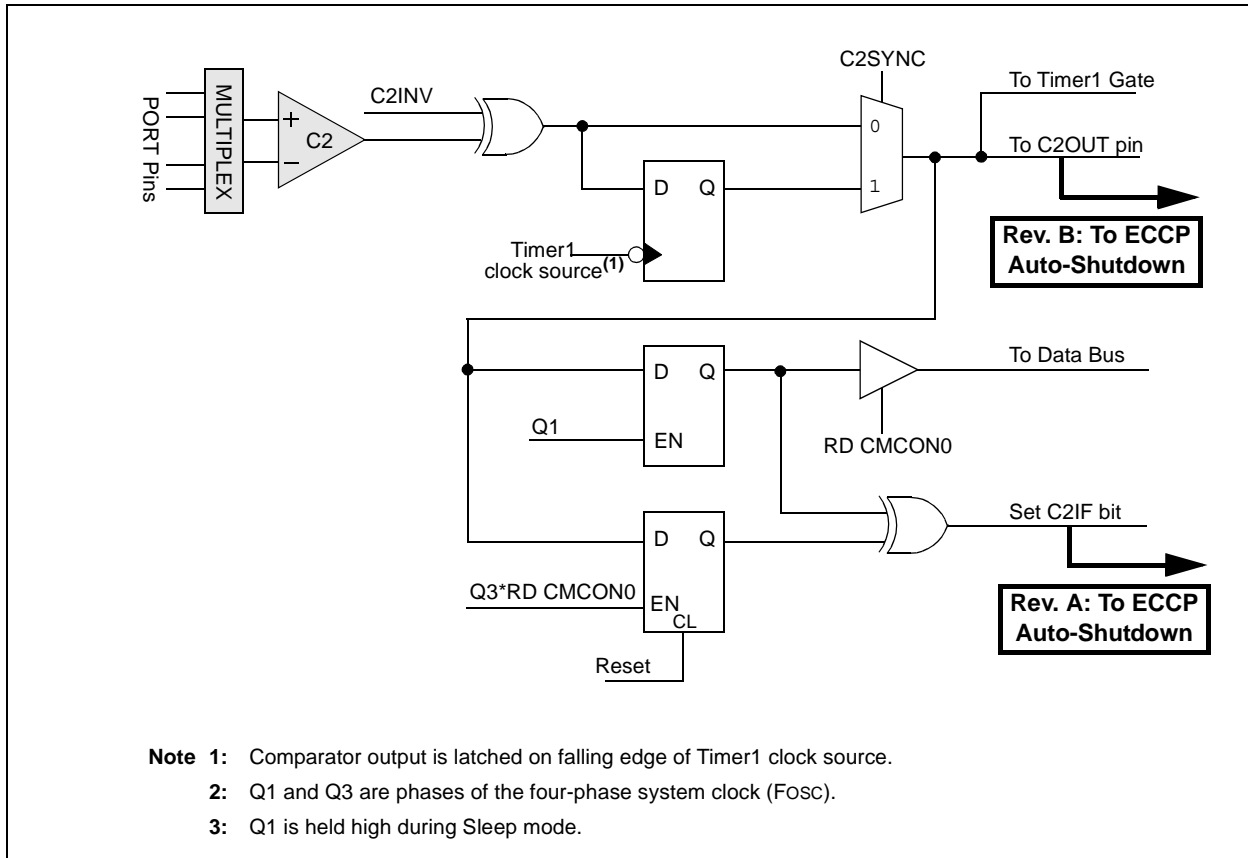
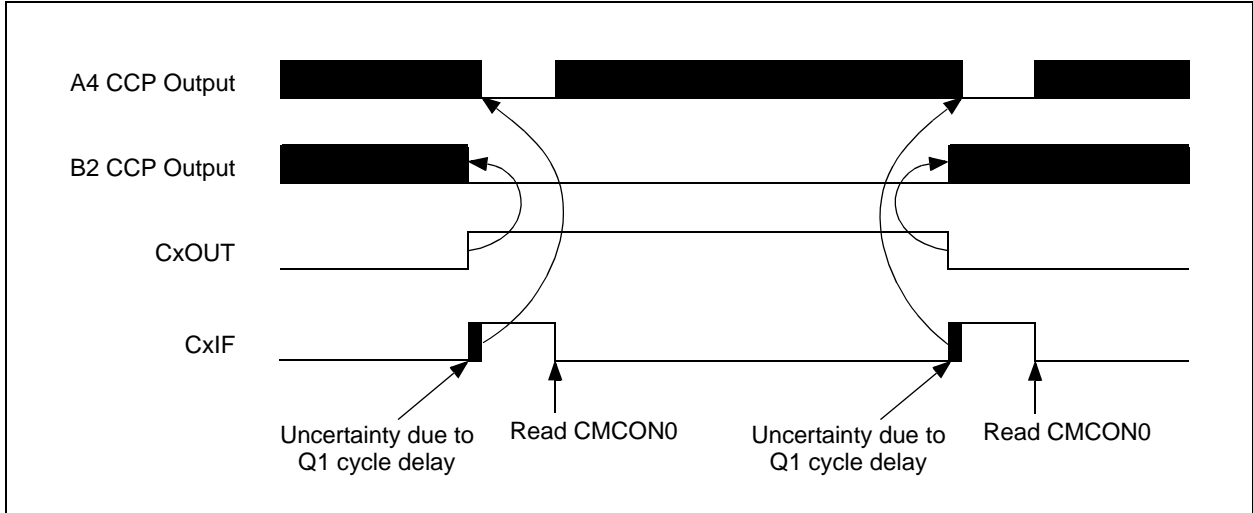


FIGURE 1: SILICON REVISION A4 VS. REVISION B2



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Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (41202D), the following clarifications and corrections should be noted.

N/A.

REVISION HISTORY

Rev A Document (7/2004)

First revision of this document. Changes made to Section 11.1.1, "CCP1 Pin Configuration".

Rev B Document (08/2004)

Issue 1 – When OPTION_REG bits, PS<2:0>, are clear, multiple spurious Resets can occur when the WDT times out.

Rev C Document (11/2004)

Added Module 2: "Data EEPROM Memory" for PIC16F684 silicon.

Rev D Document (7/2005)

Data Sheet Clarifications/Corrections Section: Added Module 2: New 4x4 QFN Package added.

Rev E Document (7/2006)

Added Module 3: ECCP with Auto-Shutdown (Silicon Rev. A4 and B2).

Clarifications/Corrections to the Data Sheet: Removed Items 1 and 2, which have been incorporated into the data sheet.

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