

SN54LS375, SN74LS375 4-BIT BISTABLE LATCHES

SDLS166 OCTOBER 1976 — REVISED MARCH 1988

- Supply Voltage and Ground on Corner Pins To Simplify P-C Board Layout

description

The SN54LS375 and SN74LS375 bistable latches are electrically and functionally identical to the SN54LS75 and SN74LS75, respectively. Only the arrangement of the terminals has been changed in the SN54LS375 and SN74LS375.

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (C) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable goes high.

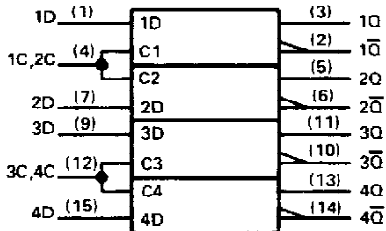
All inputs are diode-clamped to minimize transmission-line effects and simplify system design. The SN54LS375 is characterized for operation over the full military temperature range of -55°C to 125°C; SN74LS375 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(EACH LATCH)

INPUTS		OUTPUTS	
D	G	Q	\bar{Q}
L	H	L	H
H	H	H	L
X	L	Q_0	\bar{Q}_0

H = high level, L = low level, X = irrelevant
 Q_0 = the level of Q before the high-to-low transition of C.

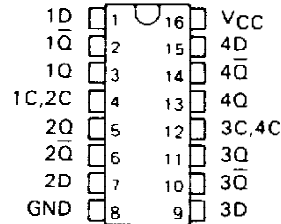
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

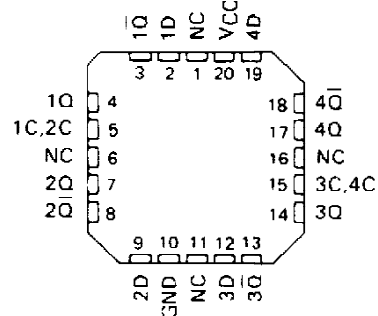
SN54LS375 . . . J OR W PACKAGE
SN74LS375 . . . D OR N PACKAGE

(TOP VIEW)



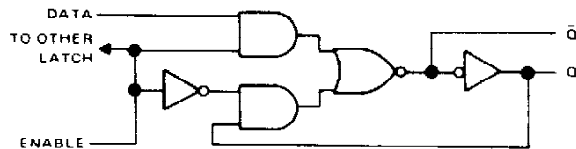
SN54LS375 . . . FK PACKAGE

(TOP VIEW)

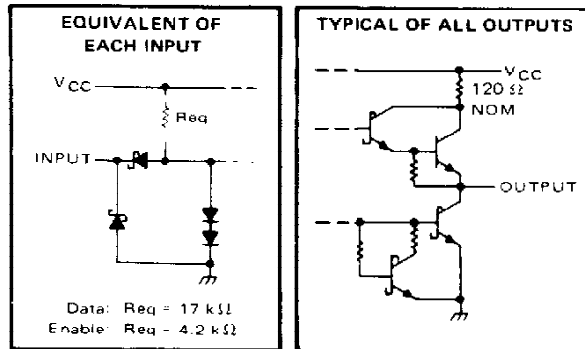


NC - No internal connection

logic diagram (each latch)



schematics of inputs and outputs



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TEXAS
INSTRUMENTS

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SN54LS375, SN74LS375

4-BIT BISTABLE LATCHES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS375	-55°C to 125°C
SN74LS375	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS375			SN74LS375			UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX			
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V		
V_{IH}	High-level input voltage	2			2			V		
V_{IL}	Low-level input voltage	0.7			0.8			V		
I_{OH}	High-level output current	-0.4			-0.4			mA		
I_{OL}	Low-level output current	4			8			mA		
t_w	Width of enabling pulse	20			20			ns		
t_{setup}	Setup time	20			20			ns		
t_{hold}	Hold time	0			0			ns		
T_A	Operating free-air temperature	-55			125			0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS375			SN74LS375			UNIT	
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX		
V_{IK}	$V_{CC} = \text{MIN.}$, $I_I = -18 \text{ mA}$	-1.5			-1.5			V	
V_{OH}	$V_{CC} = \text{MIN.}$, $V_{IH} = 2 \text{ V.}$, $V_{IL} = \text{MAX}$ $I_{OH} = -0.4 \text{ mA}$	2.5	3.5		2.7	3.5		V	
V_{OL}	$V_{CC} = \text{MIN.}$, $V_{IH} = 2 \text{ V.}$, $V_{IL} = \text{MAX}$	$I_{OL} = 4 \text{ mA}$		0.25	0.4	0.25		V	
		$I_{OL} = 8 \text{ mA}$		0.35		0.5			
I_I	$V_{CC} = \text{MAX.}$, $V_I = 7 \text{ V}$	D input		0.1		0.1		mA	
		C input		0.4		0.4			
I_{IH}	$V_{CC} = \text{MAX.}$, $V_I = 2.7 \text{ V}$	D input		20		20		μA	
		C input		80		80			
I_{IL}	$V_{CC} = \text{MAX.}$, $V_I = 0.4 \text{ V}$	D input		-0.4		-0.4		mA	
		C input		-1.6		-1.6			
I_{OS}	$V_{CC} = \text{MAX.}$	-20		-100	-20		-100	mA	
I_{CC}	$V_{CC} = \text{MAX.}$, See Note 2	6.3		12		6.3		12	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V.}$, $T_A = 25^\circ\text{C.}$

§ Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V.}$, $T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	D	O	$R_L = 2 \text{ k}\Omega$, $C_L = 15 \text{ pF}$	15	27	ns	
t_{PHL}				9	17		
t_{PLH}	D	\bar{O}		12	20	ns	
t_{PHL}				7	15		
t_{PLH}	C	O		15	27	ns	
t_{PHL}				14	25		
t_{PLH}	C	\bar{O}		16	30	ns	
t_{PHL}				7	15		

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN54LS375J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS375J	Samples
SN74LS375D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS375	Samples
SN74LS375D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS375	Samples
SN74LS375J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	0 to 70		
SN74LS375J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	0 to 70		
SN74LS375N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS375N	Samples
SN74LS375N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS375N	Samples
SN74LS375N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74LS375N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74LS375NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS375N	Samples
SN74LS375NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS375N	Samples
SN74LS375NSR	OBSOLETE	SO	NS	16		TBD	Call TI	Call TI	0 to 70		
SN74LS375NSR	OBSOLETE	SO	NS	16		TBD	Call TI	Call TI	0 to 70		
SN74LS375NSRE4	ACTIVE	SO	NS	16		TBD	Call TI	Call TI	0 to 70		Samples
SN74LS375NSRE4	ACTIVE	SO	NS	16		TBD	Call TI	Call TI	0 to 70		Samples
SN74LS375NSRG4	ACTIVE	SO	NS	16		TBD	Call TI	Call TI	0 to 70		Samples
SN74LS375NSRG4	ACTIVE	SO	NS	16		TBD	Call TI	Call TI	0 to 70		Samples
SNJ54LS375FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
SNJ54LS375FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
SNJ54LS375J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS375J	Samples
SNJ54LS375J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS375J	Samples
SNJ54LS375W	OBSOLETE			16		TBD	Call TI	Call TI	-55 to 125		

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54LS375W	OBSOLETE			16		TBD	Call TI	Call TI	-55 to 125		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54LS375, SN74LS375 :

- Catalog: [SN74LS375](#)
- Military: [SN54LS375](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



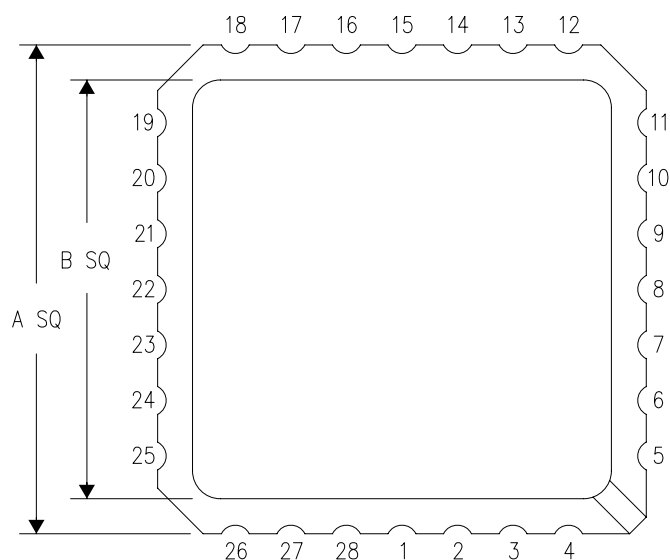
4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

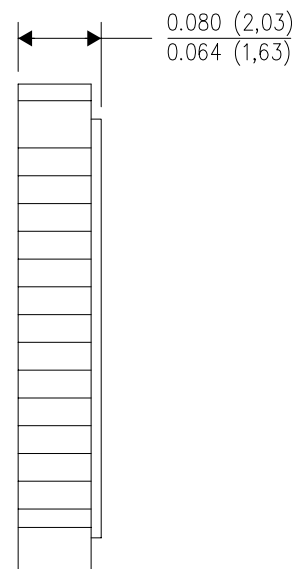
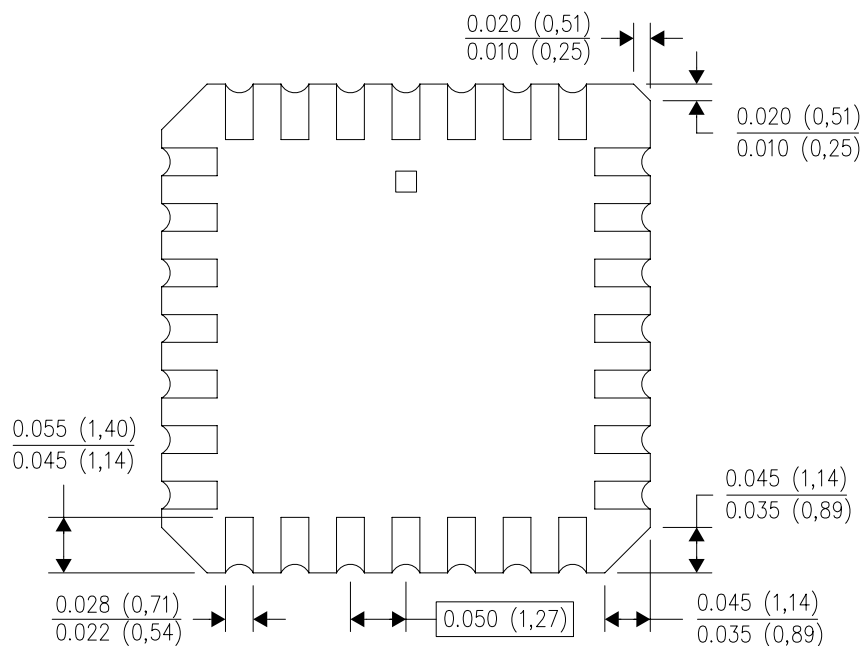
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

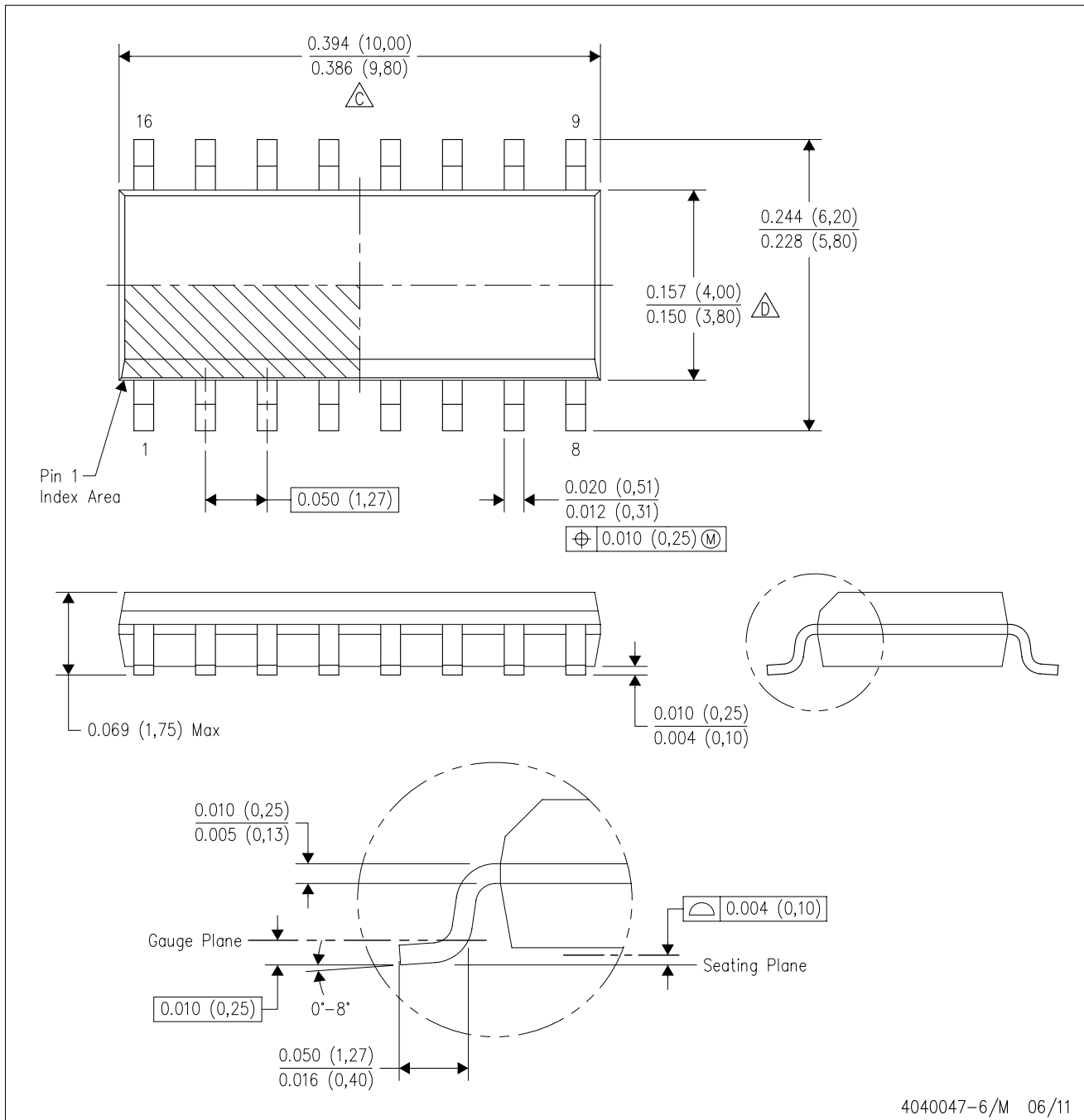
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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